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SiC MOSFETs:
Gate Drive Optimization

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ABSTRACT

For high−voltage switching power applications, silicon carbide or SiC MOSFETs bring notable advantages compared to traditional silicon MOSFETs and IGBTs. Switching high−voltage power rails in excess of 1,000 V, operating at hundreds of kHz is non−trivial and beyond the capabilities of even the best superjunction silicon MOSFETs. IGBTs are commonly used but are restricted to lower operating frequencies due to their “tailing current” and slow turn−off. As a result, silicon MOSFETs are preferred for lower voltage, high−frequency operation while IGBTs are better suited for higher voltage, high−current, low−frequency applications. SiC MOSFETs offer the best combination of high−voltage, high frequency, switching performance benefits. They are voltage−controlled, field−effect devices capable of switching the same high voltages of an IGBT at or above the switching frequencies of much lower voltage silicon MOSFETs.

SiC MOSFETs have unique gate drive requirements. In general, they require a 20−V, V_{DD} gate drive during the on−state to provide lowest on−resistance. Compared to their silicon counterparts, they exhibit lower transconductance, higher internal gate resistance and the gate turn−on threshold can be less than 2 V. As a result, the gate must be pulled below ground (typically −5 V) during the off−state. Understanding and optimizing the gate drive circuitry has a profound effect on reliability and the overall switching performance that can be achieved.

This paper highlights the unique device characteristics associated with SiC MOSFETs. Critical design requirements related to optimal gate−drive design for maximizing SiC switching performance will be described. System level considerations such as start−up, fault protection and steady state switching will also be discussed.

INTRODUCTION

Silicon carbide (SiC) is part of the wide bandgap (WBG) family of semiconductor materials used to fabricate discrete power semiconductors. As shown in Table 1, conventional silicon (Si) MOSFETs have a bandgap energy of 1.12 eV compared to SiC MOSFETs possessing 3.26 eV.

The wider bandgap energy associated with SiC and (GaN) Gallium Nitride means that it takes approximately 3 times the energy to move electrons from their valence band to the conduction band, resulting in a material that behaves more like an insulator and less like a conductor. This allows WBG semiconductors to withstand much higher breakdown voltages, highlighted by their breakdown field robustness being 10 times that of silicon. A higher breakdown field enables a reduction in device thickness for a given voltage rating which translates to lower on−resistance and higher current capability. SiC and GaN each have mobility parameters on the same order of magnitude as silicon, making both materials well suited for high−frequency switching applications. However, the parameter most differentiating SiC is its thermal conductivity being more than 3 times greater compared to silicon and GaN. Higher thermal conductivity translates to lower temperature rise for a given power dissipation. The guaranteed maximum operating temperature for commercially available SiC MOSFETs is 150°C < T_J < 200°C. Comparatively, SiC junction temperatures as high as 600°C are attainable but mostly limited by bonding and packaging techniques. This makes SiC the superior WBG semiconductor material for high−voltage, high−speed, high−current, high−temperature, switching power applications.

Table 1. SEMICONDUCTOR MATERIAL PROPERTIES

Properties	Si	4H−SiC	GaN
Bandgap Energy (eV)	1.12	3.26	3.50
Electron Mobility (cm^2/Vs)	1400	900	1250
Hole Mobility (cm^2/Vs)	600	100	200
Breakdown Field (MV/cm)	0.3	3.0	3.0
Thermal Conductivity (W/cm°C)	1.5	4.9	1.3
Maximum Junction Temperature (°C)	150	600	400

SiC MOSFETs are commonly available in the range of 650 V < B_{VDSS} <1.7 kV, with the majority focus being 1.2 kV and above. At the lower range of 650 V, traditional silicon MOSFETs and GaN outperform SiC. However, one reason to consider lower voltage SiC MOSFETs might be to take advantage of their superior thermal characteristics.

Although the dynamic switching behavior of SiC MOSFETs is quite similar to standard silicon MOSFETs, there are unique gate drive requirements dictated by their device characteristics that must be taken into consideration.

SiC MOSFET CHARACTERISTICS

Transconductance

A silicon MOSFET used in a switching power supply switches as quickly as possible between one of two operating modes or regions. The cutoff region is defined where the gate−source voltage, V_{GS}, is less than the gate−threshold voltage, V_{TH} and the semiconductor is in a high blocking state. During cutoff, the drain−source resistance, R_{DS}, is high impedance and the drain current, I_D = 0 A. The saturation region occurs when the MOSFET is fully enhanced, V_{GS} >> V_{TH}, and $R_{DS(on)}$ is at or near the minimum value, I_D is maximum and the semiconductor is in a high conduction state. As highlighted by the red trace

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shown in Figure 1, the transition between the linear (ohmic) and saturation regions is very sharp and distinct, so that as soon as $V_{GS} > V_{TH}$, drain current flows through a relatively low R_{DS}. The transconductance, g_m, is the ratio of the change in drain current to the change in gate voltage and defines the output to input gain of the MOSFET, which is the slope of the I−V output characteristic curve for any given V_{GS}.

$$g_m = \frac{\Delta I_d}{\Delta V_{GS}} \quad \text{(eq. 1)}$$

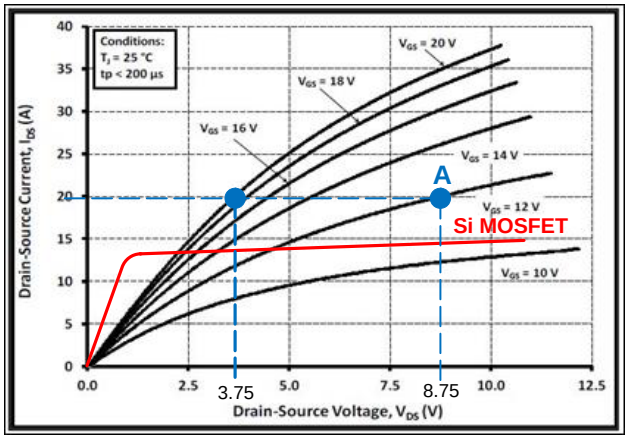

Figure 1. SiC MOSFET Output Characteristics

The slope for a silicon MOSFET I−V curve is steep in the linear region (large ΔI_D) and nearly flat when operating in saturation so it experiences very high gain (high g_m) whenever $V_{GS} > V_{TH}$. The fact that I_D is flat for a given V_{GS} means that the silicon MOSFET behaves much like a non−ideal current source when operating in saturation. Conversely, it can be seen from the output characteristic curves shown in Figure 1, that a SiC MOSFET does not exhibit a sharp transition between the linear and saturation operating modes. In fact there is no defined "saturation region" and from this point of view a SiC MOSFET behaves more like a variable resistance than a non−ideal current source. The I−V output characteristic of a SiC MOSFET does not exhibit a large ΔI_D for a small ΔV_{GS}, therefore, SiC MOSFETs are considered low gain (low g_m) devices.

$$I_D = g_m \times (V_{GS} - V_{TH}) \quad \text{(eq. 2)}$$

The only way to compensate for the low gain and force a large change in I_D is to apply a very large V_{GS}, which has a profound impact on R_{DS}. To further illustrate this point, consider the two operating points labeled A and B in Figure 1.

$$R_{DS(A)} = \frac{8.75\ V}{20\ A} = 438\ m\Omega,\ (V_{GS} = 12\ V) \quad \text{(eq. 3)}$$

$$R_{DS(B)} = \frac{3.75\ V}{20\ A} = 188\ m\Omega,\ (V_{GS} = 20\ V) \quad \text{(eq. 4)}$$

A fixed drain current of I_D = 20 A, yields V_{DS} = 8.75 V when V_{GS} = 12 V compared to V_{DS} = 3.75 V when V_{GS} is increased to 20 V. Comparing the results of equations (3) and (4), shows that the resistance and therefore, conduction loss is 2.3 times higher when operating at V_{GS} = 12 V.

As a result, SiC MOSFETs perform best when applying a maximum gate−source voltage between 18 V < V_{GS} < 20 V and some can even be as high as V_{GS} = 25 V. Operating a SiC MOSFET at low V_{GS} can result in thermal stress or possible failure due to high R_{DS}. The extenuating effect associated with the low g_m cannot be overstated. It has a direct impact upon several important dynamic characteristics that must be considered when designing an adequate gate−drive circuit: specifically, on−resistance, gate charge (Miller plateau) and over−current (DESAT) protection.

On−Resistance

As a WBG semiconductor, a SiC MOSFET presents a lower associated on−resistance per unit area for a given voltage. The on−resistance of a MOSFET consists of the contributions from several internal, V_{GS} dependent, resistive elements. Most notable are the channel resistance (R_{CH}), JFET resistance (R_J) and drift region resistance (R_{DRIFT}). R_{CH} has a negative temperature coefficient (NTC) and dominates R_{DS} at lower V_{GS}. Conversely, R_J and R_{DRIFT} have a positive temperature coefficient (PTC) and are dominant at higher V_{GS} levels. For V_{GS} > 18 V, the on−resistance has a distinct PTC characteristic. However, during lower V_{GS}, the on−resistance versus junction temperature characteristic appears parabolic as shown in Figure 2. Specifically at V_{GS} = 14 V, where R_{CH} is dominant, R_{DS} appears to have a NTC characteristic where resistance is decreasing with increasing temperature. This unique distinction of a SiC MOSFET is directly attributed to low g_m. For a silicon MOSFET, whenever $V_{GS} > V_{TH}$, R_{DS} always has a PTC.

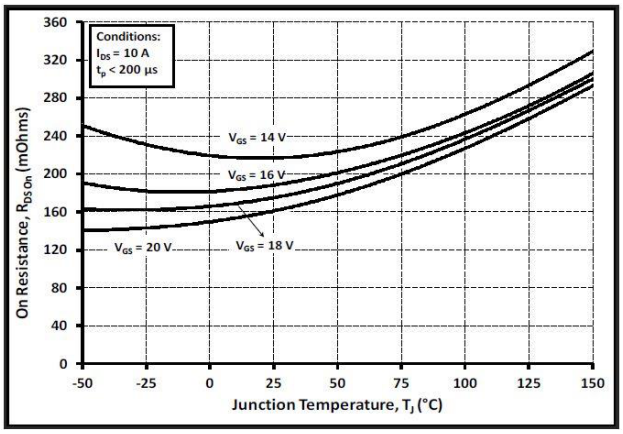

Figure 2. SiC MOSFET On−Resistance vs. Junction Temperature

The PTC attribute is heavily relied upon for current balancing whenever two or more MOSFETs are placed in parallel, as would be the case for most high current applications. During parallel operation, when one MOSFET experiences a rise in junction temperature, the PTC causes an increase in R_{DS}, decreasing the current and forcing the

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parallel MOSFET to take on additional current until a natural balance occurs. If two or more SiC MOSFETs were placed in parallel while operating with low V_{GS} (negative NTC), the result would be catastrophic. Therefore, parallel operation between SiC MOSFETs is only recommended when V_{GS} is sufficient to ensure reliable NTC operation (typically V_{GS} > 18 V).

Internal Gate Resistance

The internal gate resistance, R_{GI}, is inversely proportional to die size and for a given breakdown voltage, since a SiC MOSFET die is much smaller compared to a silicon MOSFET die, internal gate resistance tends to be higher. The real benefit of the smaller SiC MOSFET die comes in the form of lower input capacitance, C_{ISS}, which translates to lower required gate charge, Q_G. Table 2 highlights several important parameter comparisons between two different manufacturers of SiC MOSFETS (SiC_1 and SiC_2) and two best in class, 900−V and 650−V super junction, Si MOSFETs (Si_1 and Si_2).

Table 2. SEMICONDUCTOR MATERIAL PROPERTIES

III.	SiC_1	SiC_2	Si_1 SJ FET	Si_2 SJ FET
B_{VDSS} (V)	1200	1200	900	650
I_D (A)	19	22	36	15
R_{DS} (mΩ)	160	160	120	130
Q_G (nC)	34	62	270	35
Q_{GD} (nC)	14	20	115	11
C_{ISS} (pF)	525	1200	6800	1670
C_{OSS}(pF)	47	45	330	26
V_{GS} (V)	−5 to 20	−6 to 22	±20	±20
$V_{GS(TH)}$ (V)	2.5	2.8	3	3.5
R_{GI} (Ω)	6.5	13.7	0.9	1
R_{GI}xC_{ISS} (ns)	221	850	243	35

From a gate drive viewpoint, it is interesting to compare the R_{GI}xC_{ISS} time constants. The Si_2 device has the lowest time constant of 35 ns but is also a lower current, lower voltage rated MOSFET. For comparison purposes the 650−V, Si_2 MOSFET is interesting because the 1200−V, SiC_1 sample has parameters closely matched but has a significantly lower C_{ISS} at nearly twice the rated B_{VDSS}. In terms of B_{VDSS}, the Si_1 sample is a closer comparison to either of the SiC samples. Because of the low Q_G associated with SiC_1, the time constants between Si_1 and SiC_1 are closely matched even though the internal gate resistance of SiC_1 is 7 times higher.

Internal gate resistance limits the gate drive current that can be injected into the C_{ISS}. A high performance, SiC gate drive circuit needs to provide extremely low output impedance so that the driver does not become a limiting factor by adding to the already high R_{GI}. This allows the designer more freedom to control V_{DS}, dV/dt transitions by adding or reducing external gate resistance.

Gate Charge

When V_{GS} is applied, a certain amount of charge is transferred to change the gate voltage between $V_{GS(MIN)}$ (V_{EE}) and $V_{GS(MAX)}$ (V_{DD}) as fast as possible. Since the MOSFET internal capacitances are non−linear, a V_{GS} versus gate charge (Q_G) curve is helpful to identify how much charge must be delivered for a given V_{GS} level. A typical gate charge curve for a SiC MOSFET is shown in Figure 3.

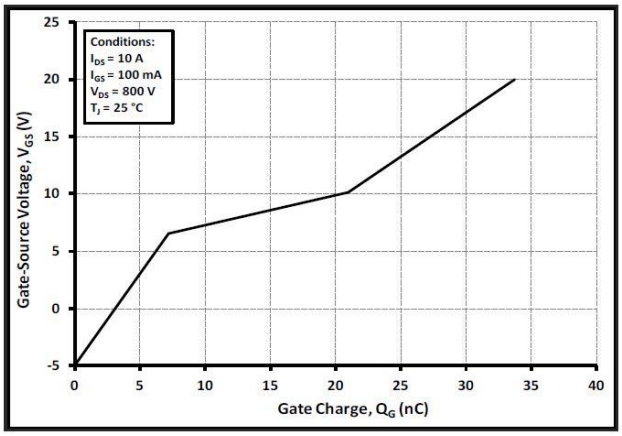

Figure 3. SiC MOSFET, Gate−Source Voltage vs. Gate Charge

It is interesting that the Miller plateau for a SiC MOSFET occurs at higher V_{GS} and is not flat as would be expected for a silicon MOSFET. A non−flat Miller plateau implies that V_{GS} is not constant over the corresponding range of charge, Q_G. This is another consequence arising from the low gm associated with SiC MOSFETs. It is also notable that Q_G = 0 nC does not occur at V_{GS} = 0 V. V_{GS} must be pulled below ground (−5 V in this case) to fully discharge the gate of a SiC MOSFET. A second reason to switch the gate negative during turn−off arises from the fact that the worse case V_{TH} can be as low as low as 1 V. Switching V_{GS} between 0V < V_{GS} < V_{DD}, with V_{TH} ~ 1 V leaves no margin for inadvertent turn−on due to spurious gate noise or V_{DS}, dV/dt−induced turn−on. As a result, nearly all SiC MOSFETs require a minimum V_{GS} of −5 V < $V_{GS(MIN)}$ < −2 V but some manufacturers specify as much as −10 V.

DESAT Protection

DESAT protection is a type of over−current detection that originated with circuits used to drive IGBTs. During the on−time, if the IGBT could no longer be held in saturation (“de−saturation”), the collector−emitter voltage would begin to rise while the full collector current was flowing. Obviously this would have a negative impact on efficiency or in the worst case, could lead to failure of the IGBT. Possible reasons for this might include: insufficient base

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current due to beta tolerance or temperature effects or short circuit or overload operation. The purpose of the so called “DESAT” function is to monitor the collector−emitter voltage of the IGBT and detect whenever such a potentially destructive condition is present.

Although the fault mechanism is slightly different, a SiC MOSFET can suffer a similar fate where V_{DS} can rise while maximum I_D is flowing. This undesirable condition can arise if the maximum V_{GS} during turn−on is too low or the gate drive turn−on edge is too slow or a short circuit or overload condition exists. The R_{DS} can increase while the full I_D is present, causing an unexpected but slow rise in V_{DS}.

Because a SiC MOSFET does not operate in a clearly defined saturation region, it never appears as constant−current source. This can be problematic, as most over−current protection schemes depend on a MOSFET emulating a non−ideal, constant current source during an over−current condition. When a SiC MOSFET undergoes a de−saturation event, V_{DS} responds very slowly, while the maximum drain current continues flowing through an increasing on−resistance. As a result, it can be possible that the drain current could reach a level 10−20 times the maximum rated pulse current (during high R_{DS}), before the drain−source voltage can respond. For a high−frequency power converter, numerous switching cycles can occur before a de−saturation fault is recognized. DESAT is therefore an important and necessary protection function that should be assigned as part of the gate drive circuitry, in addition to any over−current protection that might also be part of the power supply control.

SiC MOSFET DYNAMIC SWITCHING

Turn−On

The switching profile for a SiC MOSFET is very similar to a Si MOSFET except for the main difference being the 20−V gate−drive amplitude during turn−on and the fact that the gate must be pulled below ground during turn−off. The turn−on transition requires a large, peak, source current capable of charging the SiC internal gate capacitance as quickly as possible to minimize switching loss. As an estimate, the entire turn−on event should occur within $\Delta t <$ 10 ns, for a full V_{GS} swing of $\Delta V_{GS} = 30$ V and an estimated $C_{ISS} = C_{GS} + C_{GD} = 1000$ pF which yields a required peak current, $I_{G(SRC)}$=3 A according to equation (5):

$$I_{G(SRC)} = \frac{(C_{GS} + C_{GD)} \times \Delta V_{GS}}{\Delta t} \qquad \text{(eq. 5)}$$

The turn−on transition for a SiC MOSFET is defined by four distinct timing intervals, as shown in Figure 5. The timing intervals shown in Figure 5 and Figure 7 are representative of what would be expected from an ideal clamped inductive switching application, typical of the operating mode used in switching power supplies.

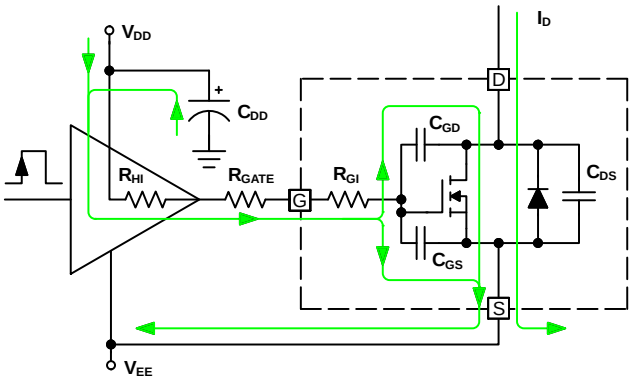

Figure 4. SiC MOSFET Source Current

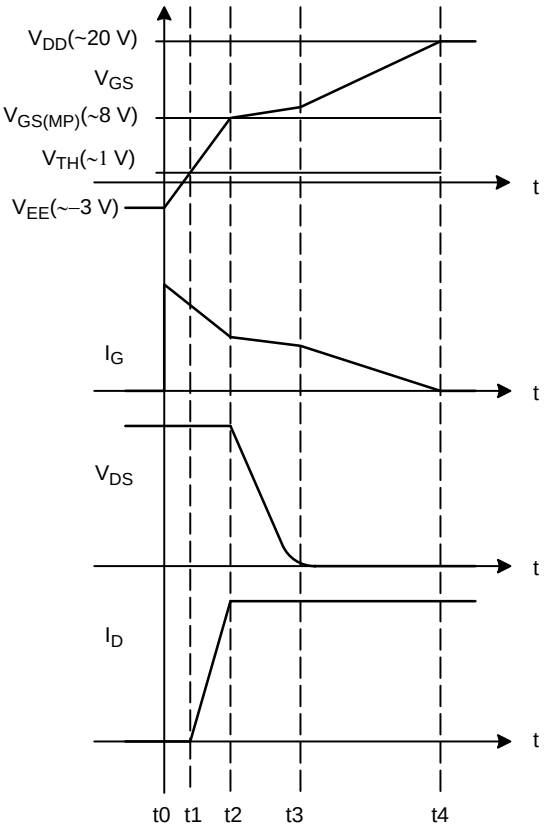

Figure 5. SiC MOSFET Turn−On Sequence

$t_0 \rightarrow t_1$: V_{GS} ramps from V_{EE} to V_{TH} as the gate drive circuit must deliver a large peak of instantaneous gate current, $I_{G(SRC)}$, supplied primarily from the charge stored in the gate driver bulk capacitor, C_{VDD}. This time interval is often referred to as “turn−on delay” since I_D and V_{DS} are unaffected while V_{GS} is below V_{TH}. Most of the gate current is used to charge C_{GS} and C_{GD}. Notice from the schematic diagram shown in Figure 4, the sourcing current flows through three resistors, R_{HI}, R_{GATE} and R_{GI}. R_{HI} is the equivalent internal resistance of the driver source, R_{GATE} is the resistance of the trace impedance plus any additional

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added dampening resistance and R_{GI} is the SiC MOSFET internal gate resistance. R_{HI} and R_{GATE} are on the order of a few Ω's but for a SiC MOSFET R_{GI} can be on the order of 10's of Ω's which is an order of magnitude higher compared to a high−voltage, Si MOSFET. Since these three resistors form an RC time constant with the SiC internal gate capacitance, sourcing adequate peak gate current is necessary to assure a fast rising edge of the gate drive signal.

$t_1 \rightarrow t_2$: As V_{GS} continues to ramp from V_{TH} to the Miller plateau, I_D begins to increase through $R_J + R_{DRIFT}$ since the R_{DS} channel resistance is not fully enhanced at low V_{GS}. V_{DS} remains at its maximum level because the SiC intrinsic body−diode is not yet in the blocking state due to the low value of I_D and the high resistive state of R_{DS}. It is advised not to operate a SiC MOSFET with V_{GS} < 13 V because of the risk of thermal runaway due to the high R_{DS} at low V_{GS}. Therefore, it is critical that the gate drive circuit be able to transition from V_{TH} to V_{GS} > 13 V as fast as possible. The time spent for $V_{TH} < V_{GS} < 13$ V should be less than a few ns to minimize $I_D^2 x R_{DS}$ dynamic power loss.

$t_2 \rightarrow t_3$: V_{GS} is at the Miller plateau which happens around 8 V for a SiC MOSFET. During this time the full load current is flowing through R_{DS} and the intrinsic body−diode no longer in its blocking state, allowing the drain voltage to fall. The channel resistance continues decreasing but R_{DS} is still dominated by R_{CH}. Although the full load current is flowing through the MOSFET drain, R_{DS} remains quite high at this low V_{GS}. Therefore, it is imperative that V_{GS} transition through this region as quickly as possible. Since the speed of this transition is driven by I_G, the peak drive current capability during the Miller plateau (~ 1/2 V_{DD}) region should be more interesting than the peak rating shown on any gate driver IC data sheets.

$t_3 \rightarrow t_4$: At $V_{GS(MP)}$ just near the end of the Miller plateau, V_{DS} falls to I_D x R_{DS} above zero. As V_{GS} transitions from ~8 V < V_{GS} < 20 V, the channel resistance, R_{CH}, continues to decrease and now $R_J + R_{DRIFT}$ are dominant over R_{CH}, resulting in a proportional decrease in V_{DS}. Most SiC MOSFETs become fully enhanced when V_{GS} > 16 V but the lowest R_{DS} value is ultimately determined by the final maximum value of V_{GS}. The remaining gate current, I_G, is split to fully charge C_{GD} and C_{GS}.

Turn−Off

The turn−off procedure for a SiC MOSFET is essentially the reverse of the turn−on sequence described previously. The role of the gate drive circuit is to sink a large amount of peak current, capable of discharging the C_{GD} and C_{GS} capacitance of the SiC MOSFET as quickly as possible. In addition, the gate driver impedance during turn−off must be as low as possible to hold the MOSFET gate low. This can be especially problematic due to the low V_{TH} associated with SiC MOSFETs. Not only does this necessitate the SiC gate being pulled below ground but the sink current capability of the gate driver must also be significantly higher compared to the rated source current. The flow of gate drive current, $I_{G(SINK)}$, is highlighted in Figure 6.

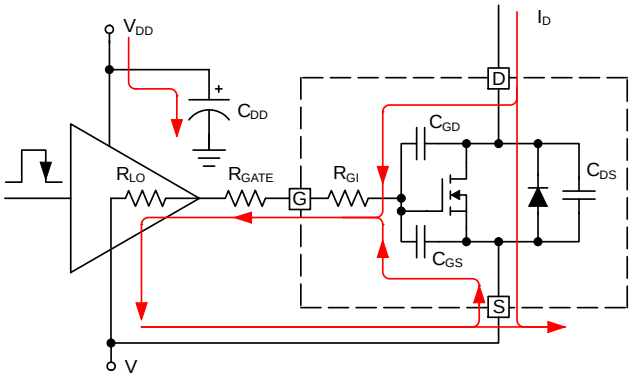

Figure 6. SiC MOSFET Sink Current

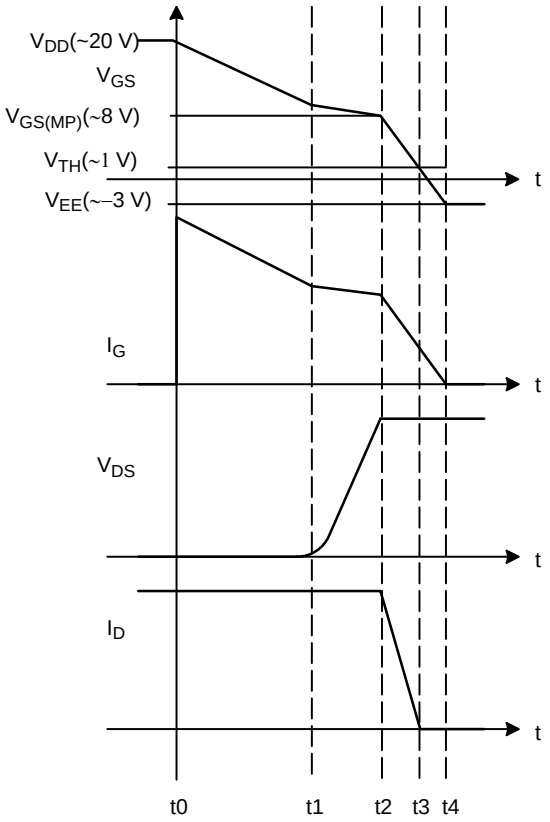

Figure 7. SiC MOSFET Turn−Off Sequence

$t_0 \rightarrow t_1$: V_{GS} ramps down from V_{DD} to the Miller plateau, $V_{GS(MP)}$. The sink current, $I_{G(SINK)}$, is primarily supplied from the charge stored in C_{GD} and C_{GS} while the gate driver bulk capacitor, C_{VDD}, is recharged by V_{DD}. The drain current, I_D, remains unchanged. As V_{GS} is decreasing, the channel resistance is increasing causing a slight increase in V_{DS} by $I_D x R_{DS}$ volts. The marginal increase in V_{DS} would be hardly noticeable except possibly near the end of the $t_0 \rightarrow t_1$ time interval.

t1→t2: During this time interval, the provision of gate current is dominated by C_{GD} since the C_{GS} capacitor sees a nearly constant V_{GS}. Across the Miller plateau, V_{DS} increases from I_D x R_{DS} to the VDS rail voltage where it is clamped by the SiC intrinsic body−diode. The drain current,

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I_D, remains unchanged from the previous interval. Since RDS is increasing due to V_{GS} <1 3 V and V_{DS} x I_D simultaneously appear across the MOSFET, the gate drive circuit should be rated to sink a significant amount of current during this time interval. During turn−off, this is the portion of the gate drive current that is most interesting to designers since it is imperative to transition through the Miller plateau region as quickly as possible.

$t_2 \rightarrow t_3$: As V_{GS} continues to decrease from the Miller plateau toward V_{TH}, I_D is ramping down to near zero during this interval. V_{DS} is now fully clamped to the drain voltage rail by the SiC intrinsic body−diode which means the C_{GD} capacitor is fully charged. As a result, most of the sink current is now flowing through C_{GS}.

$t_3 \rightarrow t_4$: I_D and V_{DS} remain unchanged. During the final turn−off interval, the SiC internal input capacitors are not fully discharged until V_{GS} falls below 0 V. Since V_{TH} is only ~1 V and to fully discharge C_{ISS}, V_{GS} must complete the turn−off sequence at a negative voltage. The importance of the gate drive circuit to provide as low impedance as possible cannot be overstated. This is especially true for high−voltage, half−bridge power topologies where the midpoint is pulled up by a high dV/dt when the high−side MOSFET conducts. A low impedance pull−down is essential for preventing inadvertent, dV/dt−induced turn−on.

In summary, the turn−on and turn−off switching states for a SiC MOSFET involve four distinct time intervals. The dynamic switching waveforms shown in Figure 5 and Figure 7 are representative of ideal operating conditions. In reality, package parasitics such as lead and bond wire inductance, parasitic capacitances and PCB layout can have a profound effect on measured waveforms. Proper component selection, best PCB layout practices and an emphasis on providing a well−designed gate−drive circuit are each essential for optimizing performance of SiC MOSFETs used in switching power applications.

DISCRETE SiC GATE DRIVE

Compensating for the low gain while achieving efficient, high−speed switching imposes the following critical requirements for a SiC gate drive circuit:

1. A SiC MOSFET specifies an asymmetrical max/min V_{GS} near the range of +25 V/−10 V. The gate drive circuit must be capable of providing nearly the full range of 35 V, V_{GS} swing to take full advantage of the SiC performance benefits. Most SiC MOSFETs will perform best when driven between −5 V > V_{GS} > 20 V. To cover the widest range of available SiC MOSFETs, the gate drive circuit should be able to withstand V_{DD} = 25 V and V_{EE} = −10 V
2. V_{GS} must have fast rise and fall edges, on the order of a few ns
3. Must be able to source high peak gate current on the order of several amps, across the entire Miller plateau region
4. Sink current capability is driven by the need to provide a very low impedance hold−down or “clamp” as the V_{GS} falls below the Miller plateau. The sink current rating should exceed what would be required by merely having to discharge the input capacitance of a SiC MOSFET. A minimum, peak sink current rating on the order of 10 A should be considered appropriate to cover high performance, half−bridge power topologies
5. Must have V_{DD} under−voltage lockout (UVLO) level that is matched to the requirement that V_{GS} > ~16 V before switching begins
6. Must have V_{EE} UVLO monitoring capability to assure the negative voltage rail is within an acceptable range
7. Must have a de−saturation function capable of detection, fault reporting and protection for long term reliable operation of the SiC MOSFET
8. Low parasitic inductance for high−speed switching
9. Small driver package able to be located as close as possible to the SiC MOSFET

Without exception, the requirements for driving a SiC MOSFET efficiently and reliably call for a very specific type of gate driver. However, most reference designs currently shown in the industry are designed based on using general purpose low−side gate drivers. One such example is shown in Figure 8.

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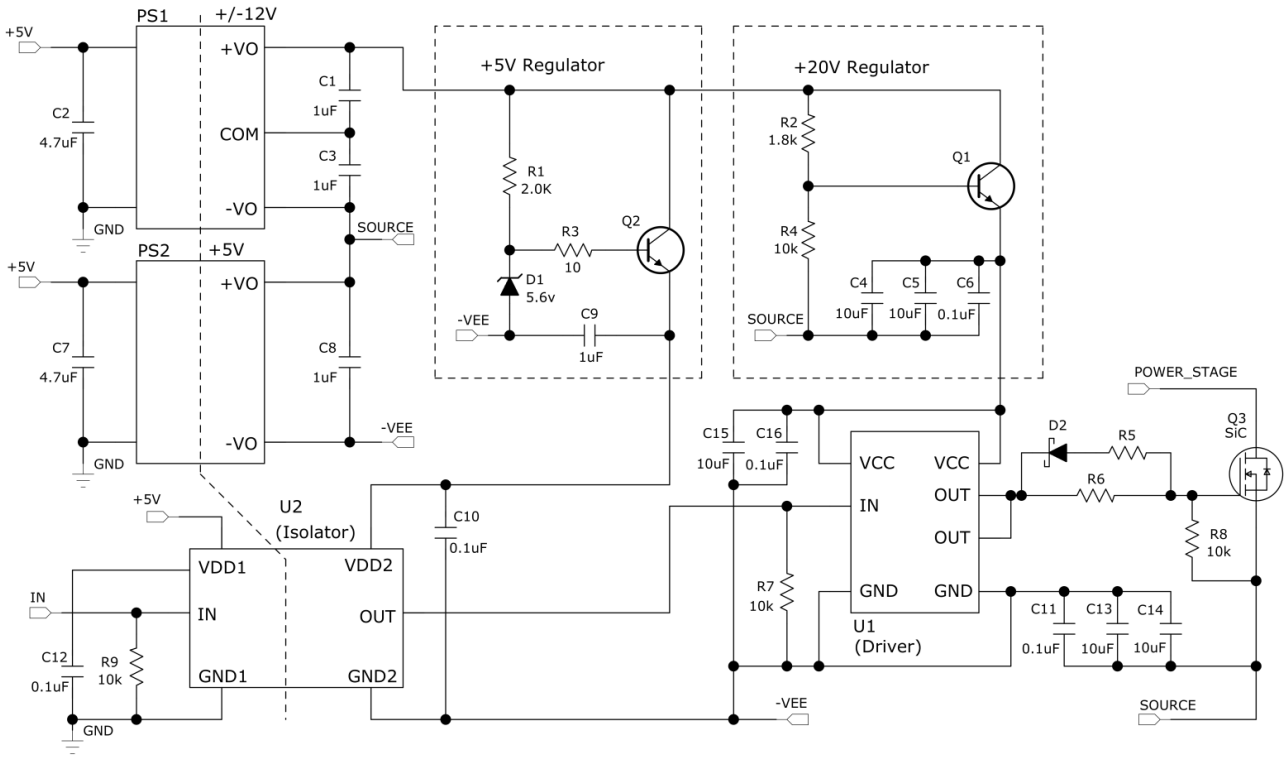

Figure 8. Standard Low−Side Driver, SiC Discrete Gate Drive Design Example

The circuit shown is floating with respect to ground so it can be used as either a low−side or high−side referenced gate drive. For either case, in the event of a power stage failure, isolation is desired to protect the control circuitry from the high−voltage seen at the power stage. Two isolated dc−dc converters, PS1 providing V_{DD} = 24 V (post−regulated to 20 V) and PS2 configured to regulate at V_{EE} = −5 V, are used to provide the V_{DD} and V_{EE} voltage rails. It should also be mentioned that these converters are dedicated to driving a single SiC load and so two would be needed for each SiC load. This is especially true for high−side gate drive applications such as the upper switch in a half−bridge, full−bridge or motor drive application. The voltage seen by the main driver, U_1, is floating by several hundred volts and is very susceptible to the high dV/dt associated with a switching SiC MOSFET. Assuming a dV/dt=100 V/ns, with just 1 pF of stray parasitic capacitance across the isolation barrier of the PS1 (or PS2) transformer results in 100 mA of peak current. 100 mA per pF emphasizes the need for low parasitic capacitance, low stray inductance and tight coupling between the V_{EE} (and V_{DD}) voltage rails and the gate driver IC.

The digital isolator, U_2, isolates the gate drive signal from the power stage and also provides the necessary level shifting. The secondary side of U_2 is then used as the input to main driver, U_1. U_1 is a generic, low−side gate driver but must be rated to handle the full V_{GS} voltage swing of 25 V (−5 V < V_{GS} < 20 V) and provides the desired source/sink current levels. Since most general purpose, low−side gate drivers are rated for a maximum V_{DD} = 20 V, may not provide adequate source/sink current and may not be available in low inductance packages, selection can be limited to only a few specific choices.

These types of gate drivers are intended to drive silicon MOSFETs and from this point of view, they lack several important requirements needed for SiC MOSFETs. For example, there is no over−current fault reporting or DESAT monitoring function available from these gate drivers. Also, the UVLO thresholds of generic gate drivers are typically defined based on 5 V < V_{DD} < 12 V. This could be problematic since the “safe” V_{DD} operating level for a SiC MOSFET is approximately V_{DD} > ~16 V at startup. And there is no UVLO monitoring available for the V_{EE} voltage rail as shown in the reference design of Figure 8. Standard Low−Side Driver, SiC Discrete Gate Drive Design Example. These voltage rails would need to be monitored elsewhere to assure that levels are acceptable for driving the SiC MOSFET into a low resistive state during turn−on and holding the gate below ground during turn−off.

Although the solution shown in Figure 8 provides the necessary functions for driving a SiC MOSFET, it is incomplete, at least according to the gate drive requirements stated at the beginning of section Discrete SIC Gate Drive. Nonetheless, without a dedicated SiC driver, most SiC gate drive circuits are presently designed this way. Any additional functions such as DESAT, voltage rail monitoring, sequencing, etc are either handled by additional dedicated circuits or ignored all together.

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NCP51705 SiC GATE DRIVER

The NCP51705 is a SiC gate driver that includes a high level of flexibility and integration making it fully compatible with any SiC MOSFET in the market. The NCP51705 top level block diagram, shown in Figure 9, includes many basic functions common to what might be expected from any general purpose gate driver, including:

1. V_{DD} positive supply voltage up to 28 V
2. High peak output current of 6 A source and 10 A sink
3. Internal 5 V reference made accessible for biasing 5 V, low−power loads up to 20 mA (digital isolator, opto−coupler, μC, etc)
4. Separate signal and power ground connections
5. Separate source and sink output pins
6. Internal thermal shutdown protection
7. Separate non−inverting and inverting TTL, PWM inputs

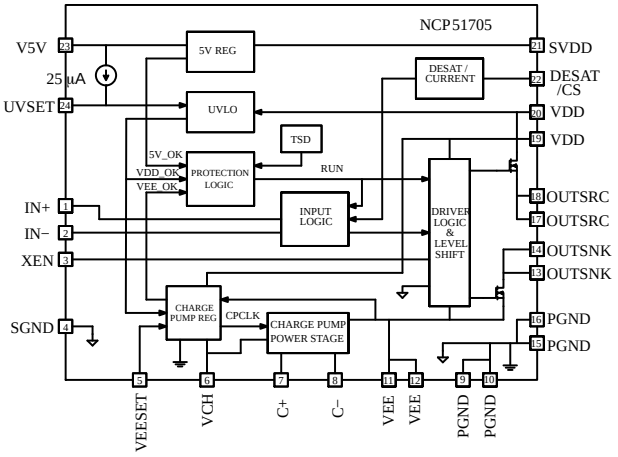

Figure 9. NCP51705 SiC Gate Driver Block Diagram

In addition, the NCP51705 is differentiated by several unique features (listed at the beginning of section Discrete SIC Gate Drive) necessary for designing a reliable SiC MOSFET gate drive circuit using minimal external components. The advantages of the NCP51705 distinguishing features are detailed in the following section.

Over−Current Protection − DESAT

The implementation of the NCP51705 DESAT function can be realized using only two external components. As shown in Figure 10, the drain−source voltage of the SiC MOSFET, Q_1 is monitored via the DESAT pin through R_1 and D_1.

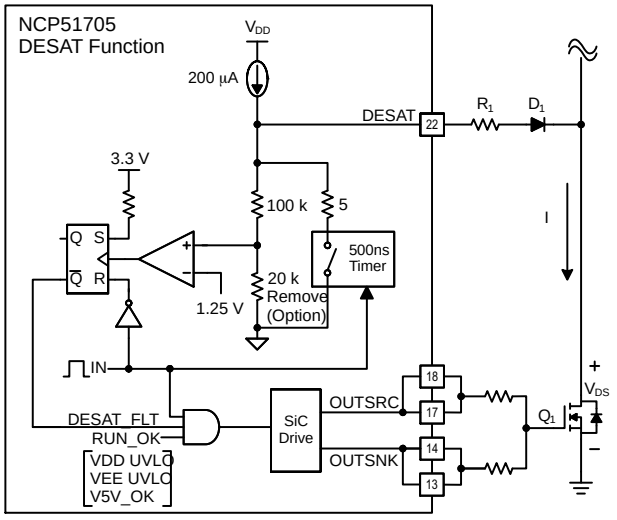

Figure 10. NCP51705 DESAT Function

During the time that Q_1 is off several hundred volts can appear across the drain−source terminals. Once Q_1 is turned on, the drain−source voltage rapidly falls and this transition from high−voltage to near zero voltage is expected to happen in less than a few hundred nano−seconds. During the turn−on transition, the leading edge of the DESAT signal is blanked by a 500−ns timer, consisting of a 5−Ω, low impedance pull−down resistance. This allows sufficient time for V_{DS} to fall while at the same time ensuring DESAT is not inadvertently activated. After 500 ns, the DESAT pin is released and the 200−μA current source provides a constant current through R_1, D_1 and the SiC MOSFET on−resistance. During the on−time, if the DESAT pin rises above 7.5 V, the DESAT comparator output goes HIGH which triggers the clock input of an RS latch. Such a fault will automatically terminate the trailing edge of the Q_NOT output on a cycle−by−cycle basis. The gate drive to the SiC MOSFET is thereby effectively reduced by an amount of time proportional to the de−saturation fault time.

The 200−μA current source is sufficient to ensure a predictable forward voltage drop across D_1 while also allowing the voltage drop across R_1 to be independent of V_{DS} during the on−time of the SiC MOSFET. If desired, DESAT protection can be disabled by connecting the DESAT pin to ground. Conversely, if the DESAT pin is left floating, or R_1 fails open, the 200−μA current source flowing through the 20−kΩ resistor, puts a constant 4 V on the non−inverting input of the DESAT comparator. This condition essentially disables the gate drive to the SiC

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MOSFET. Some applications may prefer to sense the drain current using a current sense transformer and drive the DESAT pin externally. In this case the NCP51705 includes an IC metal option to remove the 20−kΩ resistor, allowing the DESAT pin to be used as a traditional pulse−by−pulse, over−current protection function.

The voltage on the DESAT pin, V_{DESAT}, is determined by equation (6) as:

$$V_{DESAT} = (200\ \mu A \times R_1) + V_{D1} + (I_D \times R_{DS}) \quad \text{(eq. 6)}$$

After assigning the maximum value for I_D (plus allowing any additional design margin) R_1 and I_D are selected such that $V_{DESAT} < 7.5$ V. Rearranging equation (6) and solving for R_1 gives:

$$R_1 = \frac{V_{DESAT} + V_D - (I_{D1} \times R_{DS})}{200\ \mu A} \quad \text{(eq. 7)}$$

In addition to setting the maximum allowable V_{DESAT} voltage, R_1 also serves the dual purpose of limiting the instantaneous current through the junction capacitance of D_1. Because the drain voltage on the SiC MOSFET sees extremely high dV/dt, the current through the p−n junction capacitance of D_1 can become very high if R_1 is not sized appropriately. Therefore, selecting a fast, high−voltage diode with lowest junction capacitance should be a priority. Typical values for R_1 will be near the range of 5 kΩ < R_1 < 10 kΩ but this can vary according to the I_D and R_{DS} parameters of the selected SiC MOSFET. If R_1 is much smaller than 5 kΩ, the instantaneous current into the DESAT pin can be hundreds of milliamps. Conversely, if R_1 is much larger than 10 kΩ, a *RC* delay ensues as a product of R_1 and the junction capacitance of D_1. The delay can be on the order of 100 μs, resulting in an additional delay time responding to a DESAT fault.

Charge Pump – V_{EE} (VEESET)

The NCP51705 operates from a single, positive supply voltage. Operating from a single V_{DD} supply voltage implies the negative V_{EE} voltage must be generated from the gate driver IC. The use of a switched capacitor charge pump is a natural choice for producing the required negative V_{EE} voltage rail. There are many different options for architecting a charge pump. The main challenges are maintaining accurate voltage regulation during transient conditions, switching at a frequency to decrease the size of capacitors and minimize external component count, thereby reducing cost and increasing reliability.

As can be seen from the charge pump functional block diagram shown in Figure 11, only three external capacitors are required to establish the negative V_{EE} voltage rail. The charge pump power stage essentially consists of two PMOS and two NMOS switches arranged in a bridge configuration.

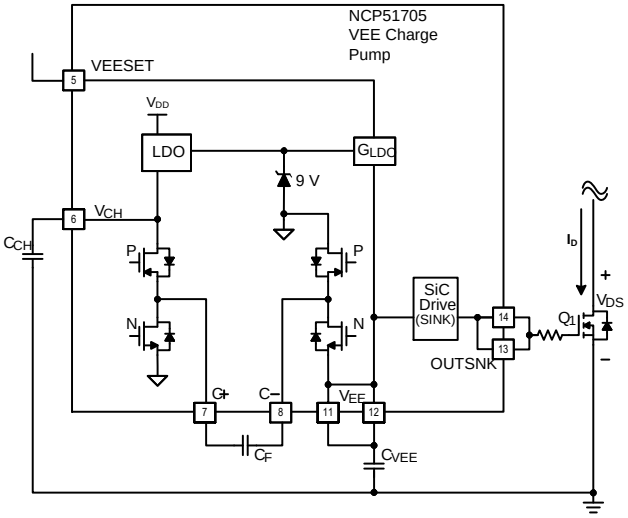

Figure 11. NCP51705 V_{EE} Charge Pump

An external flying capacitor, C_F, is connected between the midpoints of each leg of the bridge as shown. The switch timing is such that whenever the two upper PMOS devices are conducting simultaneously, V_{DD} appears across C_F. Similarly whenever, the two lower NMOS devices are conducting simultaneously, $-V_{EE}$ appears across C_F. The switching frequency is internally set at 390 kHz, with the two upper PMOS devices switching asynchronous with respect to the two lower NMOS devices. A 290 kHz, IC metal option is also available for applications desiring a lower charge pump switching frequency.

V_{EE} is regulated to the voltage set at V_{CH} which is determined by the internal low dropout regulator (LDO) voltage, programmable by VEESET. The voltage present at VEESET varies the gain (G_{LDO}) seen by the internal LDO. If VEESET is left floating (a 100−pF bypass capacitor from VEESET to SGND is recommended), then V_{EE} is set to regulate at −3 V. For a −5−V V_{EE} voltage, the VEESET pin should be connected directly to V5V (pin 23). If VEESET is connected to any voltage between 9 V and V_{DD}, then V_{EE} is clamped and set to regulate at the minimum charge pump voltage of −8 V. The charge pump starts when $V_{DD} > 7.5$ V and the V_{EE} voltage rail includes an internally fixed UVLO set to 80% of the programmed V_{EE} value. Since V_{DD} and V_{EE} are each monitored by independent UVLO circuits, the NCP51705 is smart enough to realize when both voltage rails are within limits deemed safe for a given SiC MOSFET load.

Alternatively, 0 V < OUT < V_{DD} switching can be achieved by disabling the charge pump entirely. When VEESET is connected to SGND the charge pump is disabled. With the charge pump disabled and V_{EE} tied

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directly to PGND, the output switches between 0 V < OUT < V_{DD}. It is important to note that whenever VEESET is tied to SGND, V_{EE} must be tied to PGND. During this mode of operation the internal V_{EE} UVLO function is also disabled accordingly.

Another possible configuration is to disable the charge pump but allow the use of an external negative V_{EE} voltage rail. This option permits $-V_{EE}$ < OUT < V_{DD} switching with a slight savings in IC power dissipation, since the charge pump is not switching. With VEESET connected to SGND, an external negative voltage rail can be connected directly between V_{EE} and PGND. A word of caution, since VEESET is 0 V, the internal V_{EE} UVLO is disabled and therefore the NCP51705 is unaware if the V_{EE} voltage level is within the expected range.

This simple VEESET adjustment enables the highest degree of flexibility using the fewest external components while meeting the broadest range of SiC MOSFET voltage requirements. For convenience, the configurability of VEESET is summarized in Table 3.

Table 3. SEMICONDUCTOR MATERIAL PROPERTIES

VEESET	COMMENT	V_{EE}	V_{EE} (UVLO)
V_{DD}	9 V < VEESET < V_{DD}	−8 V	−6.4 V
V5V		−5 V	−4 V
OPEN	Add C_{VEE} (100 pF) from VEESET to SGND	−3 V	−2.4 V
GND	Remove C_{VEE} and connect V_{EE} to PGND	0 V	NA
GND	Connect V_{EE} to external negative voltage supply	$-V_{EXT}$	NA

Programmable Under Voltage Lockout − UVSET

UVLO for a gate driver IC is important for protecting the MOSFET by disabling the output until V_{DD} is above a known threshold. This not only protects the load but verifies to the controller that the applied V_{DD} voltage is above the turn−on threshold. Because of the low g_m value associated with SiC MOSFETs, the optimal UVLO turn−on threshold is not a “one size fits all.” Allowing the driver output to switch at low V_{DD} can be detrimental for one SiC MOSFET but may be acceptable for another depending on heat−sinking, cooling and V_{DD} start−up time. The optimal UVLO turn−on threshold can also vary depending on how the V_{DD} voltage rail is derived. Some power systems may have a dedicated, housekeeping, bias supply while others might rely on a V_{DD} bootstrapping technique similar to Figure 13.

The NCP51705 addresses this need through a programmable UVLO turn−on threshold that can be set with a single resistor between UVSET and SGND. As shown in Figure 12, the UVSET pin is internally driven by a 25−μA current source with a series gain of 6.

The UVSET resistor, R_{UVSET}, is chosen according to a desired UVLO turn−on voltage, V_{ON}, as defined in equation (8).

$$R_{UVSET} = \frac{V_{ON}}{6 \times 25\ \mu A} \qquad \text{(eq. 8)}$$

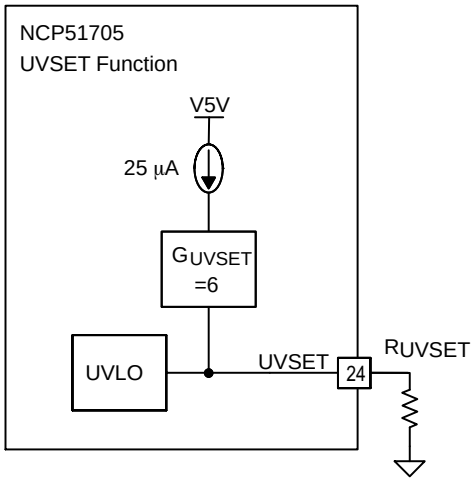

Figure 12. NCP51705 UVSET Programmable UVLO

The value for V_{ON} is typically determined from the SiC MOSFET output characteristic curves, such as those highlighted in Figure 1. Because the on−resistance of a SiC MOSFET dramatically increases even for a slight decrease in V_{GS}, the allowable UVLO hysteresis must be small. For this reason, the NCP51705 has a fixed 1−V hysteresis so that the turn−off voltage, V_{OFF}, is always 1 V less than the set V_{ON}.

For power supplies that include a dedicated housekeeping bias supply, V_{DD} is assumed to be above the desired V_{ON} threshold before the power system initiates soft−start or restart due to a fault recovery. For such systems, having a 1−V UVLO hysteresis is desirable and should not have any impact due to start−up considerations. However, some power systems start from a high−voltage and then rely on V_{DD} from a bootstrap winding as shown in Figure 13.

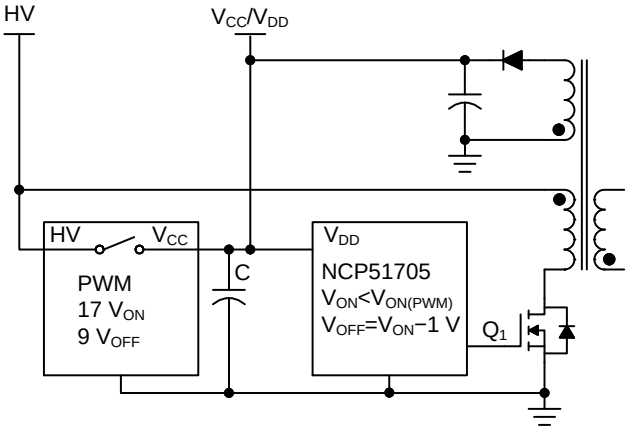

Figure 13. PWM Bootstrap Start−Up Example

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A PWM controller with high−voltage (HV) start−up capability and fixed UVLO thresholds of V_{ON} = 17 V and V_{OFF} = 9 V is shown. As HV is applied, the internal pass switch opens when HV = V_{ON} = 17 V and the PWM controller draws start−up current from C_{VCC}. During this time, C_{VCC} is discharging and Q_1 must begin switching to build up voltage in the transformer bootstrap winding. This imposes a restriction on the allowable V_{ON} that can be programmed from R_{UVSET}. UVSET must be set to a value less than the UVLO V_{ON} of the PWM controller. These start−up details are further illustrated in Figure 14 where the PWM voltage thresholds are shown in blue and the NCP51705 in red.

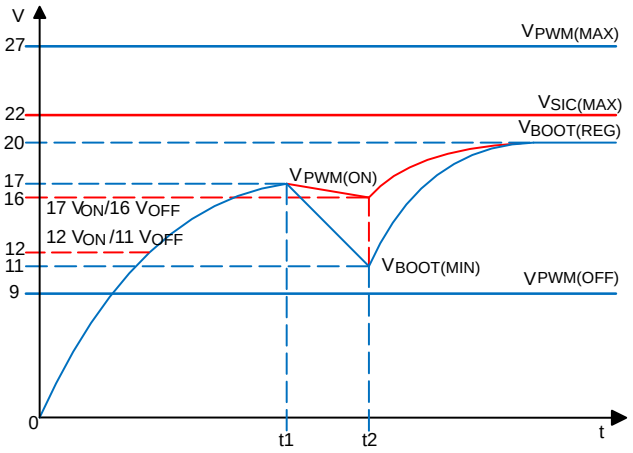

Figure 14. Bootstrap Start−Up Timing

For the purpose of switching the SiC MOSFET with the highest possible V_{GS}, it is desired to set V_{ON} as close to the UVLO turn−on of the PWM controller as possible. The trade off in doing so means ΔV = 1 V during Δt (t_2−t_1). The discharge of C_{VCC} is very shallow so a large capacitor value is required. For example, assuming the start−up current to be 1 mA, Δt = 3 ms and ΔV = 1 V, a 3−μF capacitor for C_{VCC} is required. Conversely, if V_{ON} is set to 1 V above the minimum bootstrap discharge voltage, $V_{BOOT(MIN)}$, C_{VCC} is allowed to discharge over a wider ΔV (17 V − 11 V) and a much smaller capacitor value can be used. Given the same 1 mA, Δt = 3 ms and allowing ΔV = 6 V, the required C_{VCC} capacitor value is reduced to 500 nF; a reduction by a factor of 6. However, the incurred penalty can be quite severe as the SiC MOSFET will be switching with V_{GS} = 11 V. Clearly, having the NCP51705 biased prior to start−up is the preferred approach.

Digital Synchronization and Fault Reporting – XEN

The XEN signal is a 5 V digital representation of the inverse of V_{GS}. For the purpose of reporting driver “status”, it is considered more accurate that the PWM input since it is derived from the SiC gate voltage, propagation delays are greatly decreased. The intent of this signal is that it can be used in half−bridge power topologies as a fault flag and synchronization signal as the basis for implementing cross conduction (overlap) protection. Whenever XEN is HIGH, V_{GS} is LOW and the SiC MOSFET is OFF. Therefore if XEN and the PWM input signal are both HIGH, a fault condition is detected and can be digitally assigned to take whatever precautions might be desired.

Packaging

WBG semiconductors have enabled high−voltage converters to operate much closer to low−voltage (less than 100 V) switching frequencies. For low−voltage converters, the evolution of semiconductor packaging played a key role toward the modern achievement of switching performance seen today. Dual−sided cooling, clip bonding, thermally enhanced power packages and lower inductance, leadless packages are a few examples of silicon MOSFET packaging advancements. Similarly, the size of gate driver IC packages has undergone a tremendous size reduction. Shorter die to lead, bond wire connections combined with molded leadless packages (MLP) have been essential for minimizing parasitic inductance from the driver side. The co−packaging of the driver and MOSFET (DrMOS) is the latest step toward reducing parasitic inductance, raising efficiency and reducing board area. Advancements such as DrMOS are achievable because of the comparable low−voltages involved.

In the high−voltage converter realm, minimum spacing requirements such as creepage and clearance have left high performance SiC MOSFETs stuck in low−performance TO−220 and TO−247 type packages. These packages are well established and have long been an industry standard. They are well suited for industrial applications, robust and easy to heat sink but have higher parasitic inductance due to their long leads and internal bond wires. SiC MOSFETs have now subjected these parasitic inductances to thermal stresses, frequencies and dV/dt rates never before envisioned with high−voltage, silicon transistors. Suffice to say, SiC is providing the stimulus for rethinking high−voltage discrete packaging.

Although not the case with discrete components, a SiC gate driver is able to take full advantage of the same

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packaging advancements used with drivers intended for low−voltage converters. The NCP5170 die is packaged into a 24 pin, 4 × 4 mm, thermally−enhanced MLP as shown in Figure 15.

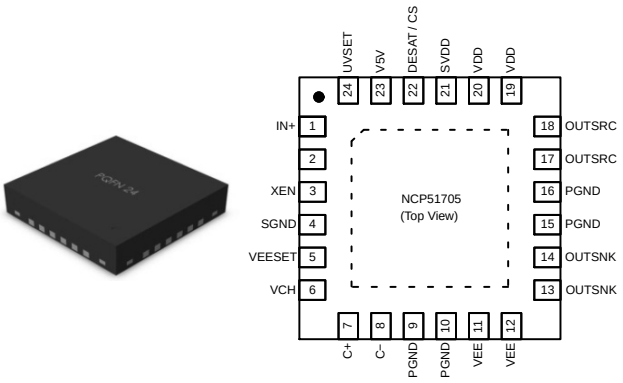

Figure 15. NCP51705 24 pin, 4 × 4 mm, MLP Packaging and Pin Out

All the high−current, power pins are doubled and located on the right−half of the IC. In addition to doubling the pins, each doubled pin connects to the die through internal double bond wires for achieving the lowest possible inductance. All low−power, digital signals are single pins only and are located on the left−half of the IC, providing a convenient, direct interface to the PWM or digital controller.

The bottom of the NCP51705 package consists of an electrically isolated, thermally conductive, exposed pad. This pad is not connected to PGND or SGND but is intended to be connected through thermal vias to an isolated copper PCB land for heat−sinking.

If thermal dissipation becomes a concern, specific attention should be paid to four dominant power dissipation contributors:

1. OUTSRC and OUTSNK losses associated with driving the external SiC MOSFET. These are gate charge related losses proportional to switching frequency. Reducing switching frequency will decrease power dissipation
2. LDO between V_{DD} and V5V, capable of sourcing up to 20 mA. Do not load the V5V any more than biasing a digital isolator or optocoupler
3. LDO between V_{DD} and VCH which is part of the internal charge pump
4. Internal charge pump power switches which can be disabled and replaced with an external negative bias, as mentioned in section Charge Pump–V_{EE} (VEESET)

SYSTEM PERFORMANCE

For V_{DD} > 7 V, the quiescent current ramps up linearly until the set UVLO threshold is crossed. The blue trace shown in Figure 16, represents V_{DD} versus I_{DD} with no input applied (non−switching), $V_{DD(UVLO)}$ = 12 V and no load on the V5V regulator. For 7 V < V_{DD} < 22 V, I_{DD} was measured to be 0.6 mA < I_{DD} < 2.3 mA. The flat line across the middle is a ~1−mA increase in I_{DD} current when V_{DD} crosses the UVLO threshold.

The red trace represent the case where a 100 kHz, 50% pulsed input was applied to IN+ while the internal charge pump is disabled. A 4.99 Ω + 2.2 nF load was used which is the equivalent input for a typical SiC MOSFET. The external source and sink resistance was 3Ω. For 12 V < V_{DD} < 22 V, I_{DD} was measured to be 3.7 mA < I_{DD} < 5.5 mA.

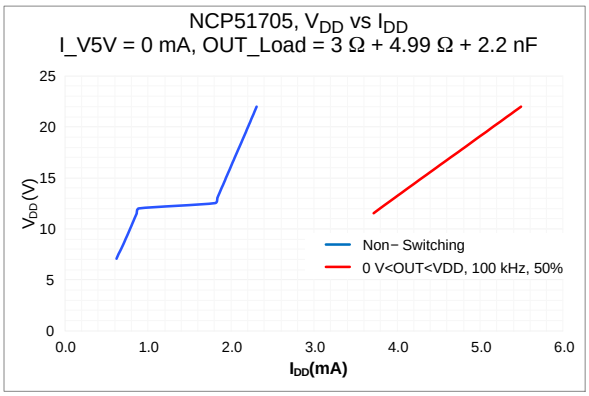

Figure 16. V_{DD} versus I_{DD}, Non−Switching versus Switching

The start−up waveform shown in Figure 17 shows IN + appearing prior to V_{DD}. V_{DD} is rising from 0 V to 20 V, with UVSET = 2 V (not shown) which equates to $V_{DD(UVLO)}$ = 12 V. V_{EE} is set to regulate at −5 V with VEESET = V5V (not shown) which equates to $V_{EE(UVLO)}$ = −4 V. The output is enabled when VEE = −4 V, even though V_{DD} > 12 V (V_{DD} = 15 V). Notice also that OUT (V_{GS}) is less than 20 V for almost 100 µs. Depending on the dV/dt rate of V_{DD} start−up, this time could be longer and therefore, the thermal stress to the SiC MOSFET should be taken into consideration when programming UVSET.

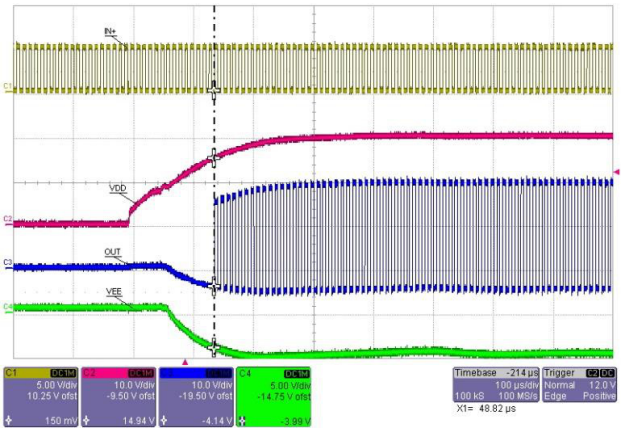

Figure 17. CH1−IN+, CH2−V_{DD}, CH3−OUT, CH4−V_{EE}; $V_{DD(UVLO)}$ = 12 V, $V_{EE(UVLO)}$ = −4 V

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The same start−up waveform is shown in Figure 18 but UVSET = 3 V (not shown) which equates to $V_{DD(UVLO)}$ = 18 V. In this case, OUT (V_{GS}) is enabled when V_{DD} = 18 V, even though V_{EE} < −4 V (V_{EE} = −5 V). Which UVLO is dominant will depend on the dV/dt rate of V_{DD} versus V_{EE}. The key point is that the NCP51705 output is disabled until both, V_{DD} and V_{EE} are above and below their respective UVLO thresholds. Compared to Figure 17, notice the effect that a higher UVLO setting has on OUT (V_{GS}), where the first OUT pulse appears near 20 V and −5 V.

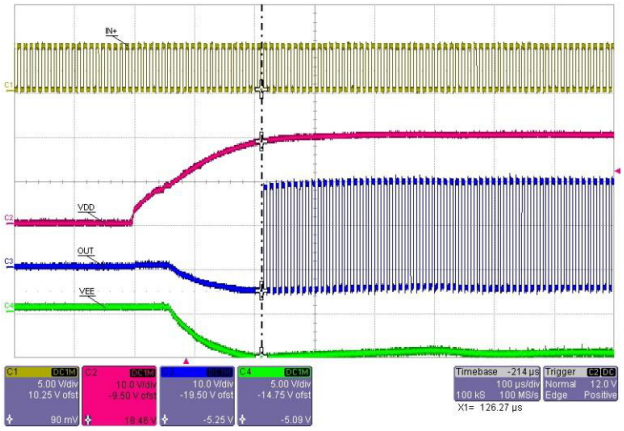

Figure 18. CH1−IN+, CH2−V_{DD}, CH3−OUT, CH4−V_{EE}; $V_{DD(UVLO)}$ = 18 V, $V_{EE(UVLO)}$ = −4 V

The NCP51705 internal charge pump has a slow control loop and the effect of this is seen by the slight undershoot and <400 μs correction observed during V_{EE} start−up shown in Figure 19. Beyond 400 μs, the V_{EE} voltage settles to the regulation set point of −3 V, −5 V or −8 V.

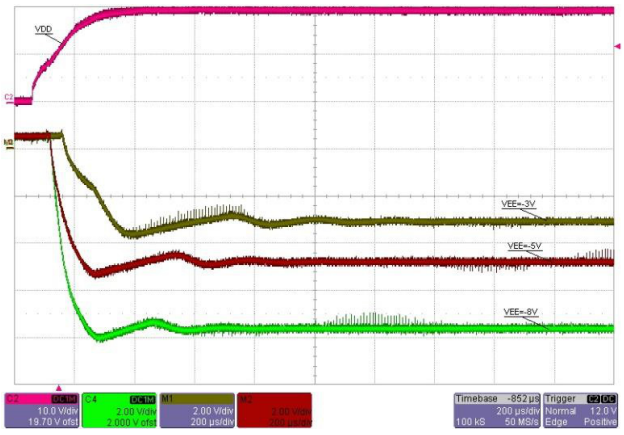

Figure 19. V_{EE} Start−Up

Shutdown operation is smooth with no glitches. As shown in Figure 20, OUT ceases switching and tracks V_{EE} which is unloaded. The discharge time from −5 V to 0 V for V_{EE} is approximately 300 ms.

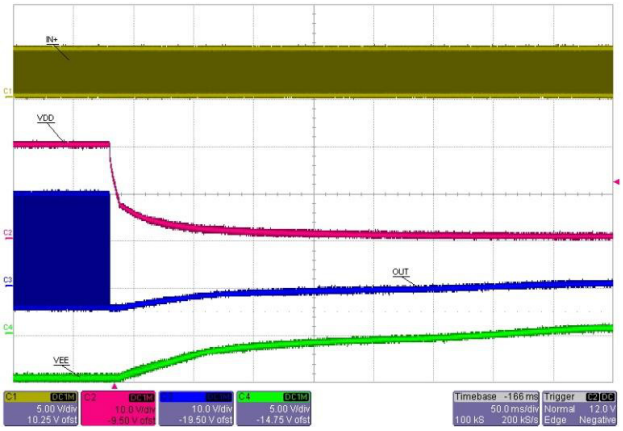

Figure 20. CH1−IN+, CH2−V_{DD}, CH3−OUT, CH4−V_{EE}; Shut−Down

A zoom of the time base from Figure 20 is shown in Figure 21. UVSET is configured for 3 V ($V_{DD(UVLO)}$ = 18 V) and the internal V_{DD} UVLO hysteresis is internally fixed at 1 V. The curser position reveals that V_{DD} = 17 V (18 V−1 V hysteresis), when the output is disabled, even though V_{EE} = −4.5 V (VEESET = V5V) and is still active according it's −4 V UVLO. Although the decay of V_{DD} is slow, a clean termination of the last output pulse can also be observed with no spurious pulses or glitches after UVLO_OFF.

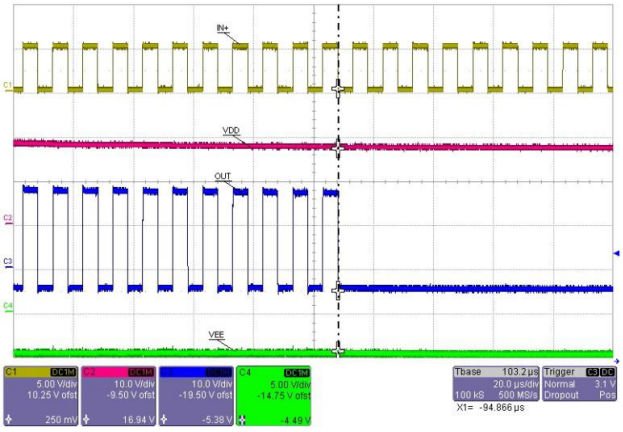

Figure 21. CH1−IN+, CH2−V_{DD}, CH3−OUT, CH4−V_{EE}; Shut−Down, V_{DD}_UVLO(OFF) = 17 V

The turn−on propagation delay is measured from 90% IN+ rising to 10% OUT rising. Although a SiC driver will operate at higher V_{DD}, most MOSFET propagation delays are specified switching into a 1−nF load with V_{DD} = 12 V.

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Figure 22 shows the measured turn−on, propagation delay, under these standard test conditions, to be 19 ns.

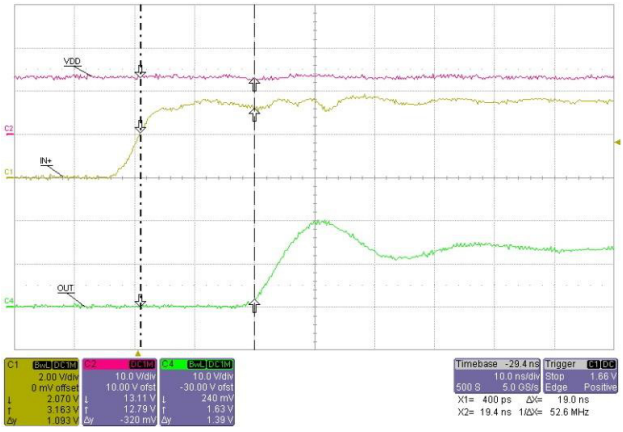

Figure 22. CH1−IN+, CH2−V_{DD}, CH4−OUT; Rising Edge Prop Delay

Similarly, the turn−off propagation delay is measured from 10% IN+ falling to 90% OUT falling. Figure 23 shows the measured turn−off, propagation delay under the same standard test conditions is 22 ns. The output rise and fall times for each edge are approximately 5 ns.

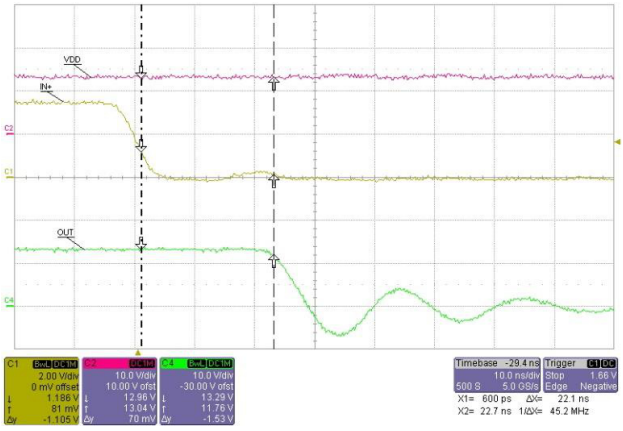

Figure 23. CH1−IN+, CH2−V_{DD}, CH4−OUT; Falling Edge Prop Delay

The DESAT and XEN waveforms are shown in Figure 24 and Figure 25 respectively. Since testing was done to verify IC validation only (no power stage), a 100−pF, fixed capacitor is connected to the DESAT pin. The waveforms shown in Figure 24 indicate DESAT is below the 7.5 V threshold and the output is switching under normal operation. If the IN+ frequency is decreased (increased on−time), the 100−pF DESAT capacitor will be allowed to charge to a higher voltage. This is shown in Figure 25 where the DESAT voltage has reached the 7.5−V threshold. The output trailing edge is terminated before the input voltage switches LOW. A shallow DESAT ramp is used to highlight the fact that no glitches appear on the terminated OUT pulse. In a switching power supply application, a small (<100 pF) external capacitor can be used on the DESAT pin for high−frequency noise filtering.

The XEN signal is the inverse of the OUT signal. Whether the driver is operating normal or under a DESAT fault, the XEN signal is shown to accurately track the inverse OUT signal for either case.

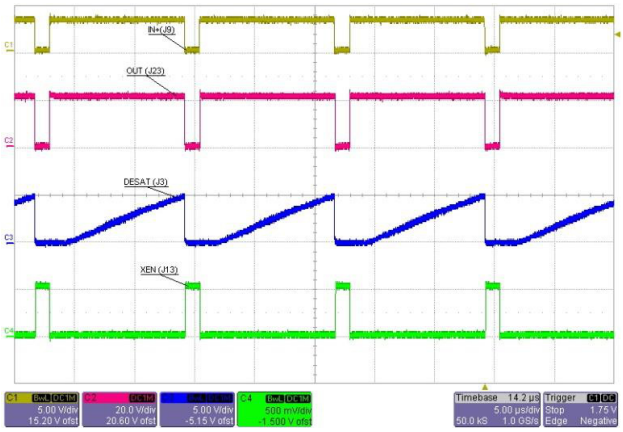

Figure 24. CH1−IN+, CH2−OUT, CH3−DESAT, CH4−XEN; V_{DESAT} < 7.5 V

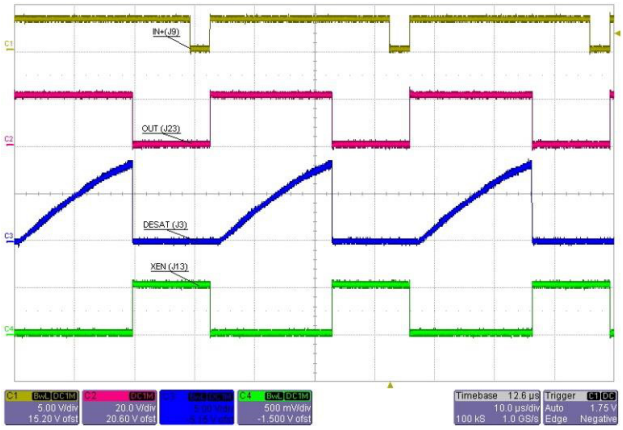

Figure 25. CH1−IN+, CH2−OUT, CH3−DESAT, CH4−XEN; V_{DESAT} = 7.5 V

APPLICATIONS

SiC MOSFETs can penetrate any application spaces where IGBTs are presently used. Some of the more common uses include high−voltage switching power supplies, hybrid and electric vehicle chargers, electric railway transportation, welders, lasers, industrial equipment and environments where high−temperature operation is critical. Two areas that are particularly interesting for SiC are solar inverters and high−voltage data centers. Higher dc voltages are beneficial for reducing wire gauge thickness, junction boxes, interconnections and ultimately minimizing conduction loss thereby increasing efficiency. Most large−scale, photovoltaic systems currently operate from a 1−kV dc bus and the trend is moving toward a 1.5−kV bus. Similarly, data centers using a 380−V distribution network can boost dc voltages as high as 800 V.

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Several fundamental application examples highlighting the NCP5170 are shown as follows.

Low−Side Switching

Figure 26 shows a top level schematic highlighting the NCP51705 used in a low−side switching application. No isolation is shown so the interface between the controller and driver is direct, though this may not always be the case. This schematic is shown to raise awareness of how few external components are required to provide a fully functional, reliable and robust SiC gate drive circuit. It should also be mentioned that although only a single VDD voltage rail is required it should be rated for at least 50 V/ns to prevent spurious current pulses described in the discrete gate drive description in section Discrete SIC Gate Drive. If the VDD voltage rail is provided by a dedicated auxiliary housekeeping power supply, special attention should be given to design a transformer featuring ultra−low, primary−secondary stray capacitance.

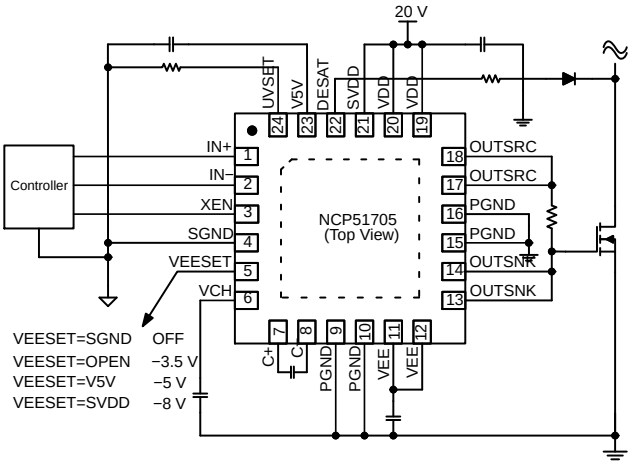

Figure 26. Low−Side Switching Example

Half−Bridge Concept

A more realistic use of SiC MOSFETs can be found in half−bridge power topologies such as the one shown in Figure 27. High power applications tend to prefer isolated drivers for both, the high−side and low−side. This implies the need for two digital isolators. Depending on the amount of IO crossing the isolation boundary, a strong debate for secondary−side control could be made for such applications. In this simplified example, IN+ and IN− (Enable) are the only two signals sourced from the digital controller and XEN is read back from the NCP51705. XEN is can be used as the timing information basis for developing gate drive timing, cross conduction prevention, dead−time adjustment and fault detection. In addition, temperature sensing, thermal management (fan control) and higher levels of fault response may also be done by the digital controller. The V5V from the NCP51705 can be used to power the secondary side of each digital isolator as shown Figure 27.

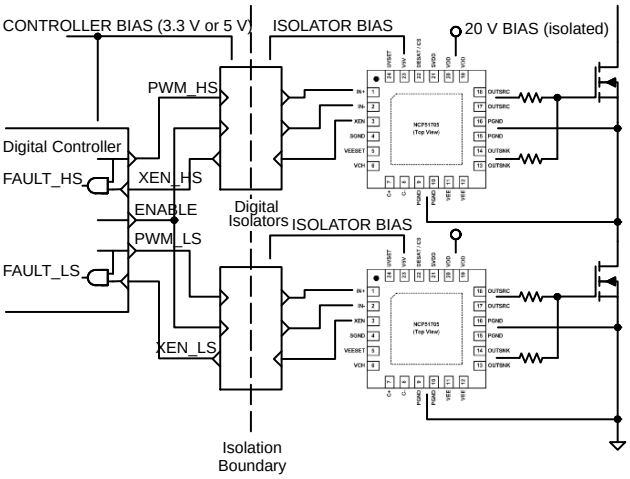

Figure 27. Half−Bride Concept

Quasi Resonant (QR) Flyback

A 100−W, QR flyback converter operating from a wide input range of 300 V < V_{IN} < 1 kV was designed using the NCP1340B1 controller and NCP51705 SiC driver. Converters of this class can typically be found in photovoltaic and industrial applications but when based on IGBT power stages, switching frequencies are in the range of 65 kHz. The schematic shown in Figure 28 is a QR flyback and the frequency is varying between 377 kHz < F_S < 430 kHz, from 100% to 25% load, at V_{IN} = 300 V.

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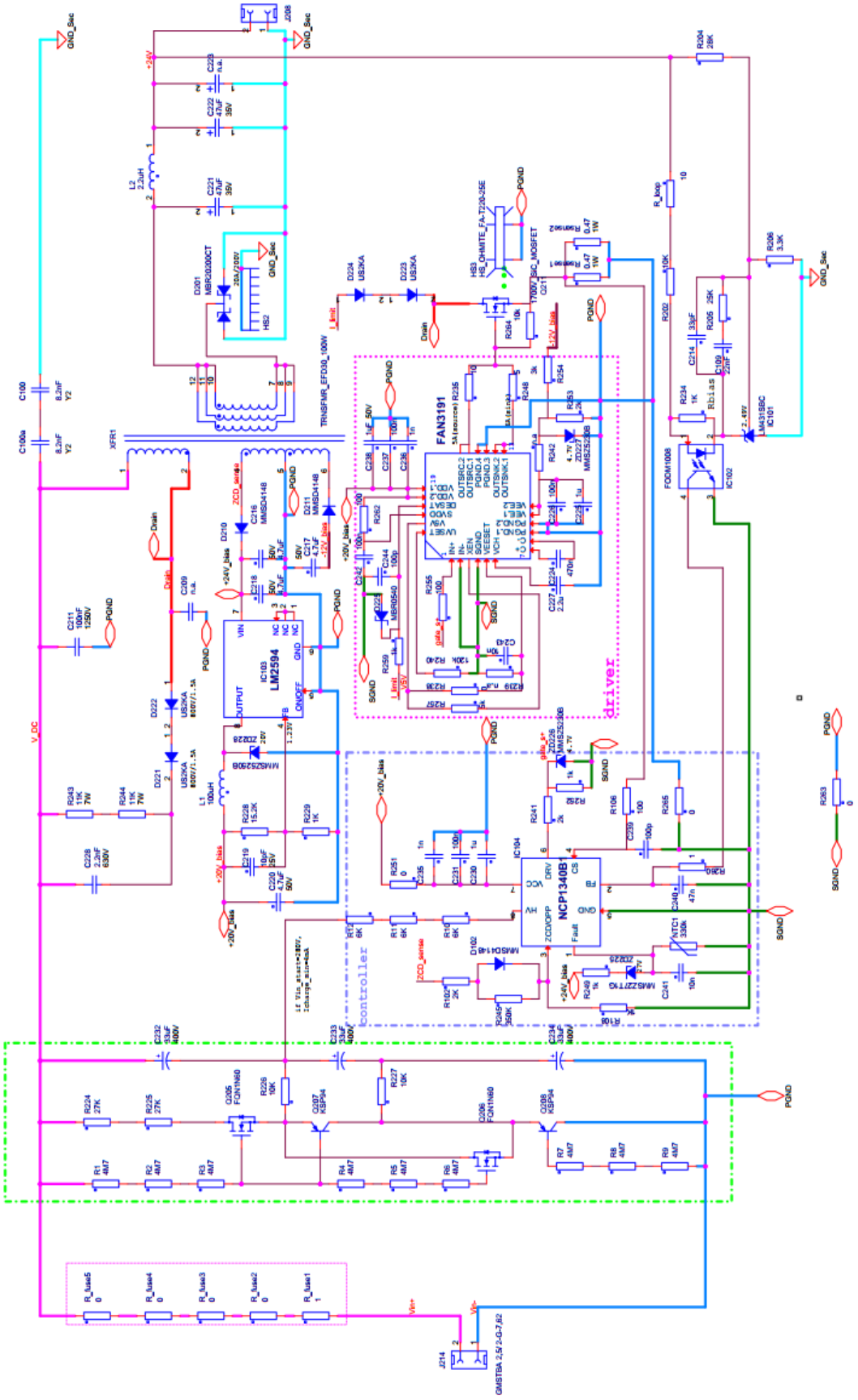

Figure 28. 1000 V to 24 V, 100 W, 400 kHz, QR Flyback

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For V_{IN} = 300 V, the drain−source voltage waveform is the sum of the input voltage and the reflected output voltage. The waveform shown in Figure 29 highlights the converter operating at full duty cycle operation (V_{IN} = 300 V) with 720 V appearing on drain−source of the SiC MOSFET. The V_{DS} rising transition is ~30 ns which equates to dV_{DS}/dt = 24 V/ns. The NCP1340B1, QR control enables a soft, resonant transition and valley switching (“near ZVS” turn−on at minimum V_{DS} resonance) on the V_{DS} falling edge and this is clearly visible on the blue waveform. Because the QR−flyback is a low−side only application and the falling dV_{DS}/dt edge is resonant, it may be possible for the SiC MOSFET to reliably switch between 0 V < V_{GS} < 20 V. Nonetheless, the design shown in Figure 28 opted for switching between −5 V < V_{GS} < 20 V resulting in more robust switching at the slight penalty of increased gate charge.

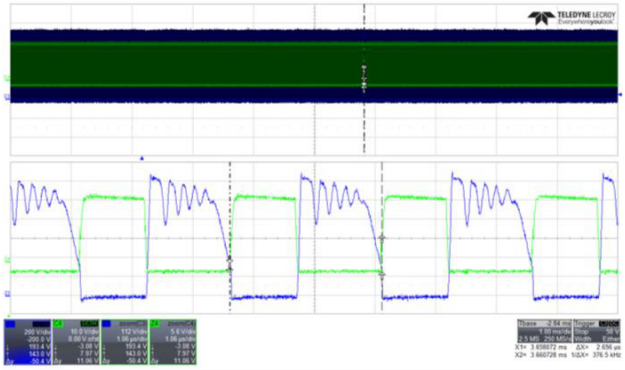

Figure 29. CH3 = V_{DS}, CH4 = V_{GS}; V_{IN} = 300 V, V_{OUT} = 24 V, I_{OUT} = 4 A, F_S = 377 kHz

General Purpose NCP5170 Customer EVB

A general purpose evaluation board (EVB) has been designed for the purpose of evaluating the NCP51705 performance in new or existing designs. The EVB does not include a power stage and is generic from the point of view that it is not dedicated to any particular topology. It can be used in any low−side or high−side power switching application. For bridge configurations two or more of these EVBs can be used at each SiC MOSFET in a totem pole type drive configuration. The EVB can be considered as an isolator + driver + TO−247 discrete module. The EVB schematic is shown in Figure 30.

The focus is to provide an ultra−compact design, where the leads of a TO−247 SiC MOSFET can be connected directly to the printed circuit board (PCB). Figure 31 shows simultaneous, top and bottom views of the EVB next to an adjacent TO−247 package for size scaling.

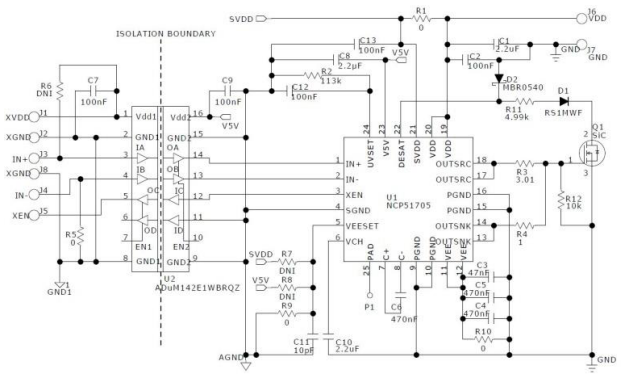

Figure 30. NCP5170 Mini EVB Schematic

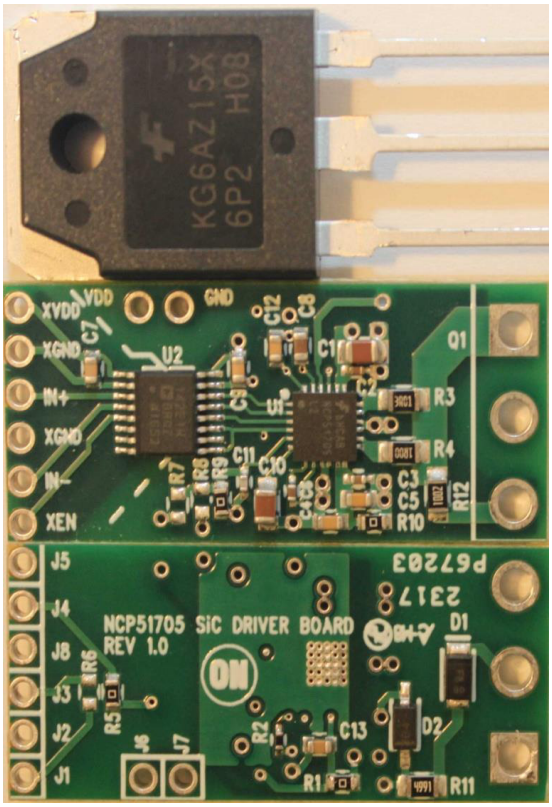

Figure 31. NCP5170 Mini EVB – Top View (35 mm x 15 mm)

When mounting into an existing power supply design and there is available PCB area in front of the TO−247, the EVB can be installed horizontally to the main power board, as shown in Figure 32. If possible, this should is the preferred mounting method.

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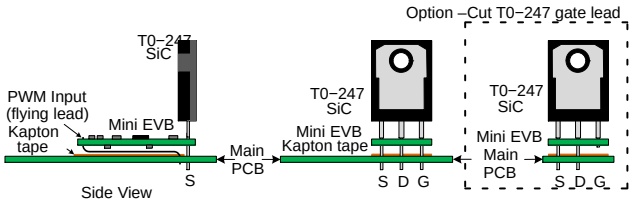

Figure 32. Horizontal EVB Installation

If large components on the main power board prevent horizontal installation, a second option is to install the EVB vertically so that it is parallel to the T0−247 package, or angled slightly away. Installing this way is less preferred due to the close proximity of the driver to the high dV/dt emitted from the TO−247 drain tab. In either case, the back tab of the TO−247 package remains exposed and can be attached to a heat−sink if necessary. Installation and operation details are available in the EVB User Guide.

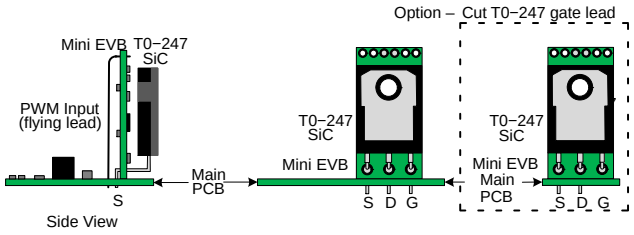

Figure 33. Vertical EVB Installation

The EVB comes initially configured to accept a PWM signal that is positive input logic (IN− connected to GND1). However, IN− can easily be used as an active enable or reconfigured for inverting input logic if desired. The driver output comes preconfigured for 0 V < V_{OUT} < V_{DD} switching. All the connections and resistor placeholders are available to reconfigure VEESET for −3 V, −5 V or −8 V V_{EE} switching. Finally, the UVSET option is preprogrammed for 17−V turn−on operation which is considered a safe level for SiC MOSFETs.

PARAMETRIC PERFORMANCE

MOSFETs and IGBTs are parametrically characterized using the well know double pulse test platform. The double pulse test method essentially applies two pulses to the gate−source of a low−side SiC MOSFET considered to be the device under test (DUT). The DUT is inserted into a socket connected to a clamped inductive switching circuit similar to the one shown in Figure 34.

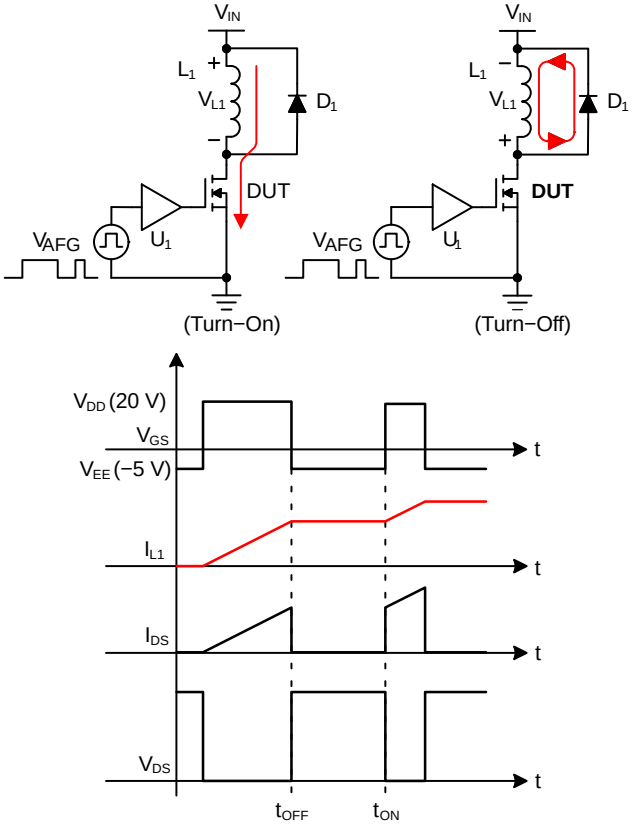

Figure 34. Double Pulse Test Circuit and Waveforms

The on−time of the first pulse is adjusted to achieve a desired peak drain−source current. The inductor is large and the off−time is short enough such that I_{L1} remains nearly constant during the off−time, freewheeling period. As a result, a second, shorter pulse is applied with the same amplitude of drain−source current. This test method allows precise control of I_D and V_{DS} necessary for establishing dynamic switching, parametric performance as well as benchmarking one device against another.

The double pulse test method can also be used to characterize gate driver performance. Leaving the SiC, DUT fixed, various gate drive circuits can be characterized as U_1 becomes the new “DUT.” dV/dt and dI/dt switching performance is compared between the NCP5170 EVB shown in Figure 30 and Figure 31 and the simple optocoupler gate drive circuit shown in Figure 35.

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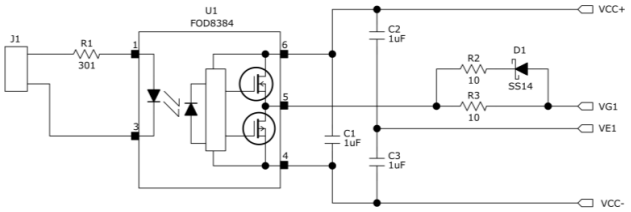

Figure 35. FOD8384 SiC Opto Gate Drive Circuit

The FOD8384 optocoupler driver is capable of withstanding V_{DD} bias up to 30 V, making it well suited for −5 V < V_{GS} < 20 V switching. Similar to the example shown in Figure 8, the FOD8384 driver is not a complete SiC MOSFET gate drive circuit. Therefore, since features between the two circuits are not comparable, test results and comparisons are limited to dynamic switching only.

The rising and falling VGS waveforms for both circuits are show for comparison in Figure 36 and Figure 37 respectively. Both circuits are using 1 Ω source and sink gate resistors. These gate drive edges are shown driving a 1.2 kV, SiC MOSFET with 600 V present on V_{DS} and 30 A flowing through I_D. The NCP51705, V_{GS} rising edge appears as purely resistive from −5 V < V_{GS} < 10 V and then capacitive *RC* charging from 10 V < V_{GS} < 20 V. This is indicative of the NCP51705, 6 A_{PK} sourcing current compared to the 1 A_{PK} sourcing current from the FOD8384. As a result the NCP51705 has a V_{GS} rise time of 37.5 ns, compared to 57.6 ns for the FOD8384 switching under the same test conditions. Similarly, the V_{GS} fall time for the NCP51705 is 25.2 ns, compared to 34.5 ns for the FOD8384.

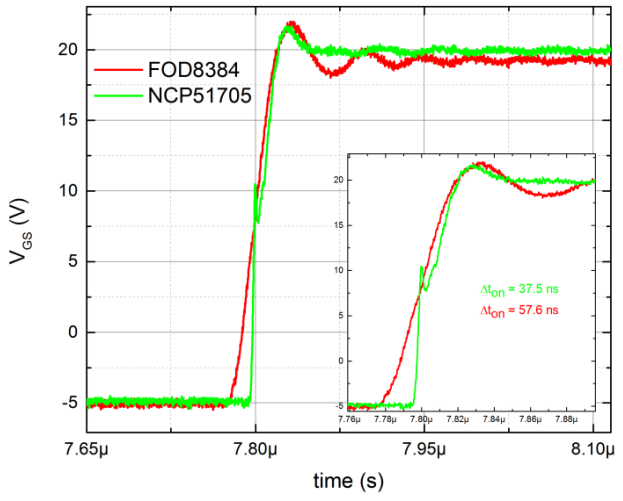

Figure 36. V_{GS} Rising Edge Comparison

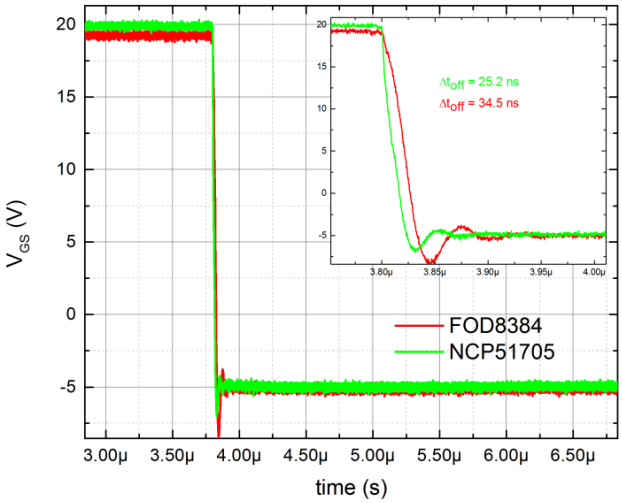

Figure 37. V_{GS} Falling Edge Comparison

A well designed gate driver IC includes low source and sink impedance so that the SiC MOSFET drain can be accurately controlled by the gate. Secondly, minimizing driver output impedance is essential for allowing the highest natural dV/dt of the SiC MOSFET. The natural dV/dt limit of a SiC MOSFET is inversely proportional to R_{LO} + R_{GATE} + R_{GI}. When R_{LO} is higher than necessary, the natural dV/dt limit of the SiC MOSFET is lowered. This makes the device more susceptible to dV/dt induced turn−on and limits the amount of dV_{DS}/dt control that can be achieved by the selection of R_{GATE}. The NCP51705 V_{DS} waveforms shown in Figure 38 reveal the high degree of dV_{DS}/dt control that is possible by simply varying R_{GATE}. For R_{GATE} = 1 Ω, dV_{DS}/dt = 72 V/ns. Increasing R_{GATE} from 1 Ω to 15 Ω reduces dV_{DS}/dt from 72 V/ns to 68 V/ns. This demonstrates that a much higher R_{GATE} can be used to obtain very fine incremental steps toward reducing dV_{DS}/dt, if desired.

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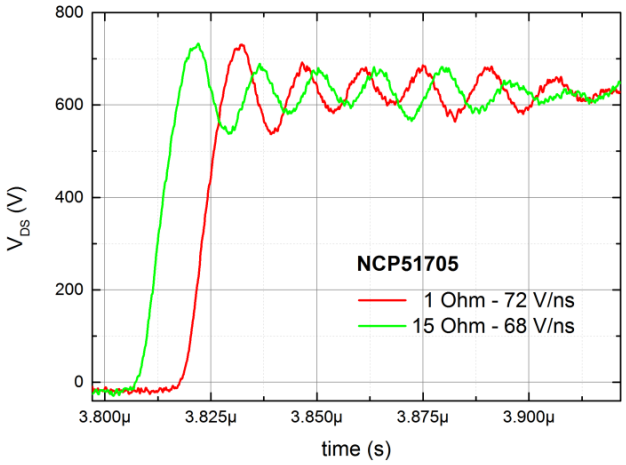

Figure 38. NCP51705 V_{DS} Rising Edge, Vary Gate Resistance

The same experiment was completed using the FOD8384 opto gate driver. Notice from the waveforms shown in Figure 39, a change in R_{GATE} from 1 Ω to 15 Ω, results in a dV_{DS}/dt rate change by more than 2:1. dV_{DS}/dt control is more influenced by smaller changes in R_{GATE} due to the higher output impedance of the FOD8384 driver. Also, notice the dV_{DS}/dt rise of the NCP51705 is more linear comparatively.

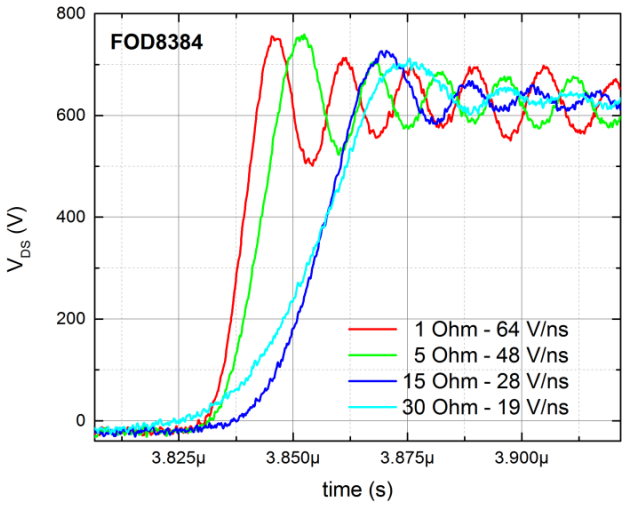

Figure 39. FOD8384 V_{DS} Rising Edge, Vary Gate Resistance

The waveforms shown in Figure 40 compare V_{DS} for each driver switching the same load from −5 V < V_{GS} < 20 V with R_{GATE} = 1 Ω. The dV_{DS}/dt rates are comparable at 72 V/ns verses 64 V/ns. The NCP51705 shows better damping and lower amplitude ringing.

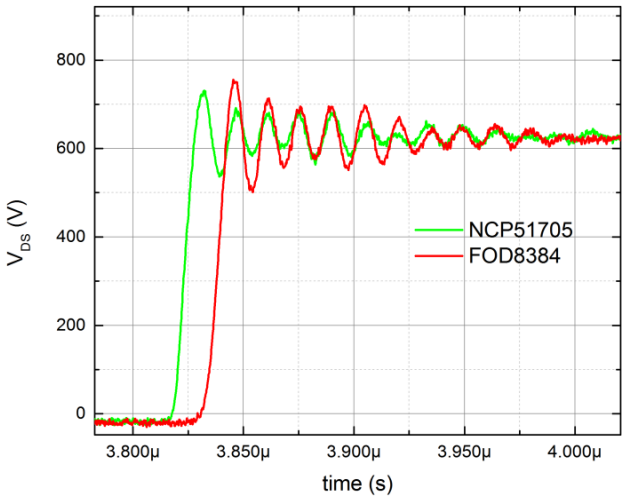

Figure 40. V_{DS} Rising Edge Compare, 1 Ω Gate Resistance

Another way the NCP51705 enables dV_{DS}/dt control is by varying the level of negative amplitude of V_{EE}. This can be done by configuring the VEESET pin according to Table 3 or by using an external negative DC power supply applied to V_{EE}. The waveforms in Figure 41 show the change in dV_{DS}/dt as V_{EE} is varied between −6 V < V_{EE} < 0 V. Notice the strong inflection and capacitive nature at low V_{DS}, for the case that 0 V < V_{GS} < 20 V. This is due to some residual gate charge from the SiC MOSFET not being fully turned off and highlights the importance of driving V_{GS} negative during turn−off.

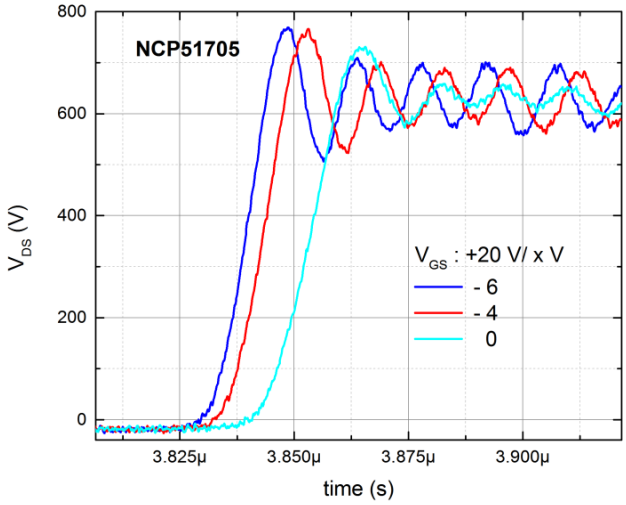

Figure 41. NCP51705 V_{DS} Rising Edge, Vary V_{EE}

The drain current measurements shown in Figure 42 were taken using a Pearson current probe. The NCP51705 current

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is falling at dI_D/dt = 3.2 A/ns yet exhibits less ringing compared to the FOD8384 drive circuit. The faster dI_D/dt of the NCP51705 correlates well to the V_{GS} falling edge waveforms shown in Figure 37.

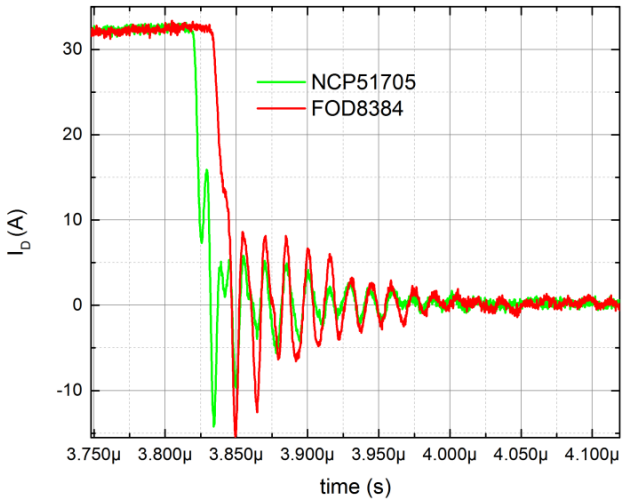

Figure 42. I_D Falling Edge Comparison

The double pulse test methodology is a test procedure traditionally used to characterize dynamic switching performance of discrete power semiconductor devices. Since the applied V_{DS} and initial I_D can be accurately controlled during turn−on and turn−off, this measuring technique has been shown to be a reliable method for characterizing gate driver IC performance in a clamped inductive switching application circuit.

CONCLUSION

This paper has highlighted some of the unique characteristics of SiC MOSFETs that must be considered when designing a high performance gate drive circuit. The low g_m or modest transconductance associated with SiC MOSFETs is particularly troublesome from a gate drive point of view. General purpose low−side gate drivers are often used but lack the necessary functions to drive a SiC MOSFET efficiently and reliably. Wide market adoption of SiC MOSFETs is, to some degree, attached to their ease of use. The NCP5170 offers designers a simple, high−performance, high−speed, solution for driving SiC MOSFETs efficiently and reliably.

Steve Mappus is a Member of the Technical Staff working as a Principal Applications Engineer in Advanced Power Conversion group from **onsemi** located in Bedford, NH, USA. In his current role, he is responsible for technology development related to power−supply controllers and MOSFET gate drive ICs. He has more than 25 years of power supply design experience, including ten years designing military and commercial power systems for avionic applications. He has spent the last fifteen years working within the field of power management semiconductors, specializing in Systems and Applications Engineering. His areas of interest include high−power converter topologies, soft−switching converters, synchronous rectification, high−frequency power conversion, WBG devices and power factor correction.

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