TEA18361T

GreenChip SMPS control IC

Rev. 2 — 12 December 2013 Product data sheet

1. General description

The TEA18361T is a controller IC for low-cost Switched Mode Power Supplies (SMPS). It is intended for flyback topologies. The built-in green functions provide high efficiency at all power levels.

At high power levels the flyback operates in Quasi-Resonant (QR) mode. At lower power levels, the controller switches to Frequency Reduction (FR) or Discontinuous Conduction Mode (DCM) and limits the peak current to approximately 25 % of the maximum peak current. Valley switching is used in all operating modes.

At low power levels, when the flyback switching frequency drops below 25 kHz, the flyback converter switches to burst mode. A special burst mode has been integrated which reduces the opto current to a minimum level, ensuring high efficiency at low power and excellent no load power performance. As the switching frequency in this mode has a minimum value of 25 kHz while the burst frequency is below 800 Hz, the frequencies are outside the audible range. During the non-switching phase of the burst mode, the internal IC supply current is minimized for further efficiency optimization.

The TEA18361T includes an accurate OverPower Protection (OPP). The OPP enables the controller to operate in overpower situations for a limited amount of time. If the output is shorted, the system switches to low-power mode where the output power is limited to a lower level.

The TEA18361T is manufactured in a high-voltage Silicon-On-Insulator (SOI) process. The SOI process combines the advantages of a low-voltage process (accuracy, high-speed protection, functions, and control), while maintaining the high-voltage capabilities (high-voltage start-up, low standby power, and an integrated X-capacitor discharge function).

The TEA18361T enables low-cost, highly efficient and reliable supplies for power requirements up to 75 W to be designed with a minimum number of external components.

All values mentioned in this data sheet are typical values, unless otherwise specified.

2. Features and benefits

2.1 General features

- SMPS controller IC for low-cost applications
- Large supply voltage range (up to 30 V)
- Integrated high-voltage start-up
- Continuous VCC regulation during start-up and protection via the HV pin, allowing a minimum VCC capacitor value
- Reduced opto current in burst mode enabling low no load power consumption
- Operating frequencies in all operating modes are outside the audible area
- Integrated X-capacitor discharge; NXP Semiconductors patented (Patent reference: 81512184EP01 (Patent pending))
- Adjustable soft start
- Power-down mode via the PROTECT pin1

2.2 Green features

- Low supply current during normal operation (0.6 mA without load)
- Low supply current during non-switching state in burst mode (0.2 mA)
- Valley switching for minimum switching losses
- Frequency reduction with fixed minimum peak current to maintain high efficiency at low output power levels

2.3 Protection features

- Mains voltage independent OverPower Protection (OPP)
- OverTemperature Protection (OTP)
- Integrated overpower time-out
- Integrated restart timer for system fault conditions
- Continuous mode protection using demagnetization detection
- Accurate OverVoltage Protection (OVP)
- General-purpose input for latched protection; for use with system OverTemperature Protection (OTP)
- Driver maximum on-time protection

3. Applications

- Applications requiring efficient and cost-effective power supply solutions up to 75 W

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA18361T/1	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

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5. Block diagram

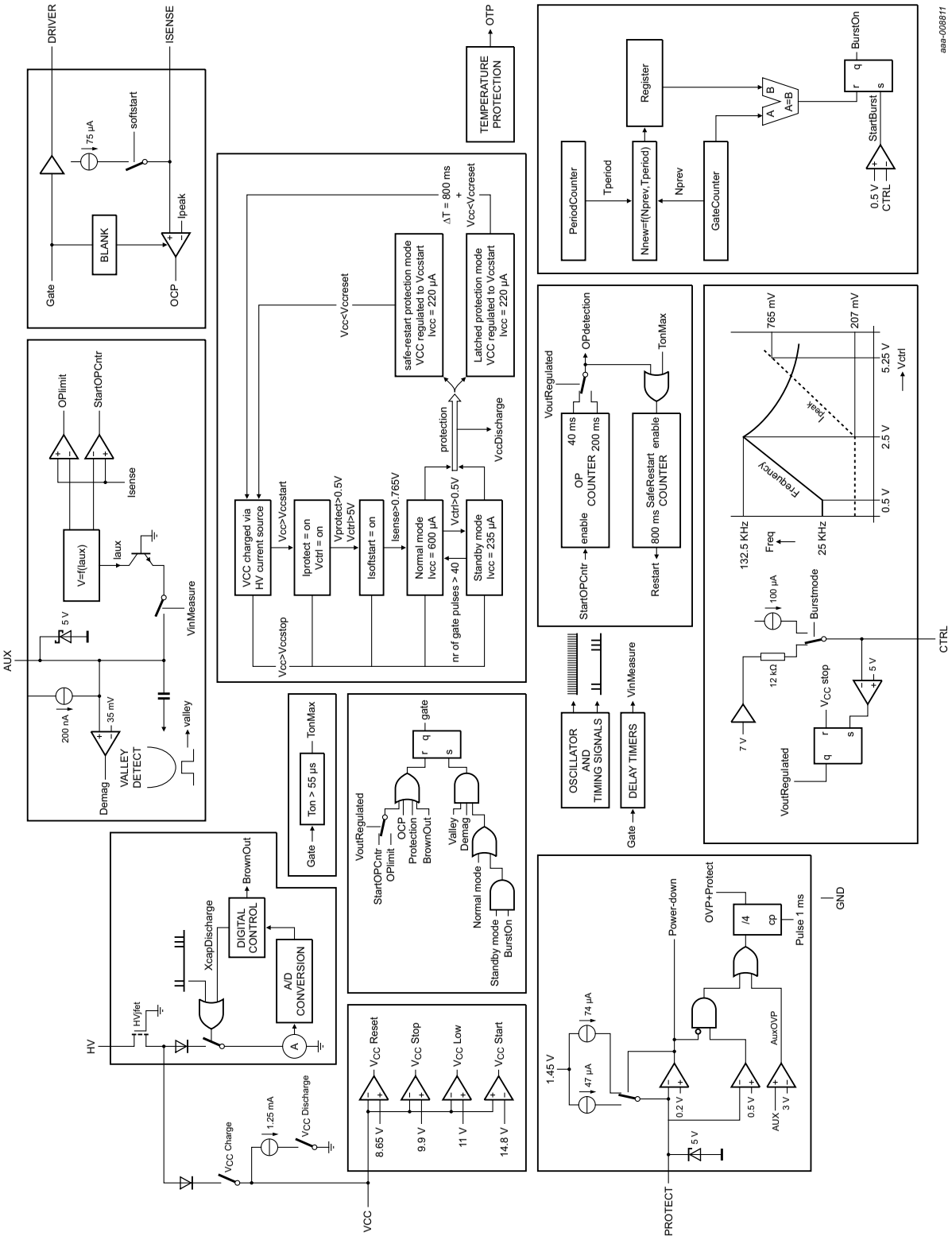


Fig 1. Block diagram

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6. Pinning information

6.1 Pinning

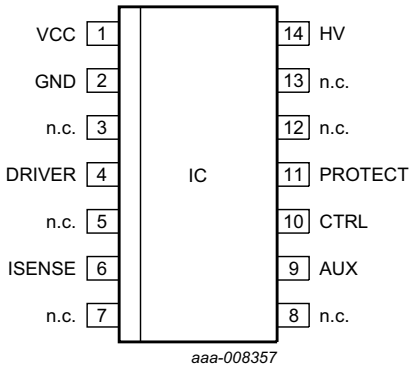


Fig 2. TEA18361T pinning diagram

6.2 Pin description

Table 2. Pin descriptions

Pin	Pin number	Description
VCC	1	supply voltage
GND	2	ground
n.c.	3	not connected
DRIVER	4	gate driver output
n.c.	5	not connected
ISENSE	6	current sense input
n.c	7	not connected
n.c.	8	not connected
AUX	9	auxiliary winding input for demagnetization timing, valley detect, overpower correction, and OVP
CTRL	10	control input
PROTECT	11	general purpose protection input; pin for power-down mode
n.c.	12	high-voltage safety spacer; not connected
n.c.	13	high-voltage safety spacer; not connected
HV	14	high voltage start-up; active X-capacitor discharge

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7. Functional description

7.1 General control

Figure 3 shows a typical configuration of the TEA18361T, including flyback circuit controller.

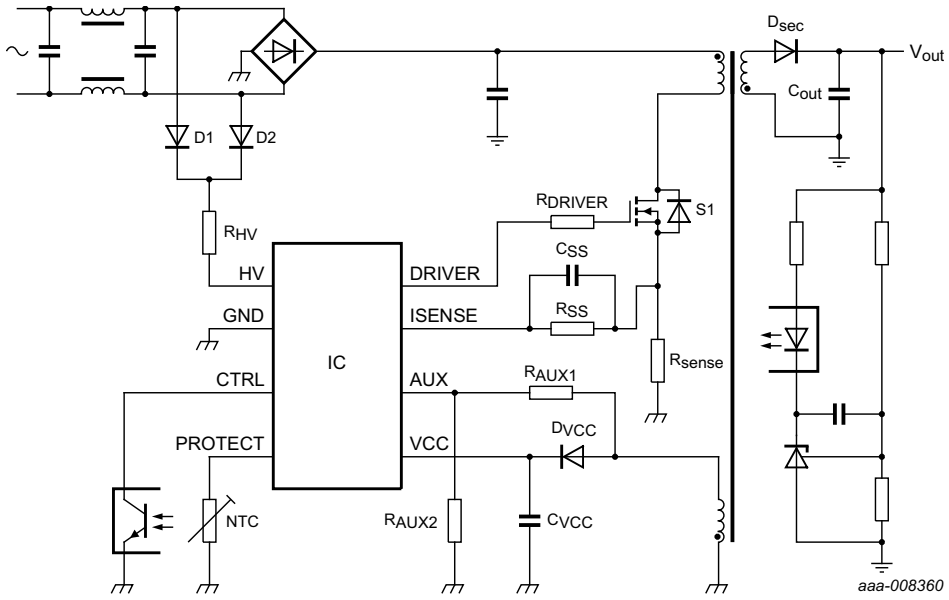


Fig 3. Typical TEA18361T configuration

7.1.1 Start-up and UnderVoltage LockOut (UVLO)

Initially, the capacitor on the VCC pin is charged from the high-voltage mains using the HV pin. As long as V_{CC} is below $V_{startup}$, the IC current consumption is minimized to 40 μA.

When V_{CC} reaches the $V_{startup}$ level, the control logic activates the internal circuitry. The IC then waits for the PROTECT pin to reach $V_{det(PROTECT)} + V_{det(hys)PROTECT}$, the CTRL pin to reach $V_{startup(CTRL)}$, and the mains voltage to increase to above the brownin level. When all these conditions are met, the soft start capacitor on the ISENSE pin (C_{SS} in Figure 3) is charged. The system starts switching. In a typical application, the supply voltage is taken over by the auxiliary winding of the transformer.

During the start-up period, the VCC pin is continuously regulated to the $V_{startup}$ level using the HV charge current until the output voltage is at its regulation level, which is detected via the CTRL pin. In this way the VCC capacitor value can be limited. Due to the limited current capability from the HV pin and depending on the mains voltage, the voltage on pin VCC can still drop slightly during the start-up period.

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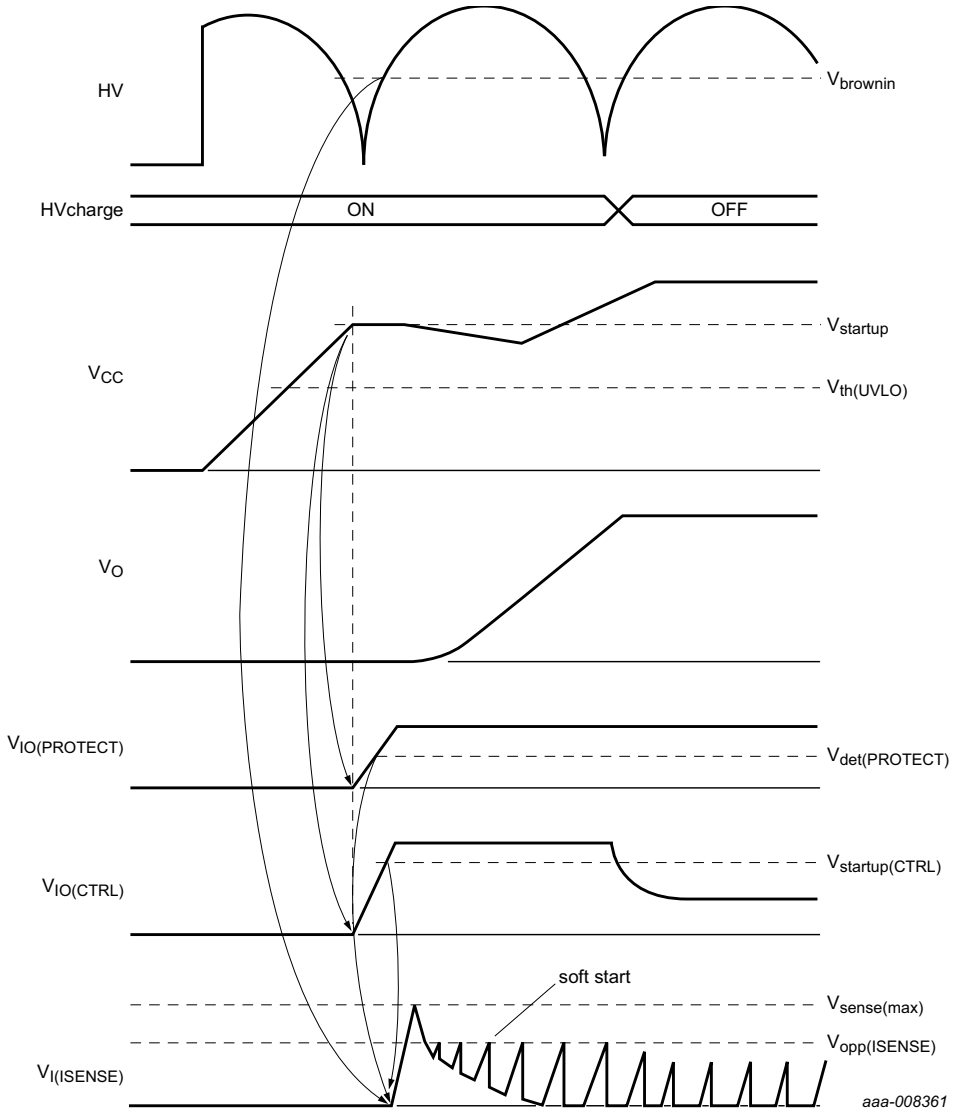


Fig 4. Start-up sequence and normal operation

7.2 Modes of operation

The TEA18361T operates in quasi-resonant mode, discontinuous conduction mode or burst mode (see Figure 5). The auxiliary winding of the flyback transformer provides demagnetization and valley detection.

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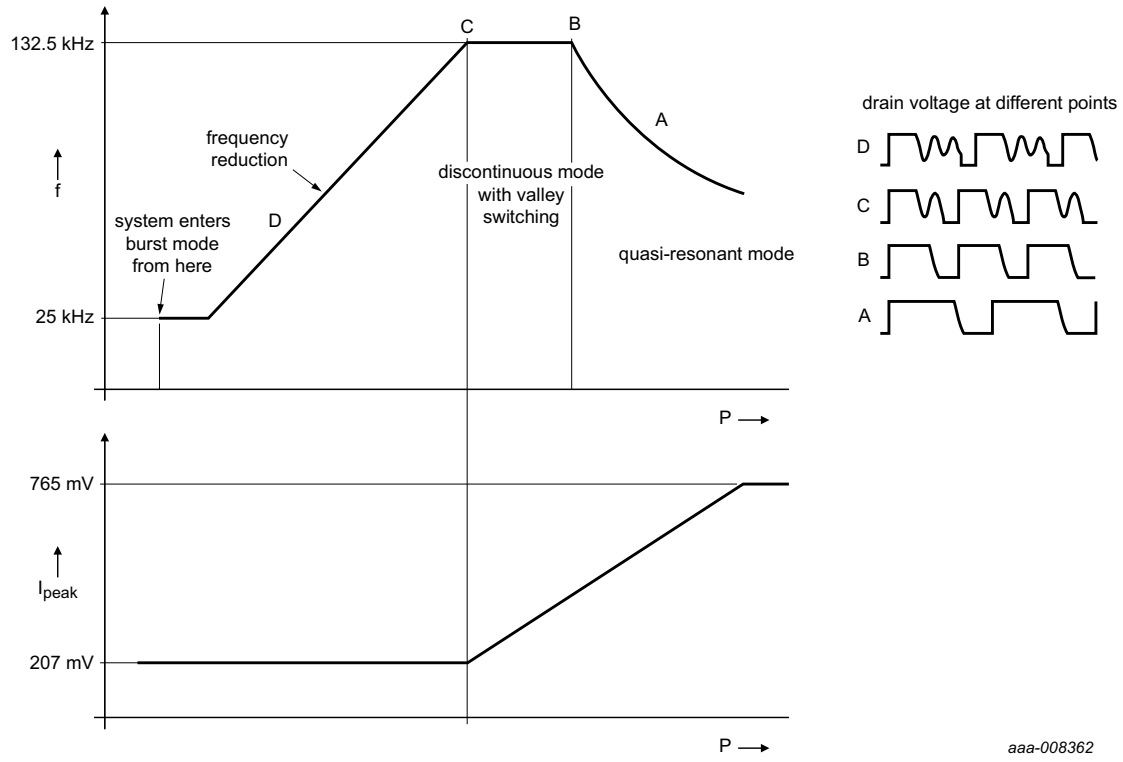


Fig 5. Modes of operation

At high output power the converter operates in quasi-resonant mode. The next converter cycle starts after demagnetization of the transformer and detection of the valley. In quasi-resonant mode switching losses are minimized because the external MOSFET is switched on while the drain-source voltage is minimal.

To prevent high-frequency operation at lower loads, the quasi-resonant operation switches to Discontinuous Conduction Mode (DCM) operation with valley skipping once the frequency reaches its maximum. This frequency limit reduces the MOSFET switch-on losses and conducted EMI.

At medium power levels, the controller enters Frequency Reduction (FR) mode. A Voltage Controlled Oscillator (VCO) controls the frequency. The minimum frequency in this mode is reduced to 25 kHz. During FR mode, the primary peak current is kept at an adjustable minimum level to maintain high efficiency. Valley switching is also active in this mode.

At low power, the converter enters the burst mode. In burst mode, the minimum switching frequency is 25 kHz.

7.3 Supply management

All internal reference voltages are derived from a temperature compensated on-chip band gap circuit. Internal reference currents are derived from a trimmed and temperature-compensated current reference circuit.

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7.4 Mains voltage measuring

In a typical application, the mains input voltage is measured using the HV pin. Once per ms the mains voltage is measured by pulling down the HV pin to ground and measuring its current. This current then reflects the input voltage.

The system determines if the mains voltage exceeds the brownin level or it is disconnected using an analog-to-digital converter and digital control (see Figure 1).

Once the mains is above the brownin level, the system is allowed to start switching (see Figure 6).

If the mains voltage is continuously below the brownout level for a period of at least 30 ms, a brownout is detected and the system immediately stops switching. This period is required to avoid that the system stops switching due to the zero crossings of the mains or during a short mains interruption.

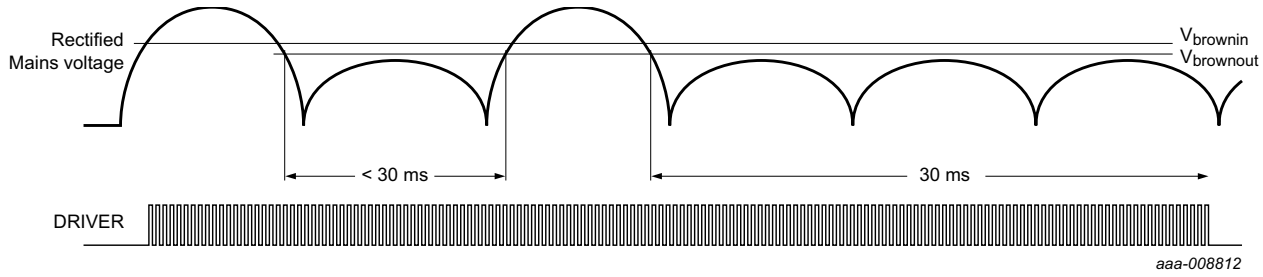


Fig 6. Mains voltage measuring

When the mains voltage is measured by pulling the HV pin to ground, the digital control calculates if there is a positive dV/dt at the mains. A positive dV/dt implies that a mains is connected.

Once a mains is detected, the measuring of the mains input voltage is stopped for a period of 6 ms to improve efficiency. In burst mode this waiting period is enlarged to 97 ms to improve efficiency.

A positive dV/dt is measured when succeeding samples cross the brownin level ($I_{bi(HV)}$) or the mains high level ($I_{IH(HV)}$; see Figure 7).

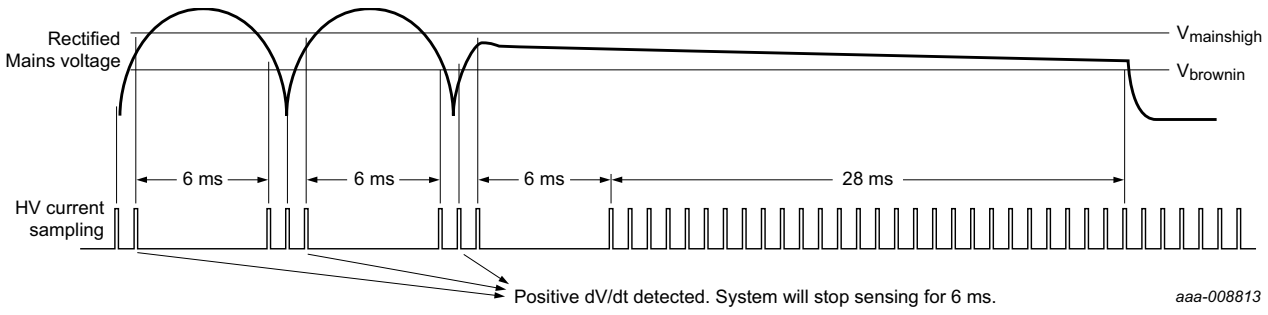


Fig 7. Detecting mains connection by +dV/dt

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If the system does not detect a positive dV/dt for 28 ms, it assumes that the mains is disconnected. In that case the HV pin is continuously pulled to ground, discharging the external X-capacitor.

7.5 Auxiliary winding

The VCC pin is connected via a diode and a capacitor to the auxiliary winding to efficiently supply the control IC.

To detect demagnetization, valley, and input and output voltage, the auxiliary winding is connected to the AUX pin via a resistive divider (see Figure 3). Each switching cycle is divided in sections. During each section the system knows if the voltage or current out of the AUX pin reflects the demagnetization, valley, input or output voltage (see Figure 8).

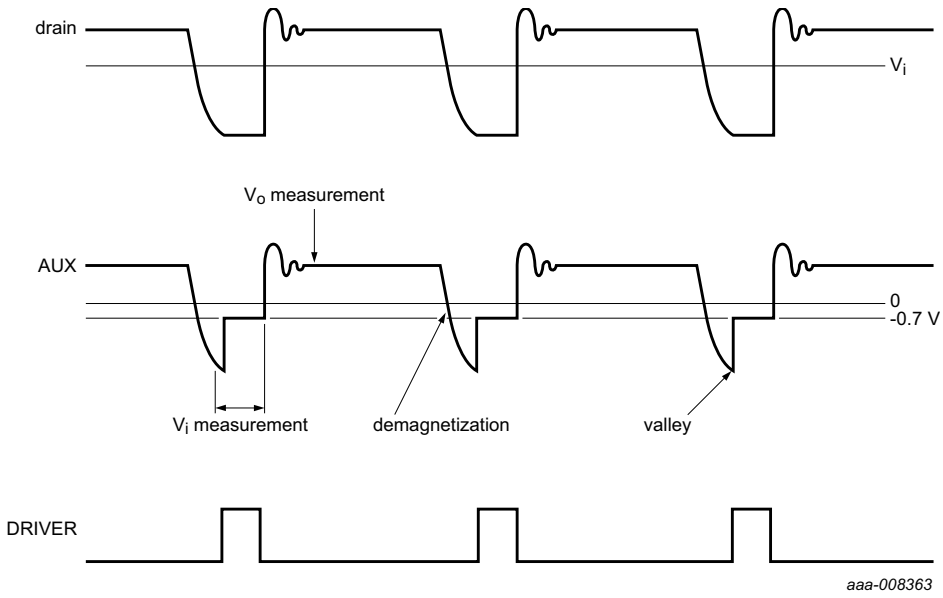


Fig 8. AUX pin used for demagnetization, valley, and input and output voltage measurement

When the external MOSFET is switched on, the voltage at the auxiliary winding reflects the input voltage. The AUX pin is clamped to −0.7 V. The output current is a measure of the input voltage. This current value is internally used for an accurate OPP.

The demagnetization, valley and output voltages are measured as a voltage on the AUX pin. In this way, the input voltage measurement and OVP can be adjusted independently.

7.6 Protection

If a protection is triggered, the controller stops switching. Depending on the protection triggered and the IC version, the protection causes a restart or latches the converter to an off state (See Table 3).

To avoid false triggering, some protections have a built-in delay.

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Table 3. Protections

Protection	Delay	Action	V_{CC} regulated
AUX open	no	wait until AUX is connected	no
brownout	30 ms	wait until $V_{mains} > V_{brownin}$	yes
maximum on-time	no	safe restart 800 ms	yes
OTP internal	no	latch	yes
OTP via the PROTECT pin	2 ms to 4 ms	latch	yes
OVP via the AUX pin	4 driver pulses[1]	latch	yes
overpower compensation	no	via AUX; cycle-by-cycle	-
overpower time-out	40 ms or 200 ms	safe restart 800 ms	yes
overpower + UVLO	no	safe restart 800 ms	yes
overcurrent protection	blanking time	cycle-by-cycle	no
UVLO	no	Wait until $V_{CC} > V_{startup}$	yes

[1] When the voltage on the PROTECT pin is between $V_{th(pd)(PROTECT)}$ and $V_{det(PROTECT)}$, the clock of the delay counter is changed from the driver pulse to 1 ms internal pulse.

When the system stops switching, the VCC pin is not supplied via the auxiliary winding anymore. Depending on the protection triggered, the VCC is regulated to $V_{startup}$ via the HV pin (see Table 3).

Releasing the latched protections or shortening the safe restart timer can be achieved by removing or shorting the mains voltage. This is called a fast latch reset. It is mainly used to shorten the test time in production (See Section 7.6.8).

7.6.1 OverPower Protection (OPP)

The overpower function is used to realize a maximum output power which is nearly constant over the full input mains.

The overpower compensation circuit measures the input voltage via the AUX pin and outputs two reference voltages (see Figure 1). If the measured voltage at the ISENSE pin exceeds the highest reference voltage ($V_{opc(ISENSE)}$) the DRIVER output is pulled low. If the measured ISENSE voltage exceeds the lower reference voltage ($V_{opp(ISENSE)}$), the OverPower counter starts. Both reference voltages depend on the measured input voltage. In this way the system allows 150 % overpower over the rated power on a cycle-by-cycle base. 100 % overpower triggers the overpower counter of 200 ms. Figure 9 shows the overpower protection curves.

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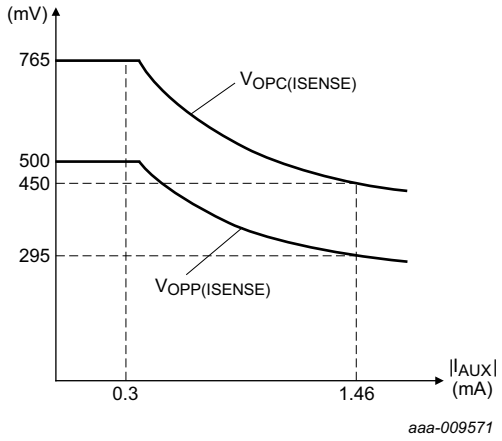


Fig 9. Overpower protection curves

During system start-up, the maximum overpower is limited to 100 % and the maximum time-out period is lowered to 40 ms. Once the output voltage is within its regulation level (voltage on the CTRL pin is below 5 V), the maximum overpower is switched to 150 % and the maximum time-out period returns to 200 ms limiting the output power to a minimum at a shorted output. Lowering the maximum output power and shortening the overpower timer ensure that the input power of the system is limited to < 5 W at a shorted output.

Due to the limited output power, the output voltage drops if the load requires more than 150 %. As a result, the V_{CC} voltage drops as well and UVLO can be triggered. To retain the same response in an overpower situation (whether UVLO is triggered or not) the system enters the protection mode (latch or safe restart) when overpower + UVLO is detected. The system entering the protection mode does not depend on the value of the OP counter.

7.6.2 OverVoltage Protection (OVP)

An accurate output OVP is implemented by measuring the voltage at the AUX pin during the secondary stroke. As the auxiliary winding voltage is a well-defined replica of the output voltage, the OVP level can be adjusted by the external resistor divider ratio $R_{AUX2} / (R_{AUX1} + R_{AUX2})$.

An internal counter of 4 gate pulses prevents false OVP detection which can occur during ESD or lightning events.

7.6.3 Protection input (PROTECT pin)

The PROTECT pin is a general purpose input pin. It can be used to switch off the converter (latched protection). The converter is stopped when the voltage on this pin is pulled below $V_{det(PROTECT)}$ (0.5 V).

The PROTECT pin can be used to create an OTP function by connecting a Negative Temperature Coefficient (NTC) resistor to this pin. A voltage on the PROTECT pin lower than 0.5 V detects overtemperature. The PROTECT current (maximum 74 μA) flowing through the external NTC resistor creates the voltage. The PROTECT voltage is clamped

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to maximum 1.45 V. At room temperature the resistance value of the NTC resistor is much higher than at high temperature. Due to the clamp, the current out of the PROTECT pin is 1.45 V divided by the resistance, which is significantly lower than 74 μA.

A filter capacitor can be connected to this pin.

To avoid false triggering, an internal filter of 2 ms to 4 ms is applied.

The PROTECT pin can also be a power-down mode pin (see Section 7.10).

7.6.4 OverTemperature Protection (OTP)

Integrated OTP ensures that the IC stops switching if the junction temperature exceeds the thermal temperature shutdown limit. OTP is a latched protection.

7.6.5 Maximum on-time

The controller limits the on-time of the external MOSFET to 55 μs. When the on-time is longer, the IC stops switching and enters safe restart mode.

7.6.6 Safe restart

If a protection is triggered and the system enters the safe restart mode, the system restarts after 800 ms. Because the system is not switching, the VCC pin is supplied from the mains via the HV pin.

After the 800 ms, the control IC measures the mains voltage. if the mains voltage exceeds the brownin level, the control IC activates the PROTECT pin current source and the internal voltage sources connected to the CTRL pin. Once the voltages on these pins reach a minimum level, the soft start capacitor on the ISENSE pin is charged and the system starts switching again.

The V_{CC} is continuously regulated to the $V_{startup}$ level until the output voltage is within the regulation level again.

7.6.7 Latched protection

If a protection is triggered and the system enters the latched protection mode, the V_{CC} is continuously regulated to the $V_{startup}$ level via the HV current source. As long as the AC voltage remains, the system does not switch.

Removing the mains for a short time is the only possibility to restart the system.

7.6.8 Fast latch reset

Fast latch reset is a simple and fast method to reset the system when it is in latched protection mode or safe restart mode. This function is used during production testing.

When the latched protection mode or safe restart mode is triggered, the voltage on pin VCC is fast discharged by an internal current source ($I_{CC(dch)}$); see Figure 10). The fast discharge avoids an additional waiting period if the VCC voltage is high. When shorting the mains, the waiting period is only the time of the discharge from $V_{startup}$ to V_{rst}.

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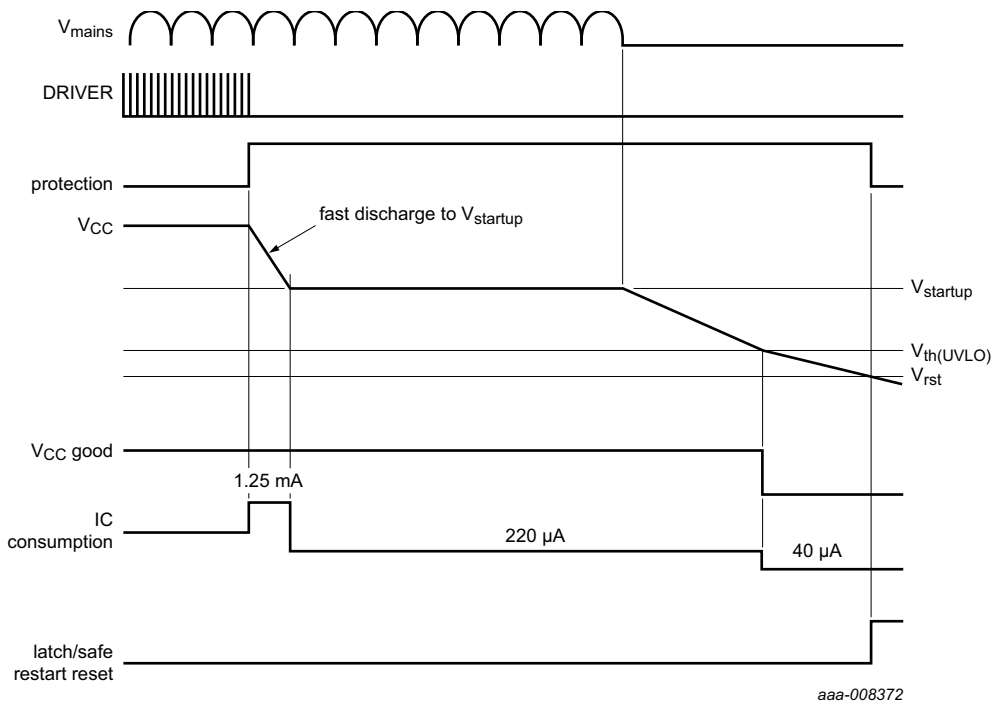


Fig 10. Fast latch reset

Using a 10 µF VCC capacitor, the fast latch reset time is below 0.6 s. If the mains is not shorted but removed, a discharged of the X-cap can cause an additional waiting time.

7.7 Burst mode operation (CTRL pin)

The controller enters the burst mode when a low output power causes the voltage on the CTRL pin to drop below 0.5 V.

During normal operation, the primary opto current can be calculated with Equation 1:

$$I_{opto} = \frac{(7\ V - V_{IO(CTRL)})}{12\ k\Omega} \quad (1)$$

This implies that without any additional measure, the maximum primary opto current in burst mode is:

$$I_{opto} = \frac{(7\ V - 0\ V)}{12\ k\Omega} = 583\ \mu A \quad (2)$$

Depending on the optocoupler used , the secondary opto current is even higher.

To achieve minimum no load input power, the internal voltage (7 V) is regulated to a value that causes the primary opto current value to be 100 µA when the system is in burst mode. The secondary opto current is then automatically also within this lower range. If the IC detects that the opto current is lower than 80 µA, the internal voltage is increased faster to achieve a small output voltage undershoot at a positive load step. Once the system enters normal operation mode, the internal voltage is slowly increased to 7 V again.

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To avoid audible noise, a special digital burst mode is implemented. The minimum switching frequency in this mode is 25 kHz. The burst mode repetition rate has a target frequency of 800 Hz (1250 μs; see Figure 11).

The amount of pulses at each burst period is defined by the requested output power. At higher output power, the amount of switching pulses increases. At low load, it decreases.

The digital circuit defines the amount of burst cycles so that the burst frequency is below the audible range (800 Hz) and the switching frequency exceeds the audible range (25 kHz). Any audible noise is avoided.

The minimum amount of switching cycles is set to 3 to ensure good efficiency at very low loads. To regulate the output power at a very low load, the system increases the burst period (< 800 Hz). The increased burst period is still outside the audible range.

To further improve the no load input power and efficiency at low loads, the current consumption of the IC is lowered to 235 μA during the non-switching period in the burst mode.

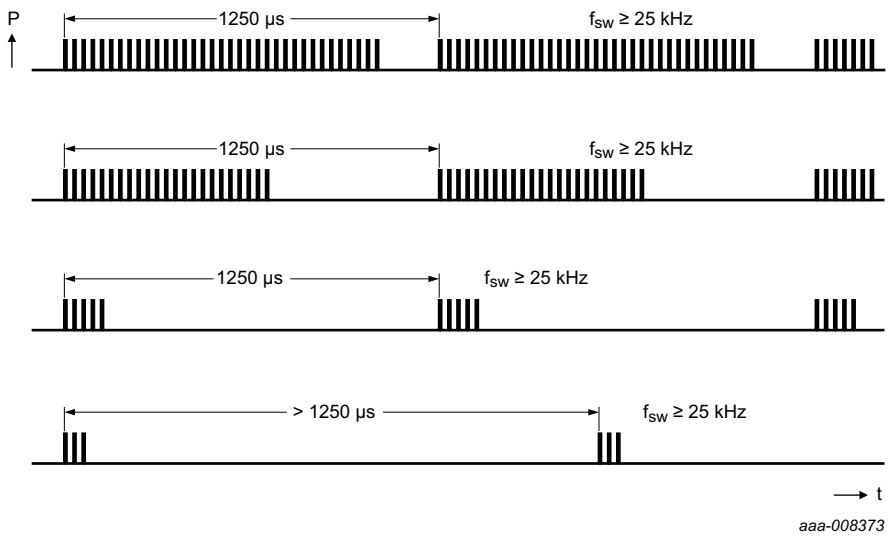


Fig 11. Burst mode operation

To achieve a good transient response in burst mode, the system starts switching immediately at an increased output load, allowing a shorter burst period. Eventually, it regulates to the required burst period by increasing the amount of driver pulses (see Figure 12).

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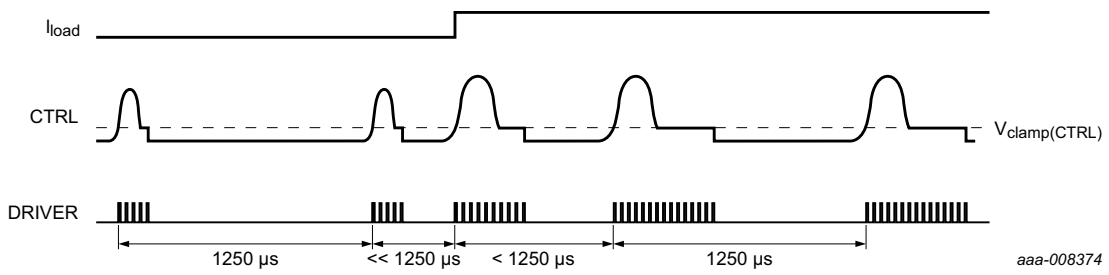
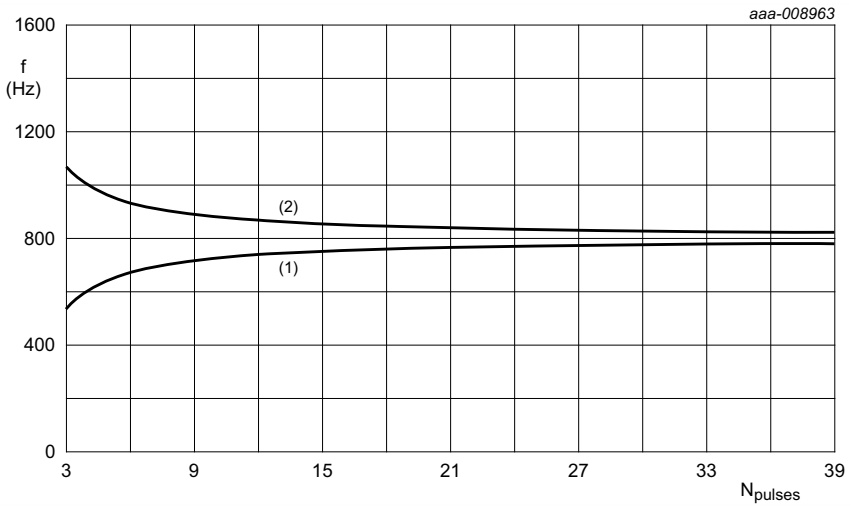


Fig 12. Transient response in burst mode

Due to the discrete number of switching cycles, the new calculated number of pulses must be 0.5 higher or lower than the existing number before one switching cycle is added or taken away. For the IC to increase or decrease the amount of switching cycles, a certain deviation from the target burst repetition frequency (800 Hz) is required because of the internal algorithm. This deviation becomes smaller when the amount of switching cycles increases. Figure 13 shows the upper and lower limits of the burst repetition frequency as a function of the number of pulses.



(1) Lower limit

(2) Upper limit

Fig 13. Upper and lower limits of burst frequency

When the amount of driver pulses within one burst period exceeds 40, the system switches to normal mode again.

During the burst period, the voltage on the CTRL pin is clamped to the minimum $V_{clamp(CTRL)}$. The current out of the CTRL pin is measured. If the current exceeds $I_{stop(CTRL)}$, the burst period is terminated regardless of digital control. This feature ensures a small overshoot at the output voltage when the load in burst mode suddenly reduces.

At the end of each burst period, the CTRL pin is pulled to the ground level for 12.5 µs, unless the current flowing from pin CTRL < 87 µA, which usually occurs at a positive load step.

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7.8 Soft start-up (ISENSE pin)

To prevent audible noise during start-up or a restart condition, a soft start feature is implemented. Before the converter starts, the soft start capacitor C_{SS} on the ISENSE pin is charged. When the converter starts switching, the primary peak current slowly increases as the soft start capacitor discharges through the soft start resistor R_{SS} (see Figure 3).

The soft start time constant is set by the external soft start capacitor and the parallel resistor values.

7.9 Driver (DRIVER pin)

The driver circuit to the gate of the power MOSFET has a current sourcing capability of 300 mA and a current sink capability of 750 mA. These capabilities allow a fast turn-on and turn-off of the power MOSFET for efficient operation.

The maximum driver output is limited to 10.5 V. The DRIVER output pin can be connected to the gate of a MOSFET directly or via a resistor.

7.10 Power-down mode

To achieve extremely low no-load standby power, the IC can be forced to power-down mode using an external signal on the PROTECT pin (see Figure 14).

When the voltage on the PROTECT pin is pulled below $V_{th(pd)PROTECT}$, the system enters the power-down mode. The voltage on the CTRL pin is lowered to 0 V. The IC automatically runs in burst mode with the voltage on pin VCC regulated at the $V_{restart}$ level. The primary and secondary opto current is saved. The current out of the PROTECT pin is reduced from 74 μA to 47 μA to save current consumption (See Figure 15).

To avoid that the latched protection is accidentally triggered when the system enters or comes out of the power-down mode, the latched protection is blocked when the voltage on the PROTECT pin is lower than $V_{th(pd)PROTECT}$.

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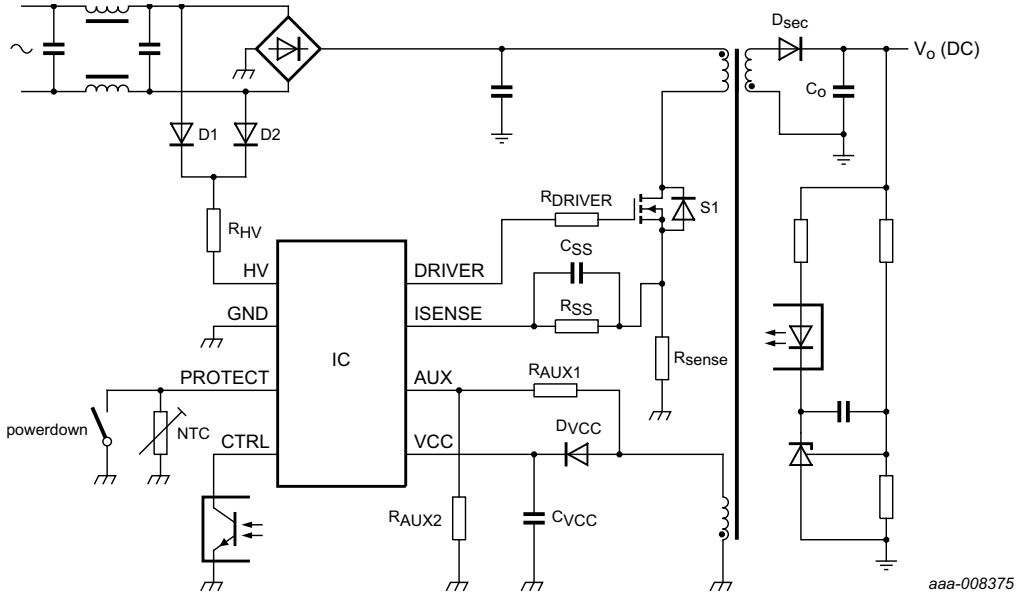


Fig 14. TEA18361T application diagram of power-down feature

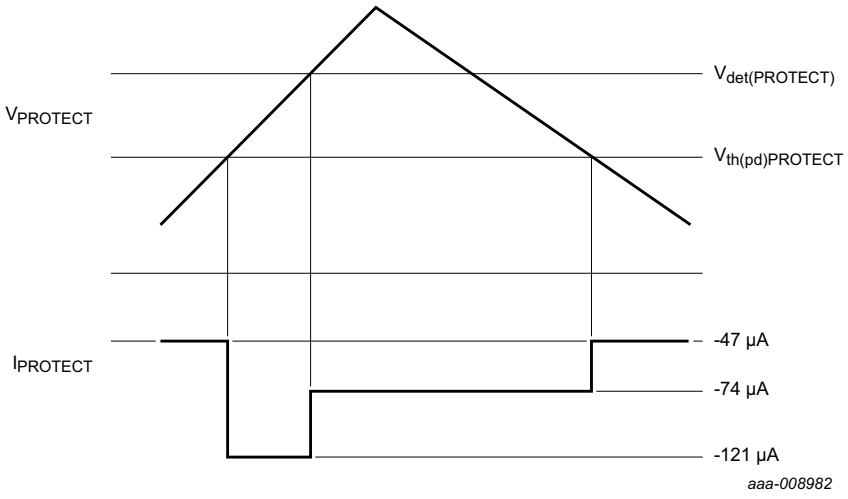


Fig 15. PROTECT pin current entering and leaving power down mode

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8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Voltages						
$V_{IO(HV)}$	input/output voltage on pin HV			–0.4	+700	V
V_{CC}	supply voltage	continuous		–0.4	+30	V
		t < 100 ms		-	+35	V
$V_{IO(CTRL)}$	input/output voltage on pin CTRL			–0.4	+12	V
$V_{I(ISENSE)}$	input voltage on pin ISENSE			–0.4	+12	V
$V_{IO(PROTECT)}$	input/output voltage on pin PROTECT	current limited		–0.4	+5	V
$V_{IO(AUX)}$	input/output voltage on pin AUX	current limited		–5	+5	V
$V_{O(DRIVER)}$	output voltage on pin DRIVER			–0.4	+12	V
Currents						
$I_{IO(AUX)}$	input/output current on pin AUX			–1.5	+1	mA
$I_{IO(HV)}$	input/output current on pin HV			–1	+5	mA
$I_{IO(CTRL)}$	input/output current on pin CTRL			–3	0	mA
$I_{IO(PROTECT)}$	input/output current on pin PROTECT			–1	+1	mA
$I_{O(DRIVER)}$	output current on pin DRIVER	δ < 10 %		–0.4	+1	A
General						
P_{tot}	total power dissipation	T_{amb} < 75 °C		-	1	W
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			–40	+150	°C
ESD						
V_{ESD}	electrostatic discharge voltage	class 1				
		human body model	[1]			
		pin HV		–1000	+1000	V
		all other pins		–2000	+2000	V
		charged device model	[2]	–500	+500	V

[1] Equivalent to discharge a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] Equivalent to discharge a 200 pF capacitor through a 0.75 μH coil and 10 Ω.

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9. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; JEDEC test board	73	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	in free air; JEDEC test board	33.1	K/W

10. Characteristics

Table 6. Characteristics

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Start-up current source (HV pin)						
$I_{startup(HV)}$	start-up current on pin HV	V_{HV} > 10 V	0.8	1.1	1.4	mA
		$V_{CC} > V_{startup}$; HV not sampling	-	-	1	µA
V_{clamp}	clamp voltage	I_{HV} < 2 mA	-	-	680	V
Supply voltage management (VCC pin)						
$V_{startup}$	start-up voltage		13.4	14.9	16.4	V
$V_{restart}$	restart voltage	burst mode	9.9	11	12.1	V
$V_{th(UVLO)}$	undervoltage lockout threshold voltage		9	9.9	10.8	V
V_{rst}	reset voltage		7.75	8.65	9.55	V
$I_{CC(startup)}$	start-up supply current	V_{HV} = 0 V	-	40	-	µA
		V_{HV} > 10 V	–1.35	–1.05	–0.75	mA
$I_{CC(oper)}$	operating supply current	driver unloaded; excluding opto current	500	600	700	µA
$I_{CC(burst)}$	burst mode supply current	non-switching; excluding opto current	200	235	270	µA
$I_{CC(prot)}$	protection supply current		185	220	255	µA
$I_{CC(dch)}$	discharge supply current	latched protection; $V_{CC} > V_{startup}$	0.9	1.25	1.6	mA
Mains detect (HV pin)						
$t_{p(HV)}$	pulse duration on pin HV	measuring mains voltage	18	20	22	µs
$f_{meas(HV)}$	measurement frequency on pin HV	measuring mains voltage	0.9	1.0	1.1	kHz
$t_{d(norm)HV}$	normal mode delay time on pin HV	measuring mains voltage	5	6	7	ms
$t_{d(burst)HV}$	burst mode delay time on pin HV	measuring mains voltage	87	97	107	ms
$I_{bo(HV)}$	brownout current on pin HV		552	587	622	µA

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Table 6. Characteristics *…continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{bi(HV)}$	brownin current on pin HV		623	663	703	µA
$I_{bo(hys)HV}$	hysteresis of brownout current on pin HV		-	76	-	µA
$I_{IH(HV)}$	HIGH-level input current on pin HV		1186	1262	1338	µA
$I_{IL(HV)}$	LOW-level input current on pin HV		1118	1190	1262	µA
$I_{HL(hys)HV}$	HIGH to LOW hysteresis current on pin HV		-	72	-	µA
$I_{clamp(HV)}$	clamp current on pin HV	during measurement time	-	-	1.7	mA
$V_{meas(HV)}$	measurement voltage on pin HV	brownin/brownout	-	2.6	-	V
$t_{d(dch)}$	discharge delay time	X capacitor discharge; pin HV	-	28	-	ms
$t_{d(det)bo}$	brownout detection delay time		-	30	-	ms
Peak current control (pin CTRL)						
$V_{IO(CTRL)}$	input/output voltage on pin CTRL	minimum flyback peak current	2.3	2.5	2.7	V
		maximum flyback current	4.9	5.25	5.6	V
$R_{int(CTRL)}$	internal resistance on pin CTRL		10	12	14	kΩ
$I_{IO(CTRL)}$	input/output current on pin CTRL	normal mode				
		V_{CTRL} = 1.5 V	–0.58	–0.48	–0.38	mA
		V_{CTRL} = 3.5 V	–0.385	–0.315	–0.245	mA
$V_{startup(CTRL)}$	start-up voltage on pin CTRL		4.7	5	5.3	V
Burst mode (pin CTRL)						
$V_{th(burst)}$	burst mode threshold voltage		0.42	0.5	0.58	V
T_{burst}	burst mode period		-	1250	-	µs
$f_{sw(min)}$	minimum switching frequency	burst mode	23	25	27	kHz
$I_{regd(CTRL)}$	regulated current on pin CTRL	burst mode	–115	–100	–85	µA
$V_{clamp(CTRL)}$	clamp voltage on pin CTRL	burst mode; system switching	0.44	0.5	0.56	V
$I_{stop(CTRL)}$	stop current on pin CTRL	burst mode; system switching; including regulated output current	–820	–750	–680	µA

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Table 6. Characteristics *...continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{pd(CTRL)}$	pull-down time on pin CTRL		10	12.5	15	µs
$I_{det(CTRL)}$	detection current on pin CTRL	positive load step	65	80	95	µA
		disable pulling down the CTRL pin	77	87	97	µA
Oscillator						
$f_{sw(max)}$	maximum switching frequency		125	132.5	140	kHz
$f_{sw(min)}$	minimum switching frequency		23	25	27	kHz
$V_{start(red)f}$	frequency reduction start voltage	pin CTRL	2.3	2.5	2.7	V
Current sense (pin ISENSE)						
$V_{sense(max)}$	maximum sense voltage	$\Delta V/\Delta t$ = 0 V/s; I_{AUX} = 0 µA; V_{CTRL} = 5.5 V	700	765	830	mV
		frequency reduction mode; $\Delta V/\Delta t$ = 0 mV/µs; I_{AUX} = 0 µA; V_{CTRL} = 1.0 V	190	207	225	mV
$t_{PD(sense)}$	sense propagation delay	from the ISENSE pin reaching $V_{sense(max)}$ to driver off; V_{ISENSE} pulse-stepping 100 mV around $V_{sense(max)}$	-	120	-	ns
t_{leb}	leading edge blanking time		275	325	375	ns
Soft start (pin ISENSE)						
$I_{start(soft)}$	soft start current		−85	−75	−65	µA
$V_{start(soft)}$	soft start voltage	enable voltage	-	$V_{sense(max)}$	-	V
$R_{start(soft)}$	soft start resistance		12	-	-	kΩ
Demagnetization and valley control (pin AUX)						
$V_{det(demag)}$	demagnetization detection voltage		20	35	50	mV
$I_{prot(AUX)}$	protection current on pin AUX		-	−200	-	nA
$t_{blank(det)demag}$	demagnetization detection blanking time		1.8	2.2	2.6	µs
$(\Delta V/\Delta t)_{vrec}$	valley recognition voltage change with time	positive $\Delta V/\Delta t$	0.25	0.37	0.49	V/µs
		negative $\Delta V/\Delta t$	−2.35	−1.9	−1.45	V/µs
$t_{d(vrec-swon)}$	valley recognition to switch-on delay time		-	120	-	ns
$V_{clamp(AUX)}$	clamp voltage on pin AUX	I_{AUX} = 1 mA	4.4	4.8	5.2	V

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Table 6. Characteristics *…continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{sup(xfmr_ring)}$	transformer ringing suppression time		1.9	2.3	2.7	µs
Maximum on-time (pin DRIVER)						
$t_{on(max)}$	maximum on-time		45	55	65	µs
Driver (pin DRIVER)						
$I_{source(DRIVER)}$	source current on pin DRIVER	V_{DRIVER} = 2 V	-	–0.3	–0.25	A
$I_{sink(DRIVER)}$	sink current on pin DRIVER	V_{DRIVER} = 2 V	0.25	0.3	-	A
		V_{DRIVER} = 10 V	0.6	0.75	-	A
$V_{O(DRIVER)max}$	maximum output voltage on pin DRIVER		9	10.5	12	V
Overpower compensation (pin ISENSE and pin AUX)						
$V_{clamp(AUX)}$	clamp voltage on pin AUX	primary stroke; I_{AUX} = –0.3 mA	–0.8	–0.7	–0.6	V
$t_{d(clamp)AUX}$	clamp delay time on pin AUX	after rising edge of pin DRIVER	580	665	750	ns
		after falling edge of pin DRIVER	1.8	2.2	2.6	µs
$V_{opc(ISENSE)}$	overpower compensation voltage on pin ISENSE	I_{AUX} = –0.3 mA	700	765	830	mV
		I_{AUX} = –1.46 mA	400	450	500	mV
$V_{opp(ISENSE)}$	overpower protection voltage on pin ISENSE	counter trigger level				
		I_{AUX} = –0.3 mA	450	500	550	mV
		I_{AUX} = –1.46 mA	265	295	325	mV
$t_{d(opp)}$	overpower protection delay time	start-up mode; V_{CTRL} > 5 V	36	40	44	ms
		normal mode	180	200	220	ms
$t_{d(restart)}$	restart delay time		720	800	820	ms
External protection (pin PROTECT)						
$V_{det(PROTECT)}$	detection voltage on pin PROTECT		0.47	0.5	0.53	V
$V_{det(hys)PROTECT}$	hysteresis of detection voltage on pin PROTECT		-	50	-	mV
$I_{O(PROTECT)}$	output current on pin PROTECT	normal mode	–79	–74	–69	µA
		power-down mode	–55	–47	–40	µA
$V_{clamp(PROTECT)}$	clamp voltage on pin PROTECT		1.25	1.45	1.65	V
Power-down mode (pin PROTECT)						
$V_{th(pd)PROTECT}$	power-down threshold voltage on pin PROTECT		0.18	0.2	0.22	V
$V_{hys(pd)}$	power-down hysteresis voltage		-	20	-	mV

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Table 6. Characteristics *…continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Overvoltage protection (pin AUX)						
$V_{ovp(AUX)}$	overvoltage protection voltage on pin AUX		2.88	3	3.12	V
$t_{det(ovp)}$	overvoltage protection detection time	in the secondary stroke	1.9	2.3	2.7	µs
Temperature protection						
$T_{pl(IC)}$	IC protection level temperature		130	140	150	°C

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11. Application information

A power supply with TEA18361T is a flyback converter operating in QR mode or DCM (See Figure 3).

Capacitor C_{VCC} buffers the IC supply voltage. The IC supply voltage is powered from the mains via D1, D2, R_{HV} during start-up. It is powered via the auxiliary winding during normal operation. R_{HV} defines the current into the HV pin for brownout detection and mains detection.

Sense resistor R_{sense} converts the current through MOSFET S1 into a voltage on pin ISENSE. The value of R_{sense} defines the maximum primary peak current through MOSFET S1. Resistor R_{SS} and capacitor C_{SS} define the soft start time.

Resistor R_{DRIVER} is required to limit the current spikes to pin DRIVER because of parasitic inductance of the current sense resistor R_{sense}. R_{DRIVER} also dampens possible oscillation of MOSFET S1. Adding a bead on the gate pin of MOSFET S1 can be required to prevent local oscillations of the MOSFET.

The PROTECT pin can be connected to a Negative Temperature Coefficient (NTC) resistor. The protection is activated when the resistor drops below a value of $V_{det(PROTECT)} / I_{O(PROTECT)} = 6.7\ k\Omega$. Shorting the PROTECT pin to ground by an external switch or optocoupler can activate the power-down mode.

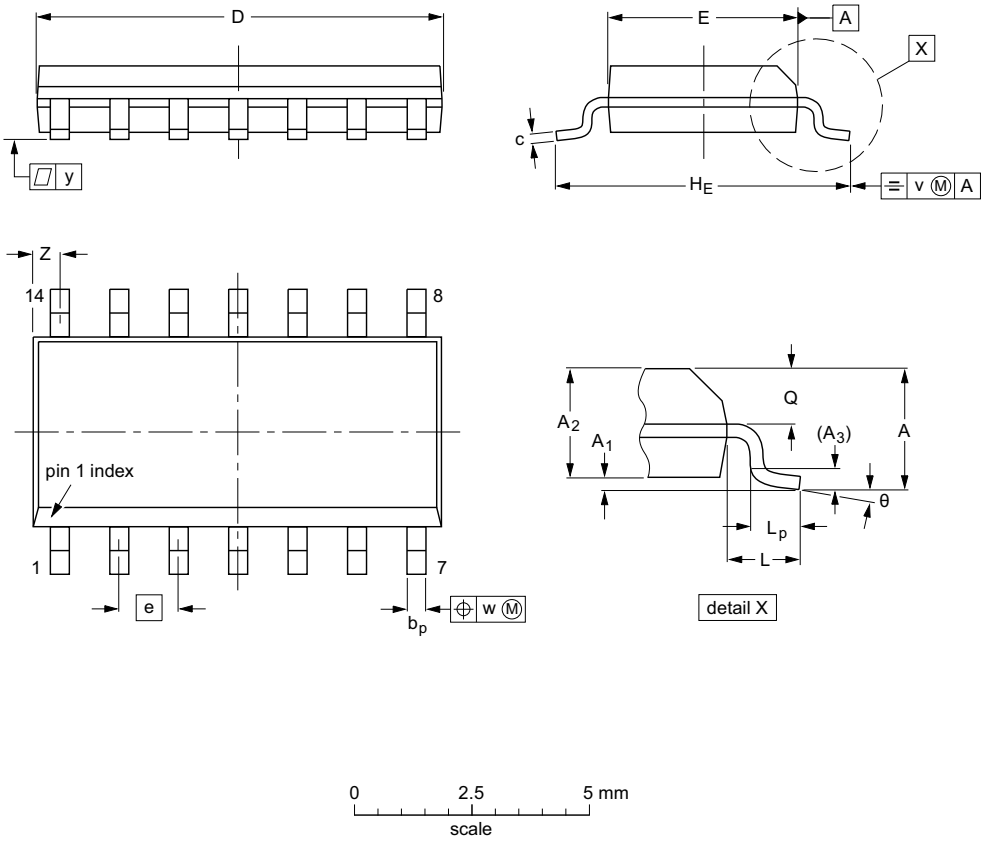
The resistor R_{AUX2} determines the compensation for input voltage variation. The ratio of R_{AUX1} and R_{AUX2} determines the overvoltage protection at the AUX pin.

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12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 16. Package outline SOT108-1 (SO14)

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13. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA18361T v.2	20131212	Product data sheet	-	TEA18361T v.1
Modifications:	• The data sheet status has changed from preliminary to product. • Table 1 “Ordering information” has been updated.			
TEA18361T v.1	20131204	Preliminary data sheet	-	-

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14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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16. Contents

1 General description 1
2 Features and benefits 2
2.1 General features 2
2.2 Green features 2
2.3 Protection features 2
3 Applications 2
4 Ordering information 2
5 Block diagram 3
6 Pinning information 4
6.1 Pinning 4
6.2 Pin description 4
7 Functional description 5
7.1 General control 5
7.1.1 Start-up and UnderVoltage LockOut (UVLO) . . 5
7.2 Modes of operation 6
7.3 Supply management 7
7.4 Mains voltage measuring 8
7.5 Auxiliary winding 9
7.6 Protection 9
7.6.1 OverPower Protection (OPP) 10
7.6.2 OverVoltage Protection (OVP) 11
7.6.3 Protection input (PROTECT pin) 11
7.6.4 OverTemperature Protection (OTP) 12
7.6.5 Maximum on-time 12
7.6.6 Safe restart 12
7.6.7 Latched protection 12
7.6.8 Fast latch reset 12
7.7 Burst mode operation (CTRL pin) 13
7.8 Soft start-up (ISENSE pin) 16
7.9 Driver (DRIVER pin) 16
7.10 Power-down mode 16
8 Limiting values 18
9 Thermal characteristics 19
10 Characteristics 19
11 Application information 24
12 Package outline 25
13 Revision history 26
14 Legal information 27
14.1 Data sheet status 27
14.2 Definitions 27
14.3 Disclaimers 27
14.4 Trademarks 28
15 Contact information 28
16 Contents 29

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Date of release: 12 December 2013
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