TEA1833LTS

GreenChip SMPS control IC

Rev. 1.1 — 8 February 2023 Product data sheet

1 General description

The TEA1833LTS is a low-cost switched-mode power supply (SMPS) controller IC intended for flyback topologies. The TEA1833LTS operates in peak current and frequency control mode. Frequency jitter has been implemented to reduce electromagnetic interference (EMI). Slope compensation is integrated for continuous conduction mode (CCM) operation.

The TEA1833LTS IC features overpower protection (OPP). The controller accepts an overpower situation up to 200 % for a limited time.

Mains undervoltage protection (brownin/brownout), output overvoltage protection (OVP), and overtemperature protection (OTP) can be implemented using a minimal number of external components.

At low-power levels, the primary peak current is set to 22 % of the maximum peak current. The switching frequency is reduced to limit the switching losses. The combination of fixed frequency operation at high output power and frequency reduction at low output power provides high efficiency over the total load range.

The TEA1833LTS makes the design of low-cost, highly efficient, and reliable supplies easier by requiring a minimum number of external components. The device is especially suited for medium power applications.

2 Features and benefits

- SMPS controller IC enabling low-cost applications
- Large input voltage range (10.5 V to 36 V)
- Integrated overvoltage protection (OVP) on the VCC pin
- Accurate overvoltage protection (OVP) via the ISENSE pin
- Dedicated burst mode, allowing a low VCC capacitor value
- Very low supply current during start-up and restart (11 µA typical)
- Low supply current during normal operation (0.58 mA typical without load)
- Adaptive internal overpower timeout
- Overpower protection including high/low line compensation
- Fixed switching frequency with frequency jitter to reduce EMI
- Frequency reduction with fixed minimum peak current to maintain high efficiency at low output power levels
- Peak power operation up to 200 % by frequency increase and peak current increase
- Slope compensation for CCM operation
- Limitation of switching frequency at high mains to reduce the maximum drain voltage
- Integrated soft-start
- Drive capability 300 mA source, 750 mA sink
- Maximum duty cycle set at 90 %
- Mains undervoltage protection (brownin/brownout)
- Output short-circuit protection (OSCP), avoiding transformer saturation
- External overtemperature protection (OTP)
- IC overtemperature protection
- Maximum duty cycle protection and brownin/brownout protection cause a restart, all other protections are latched

3 Applications

- All applications that require an efficient and cost-effective power supply solution. The TEA1833LTS is especially suited for medium power applications.

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4 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA1833LTS/1	TSOP6	plastic surface-mounted package; 6 leads	SOT457

5 Marking

Table 2. Marking

Type number	Marking code
TEA1833LTS/1	EA1833L

6 Block diagram

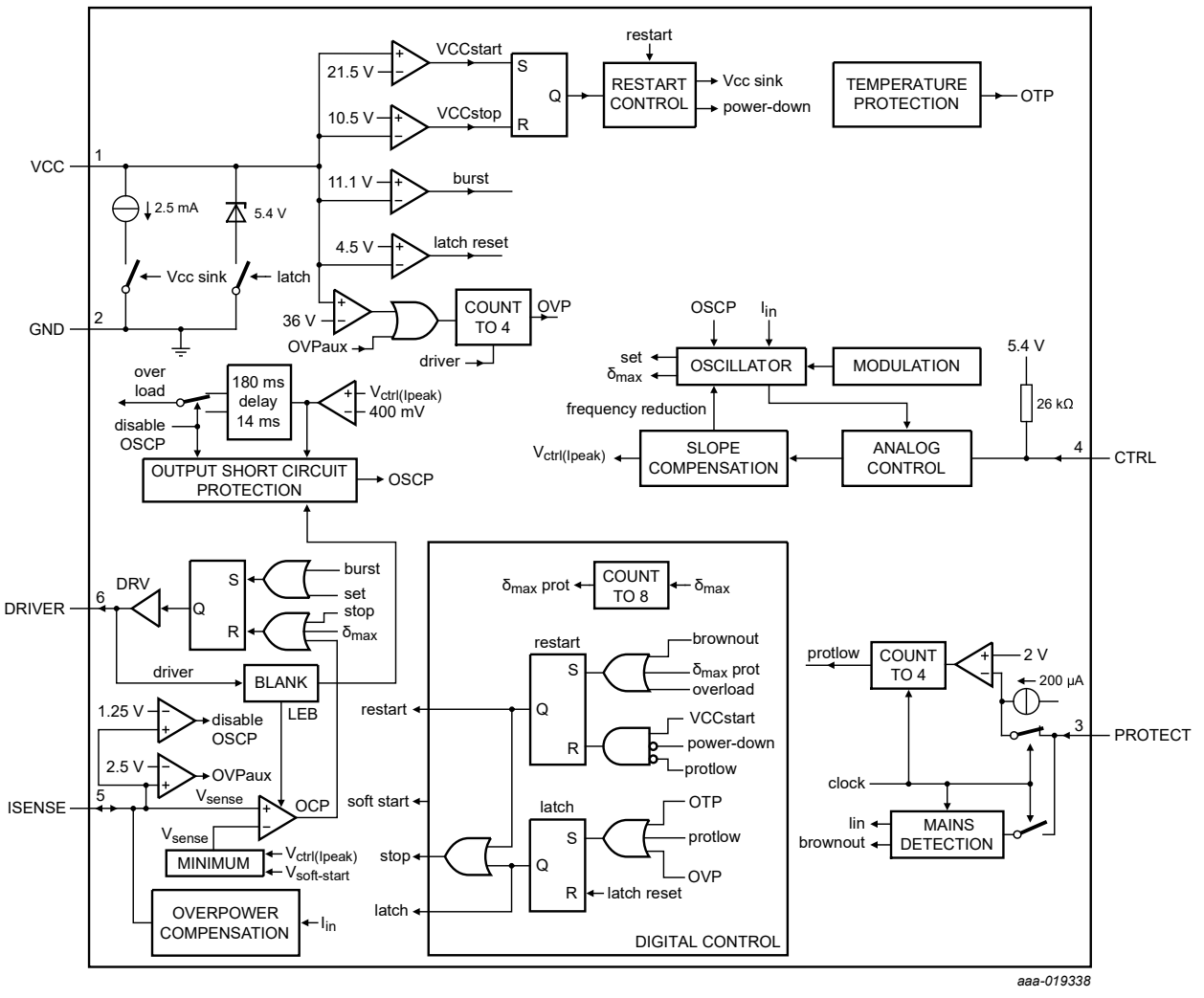


Figure 1. TEA1833LTS block diagram

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7 Pinning information

7.1 Pinning

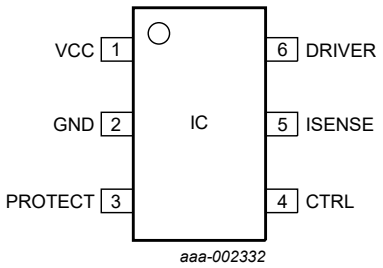


Figure 2. TEA1833LTS pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
VCC	1	supply voltage
GND	2	ground
PROTECT	3	protection and mains detect input
CTRL	4	control input
ISENSE	5	current sense and accurate OVP input
DRIVER	6	gate driver output

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8 Functional description

8.1 General control

The TEA1833LTS contains a controller for a flyback circuit. Figure 3 shows a typical configuration.

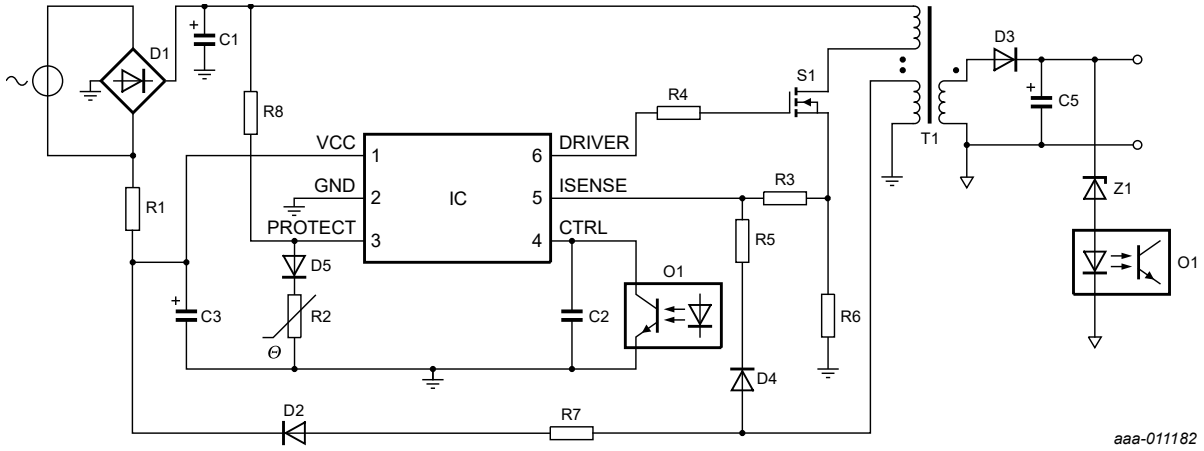


Figure 3. TEA1833LTS typical configuration

8.2 Start-up and undervoltage lockout (UVLO)

Initially, the capacitor on the VCC pin, C3, is charged from the high-voltage mains via resistor R1.

As long as the voltage on the VCC pin is below $V_{startup}$, the IC current consumption is low (11 µA typical). When the voltage on the VCC pin reaches $V_{startup}$, the IC first checks the PROTECT pin. Only when the current exceeds the brownin level ($I_{mains(bi)}$) during mains detect and the voltage surpasses $V_{det(PROTECT)}$ during external OTP measurement, the IC starts switching. An internal soft-start time of 3.5 ms allows the ISENSE peak voltage to increase gradually to prevent audible noise. In a typical application, the auxiliary winding of the transformer takes over the supply voltage.

If a protection is triggered, the controller stops switching. Depending on the protection triggered, it either causes a restart or latches the converter to an off-state.

The brownin/brownout, maximum duty cycle protections cause a safe restart. OPP, UVLO, the internal and external OVP, and the internal and external OTP latch the converter to an off-state.

A restart protection disables the switching of the IC. The supply voltage of the IC drops to the UVLO level. When the UVLO level is reached, the IC switches to power-down mode, where it consumes a low supply current (11 µA typical). The VCC capacitor is recharged via R1 until the VCC start-up level is reached. The IC starts switching again.

When a latched protection is triggered, the TEA1833LTS immediately enters the power-down mode. The VCC pin is clamped to a voltage just above the latch protection reset voltage ($V_{rst(latch)}$ + 1 V).

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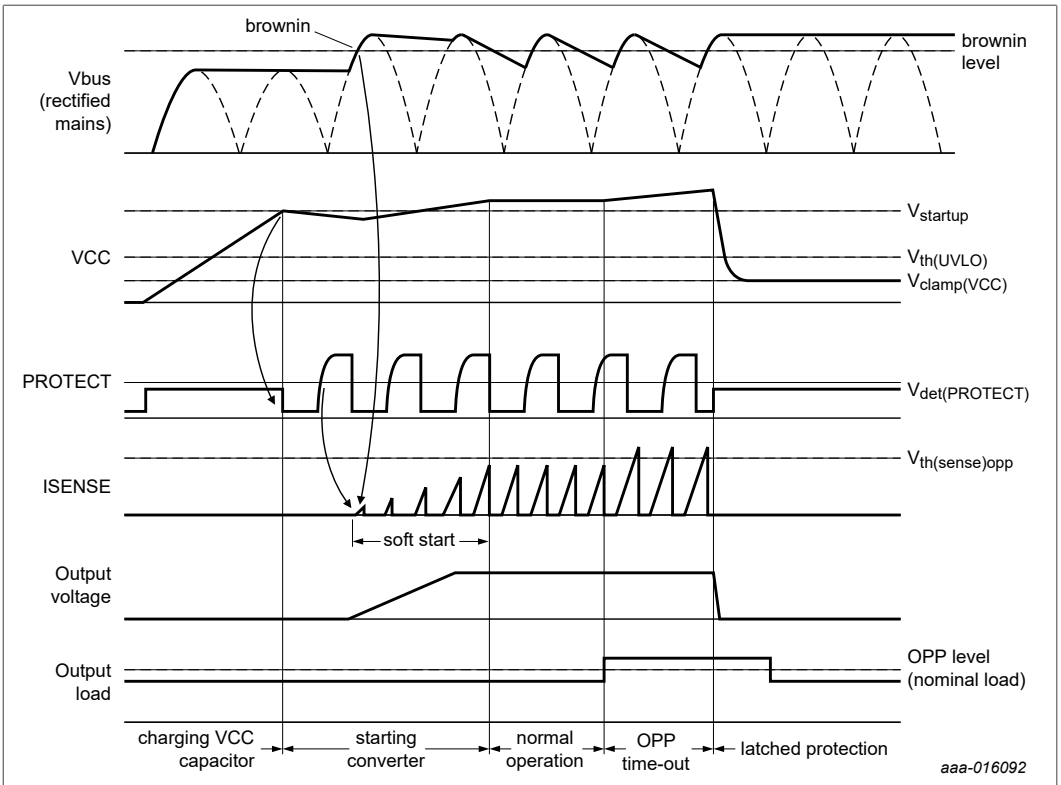


Figure 4. Start-up sequence, normal operation, and latched protection

When the voltage on pin VCC drops to below the $V_{th(UVLO)}$ level during normal operation, the controller stops switching. The TEA1833LTS activates the latched protection and enters the power-down mode. This mechanism avoids that, during a short circuit, a restart occurs when the supply voltage reaches $V_{th(UVLO)}$ before the OPP timeout is reached (see Section 8.7).

8.3 Supply management

All internal reference voltages are derived from a temperature-compensated on-chip band gap circuit. Internal reference currents are derived from a trimmed and temperature-compensated current reference circuit.

8.4 External overtemperature protection and mains detect input (pin PROTECT)

The PROTECT input combines the functions of the mains voltage detection (browin/brownout) and the external overtemperature protection (OTP). An internal clock separates the period of measuring the mains voltage and the period of detecting external overtemperature protection (OTP). In a typical application, the PROTECT pin is connected to the mains via a resistor. It is connected to ground via a negative temperature coefficient (NTC) thermistor and a diode.

When measuring the mains voltage, the PROTECT pin is regulated to 0.25 V to prevent that the external diode conducts current. The current into the PROTECT pin is measured and stored. When the measured current exceeds the brownin level, the system is allowed to start switching. If the mains voltage is continuously below the brownout level for at least 32 ms, a brownout is detected. The system immediately stops switching and

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performs a restart. The VCC capacitor is discharged to the UVLO level and then charged to $V_{startup}$ once before switching recommences (See Figure 5).

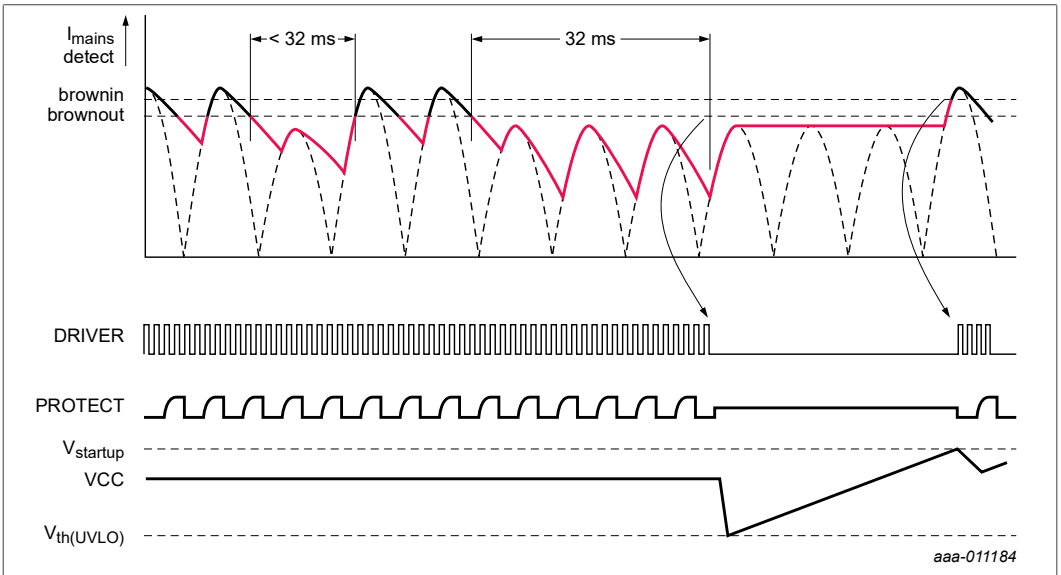


Figure 5. Mains detection

When detecting the external temperature, a current of 200 µA (typical) out of the PROTECT pin flows through the external capacitor and the NTC thermistor. If the PROTECT voltage at the end of the measuring period is below $V_{det(PROTECT)}$ for four consecutive measuring cycles, the IC detects overtemperature. It activates a latched protection.

The offset due to the current from the mains is canceled internally by remembering the sinking current I_{in} when measuring the mains voltage (see Figure 6). The stored current is also used as the input of high/low line compensation and for the maximum switching frequency limitation.

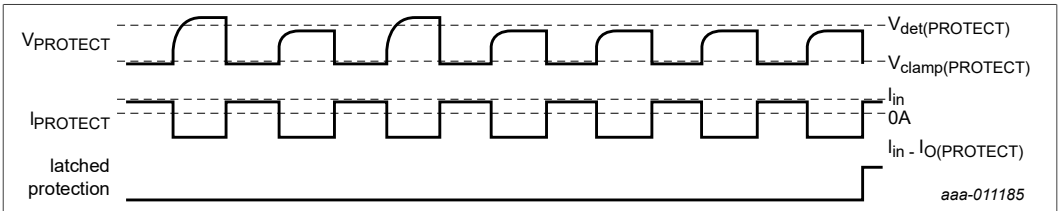


Figure 6. External overtemperature protection

An internal clamp of 4.1 V (typical) protects this pin from excessive voltages.

8.5 Duty cycle control (pin CTRL)

Pin CTRL regulates the output power of the converter. This pin is connected to an internal voltage source of 5.4 V via an internal resistor (typical resistance: 26 kΩ).

The CTRL pin voltage sets the peak current which is measured using the ISENSE pin (see Section 8.8). At low output power, the switching frequency is reduced (see Section 8.12). The maximum duty cycle is limited to 90 % (typical).

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After eight consecutive converter strokes at maximum duty cycle, the restart protection is activated. In a restart, the VCC capacitor is quickly discharged to the $V_{th(UVLO)}$ level and recharged to the start-up level from the high-voltage mains, before switching recommences.

8.6 Slope compensation (pin CTRL)

A slope compensation circuit is integrated for CCM. The slope compensation ensures stable operation for duty cycles exceeding 50 %.

8.7 Overpower timer

A temporary overload situation is allowed. If V_{sense} (see Figure 1) set by pin CTRL exceeds 400 mV, an internal timer is started. If the overload situation continues to exist for more than 160 ms (typical), an overpower protection (OPP) is triggered (see Figure 7).

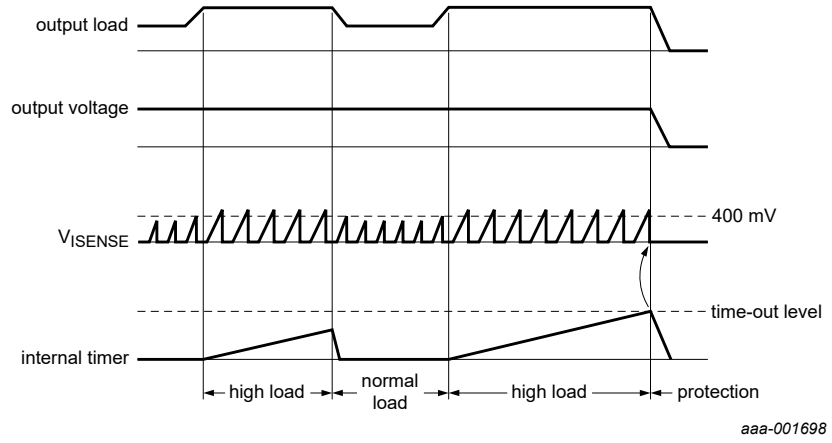


Figure 7. Overpower delay

The TEA1833LTS activates the latched protection and enters the power-down mode. To prevent a restart when, during a short circuit of the output VCC drops to below $V_{th(UVLO)}$ earlier than the OPP timeout is reached, this protection is also latched (see Section 8.2).

8.8 Current mode control (pin ISENSE)

Current mode control is used because it ensures a good line regulation.

Pin ISENSE senses the primary current across external resistor R6 and compares it with an internal control voltage. The internal control voltage is proportional to the CTRL pin voltage (see Figure 8).

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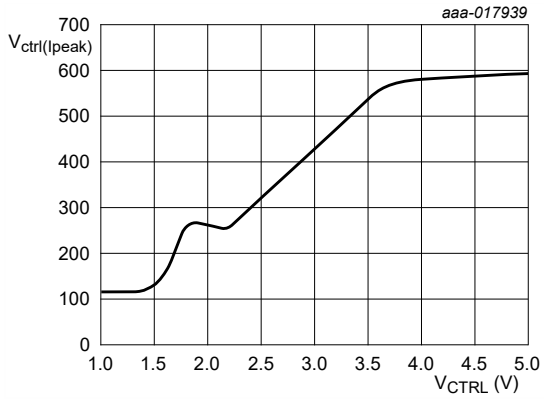


Figure 8. Peak current control

Leading-edge blanking prevents false triggering due to capacitive discharge when switching on the external power switch (see Figure 9).

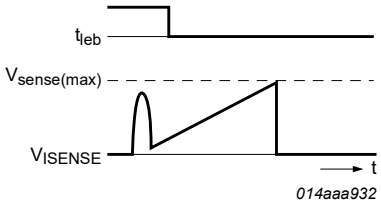


Figure 9. Leading-edge blanking

8.9 Overvoltage protection (pin ISENSE)

Accurate overvoltage protection can be realized at the ISENSE pin by sensing the auxiliary voltage. During the primary stroke, diode D4 (see Figure 3) is blocked so that the converter still works under current mode control. During the secondary stroke, the ISENSE voltage represents the output voltage via the resistor divider R5 and R3 (see Figure 3). The ISENSE voltage is sampled 2 µs after the gate signal drops to avoid the ringing of the transformer. If the sampled voltage exceeds $V_{ovp(ISENSE)}$ for four consecutive switching cycles, the IC triggers the latched protection.

8.10 Overvoltage protection (pin VCC)

An overvoltage protection (OVP) circuit is connected to the VCC pin. When the V_{CC} exceeds $V_{th(OVP)}$ (36 V typical) for four consecutive switching cycles, the IC triggers the latched protection. When V_{CC} drops to below $V_{th(OVP)}$ before count = 4 is reached, the counter is reset to zero.

8.11 Output short-circuit protection (OSCP)

A flyback controller operating in CCM at a fixed frequency turns on the primary MOSFET after a predefined period (see Figure 10). The minimum on-time equals the blanking time. If after the blanking time the measured peak current (V_{ISENSE}) is higher than the I_{peak} regulation level, the driver is switched off.

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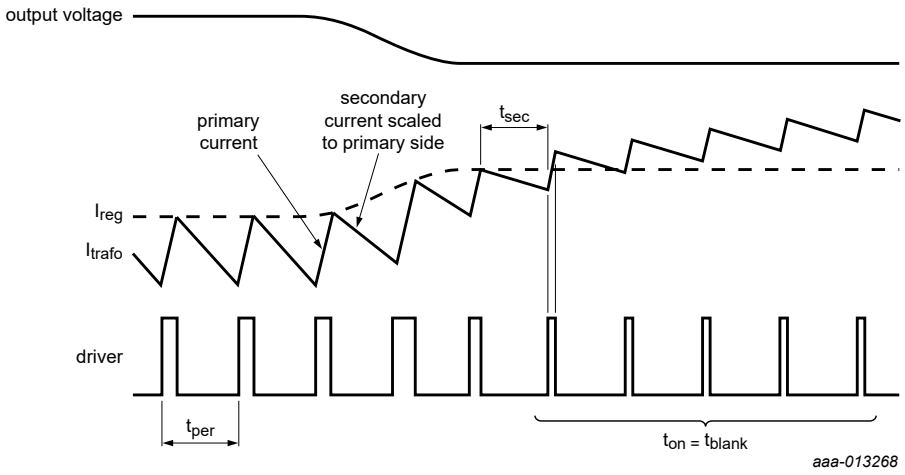


Figure 10. Peak current runaway

The output voltage can drop, for instance, because a load is too high or a short-circuit event occurs. If the output voltage drops, the decrease of the transformer current during the secondary stroke time (t_{sec}) becomes less. As a result, the next cycle starts at a higher peak current.

Also, at the next cycle, the minimum on-time equals the blanking time. During this blanking time, the peak current can increase to above the targeted regulation level. If the transformer current does not decrease sufficiently during the secondary stroke, the peak current can continuously increase to such a level that the transformer saturates (see Figure 10).

To avoid this continuous peak current increase, also called runaway, the IC features a special protection (see Figure 11).

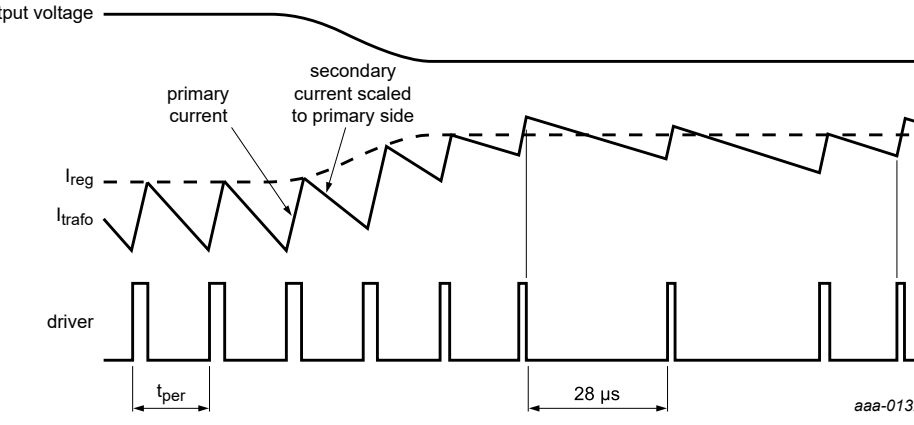


Figure 11. OSCP peak current runaway

If the system detects that the peak current already exceeds the targeted level after 1 µs, the next switching period time is extended from 7.7 µs (f_{sw} = 130 kHz) to 28 µs (f_{sw} = 36 kHz). The time of the secondary stroke is then sufficient to decrease the transformer current to below the targeted peak current again.

To avoid activation at low loads, the OSCP is only enabled when the overpower timer is active. Additionally, to avoid activation during peak power, V_{out} must be below half the OVP level.

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The V_{out} level is measured on the ISENSE pin in a similar way that the overvoltage protection is measured.

To limit the input power during a short circuit or an overload event, the OPP time is reduced to 50 % when OSCP is enabled.

8.12 Peak power, high-power medium power, and low-power operation

During high-power operation, with the converter running at a 65 kHz (typical) fixed frequency, the power is controlled by varying the peak current.

A peak power mode is implemented to supply a short overload situation. In peak power mode, both frequency and peak current are increased.

In medium power operation, lowering the switching frequency to 25 kHz reduces the switching losses.

In low-power operation, lowering of the switching frequency to below 25 kHz further reduces switching losses. The switching frequency of the converter is reduced while the peak current is set to 22 % of the maximum peak current (see Figure 8 and Figure 12).

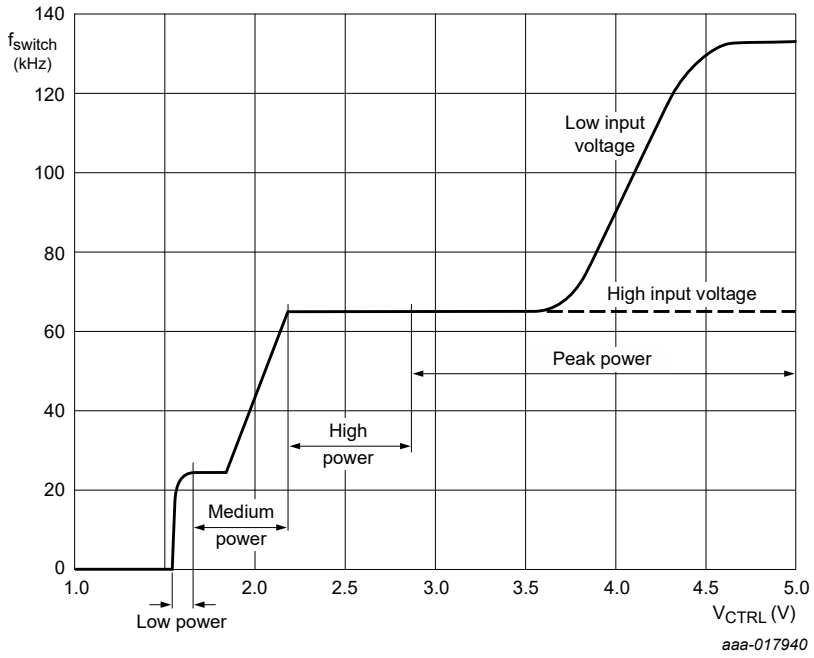


Figure 12. Frequency control

8.13 Overpower or high/low line compensation

The overpower compensation function can be used to realize a maximum output power which is nearly constant over the full input mains. The overpower compensation circuit measures the mains detect input current on the PROTECT pin and outputs a proportionally dependent current on the ISENSE pin. The DC voltage across resistor R3 (see Figure 3) limits the maximum peak current on the current sense resistor (see Figure 13).

At low output power levels, the overpower compensation circuit is switched off.

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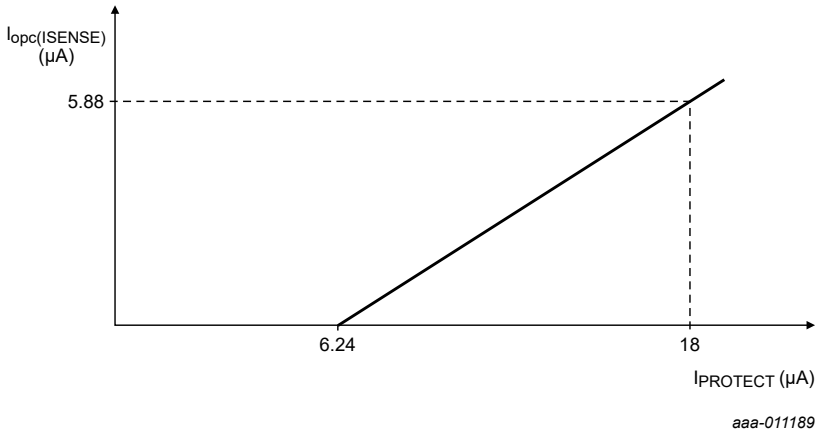


Figure 13. Overpower compensation

8.14 Burst mode

If the CTRL voltage (V_{CTRL}) < 1.45 V, the system is not switching. It waits until the V_{CTRL} exceeds this minimum level before starting the next cycle. During this period, the TEA1833LTS discharges the primary VCC capacitor. If the voltage on the VCC pin then drops to below the burst threshold level ($V_{th(burst)}$), the system asserts two DRIVER pulses to recharge the VCC capacitor. The assertion avoids that the voltage on the VCC pin drops to below the UVLO level during a large off-time.

Worst off-time occurs when there is a load transient from peak load to no-load. The output voltage shows an overshoot and stops switching until the output voltage drops to below the regulation level while there is no-load at the output.

For minimum no-load input power, the chosen value of the external capacitor at the VCC pin must be high enough to prevent that the voltage on the VCC pin drops below the burst threshold level at continuous no-load operation. The burst mode is only intended to assist at load changes until the output voltage drops to below the regulation level while there is no-load at the output.

8.15 Limitation of the maximum switching frequency

At high mains, the maximum switching frequency is limited (see Figure 14). The 130 kHz switching frequency is required at low mains only. At high mains, the high switching frequency during peak power causes an unnecessary high voltage on the drain of the MOSFET, because the high switching frequency increases the clamp voltage.

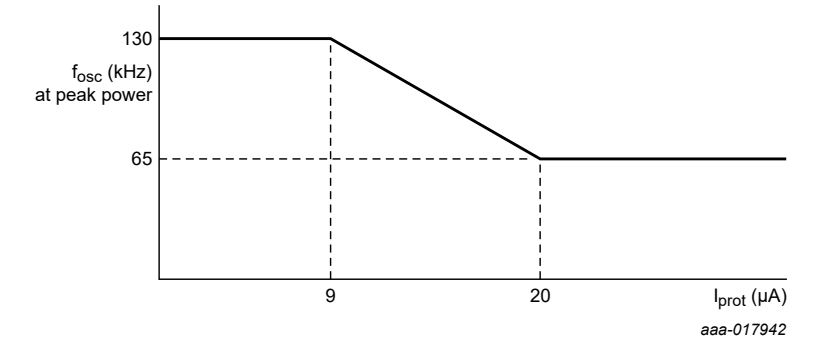


Figure 14. Switching frequency limitation

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8.16 Driver (pin DRIVER)

The driver circuit to the gate of the power MOSFET has a current sourcing capability of typically 300 mA and a current sink capability of typically 750 mA. These capabilities enable a fast turn-on and turn-off of the power MOSFET for efficient operation.

8.17 Overtemperature protection (OTP)

If the junction temperature exceeds the thermal shutdown limit, integrated overtemperature protection ensures that the IC stops switching.

OTP is a latched protection. It can be reset by removing the voltage on pin VCC.

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9 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{CC}	supply voltage		−0.4	+40	V
$V_{PROTECT}$	voltage on pin PROTECT	current limited	−0.4	+5	V
V_{CTRL}	voltage on pin CTRL		−0.4	+5.5	V
V_{ISENSE}	voltage on pin ISENSE	current limited to 2 mA	−0.7	+5	V
Currents					
I_{VCC}	current on pin VCC	δ < 10 %	-	0.4	A
$I_{I(PROTECT)}$	input current on pin PROTECT		−1	+1	mA
I_{CTRL}	current on pin CTRL		−3	0	mA
I_{ISENSE}	current on pin ISENSE		−10	+0.5	mA
I_{DRIVER}	current on pin DRIVER	δ < 10 %	−0.4	+1	A
General					
P_{tot}	total power dissipation	T_{amb} < 75 °C	-	0.29	W
T_{stg}	storage temperature		−55	+150	°C
T_j	junction temperature		−40	+150	°C
ESD					
V_{ESD}	electrostatic discharge voltage	human body model (HBM); JEDEC class 2; all pins	−2500	+2500	V
		charged device model (CDM); JEDEC class 3; all pins	−750	+750	V

10 Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; single-layer JEDEC test board	259	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	in free air; JEDEC test board	152	K/W

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11 Characteristics

Table 6. Characteristics

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage management (pin VCC)						
$V_{startup}$	start-up voltage		20.2	22	24	V
$V_{th(UVLO)}$	undervoltage lockout threshold voltage		9.4	10.5	11.6	V
V_{hys}	hysteresis voltage	$V_{startup} - V_{th(UVLO)}$	8.5	11.5	14.5	V
$V_{th(burst)}$	burst mode threshold voltage		-	11.1	-	V
$\Delta V_{th(burst-UVLO)}$	burst mode to UVLO threshold voltage difference	$V_{th(burst)} > V_{th(UVLO)}$ [1]	0.5	0.6	0.7	V
$V_{rst(latch)}$	latched reset voltage		3.5	4.5	5.5	V
$V_{clamp(VCC)}$	clamp voltage on pin VCC	latched protection mode; I_{CC} = 15 µA	$V_{rst(latch)}$ + 1	-	-	V
		latched protection mode; I_{CC} = 500 µA	-	-	$V_{rst(latch)}$ + 4	V
$I_{CC(startup)}$	start-up supply current	$V_{CC} < V_{startup}$	9	11	16	µA
$I_{CC(oper)}$	operating supply current	no-load on pin DRIVER; δ = 2 %; excluding optocurrent	-	0.58	-	mA
		no-load on pin DRIVER; δ = 25 %; excluding optocurrent	-	0.62	-	mA
$I_{CC(restart)}$	restart supply current		1	2.5	-	mA
Protection input (pin PROTECT)						
$V_{det(PROTECT)}$	detection voltage on pin PROTECT	$I_{I(PROTECT)}$ = −200 µA	1.95	2	2.05	V
$I_{O(PROTECT)}$	output current on pin PROTECT	$V_{PROTECT} = V_{det(PROTECT)}$	−212.5	−200	−187.5	µA
$V_{clamp(PROTECT)}$	clamp voltage on pin PROTECT	$I_{I(PROTECT)}$ = 6 µA; mains detect period; $C_{max(PROTECT)}$ = 10 pF	205	260	315	mV
		$I_{I(PROTECT)} \geq$ −200 µA; OTP measurement period [2]	3.5	4.1	4.7	V
Mains detect (pin PROTECT)						
$I_{mains(bi)}$	mains brownin current		5.28	5.7	6.12	µA
$I_{mains(bo)}$	mains brownout current		4.63	5.0	5.37	µA

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Table 6. Characteristics *...continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Peak current control (pin CTRL)						
V_{CTRL}	voltage on pin CTRL	for minimum flyback peak current	1.3	1.6	1.9	V
		for maximum flyback peak current	3.4	3.9	4.3	V
$R_{int(CTRL)}$	internal resistance on pin CTRL		20	26	32	kΩ
$I_{O(CTRL)}$	output current on pin CTRL	V_{CTRL} = 1.4 V	−183	−138	−93	µA
		V_{CTRL} = 3.7 V	−67.5	−50	−32.5	µA
Pulse width modulator						
f_{osc}	oscillator frequency	OSCP	30	38	46	kHz
		peak power	118	130	142	kHz
		high power	60.5	65	69.5	kHz
		medium power	21	26	31	kHz
f_{mod}	modulation frequency		195	260	325	Hz
Δf_{mod}	modulation frequency variation	high power	±3	±4	±5	kHz
δ_{max}	maximum duty cycle		86	90	94	%
$N_{cy(sw)\delta max}$	number of switching cycles with maximum duty cycle	to trigger maximum duty cycle protection	7	-	8	
V_{CTRL}	voltage on pin CTRL	for zero duty cycle	1.15	1.45	1.75	V
		for start of frequency reduction from medium to low power	1.4	1.6	1.8	V
		for end of frequency reduction from high to medium power mode	1.6	1.8	2.0	V
		for start of frequency reduction from high to medium power mode	1.9	2.15	2.40	V
		for start of frequency increase from high to peak power mode	3.55	3.8	4.05	V
		for maximum frequency (peak power mode); at low mains; I_{prot} < 8.5 µA	4.45	4.75	5.05	V
Overpower protection						
$t_{to(opp)}$	overpower protection time-out time		160	180	200	ms

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Table 6. Characteristics *...continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Current sense and overpower compensation (pin ISENSE)						
$V_{sense(max)}$	maximum sense voltage	ΔV/Δt = 0 V/s	0.555	0.590	0.625	V
$t_{PD(sense)}$	sense propagation delay		130	155	180	ns
$V_{th(sense)opp}$	overpower protection sense threshold voltage		380	410	440	mV
$\Delta V_{ISENSE}/\Delta t$	slope compensation voltage on pin ISENSE	high-power mode	-	20	-	mV/µs
t_{leb}	leading edge blanking time		275	325	375	ns
$I_{opc(ISENSE)}$	overpower compensation current on pin ISENSE	$I_{PROTECT}$ = 10 µA; $V_{ctrl(Ipeak)}$ > 400 mV	−1.5	−2	−2.5	µA
		$I_{PROTECT}$ = 18 µA; $V_{ctrl(Ipeak)}$ > 400 mV	−5.5	−6	−6.5	µA
Soft start (pin ISENSE)						
$t_{start(soft)}$	soft start time		2.7	3.5	4.2	ms
Driver (pin DRIVER)						
$I_{source(DRIVER)}$	source current on pin DRIVER	V_{DRIVER} = 2 V	-	−0.3	−0.25	A
$I_{sink(DRIVER)}$	sink current on pin DRIVER	V_{DRIVER} = 2 V	0.25	0.3	-	A
		V_{DRIVER} = 10 V	0.6	0.75	-	A
$V_{O(DRIVER)max}$	maximum output voltage on pin DRIVER		9	10.5	12	V
Overvoltage protection (pins VCC and ISENSE)						
$V_{ovp(VCC)}$	overvoltage protection voltage on pin VCC		34.8	36	37.2	V
$V_{ovp(ISENSE)}$	overvoltage protection voltage on pin ISENSE		2.4	2.5	2.6	V
$t_{blank(ovp)ISENSE}$	overvoltage protection blanking time on pin ISENSE		1.7	2.1	2.5	µs
$N_{cy(ovp)}$	number of overvoltage protection cycles		4	4	4	
Output short circuit protection[3]						
$V_{dis(oscp)ISENSE}$	output short circuit protection disable voltage on pin ISENSE	OSCP is disabled when V_{ISENSE} exceeds $V_{dis(oscp)ISENSE}$	1.2	1.25	1.3	V
$t_{to(oscp)}$	output short circuit protection time-out time		11	14	17	ms

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Table 6. Characteristics *...continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Temperature protection						
$T_{pl(IC)}$	IC protection level temperature		130	140	150	°C

[1] Guaranteed by design.
[2] The clamp voltage on the PROTECT pin is lowered when the IC is in power-down mode. (latched or restart protection).
[3] The output short-circuit protection (OSCP) is only enabled when the voltage level on the ISENSE pin during the secondary stroke is below $V_{dis(oscp)ISENSE}$ level (half the $V_{ovp(ISENSE)}$ level). When enabled, the OSCP becomes active when the V_{sense} level exceeds $V_{th(sense)opp}$ and the V_{sense} level is reached within 1 µs (cycle-by-cycle). The switching period is then stretched to 28 µs (36 kHz, f_{osc} OSCP).

12 Application information

A power supply with the TEA1833LTS is a flyback converter which operates in both discontinuous conduction mode (DCM) and continuous conduction mode (CCM). Which mode depends on the input voltage and output power.

Resistor R1 charges the small buffer capacitor C3 at start-up. The auxiliary winding takes over during normal operation.

The driver pin switches the MOSFET. Resistor R4 is added to protect the driver against switching spikes due to parasitics (inductance and capacitance of tracks, MOSFET, and transformer).

Resistor R6 converts the MOSFET current to a voltage. It is measured on the ISENSE pin. The R6 value determines the maximum primary peak current through the MOSFET.

The measured peak current is compensated for the mains input voltage using a current through resistor R3 that is proportional to the bus voltage of capacitor C1. During the secondary stroke, the auxiliary voltage is measured using diode D4 and resistors R5, R3, and R6. The measured value can be used for an overvoltage protection for the output voltage.

Place capacitor C2 close to the CTRL pin to suppress noise.

The PROTECT pin cycles between mains voltage detect and external overtemperature measurement. During mains voltage detection, the current through resistor R8 is measured. This current relates to the voltage on capacitor C1 and the input voltage. The current is used to realize brownin, brownout, and input voltage compensation for the overpower protection.

During overtemperature protection, a current is sourced from the pin. The voltage over diode D5 and NTC resistor R2 is measured. A fixed comparator level detects when the NTC value drops too much.

To avoid pickup of disturbance, place both resistor R8 and diode D5/resistor R2 as close as possible to the pin.

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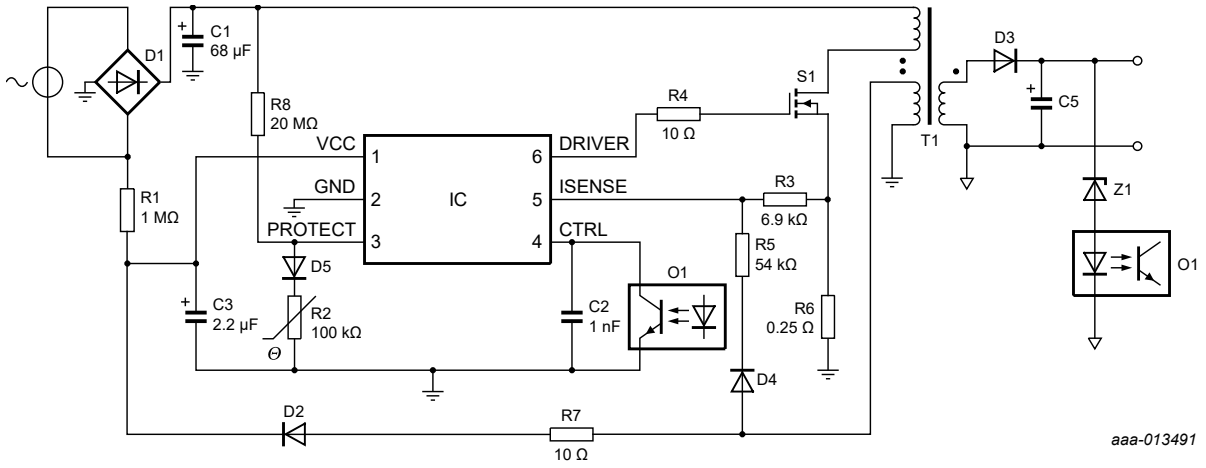


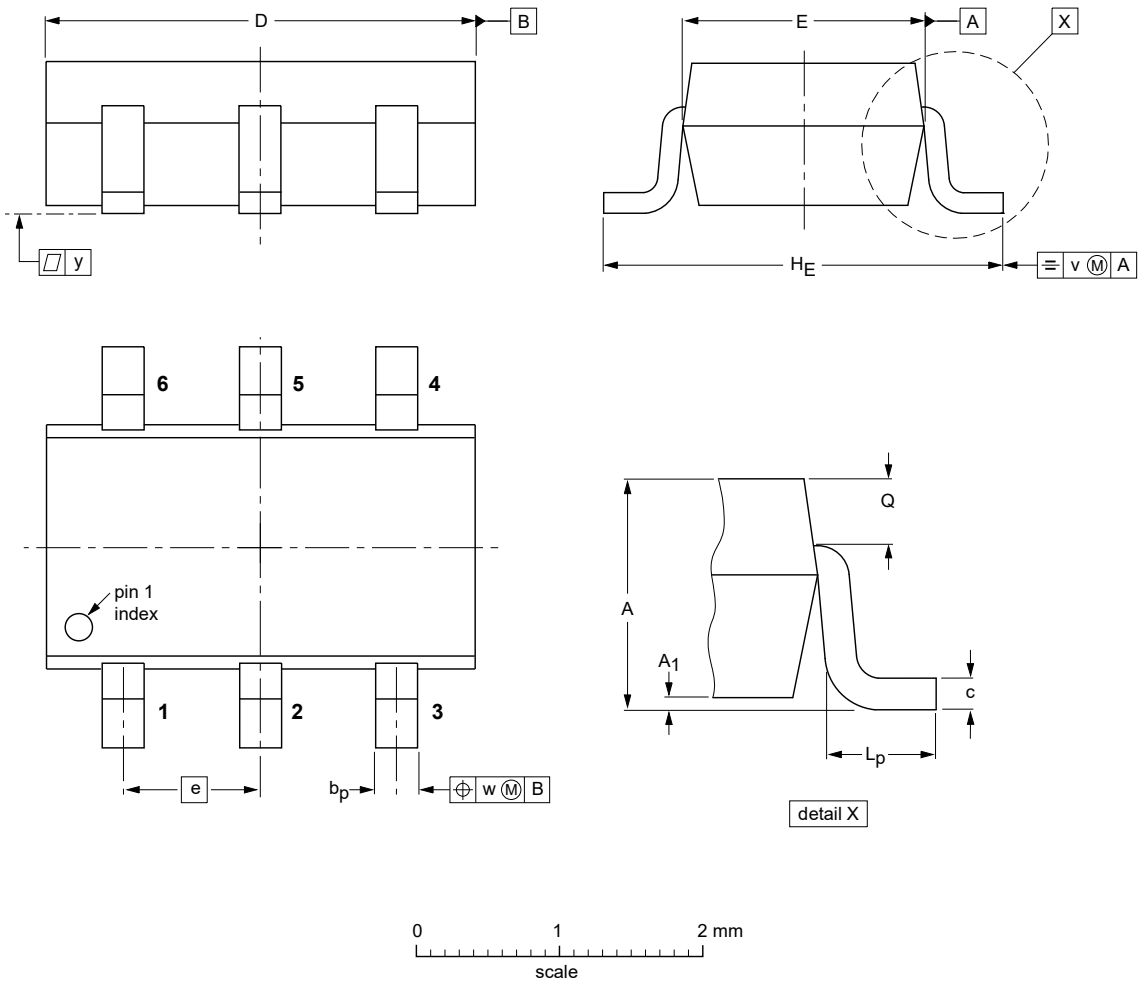
Figure 15. TEA1833LTS application diagram

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13 Package outline

Plastic surface-mounted package (TSOP6); 6 leads **SOT457**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT457			SC-74			~~05-11-07~~ 06-03-16

Figure 16. Package outline SOT457 (TSOP6)

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14 Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA1833LTS v.1.1	20230208	Product data sheet	-	TEA1833LTS v.1
Modifications:	• Section 5 "Marking" has been added to this document. • The document template has been updated.			
TEA1833LTS v.1	20170622	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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