TEA1733LT

GreenChip SMPS control IC

Rev. 8 — 16 July 2013 Product data sheet

1. General description

The TEA1733LT/N1 is a low cost Switched Mode Power Supply (SMPS) controller ICs intended for flyback topologies. They operate in fixed frequency mode. To reduce ElectroMagnetic Interference (EMI), frequency jitter has been implemented. Slope compensation is integrated for Continuous Conduction Mode (CCM) operation.

The TEA1733LT/N1 includes OverPower Protection (OPP). This enables the controller to operate under overpower situations for a limited amount of time.

Two pins, VINSENSE and PROTECT, are reserved for protection purposes. Input UnderVoltage Protection (UVP) and OverVoltage Protection (OVP), output OVP and OverTemperature Protection (OTP) can be implemented using a minimal number of external components.

At low power levels the primary peak current is set to 25 % of the maximum peak current and the switching frequency is reduced to limit switching losses. The combination of fixed frequency operation at high output power and frequency reduction at low output power provides high-efficiency over the total load range.

The TEA1733LT/N1 enables low cost, highly efficient and reliable supplies for power requirements up to 75 W to be designed easily and with a minimum number of external components.

2. Features and benefits

2.1 Features

- SMPS controller IC enabling low-cost applications
- Large input voltage range (12 V to 30 V)
- Very low supply current during start-up and restart (typically 10 μA)
- Low supply current during normal operation (typically 0.5 mA without load)
- Overpower or high/low line compensation
- Adjustable overpower time-out
- Adjustable overpower restart timer
- Fixed switching frequency with frequency jitter to reduce EMI
- Frequency reduction with fixed minimum peak current to maintain high-efficiency at low output power levels
- Slope compensation for CCM operation
- Low and adjustable OverCurrent Protection (OCP) trip level

- Adjustable soft start operation
- Two protection inputs (e.g. for input UVP and OVP, OTP and output OVP)
- IC overtemperature protection

3. Applications

- All applications requiring efficient and cost-effective power supply solutions up to 75 W.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA1733LT/N1	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

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5. Block diagram

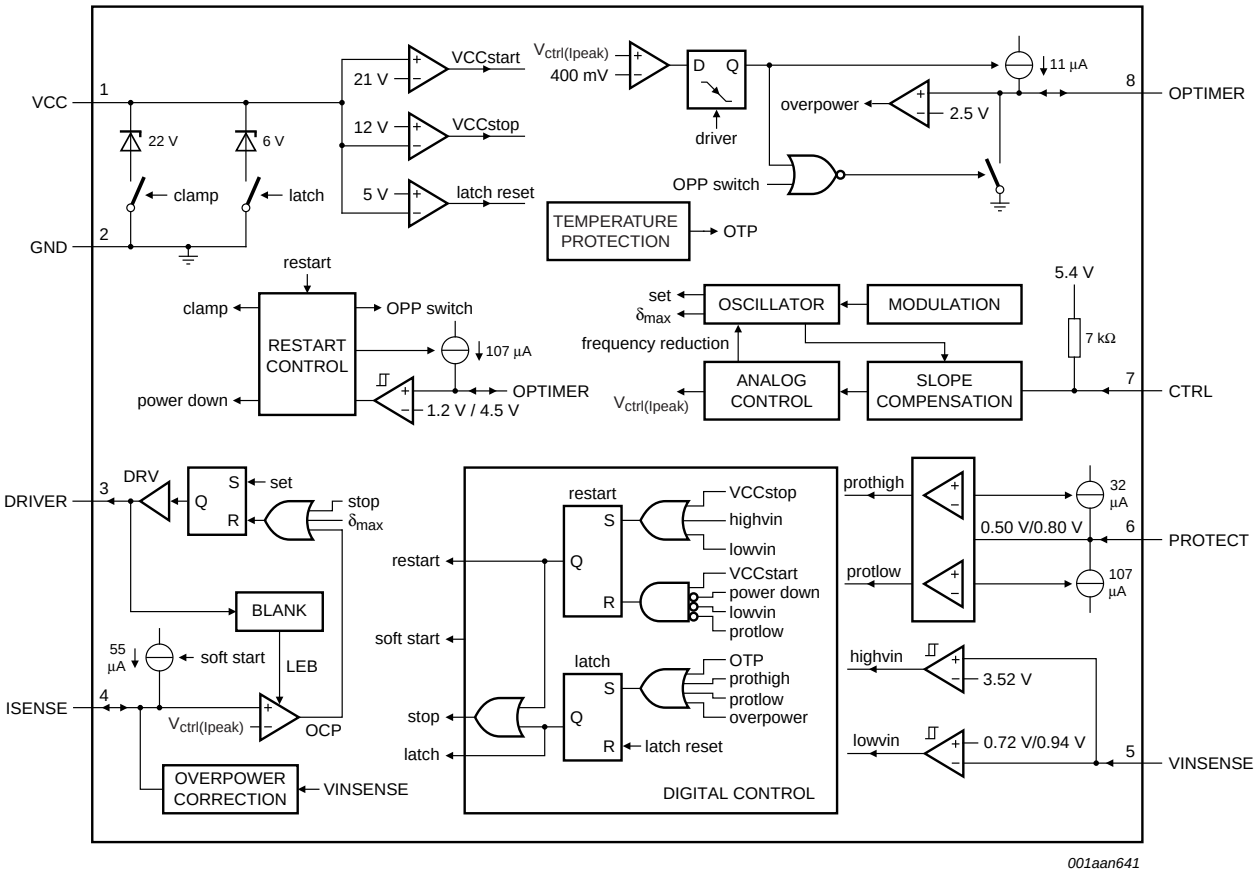


Fig 1. Block diagram TEA1733LT/N1

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6. Pinning information

6.1 Pinning

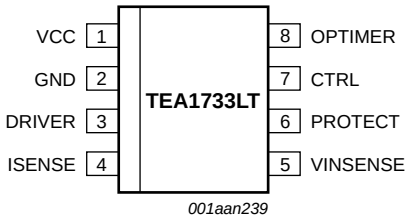


Fig 2. Pinning diagram SOT96-1 (SO8)

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
VCC	1	supply voltage
GND	2	ground
DRIVER	3	gate driver output
ISENSE	4	current sense input
VINSENSE	5	input voltage protection input
PROTECT	6	general purpose protection input
CTRL	7	control input
OPTIMER	8	overpower and restart timer

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7. Functional description

7.1 General control

The TEA1733LT/N1 contains a flyback circuit controller, a typical configuration of which is shown in Figure 3.

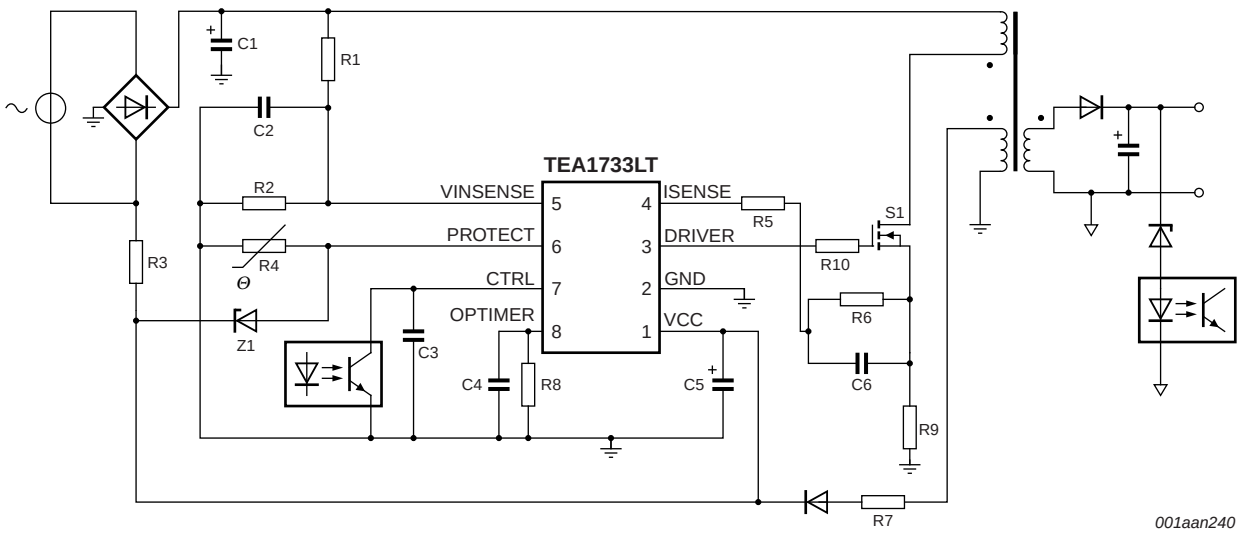


Fig 3. Typical configuration

7.2 Start-up and UnderVoltage LockOut (UVLO)

Initially, the capacitor on the VCC pin is charged from the high voltage mains via resistor R3.

If V_{CC} is lower than $V_{startup}$, the IC current consumption is low (typically 10 μA). When V_{CC} reaches $V_{startup}$, the IC first waits for the VINSENSE pin to reach the $V_{start(VINSENSE)}$ voltage and PROTECT pin to reach the $V_{det(L)(PROTECT)}$ voltage. When both levels are reached, the IC charges the ISENSE pin to the $V_{start(soft)}$ level and starts switching. In a typical application, the supply voltage is taken over by the auxiliary winding of the transformer.

If a protection is triggered the controller stops switching. Depending on the protection triggered, the protection causes a restart or latches the converter to an off-state.

A restart caused by a protection rapidly charges the OPTIMER pin to 4.5 V (typical). The TEA1733LT/N1 enters Power-down mode until the OPTIMER pin discharges down to 1.2 V (typical). In Power-down mode, the IC consumes a very low supply current (10 μA typical) and the VCC pin is clamped at 22 V (typical) by an internal clamp circuit. When the voltage on pin OPTIMER drops below 1.2 V (typical) and the VCC pin voltage is above the VCC start-up voltage (See Figure 4), the IC restarts.

When a latched protection is triggered, the TEA1733LT/N1 immediately enters Power-down mode. The VCC pin is clamped to a voltage just above the latch protection reset voltage ($V_{rst(latch)}$ + 1 V).

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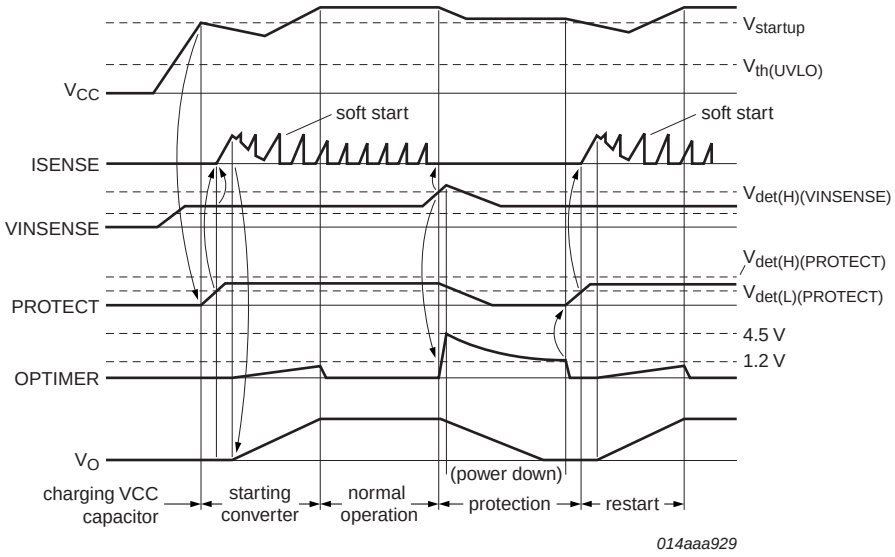


Fig 4. Start-up sequence, normal operation and restart sequence

When the voltage on pin VCC drops below the $V_{th(UVLO)}$ level during normal operation, the controller stops switching. The TEA1733LT/N1 enters Restart mode. In Restart mode, the driver output is disabled and the VCC pin is recharged via resistor R3 to the rectified mains.

7.3 Supply management

All internal reference voltages are derived from a temperature compensated on-chip band gap circuit. Internal reference currents are derived from a trimmed and temperature compensated current reference circuit.

7.4 Input voltage detection (VINSENSE pin)

In a typical application the mains input voltage can be detected by the VINSENSE pin. Switching will not take place until the voltage on VINSENSE has reached the $V_{start(VINSENSE)}$ voltage (typically 0.94 V).

When the VINSENSE voltage drops below $V_{det(L)(VINSENSE)}$ (typically 0.72 V) or exceeds $V_{det(H)(VINSENSE)}$ (typically 3.52 V), the converter stops switching and performs a restart.

If pin VINSENSE is left open or disconnected, the pin is pulled up by the internal 20 nA (typical) current source to reach the $V_{det(H)(VINSENSE)}$ level. This triggers restart protection.

An internal clamp of 5.2 V (typical) protects this pin from overvoltages.

7.5 Protection input (PROTECT PIN)

Pin PROTECT is a general purpose input pin, which can be used to switch off the converter (latched protection). The converter is stopped when the voltage on this pin is pulled above $V_{det(H)(PROTECT)}$ (typically 0.8 V) or below $V_{det(L)(PROTECT)}$ (typically 0.5 V). A current of 32 μA (typical) flows out of the chip when the pin voltage is at the $V_{det(L)(PROTECT)}$ level. A current of 107 μA (typical) flows into the chip when the pin voltage is at the $V_{det(H)(PROTECT)}$ level.

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The PROTECT input can be used to create overvoltage detection and OTP functions.

A small capacitor can be connected to the pin if the protections on this pin are not used.

An internal clamp of 4.1 V (typical) protects this pin from overvoltages.

7.6 Duty cycle control (CTRL pin)

The output power of the converter is regulated by the CTRL pin. This pin is connected to an internal 5.4 V supply using an internal 7 kΩ resistor.

The CTRL pin voltage sets the peak current which is measured using the ISENSE pin (see Section 7.10). At a low output power the switching frequency is also reduced (see Section 7.12). The maximum duty cycle is limited to 72 % (typical).

TEA1733LT/N1 does not trigger any protection when maximum duty cycle is reached.

7.7 Slope compensation (CTRL pin)

A slope compensation circuit is integrated in the IC for CCM. Slope compensation guarantees stable operation for duty cycles greater than 50 %.

7.8 Overpower timer (OPTIMER pin)

If the OPTIMER pin is connected to capacitor C4 (see Figure 3), a temporary overload situation is allowed. $V_{ctrl(Ipeak)}$ is set by the CTRL. When $V_{ctrl(Ipeak)}$ is above 400 mV, the $I_{IO(OPTIMER)}$ current (11 μA typical) is sourced from the OPTIMER pin. If the voltage on the OPTIMER pin reaches the $V_{prot(OPTIMER)}$ voltage (2.5 V typical) the OverPower Protection (OPP) is triggered (see Figure 5).

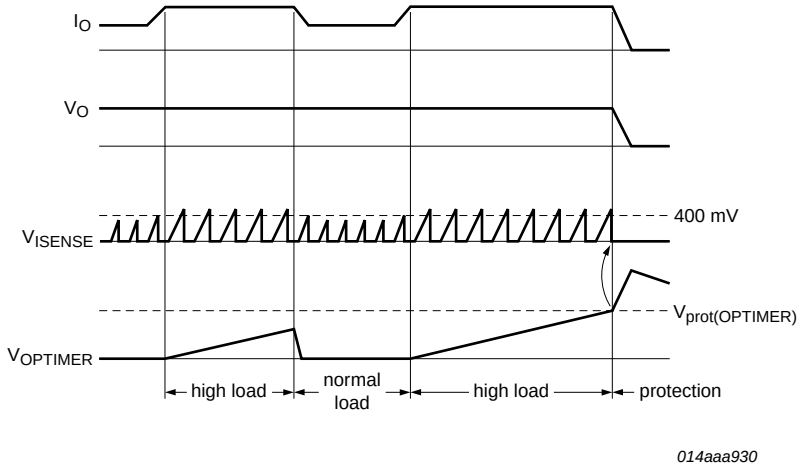


Fig 5. Overpower delay

TEA1733LT/N1: when the $V_{prot(OPTIMER)}$ voltage is reached, it is latched in the off state.

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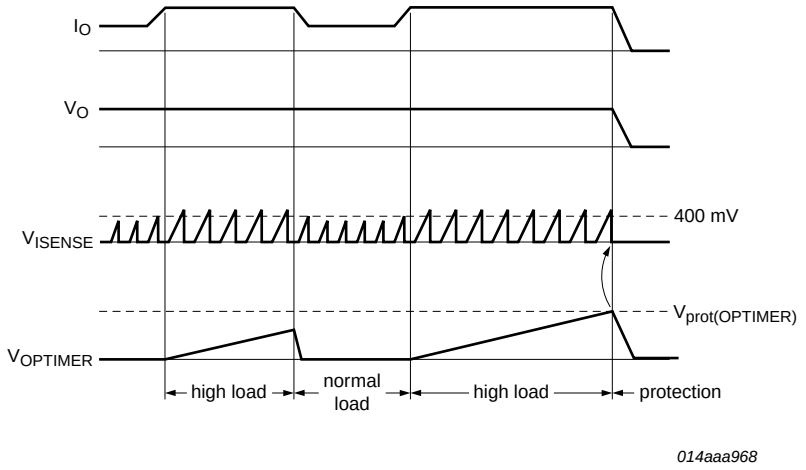


Fig 6. Overpower delay: latched

7.9 Current mode control (ISENSE pin)

Current mode control is used for its good line regulation.

The primary current is sensed by the ISENSE pin across an external resistor R9 (see Figure 3) and compared with an internal reference voltage. The internal reference voltage is proportional to the CTRL pin voltage (see Figure 7).

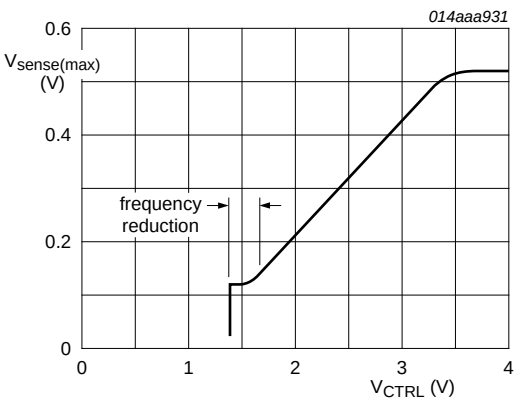


Fig 7. Peak current control using pin ISENSE

Leading edge blanking prevents false triggering due to capacitive discharge when switching on the external power switch (see Figure 8).

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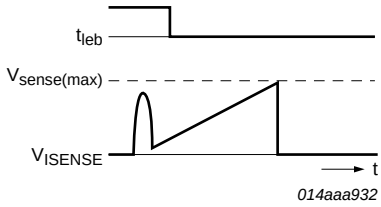


Fig 8. Leading edge blanking using pin ISENSE

7.10 Overpower or high/low line compensation (VINSENSE and ISENSE pins)

The overpower compensation function can be used to realize a maximum output power which is nearly constant over the full input mains.

The overpower compensation circuit measures the input voltage on the VINSENSE pin and outputs a proportionally dependent current on the ISENSE pin. The DC voltage across the soft start resistor limits the maximum peak current on the current sense resistor.

At low output power levels the overpower compensation circuit is switched off (See Figure 9).

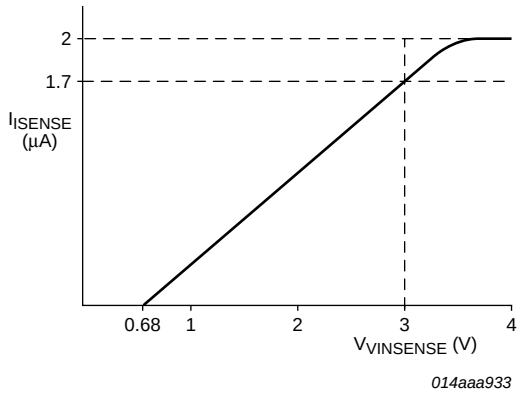


Fig 9. Overpower compensation using pins VINSENSE and ISENSE

7.11 Soft start-up (ISENSE pin)

To prevent audible noise during start-up or a restart condition, a soft start is made. Before the converter starts, the soft start capacitor C6 (see Figure 3) on the ISENSE pin is charged. When the converter starts switching, the primary peak current slowly increases as the soft start capacitor discharges through the soft start resistor (R6, see Figure 3).

The soft start time constant is set by the soft start capacitor value chosen. The soft start resistor value must also be taken into account, but this value is typically defined by the overpower compensation (see Section 7.10).

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7.12 Low power operation

In low power operation switching losses are reduced by lowering the switching frequency. The converter switching frequency is reduced and the peak current is set to 25 % of the maximum peak current (see Figure 7 and Figure 10).

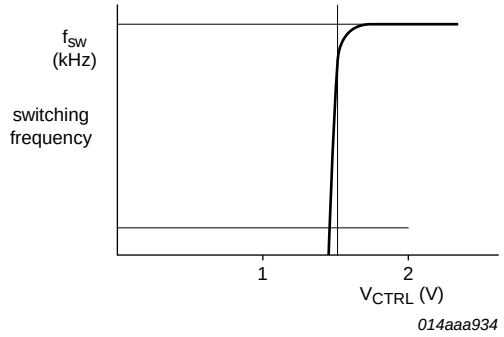


Fig 10. Frequency control

7.13 Driver (DRIVER pin)

The driver circuit to the gate of the power MOSFET has a current sourcing capability of typically 300 mA and a current sink capability of typically 750 mA. This allows for a fast turn-on and turn-off of the power MOSFET for efficient operation.

7.14 OverTemperature Protection (OTP)

Integrated overtemperature protection ensures the IC stops switching if the junction temperature exceeds the thermal temperature shutdown limit.

OTP is a latched protection and it can be reset by removing the voltage on pin VCC.

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8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Voltages						
V_{CC}	supply voltage	continuous		–0.4	+30	V
		t < 100 ms		-	35	V
$V_{VINSENSE}$	voltage on pin VINSENSE	current limited		–0.4	+5.5	V
$V_{PROTECT}$	voltage on pin PROTECT	current limited		–0.4	+5	V
V_{CTRL}	voltage on pin CTRL			–0.4	+5.5	V
$V_{IO(OPTIMER)}$	input/output voltage on pin OPTIMER			–0.4	+5	V
V_{ISENSE}	voltage on pin ISENSE	current limited		–0.4	+5	V
Currents						
I_{CC}	current on pin VCC	δ < 10 %		-	+0.4	A
$I_{I(VINSENSE)}$	input current on pin VINSENSE			–1	+1	mA
$I_{I(PROTECT)}$	input current on pin PROTECT			–1	+1	mA
I_{CTRL}	current on pin CTRL			–3	0	mA
I_{ISENSE}	current on pin ISENSE			–10	+1	mA
I_{DRIVER}	current on pin DRIVER	δ < 10 %		–0.4	+1	A
General						
P_{tot}	total power dissipation	T_{amb} < 75 °C		-	0.5	W
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			–40	+150	°C
ESD						
V_{ESD}	electrostatic discharge voltage	class 1				
		human body model	[1]	-	4000	V
		machine model	[2]	-	300	V
		charged device model		-	750	V

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] Equivalent to discharging a 200 pF capacitor through a 0.75 μH coil and a 10 Ω resistor.

9. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; JEDEC test board	150	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	in free air; JEDEC test board	79	K/W

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10. Characteristics

Table 5. Characteristics

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage management (pin VCC)						
$V_{startup}$	start-up voltage		18.6	20.6	22.6	V
$V_{th(UVLO)}$	undervoltage lockout threshold voltage		11.2	12.2	13.2	V
$V_{clamp(VCC)}$	clamp voltage on pin VCC	activated during restart	-	$V_{startup}$ + 1	-	V
		activated during latched protection	-	$V_{rst(latch)}$ + 1	-	V
V_{hys}	hysteresis voltage	$V_{startup} - V_{th(UVLO)}$	8	9	10	V
$I_{CC(startup)}$	start-up supply current	$V_{CC} < V_{startup}$	5	10	15	µA
$I_{CC(oper)}$	operating supply current	no load on pin DRIVER	0.4	0.5	0.6	mA
$V_{rst(latch)}$	latched reset voltage		4	5	6	V
Input voltage sensing (pin VINSENSE)						
$V_{start(VINSENSE)}$	start voltage on pin VINSENSE	detection level	0.89	0.94	0.99	V
$V_{det(L)(VINSENSE)}$	LOW-level detection voltage on pin VINSENSE		0.68	0.72	0.76	V
$V_{det(H)(VINSENSE)}$	HIGH-level detection voltage on pin VINSENSE		3.39	3.52	3.65	V
$I_{O(VINSENSE)}$	output current on pin VINSENSE		-	–20	-	nA
$V_{clamp(VINSENSE)}$	clamp voltage on pin VINSENSE	$I_{I(VINSENSE)}$ = 50 µA	-	5.2	-	V
Protection input (pin PROTECT)						
$V_{det(L)(PROTECT)}$	LOW-level detection voltage on pin PROTECT		0.47	0.50	0.53	V
$V_{det(H)(PROTECT)}$	HIGH-level detection voltage on pin PROTECT		0.75	0.8	0.85	V
$I_{O(PROTECT)}$	output current on pin PROTECT	$V_{PROTECT} = V_{low(PROTECT)}$	–34	–32	–30	µA
		$V_{PROTECT} = V_{high(PROTECT)}$	87	107	127	µA
$V_{clamp(PROTECT)}$	clamp voltage on pin PROTECT	$I_{I(PROTECT)}$ = 200 µA [1]	3.5	4.1	4.7	V
Peak current control (pin CTRL)						
V_{CTRL}	voltage on pin CTRL	for minimum flyback peak current	1.5	1.8	2.1	V
		for maximum flyback peak current	3.4	3.9	4.3	V
$R_{int(CTRL)}$	internal resistance on pin CTRL		5	7	9	kΩ
$I_{O(CTRL)}$	output current on pin CTRL	V_{CTRL} = 1.4 V	–0.7	–0.5	–0.3	mA
		V_{CTRL} = 3.7 V	–0.28	–0.2	–0.12	mA

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Table 5. Characteristics *…continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pulse width modulator						
f_{osc}	oscillator frequency		62	66.5	71	kHz
f_{mod}	modulation frequency		210	280	350	Hz
Δf_{mod}	modulation frequency variation		± 3	± 4	± 5	kHz
δ_{max}	maximum duty cycle		68.5	72	79	%
$V_{start(red)f}$	frequency reduction start voltage	pin CTRL	1.5	1.8	2.1	V
$V_{\delta(zero)}$	zero duty cycle voltage	pin CTRL	1.25	1.55	1.85	V
Overpower protection (pin OPTIMER)						
$V_{prot(OPTIMER)}$	protection voltage on pin OPTIMER		2.4	2.5	2.6	V
$I_{prot(OPTIMER)}$	protection current on pin OPTIMER	no overpower situation	100	150	200	µA
		overpower situation	–12.2	–10.7	–9.2	µA
Restart timer (pin OPTIMER)						
$V_{restart(OPTIMER)}$	restart voltage on pin OPTIMER	low level	0.8	1.2	1.6	V
		high level	4.1	4.5	4.9	V
$I_{restart(OPTIMER)}$	restart current on pin OPTIMER	charging OPTIMER capacitor	–127	–107	–87	µA
		discharging OPTIMER capacitor	–0.1	0	0.1	µA
Current sense (pin ISENSE)						
$V_{sense(max)}$	maximum sense voltage	$\Delta V/\Delta t$ = 50 mV/µs; $V_{VINSENSE}$ = 0.78 V	0.48	0.51	0.54	V
		$\Delta V/\Delta t$ = 200 mV/µs; $V_{VINSENSE}$ = 0.78 V	0.50	0.53	0.56	V
$V_{th(sense)opp}$	overpower protection sense threshold voltage		370	400	430	mV
$\Delta V_{ISENSE}/\Delta t$	slope compensation voltage on pin ISENSE	$\Delta V/\Delta t$ = 50 mV/µs	17	25	33	mV/µs
t_{leb}	leading edge blanking time		250	300	350	ns
Overpower compensation (pin VINSENSE and pin ISENSE)						
$I_{opc(ISENSE)}$	overpower compensation current on pin ISENSE	$V_{VINSENSE}$ = 1 V; $V_{sense(max)}$ > 400 mV	-	0.28	-	µA
		$V_{VINSENSE}$=3 V; $V_{sense(max)}$ > 400 mV	-	1.7	-	µA

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Table 5. Characteristics *...continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Soft start (pin ISENSE)						
$I_{start(soft)}$	soft start current		–63	–55	–47	µA
$V_{start(soft)}$	soft start voltage	V_{CTRL} = 4 V; enable voltage	-	$V_{sense(max)}$	-	V
$R_{start(soft)}$	soft start resistance		12	-	-	kΩ
Driver (pin DRIVER)						
$I_{source(DRIVER)}$	source current on pin DRIVER	V_{DRIVER} = 2 V	-	–0.3	–0.25	A
$I_{sink(DRIVER)}$	sink current on pin DRIVER	V_{DRIVER} = 2 V	0.25	0.3	-	A
		V_{DRIVER} = 10 V	0.6	0.75	-	A
$V_{O(DRIVER)max}$	maximum output voltage on pin DRIVER		9	10.5	12	V
Temperature protection						
$T_{pl(IC)}$	IC protection level temperature		130	140	150	°C

[1] The clamp voltage on the PROTECT pin is lowered when the IC is in power-down (latched or restart protection).

11. Application information

A power supply with the TEA1733LT/N1 is a flyback converter operating in Continuous conduction mode (See Figure 11).

Capacitor C5 buffers the IC supply voltage, which is powered via resistor R3 at start-up and via the auxiliary winding during normal operation. Sense resistor R9 converts the current through the MOSFET S1 into a voltage on pin ISENSE. The value of R9 defines the maximum primary peak current on MOSFET S1. Resistor R7 reduces the peak current to capacitor C5.

In the example shown in Figure 11, the PROTECT pin is used for OVP and OTP. The OVP level is set by diode Z1 to V_{CC} = 25.8 V. The OTP level is set by Negative Temperature Coefficient (NTC) resistor R4. The VINSENSE pin is used for mains voltage detection and resistors R1 and R2 set the start voltage to about 80 V (AC). The overpower protection time is defined by capacitor C4 is set at 60 ms.

The restart time is defined by capacitor C4 and resistor R8 at 0.5 s.

Resistor R6 and capacitor C6 define the soft start time. Resistor R5 prevents the soft start capacitor C6 from being charged during normal operation caused by negative voltage spikes across the current sense resistor R9.

Capacitor C3 reduces noise on the CTRL pin.

See the application note for more information (Ref. 1).

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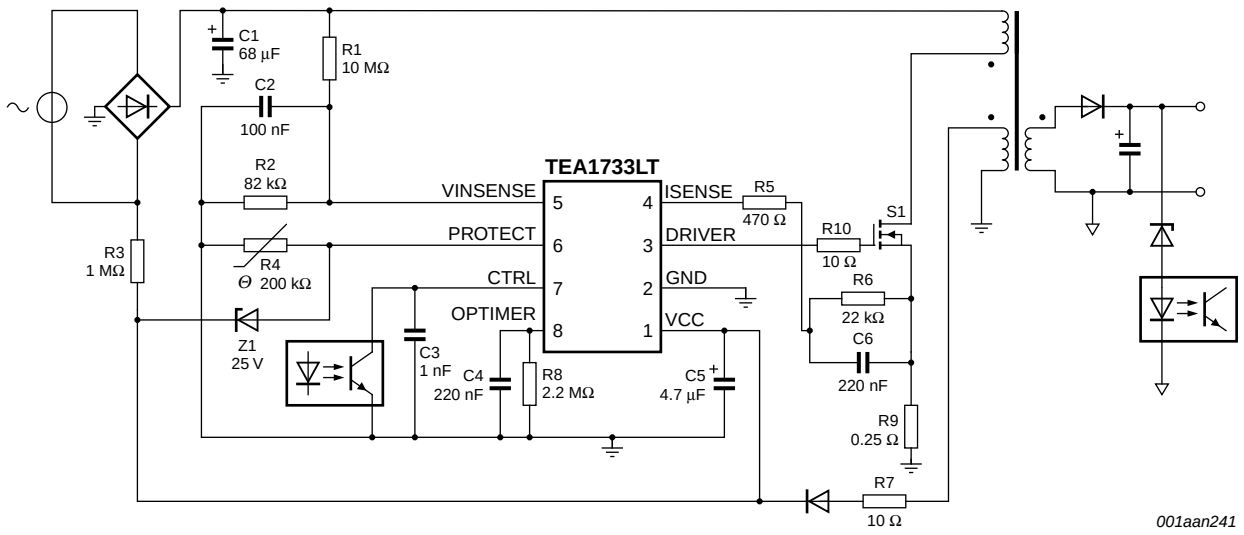


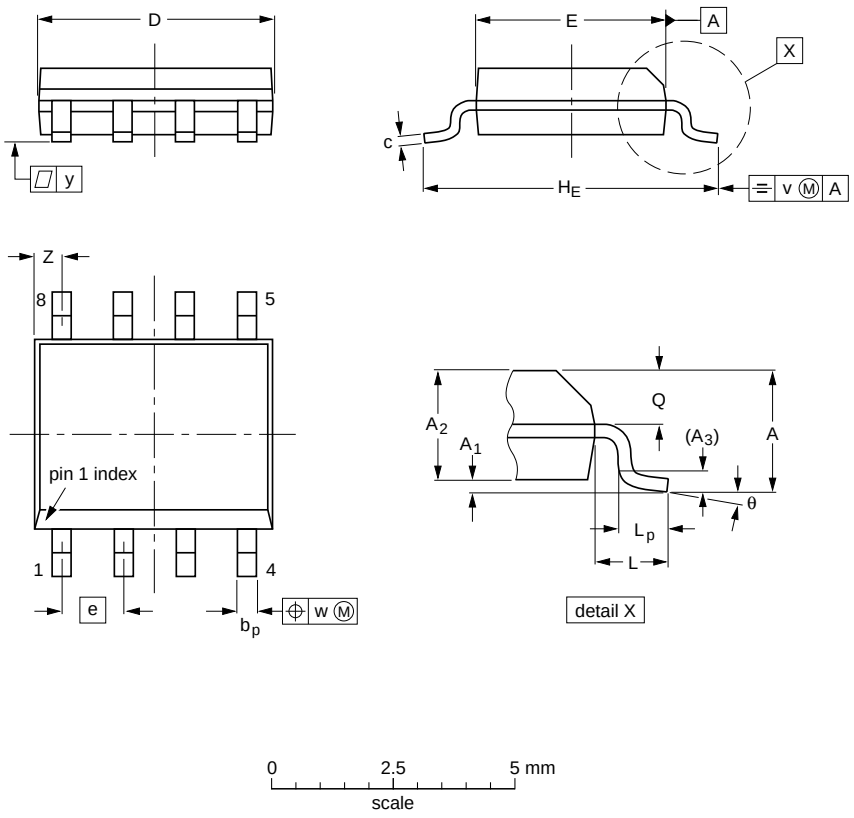
Fig 11. Typical application

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12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 12. Package outline SOT96-1 (SO8)

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13. References

[1] **AN10868 —** GreenChip TEA1733 series fixed frequency flyback controller

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14. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA1733LT v.8	20130716	Product data sheet	-	TEA1733LT v.7
Modifications:	• Section 11 “Application information” has been updated. • Section 13 “References” has been added.			
TEA1733LT v.7	20130409	Product data sheet	-	TEA1733LT v.6
TEA1733LT v.6	20110125	Product data sheet	-	TEA1733T_LT_P v.5
TEA1733T_LT_P v.5	20101119	Product data sheet	-	TEA1733T_LT_P v.4
TEA1733T_LT_P v.4	20100823	Product data sheet	-	TEA1733T_LT_P_LP v.3
TEA1733T_LT_P_LP v.3	20100520	Product data sheet	-	TEA1733T_TEA1733LT v.2
TEA1733T_TEA1733LT v.2	20100326	Product data sheet	-	TEA1733T_TEA1733LT v.1
TEA1733T_TEA1733LT v.1	20091026	Objective data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 16 July 2013
Document identifier: TEA1733LT

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