# Capacitor-Coupled, Switched Shunt, (CCSS) Regulator

## Features

- Efficiencies up to 75% at 20mA
- Less than 20mW standby power
- Optional 6.0V, 12V or 24V fixed output voltage, or adjustable from 6.0V to 28V
- Output current scalable up to 50mA
- 120VAC to 240VAC input
- No magnetics
- Inherent short circuit protection

## Applications

- Household appliances
- White goods
- Lighting controls
- Utility meters

## General Description

The Supertex SR10 is a non-isolated, capacitor-coupled, switched shunt regulator designed to operate directly from the AC line. Output voltage can be either fixed at 6.0V, 12V, or 24V using an internal feedback divider or be adjusted over a 6.0V to 28V range using an external feedback divider. Output current capability is scalable to 50mA, by selection of the series coupling capacitor ($C_S$) on the AC line. Standby power can be under 20mW, and efficiencies of 75% are possible depending upon configuration and degree of transient protection.

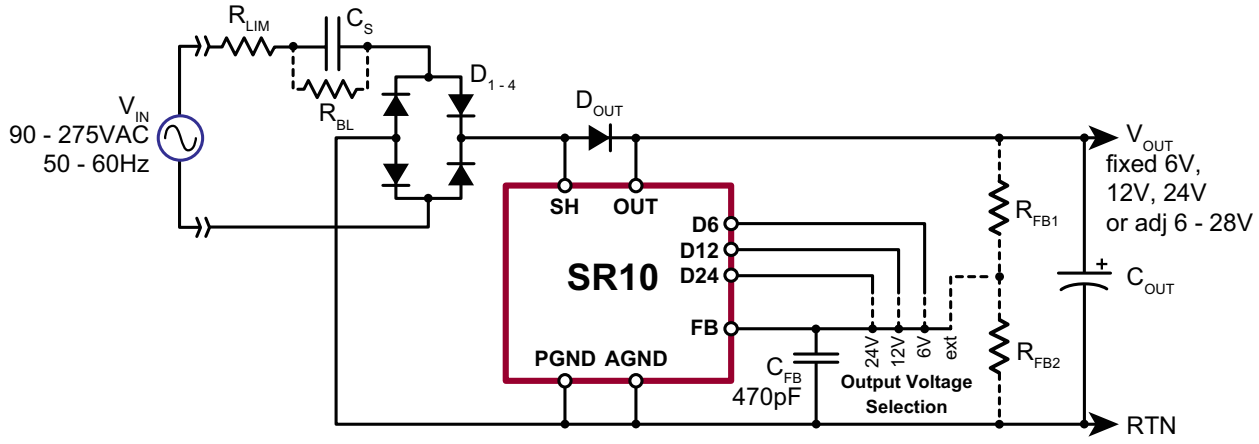
All components except for $C_S$ are low voltage, easing PCB layout and alleviating high voltage creepage concerns.

Inherent short circuit protection is afforded by the reactance of the $C_S$ series capacitor, which limits current even with a dead short on the output. Overcurrent protection (OCP) shuts off the shunt during a line transient.

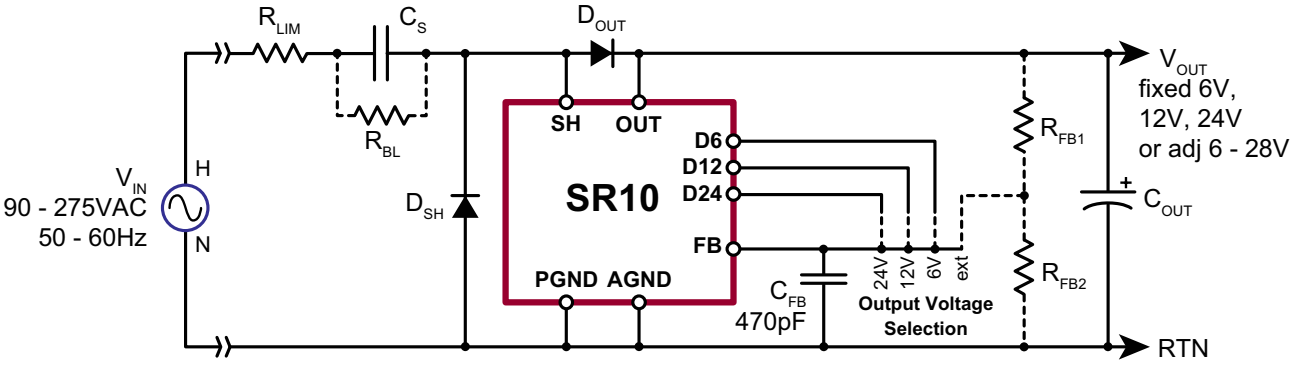
Refer to application note AN-H65 for further information.

## Typical Application Circuits

### Full-wave Rectification




### Half-wave Rectification

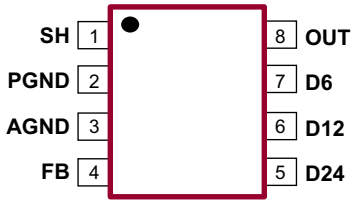


## Ordering Information

| Part Number | Package Option | Packing |
|---|---|---|
| SR10LG-G | 8-Lead SOIC | 2500/Reel |

*-G indicates package is RoHS compliant ('Green')*

## Pin Configuration



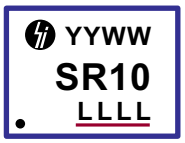

**8-Lead SOIC**
*(top view)*

## Absolute Maximum Ratings

| Parameter | Value |
|---|---|
| $V_{OUT}$, $V_{SH}$ | 40V |
| $V_{FB}$ | 5.0V |
| PGND – AGND | ±300mV |
| $I_{IN(RMS)}$ (SH to PGND) | 300mARMS |
| $I_{DSH}$ (PGND to SH) | 300mA |
| Operating junction temperature | -40°C to +125°C |

*Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.*

## Product Marking




YY = Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

*Package may or may not include the following marks: Si or*

**8-Lead SOIC**

## Typical Thermal Resistance

| Package | $\theta_{ja}$ |
|---|---|
| 8-Lead SOIC | 101°C/W* |

## Recommended Operating Conditions

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_{SH}$ | Peak shunt current | See Maximum Shunt Current Graph | | | | --- |
| $V_{OUT}$ | Output voltage | 6.0 | - | 28 | V | --- |

## Electrical Characteristics *(Unless otherwise noted, $T_A$ = 25°C, Voltages referenced to PGND/AGND pin)*

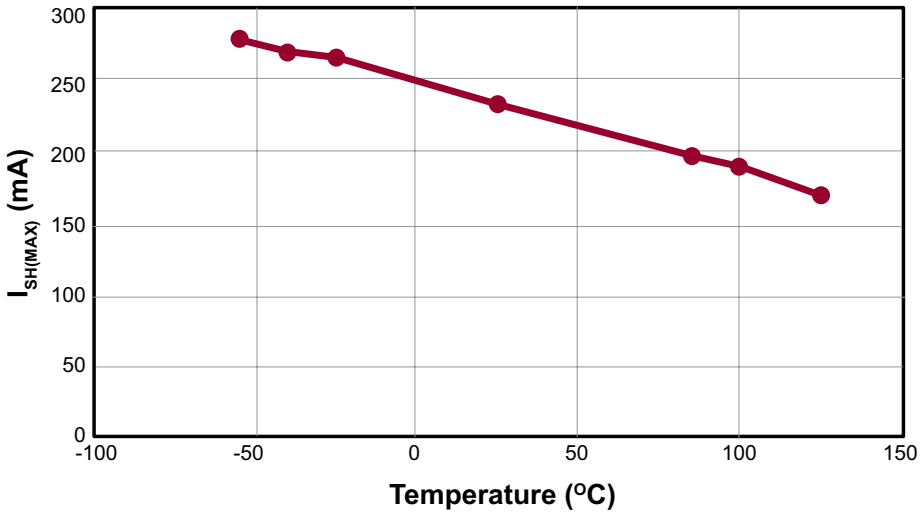
| Sym | Parameter | | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| $V_{FB}$ | Feedback threshold<br>(shunt turn-off) | | 1.02<br>1.02 | 1.20<br>1.20 | 1.38<br>1.38 | V | $T_A$ = 25°C<br>$T_A$ = -40°C to +85°C[1] |
| $I_{FB}$ | FB input bias current | | - | - | ±1.0 | µA | --- |
| $A_{DIV}$ | Internal feedback divider ratio: | D6<br>D12<br>D24 | 4.85<br>9.70<br>19.40 | 5.00<br>10.00<br>20.00 | 5.15<br>10.30<br>20.60 | V/V | $V_{OUT}$ = 6.0V<br>$V_{OUT}$ = 12V<br>$V_{OUT}$ = 24V |
| $R_{DIV}$ | Internal divider resistance[1] | | - | 500 | - | kΩ | OUT to AGND |
| $R_{SH}$ | Shunt on resistance | | - | 3.0 | 7.0 | Ω | 100mA SH to PGND<br>100mA PGND to SH |
| $I_{SH}$ | Max shunt current | | 220 | - | - | mA | $V_{SH}$ < 1.2V, 25°C |
| | | | 180 | - | - | | 85°C[1] |
| $V_D$ | Shunt diode voltage drop | | - | 880 | - | mV | $I_D$ = 220mA |

***Note:***
1. *Guaranteed by design.*

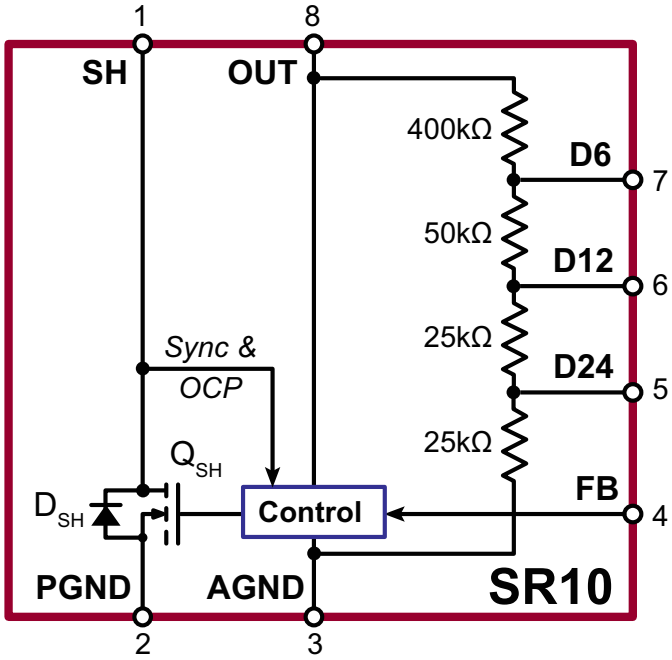
## Electrical Characteristics *(Unless otherwise noted, $T_A$ = 25°C, Voltages referenced to PGND/AGND pin)*

| Sym | Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| $I_{BIAS}$ | Bias current into OUT pin | - | 220 | 400 | µA | 28V applied to the OUT pin |
| $R_{PD}$ | Pull-down resistance on SH | 40 | 50 | 60 | kΩ | $V_{SH}$ = 1.5V |
| $V_{SYNC}$ | Voltage at SH to turn the shunt on (SYNC) | 2.0 | 2.3 | 2.5 | V | --- |
| $V_{OCP}$ | Voltage at SH to turn the shunt off when on (OCP) | 2.0 | 2.3 | 2.5 | V | Shunt on |
| $t_{FALL}$ | Shunt current fall time | - | 15 | - | µs | 90 - 10%, $I_{SH}$ = 100mA |
| $t_{OCP}$ | OCP response time | - | 15 | - | µs | Shunt on, $I_{SHUNT}$ < 10mA, See Figure 3 |

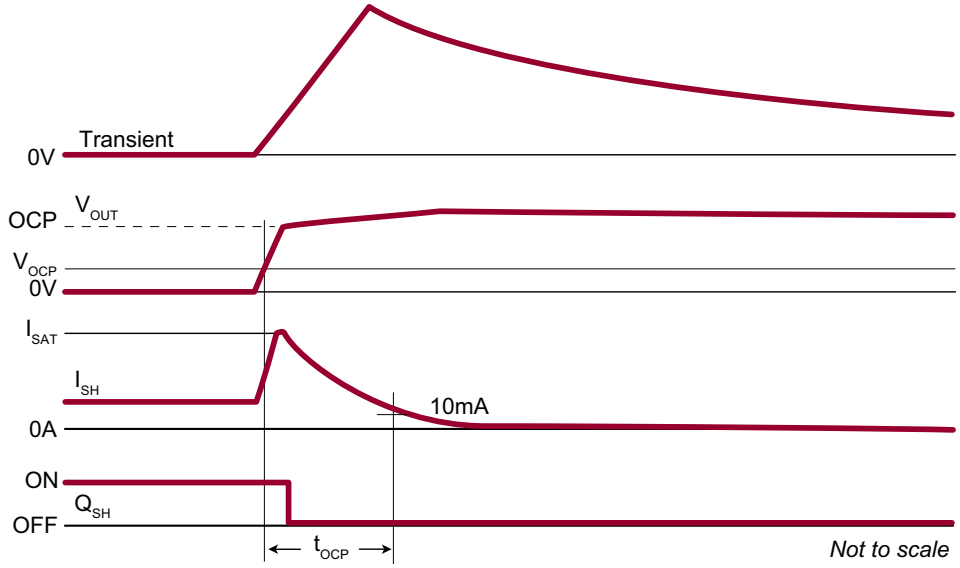
## Maximum Shunt Current



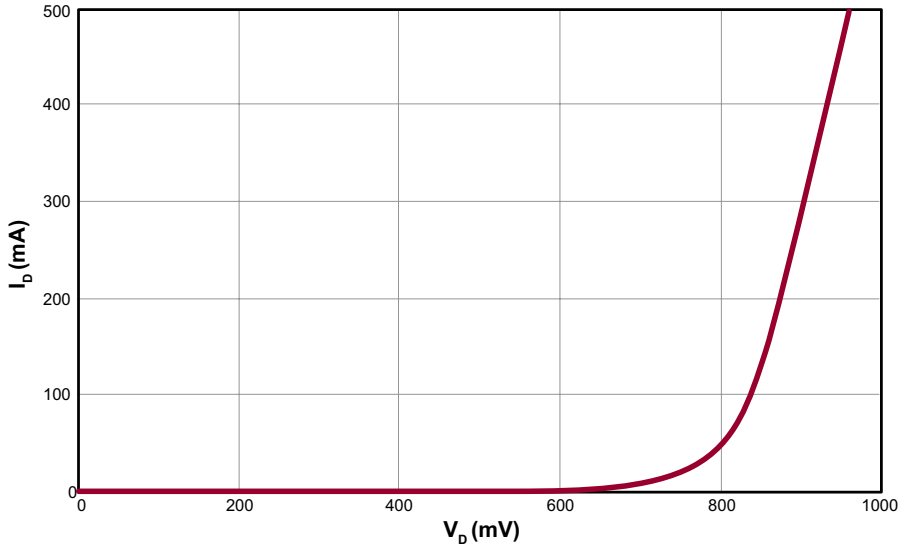

## Internal Block Diagram



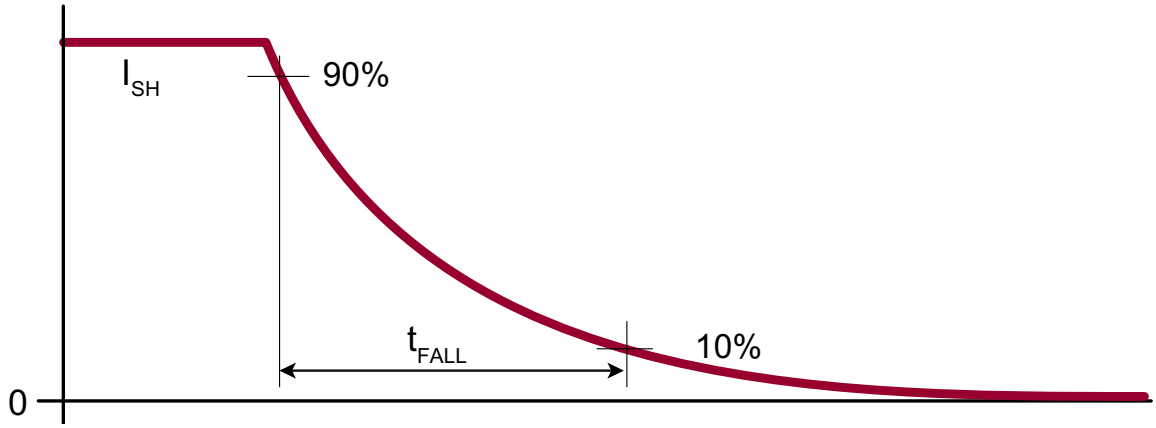
## Figure 1: OCP Timing




## Figure 2: Shunt Diode Characteristics



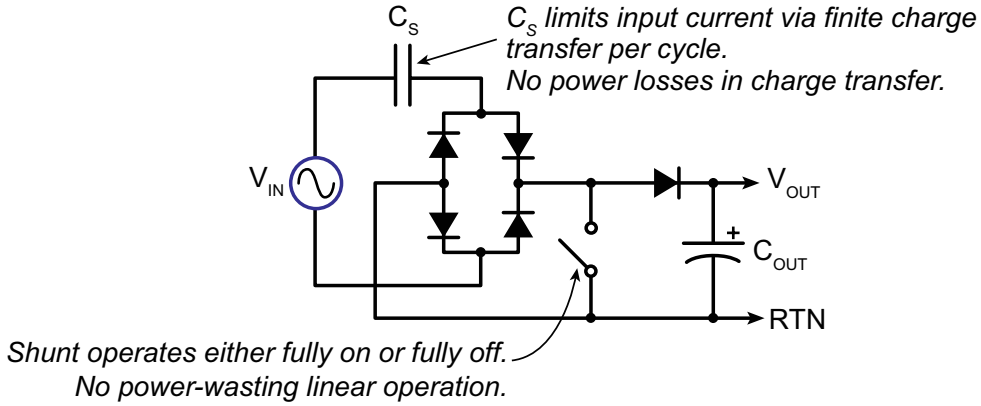

## Figure 3: Shunt Turn-off Fall Time



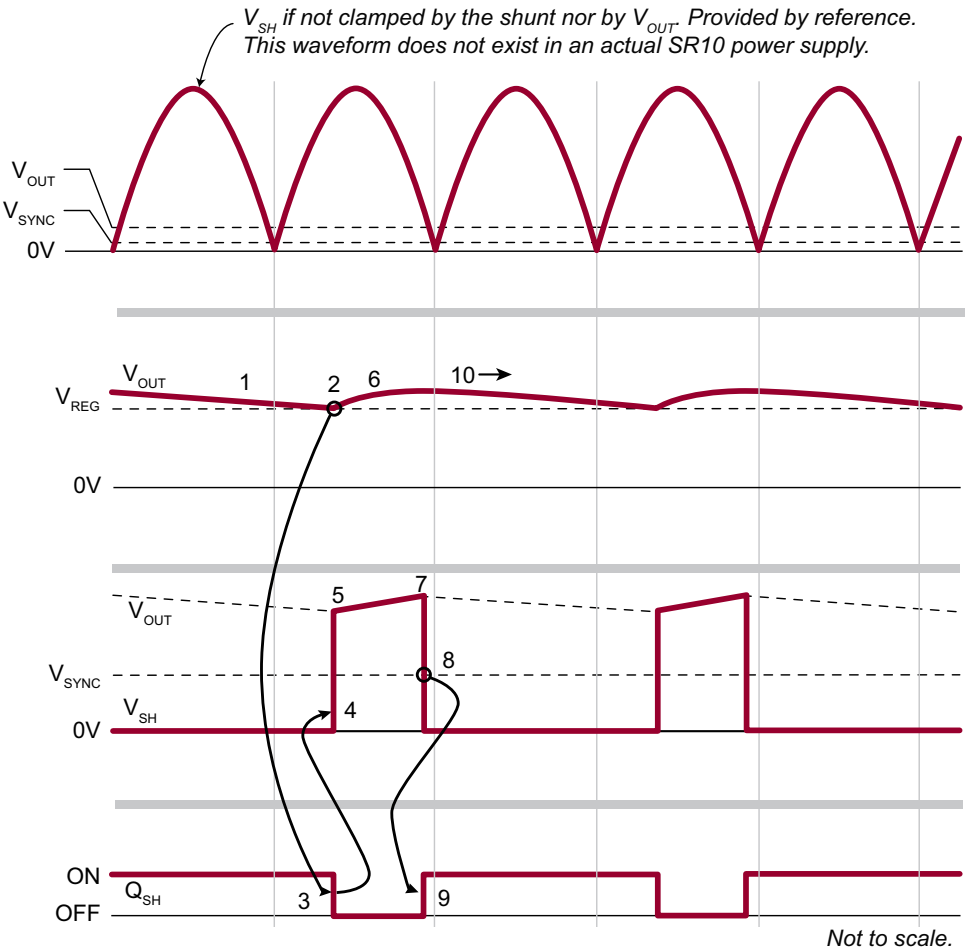
## Application Information

The SR10 is a capacitor-coupled, switched shunt regulator. Capacitor-coupling to the AC line limits input current due to the finite charge per cycle that can be transferred. Contrasting with a traditional Zener shunt, the switched shunt operates either fully on or fully off, resulting in low standby power consumption.

## Simplified Schematic




## Timing




1. *Output voltage decays under load until ...*
2. *it hits the regulation point which...*
3. *turns off the shunt...*
4. *freeing $V_{SH}$ to rise...*
5. *until it is clamped by $V_{OUT}$ where...*
6. *Input current flows to the output, causing $V_{OUT}$ to rise...*
7. *until $V_{SH}$ falls below $V_{OUT}$.*
8. *When it reaches $V_{SYNC}$...*
9. *the shunt is turned on and current no longer flows to the output.*
10. *The cycle repeats.*

## Output Current Capability

Output current capability is largely a function of capacitor $C_S$ and the input voltage. The following table provides approximate current capability for various $C_S$ values and line voltages. Actual current will be less due to losses. Higher output voltages slightly reduce output current capability.

### $C_S$ Table

The following table is based on the previously provided equations for $C_S$. Actual output current may be less due to losses (~5% less). AC line voltage is assumed to be 90 - 135VRMS @ 60Hz or 190 - 275VRMS @ 50Hz. Slashed cells exceed recommended operating conditions for peak shunt current at 85°C.

For universal 120V and 240V operation choose $C_S$ based on 120VAC and make sure that operation at 240VAC does not fall in a slashed cell. The relevant cells are adjacent to each other. For example, if 50mA at 12V is needed and full rectification used, a $C_S$ capacitor of 2.2µF ± 10% provides 53.8mA at 120VAC (90VAC low line). But at 240VAC, the cell to the right (240VAC column) is slashed, and universal operation is not possible. This assumes 120VAC low line is 90VAC and 240VAC high line is 275VAC. For other high/low voltages use the equations.

### Output current capability (mA)

| $C_S$ | $C_S$ Tol | 6V Output | | | | 12V Output | | | | 24V Output | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Half | | Full | | Half | | Full | | Half | | Full | |
| | | 120V 60Hz | 240V 50Hz | 120V 60Hz | 240V 50Hz | 120V 60Hz | 240V 50Hz | 120V 60Hz | 240V 50Hz | 120V 60Hz | 240V 50Hz | 120V 60Hz | 240V 50Hz |
| 220nF | 10% | 2.9 | 5.2 | 5.7 | 10.3 | 2.9 | 5.2 | 5.4 | 10.1 | 2.7 | 5.1 | 4.8 | 9.6 |
| | 20% | 2.6 | 4.7 | 5.0 | 9.2 | 2.5 | 4.6 | 4.8 | 9.0 | 2.4 | 4.5 | 4.3 | 8.5 |
| 330nF | 10% | 4.4 | 7.9 | 8.5 | 15.5 | 4.3 | 7.8 | 8.1 | 15.1 | 4.1 | 7.6 | 7.2 | 14.4 |
| | 20% | 3.9 | 7.0 | 7.6 | 13.8 | 3.8 | 6.9 | 7.2 | 13.4 | 3.6 | 6.8 | 6.4 | 12.8 |
| 470nF | 10% | 6.3 | 11.2 | 12.1 | 22.0 | 6.1 | 11.1 | 11.5 | 21.5 | 5.8 | 10.8 | 10.3 | 20.5 |
| | 20% | 5.6 | 10.0 | 10.8 | 19.6 | 5.4 | 9.9 | 10.2 | 19.1 | 5.2 | 9.6 | 9.1 | 18.2 |
| 680nF | 10% | 9.1 | 16.2 | 17.5 | 31.9 | 8.9 | 16.0 | 16.6 | 31.2 | 8.4 | 15.7 | 14.9 | 29.7 |
| | 20% | 8.1 | 14.4 | 15.6 | 28.4 | 7.9 | 14.3 | 14.8 | 27.7 | 7.5 | 13.9 | 13.2 | 26.4 |
| 1.0µF | 10% | 13.3 | 23.9 | 25.7 | 46.9 | 13.0 | 23.6 | 24.4 | 45.8 | 12.4 | 23.0 | 21.9 | 43.7 |
| | 20% | 11.9 | 21.2 | 22.9 | 41.7 | 11.6 | 21.0 | 21.7 | 40.7 | 11.0 | 20.5 | 19.4 | 38.8 |
| 1.5µF | 10% | 20.0 | 35.8 | 38.6 | 70.4 | 19.5 | 35.4 | 36.7 | 68.7 | 18.6 | 34.6 | 32.8 | 65.5 |
| | 20% | 17.8 | 31.8 | 34.3 | 62.5 | 17.4 | 31.4 | 32.6 | 61.1 | 16.5 | 30.7 | 29.1 | 58.2 |
| 2.2µF | 10% | 29.4 | 52.5 | 56.6 | 103.2 | 28.6 | 51.9 | 53.8 | 100.8 | 27.2 | 50.7 | 48.1 | 96.1 |
| | 20% | 26.1 | 46.6 | 50.3 | 91.7 | 25.5 | 46.1 | 47.8 | 89.6 | 24.2 | 45.1 | 42.7 | 85.4 |

= *Exceeds Recommended Operating Limits*

## Output Voltage

The output voltage may be adjusted over the range of 6V to 28V using either the SR10's internal feedback divider or by using an external divider. The internal divider has taps for 6V, 12V, and 24V which are brought out to pins D6, D12, and D24 respectively. Connecting the appropriate tap to the feedback pin (FB) provides the chosen output voltage.

If an output voltage other than that provided by the internal divider is required, an external feedback divider from $V_{OUT}$ to the FB pin may be used. The range is from 6V to 28V.

| FB pin connected to... | Output Voltage |
|---|---|
| D6 | 6V |
| D12 | 12V |
| D24 | 24V |
| External divider | $V_{OUT} = 1.2V \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$ |

***Note:***
*A 470pF capacitor from FB pin to AGND pin minimizes the effects of a noisy AC line.*

## Pin Description

| Name | Pin | Description |
|---|---|---|
| SH | 1 | Shunt |
| PGND | 2 | Power ground for the shunt |
| AGND | 3 | Analog ground for the controller |
| FB | 4 | Feedback input |
| D24 | 5 | Internal feedback divider 24V tap |
| D12 | 6 | Internal feedback divider 12V tap |
| D6 | 7 | Internal feedback divider 6.0V tap |
| OUT | 8 | Connect to regulator output |

***Note:***
*All pins are low voltage.*

## Additional Information

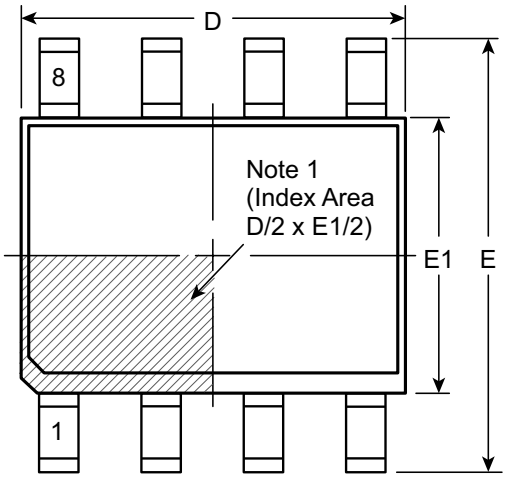
For a more detailed description or for sample circuits, an application note and a demo board are available.

**AH-H65** **CCSS Application Note**
- Explains the operating principle of the capacitor-coupled, switched shunt regulator
- Provides design equations and guidelines
- Specifies special testing considerations

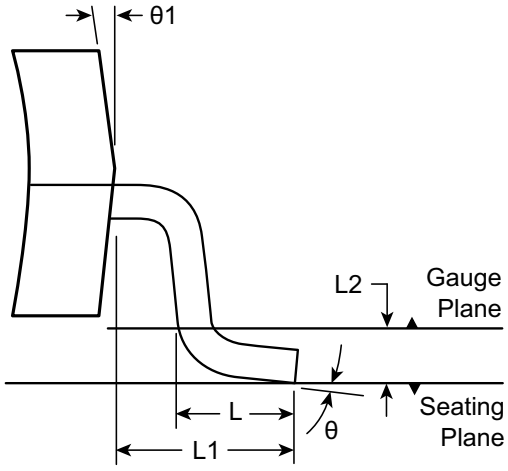
**SR10DB1** **SR10 Demo Board**
- Jumper-selectable half-wave or full-wave recitfication
- Jumper-selectable output voltage
- Socketed components allow easy optimization

# 8-Lead SOIC (Narrow Body) Package Outline (LG)

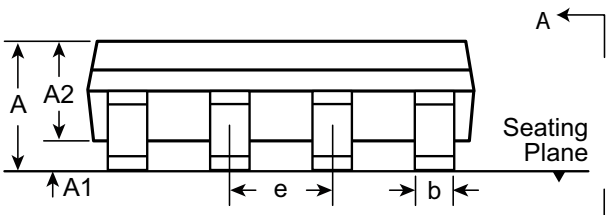
***4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch***



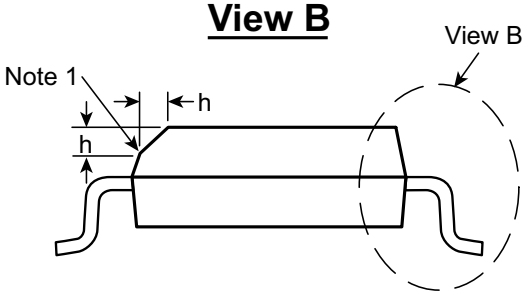

**Top View**




**View B**




**Side View**




**View A-A**

***Note:***

1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

| Symbol | | A | A1 | A2 | b | D | E | E1 | e | h | L | L1 | L2 | θ | θ1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Dimension (mm) | MIN | 1.35* | 0.10 | 1.25 | 0.31 | 4.80* | 5.80* | 3.80* | 1.27 BSC | 0.25 | 0.40 | 1.04 REF | 0.25 BSC | 0° | 5° |
| | NOM | - | - | - | - | 4.90 | 6.00 | 3.90 | | - | - | | | - | - |
| | MAX | 1.75 | 0.25 | 1.65* | 0.51 | 5.00* | 6.20* | 4.00* | | 0.50 | 1.27 | | | 8° | 15° |

*JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.*

** This dimension is not specified in the JEDEC drawing.*

***Drawings are not to scale.***

***Supertex Doc. #:** DSPD-8SOLGTG, Version I041309.*

*(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)*

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