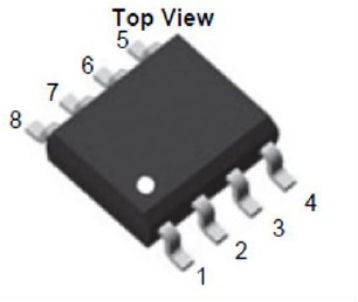
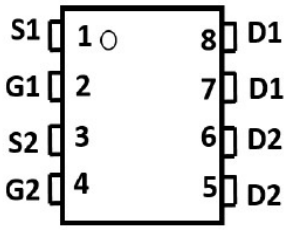
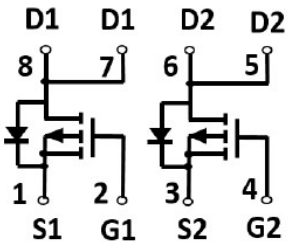
# P-Channel Enhancement Mode Field Effect Transistor




**SOP-8**




## Product Summary

- $V_{DS}$ -30V
- $I_D$ -7.1A
- $R_{DS(ON)}$( at VGS=-10V) ＜25mohm
- $R_{DS(ON)}$( at VGS=-4.5V) ＜40mohm
- 100% $\nabla V_{DS}$ Tested

## General Description

- Trench Power LV MOSFET technology
- High density cell design for low $R_{DS(ON)}$
- High Speed switching

## Applications

- Battery protection
- Load switching
- Power management

■ **Absolute Maximum Ratings** ($T_A$=25℃unless otherwise noted)

| Parameter | | Symbol | Limit | Unit |
|---|---|---|---|---|
| Drain-source Voltage | | $V_{DS}$ | -30 | V |
| Gate-source Voltage | | $V_{GS}$ | ±20 | V |
| Drain Current | | $I_D$ | -7.1 | A |
| Pulsed Drain Current [A] | | $I_{DM}$ | -20 | A |
| Total Power Dissipation | $T_A$=25℃ | $P_D$ | 2.5 | W |
| | $T_A$=70℃ | | 1.6 | W |
| Thermal Resistance Junction-to-Ambient [B] | | $R_{\theta JA}$ | 50 | ℃/ W |
| Junction and Storage Temperature Range | | $T_J$ ,$T_{STG}$ | -55～+150 | ℃ |

## ■ Electrical Characteristics ($T_J$=25℃ unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Static Parameter** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$=0V, $I_D$=-250μA | -30 | | | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=-30V,$V_{GS}$=0V | | | -1 | μA |
| Gate-Body Leakage Current | $I_{GSS}$ | $V_{GS}$=±20V, $V_{DS}$=0V | | | ±100 | nA |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$= $V_{GS}$, $I_D$=-250μA | -1.0 | -1.5 | -2.5 | V |
| Static Drain-Source On-Resistance | $R_{DS(ON)}$ | $V_{GS}$=-10V, $I_D$=-7A | | 20 | 25 | mΩ |
| | | $V_{GS}$=-4.5V, $I_D$=-5A | | 30 | 40 | |
| Diode Forward Voltage | $V_{SD}$ | $I_S$=-7A,$V_{GS}$=0V | | | -1.2 | V |
| **Dynamic Parameters** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$=-15V,$V_{GS}$=0V,f=1MHZ | | 1488 | | pF |
| Output Capacitance | $C_{oss}$ | | | 178 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 164 | | |
| **Switching Parameters** | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{GS}$=-10V,$V_{DS}$=-15V,$I_D$=-7.1A | | 28.44 | | nC |
| Gate-Source Charge | $Q_{gs}$ | | | 5.25 | | |
| Gate-Drain Charge | $Q_{gd}$ | | | 5.17 | | |
| Reverse Recovery Chrage | $Q_{rr}$ | $I_F$=-5A, di/dt=100A/us | | 5.3 | | |
| Reverse Recovery Time | $t_{rr}$ | | | 14 | | ns |
| Turn-on Delay Time | $t_{D(on)}$ | $V_{GS}$=-10V, $V_{DS}$=-15V, $I_D$=-7.1A $R_{GEN}$=2.5Ω | | 10 | | |
| Turn-on Rise Time | $t_r$ | | | 44 | | |
| Turn-off Delay Time | $t_{D(off)}$ | | | 54 | | |
| Turn-off fall Time | $t_f$ | | | 58 | | |

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

## ■ Typical Performance Characteristics

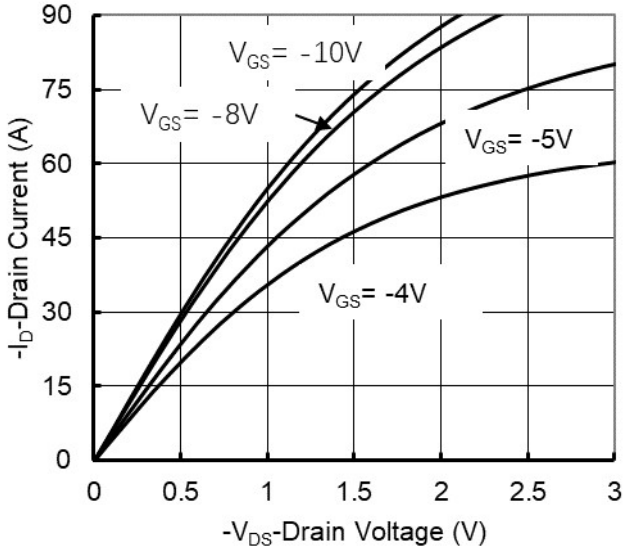



**Figure 1. Output Characteristics**

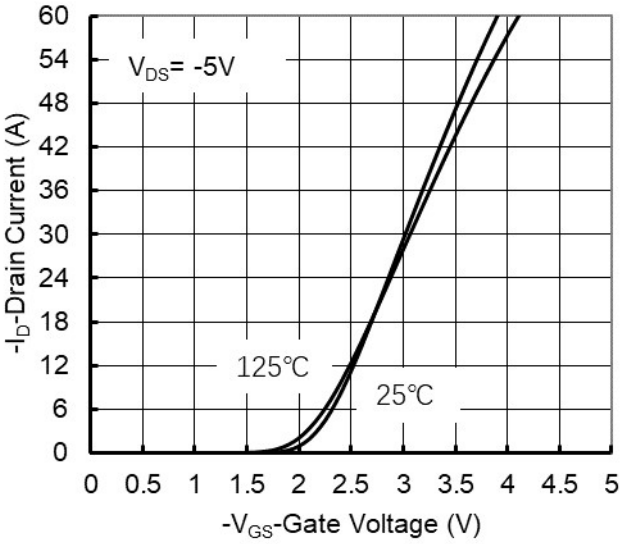



**Figure 2. Transfer Characteristics**

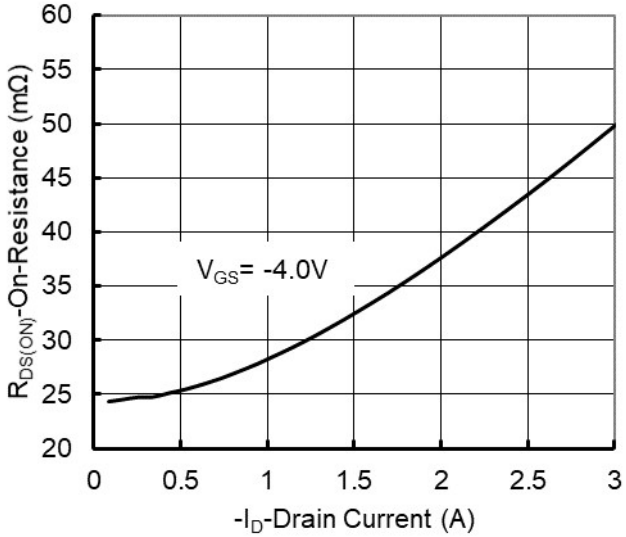



**Figure 3. On-Resistance vs. Drain Current and Gate Voltage**

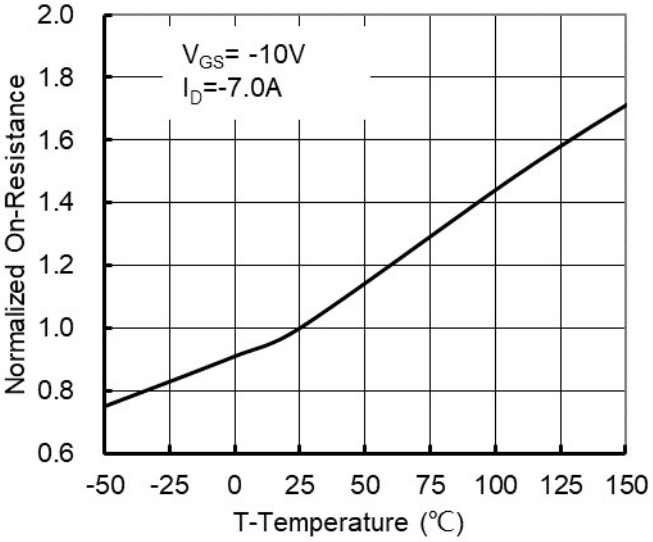



**Figure 4. On-Resistance vs. Junction Temperature**

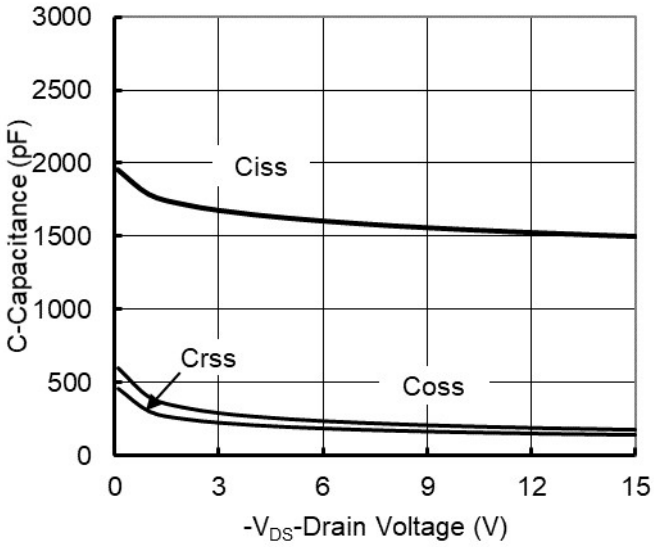



**Figure 5. Capacitance Characteristics**

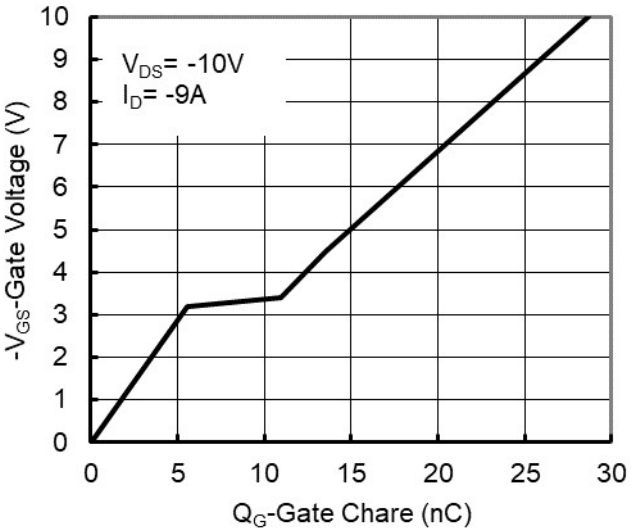



**Figure 6. Gate Charge**

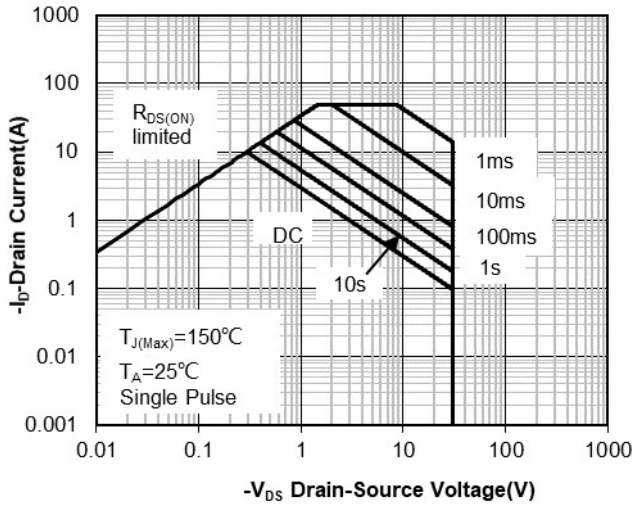



**Figure 7. Safe Operation Area**

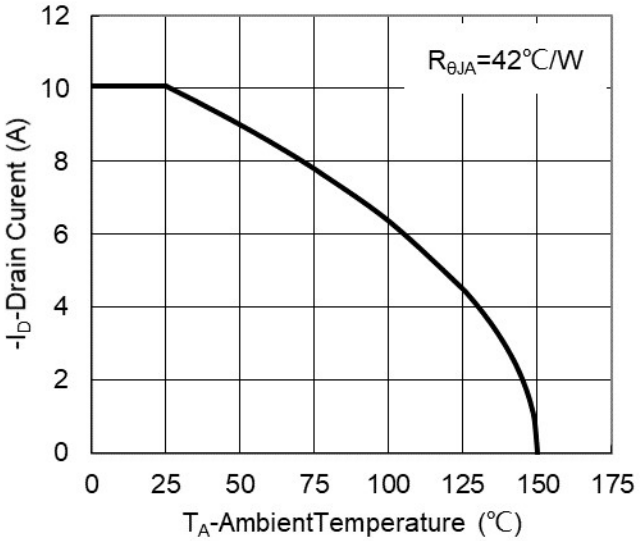
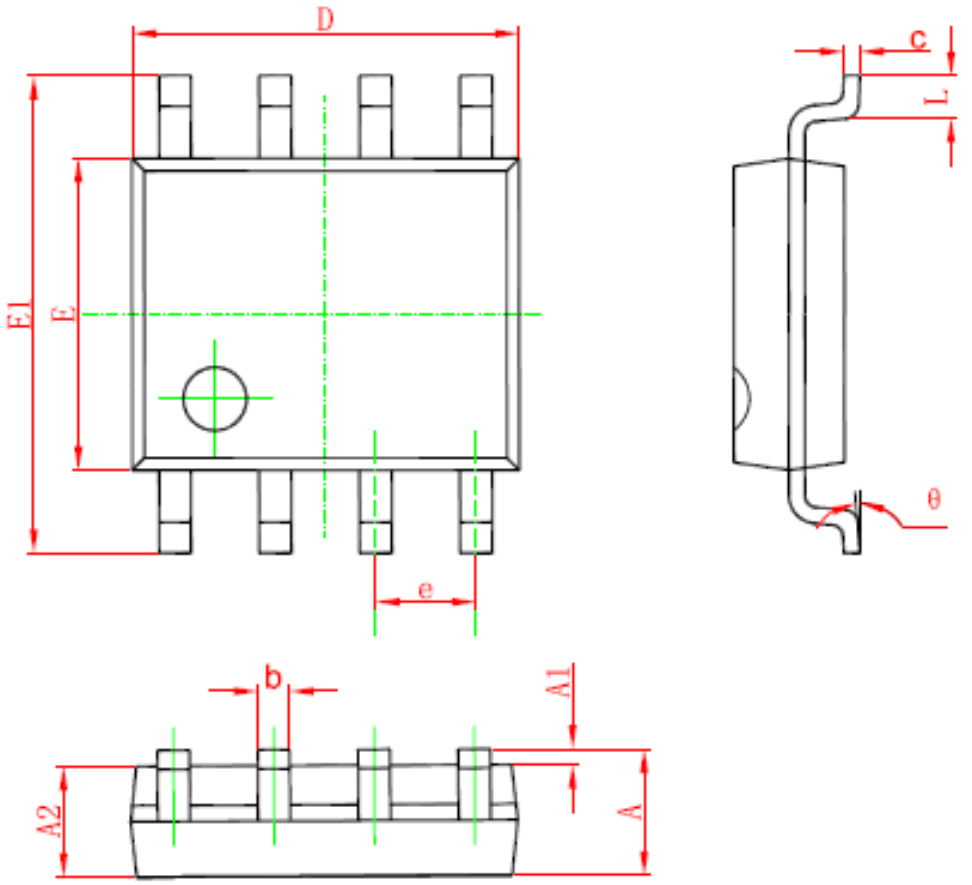



**Figure 8. Maximum Continuous Drain Current vs Ambient Temperature**

## ■ SOP-8 Package information




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| b | 0.330 | 0.510 | 0.013 | 0.020 |
| c | 0.170 | 0.250 | 0.006 | 0.010 |
| D | 4.700 | 5.100 | 0.185 | 0.200 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.200 | 0.228 | 0.244 |
| e | 1.270(BSC) | | 0.050(BSC) | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

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