S-8262A Series

BATTERY PROTECTION IC FOR 2-SERIAL-CELL PACK

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Rev.1.0_03

S-8262A Series is a protection IC for 2-serial-cell lithium-ion / lithium polymer rechargeable batteries and includes high-accuracy voltage detectors and delay circuits.
The S-8262A Series has an alarm signal output pin (AO pin) which outputs the alarm detection signal.
The alarm detection signal is output prior to the charge control FET signal by overcharge detection.

NOT RECOMMENDED FOR NEW DESIGN

■ Features

- High-accuracy voltage detection for each cell

Overcharge detection voltage n (n = 1, 2)	3.900 V to 4.500 V (5 mV steps)	Accuracy ±20 mV (Ta = +25°C) Accuracy ±25 mV (Ta = −10°C to +60°C)
Overcharge release voltage n (n = 1, 2)	3.800 V to 4.500 V*1	Accuracy ±30 mV
Overdischarge detection voltage n (n = 1, 2)	2.000 V to 3.000 V (10 mV steps)	Accuracy ±50 mV
Overdischarge release voltage n (n = 1, 2)	2.000 V to 3.400 V*2	Accuracy ±100 mV
Discharge overcurrent 1 detection voltage	0.050 V to 0.200 V (10 mV steps)	Accuracy ±10 mV
Discharge overcurrent 2 detection voltage	0.200 V to 0.400 V (20 mV steps)	Accuracy ±20 mV
Load short-circuiting detection voltage	0.700 V (fixed)	Accuracy ±100 mV
Charge overcurrent detection voltage	−0.400 V to −0.050 V (25 mV steps)	Accuracy ±20 mV

- Detection delay times are generated only by an internal circuit (external capacitors are unnecessary). Accuracy ±20%
- High-withstand voltage (VM pin and CO pin: Absolute maximum rating = 28 V)
- 0 V battery charge function "available" / "unavailable" is selectable.
- Wide operating temperature range Ta = −40°C to +85°C
- Low current consumption
  - During operation 8.0 µA max. (Ta = +25°C)
  - During power-down 0.1 µA max. (Ta = +25°C)
- Lead-free (Sn 100%), halogen-free

***1.** Overcharge release voltage = Overcharge detection voltage − Overcharge hysteresis voltage
(Overcharge hysteresis voltage n (n = 1, 2) can be selected as 0 V or from a range of 0.1 V to 0.4 V in 25 mV steps.)

***2.** Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage
(Overdischarge hysteresis voltage n (n = 1, 2) can be selected as 0 V or from a range of 0.1 V to 0.7 V in 100 mV steps.)

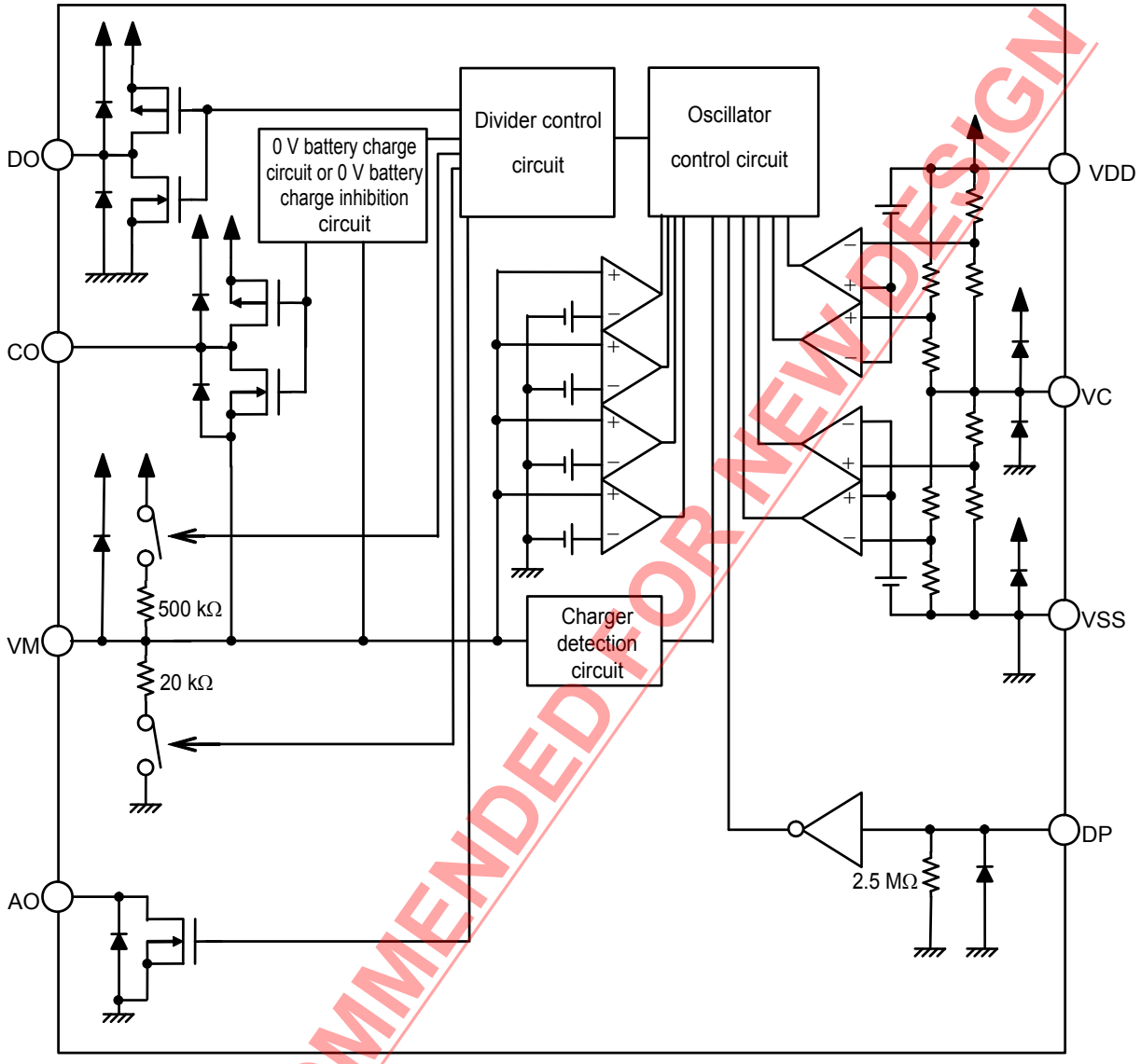
■ Applications

- Lithium-ion rechargeable battery packs
- Lithium polymer rechargeable battery packs

■ Package

- SNT-8A

■ Block Diagram



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Remark All diodes shown in figure are parasitic diodes.

Figure 1

■ Product Name Structure

1. Product name

S-8262A xx - I8T1 U

Environmental code
U: Lead-free (Sn 100%), halogen-free

Package abbreviation and IC packing specifications*1
I8T1: SNT-8A, Tape

Serial code*2
Sequentially set from AA to ZZ

***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SNT-8A	PH008-A-P-SD	PH008-A-C-SD	PH008-A-R-SD	PH008-A-L-SD

3. Product name list

3. 1 SNT-8A

Table 2

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Over-discharge Detection Voltage [V_{DL}]	Over-discharge Release Voltage [V_{DU}]	Discharge Overcurrent 1 Detection Voltage [V_{DIOV1}]	Discharge Overcurrent 2 Detection Voltage [V_{DIOV2}]	Charge Overcurrent Detection Voltage [V_{CIOV}]	0 V Battery Charge Function	Power-down Function	Delay Time Combination*1
S-8262AAA-I8T1U	4.225 V	4.100 V	2.000 V	2.000 V	0.100 V	0.300 V	−0.100 V	Available	Available	(1)
S-8262AAB-I8T1U	4.225 V	4.100 V	2.000 V	2.000 V	0.100 V	0.300 V	−0.100 V	Available	Available	(2)

***1.** Refer to **Table 3** about the details of the delay time combinations.

Remark Please contact our sales office for the products with detection voltage value other than those specified above.

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Table 3 (1 / 2)

Delay Time Combination	Overcharge Detection Delay Time [t_{CU}]	Overcharge Release Delay Time [t_{CL}]	Overcharge Alarm Detection Delay Time [t_{AU}]	Overcharge Alarm Release Delay Time [t_{AL}]	Overdischarge Detection Delay Time [t_{DL}]
(1)	8.2 s	2 ms	8 ms	128 ms	128 ms
(2)	8.2 s	2 ms	8 ms	128 ms	128 ms

Table 3 (2 / 2)

Delay Time Combination	Discharge Overcurrent 1 Detection Delay Time [t_{DIOV1}]	Discharge Overcurrent 2 Detection Delay Time [t_{DIOV2}]	Load Short-circuiting Detection Delay Time [t_{SHORT}]	Charge Overcurrent Detection Delay Time [t_{CIOV}]
(1)	128 ms	8 ms	280 µs	8 ms
(2)	64 ms	4 ms	280 µs	8 ms

Remark The delay times can be changed within the range listed **Table 4**. For details, please contact our sales office.

Table 4

Delay Time	Symbol	Selection Range			Remark
Overcharge detection delay time	t_{CU}	2.1 s	4.1 ms	8.2 s*1	Select a value from the left.
Overcharge release delay time	t_{CL}	1 ms	2 ms*1	4 ms	Select a value from the left.
Overcharge alarm detection delay time	t_{AU}	4 ms	8 ms*1	16 ms	Select a value from the left.
Overcharge alarm release delay time	t_{AL}	128 ms*1	256 ms	512 ms	Select a value from the left.
Overdischarge detection delay time	t_{DL}	32 ms	64 ms	128 ms*1	Select a value from the left.
Discharge overcurrent 1 detection delay time	t_{DIOV1}	64 ms	128 ms*1	256 ms	Select a value from the left.
Discharge overcurrent 2 detection delay time	t_{DIOV2}	4 ms	8 ms*1	16 ms	Select a value from the left.
Load short-circuiting detection delay time	t_{SHORT}	280 µs*1	500 µs	1 ms	Select a value from the left.
Charge overcurrent detection delay time	t_{CIOV}	4 ms	8 ms*1	16 ms	Select a value from the left.

***1.** This value is the delay time of the standard products.

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■ Pin Configuration

1. SNT-8A

Top view

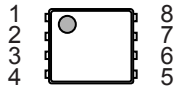

Figure 2

Table 5

Pin No.	Symbol	Description
1	CO	Connection pin of charge control FET gate (CMOS output)
2	DO	Connection pin of discharge control FET gate (CMOS output)
3	AO	Overcharge alarm signal output pin (Nch open drain output)
4	VSS	Input pin for negative power supply, connection pin for negative voltage of battery 2
5	VC	Connection pin for negative voltage of battery 1, connection pin for positive voltage of battery 2
6	VDD	Input pin for positive power supply, connection pin for positive voltage of battery 1
7	DP	Test mode switching pin (shortening delay time)
8	VM	Voltage detection pin between VM pin and VSS pin (Overcurrent / charger detection pin)

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■ Absolute Maximum Ratings

Table 6

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin	V_{DS}	VDD	V_{SS} − 0.3 to V_{SS} + 12	V
VC pin input voltage	V_{VC}	VC	V_{SS} − 0.3 to V_{DD} + 0.3	V
DP pin input voltage	V_{DP}	DP	V_{SS} − 0.3 to V_{SS} + 12	V
VM pin input voltage	V_{VM}	VM	V_{DD} − 28 to V_{DD} + 0.3	V
DO pin output voltage	V_{DO}	DO	V_{SS} − 0.3 to V_{DD} + 0.3	V
CO pin output voltage	V_{CO}	CO	V_{VM} − 0.3 to V_{DD} + 0.3	V
AO pin output voltage	V_{AO}	AO	V_{SS} − 0.3 to V_{SS} + 12	V
Power dissipation	P_D	−	450*1	mW
Operating ambient temperature	T_{opr}	−	−40 to +85	°C
Storage temperature	T_{stg}	−	−55 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name: JEDEC STANDARD51-7

Caution **The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

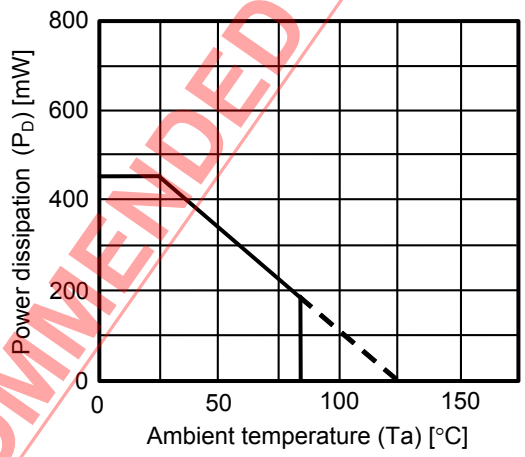

Figure 3 Package Power Dissipation (When Mounted on Board)

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■ Electrical Characteristics

1. Ta = +25°C

Table 7 (1 / 2)

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
DETECTION VOLTAGE							
Overcharge detection voltage n (n = 1, 2)	V_{CUn}	–	V_{CU} – 0.020	V_{CU}	V_{CU} + 0.020	V	1
		Ta = –10°C to +60°C*1	V_{CU} – 0.025	V_{CU}	V_{CU} + 0.025	V	1
Overcharge release voltage n (n = 1, 2)	V_{CLn}	–	V_{CL} – 0.030	V_{CL}	V_{CL} + 0.030	V	1
Overdischarge detection voltage n (n = 1, 2)	V_{DLn}	–	V_{DL} – 0.050	V_{DL}	V_{DL} + 0.050	V	2
Overdischarge release voltage n (n = 1, 2)	V_{DUn}	–	V_{DU} – 0.100	V_{DU}	V_{DU} + 0.100	V	2
Discharge overcurrent 1 detection voltage	V_{DIOV1}	–	V_{DIOV1} – 0.010	V_{DIOV1}	V_{DIOV1} + 0.010	V	2
Discharge overcurrent 2 detection voltage	V_{DIOV2}	–	V_{DIOV2} – 0.020	V_{DIOV2}	V_{DIOV2} + 0.020	V	2
Load short-circuiting detection voltage	V_{SHORT}	–	0.600	0.700	0.800	V	2
Charge overcurrent detection voltage	V_{CIOV}	–	V_{CIOV} – 0.020	V_{CIOV}	V_{CIOV} + 0.020	V	2
0 V BATTERY CHARGE FUNCTION							
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charge function "available"	0.0	0.7	1.0	V	2
0 V battery charge inhibition battery voltage	V_{0INH}	0 V battery charge function "unavailable"	0.4	0.8	1.1	V	2
INTERNAL RESISTANCE							
Resistance between VM pin and VDD pin	R_{VMD}	V1 = V2 = 1.8 V, V3 = 0 V	160	500	1500	kΩ	3
Resistance between VM pin and VSS pin	R_{VMS}	V1 = V2 = 3.5 V, V3 = 1.0 V	10	20	40	kΩ	3
INPUT VOLTAGE							
Operating voltage between VDD pin and VSS pin	V_{DSOP1}	–	1.5	–	10	V	–
DP pin voltage "H"	V_{DPH}	V1 = V2 = 3.5 V	V_{DS} × 0.6	–	V_{DS} × 0.9	V	4
DP pin voltage "L"	V_{DPL}	V1 = V2 = 3.5 V	V_{DS} × 0.1	–	V_{DS} × 0.4	V	4
INPUT CURRENT							
Current consumption during operation	I_{OPE}	V1 = V2 = 3.5 V, V3 = 0 V	–	4.0	8.0	μA	2
Current consumption during power-down	I_{PDN}	V1 = V2 = 1.5 V, V3 = 3.0 V	–	–	0.1	μA	2
VC pin current	I_{VC}	V1 = V2 = 3.5 V, V3 = 0 V	0.2	0.7	1.5	μA	2
OUTPUT RESISTANCE							
CO pin resistance "H"	R_{COH}	V1 = V2 = 3.5 V, V3 = 0 V, V5 = 6.5 V	2.5	5	10	kΩ	4
CO pin resistance "L"	R_{COL}	V1 = V2 = 4.7 V, V3 = 0 V, V5 = 0.5 V	2.5	5	10	kΩ	4
DO pin resistance "H"	R_{DOH}	V1 = V2 = 3.5 V, V3 = 0 V, V6 = 6.5 V	5	10	20	kΩ	4
DO pin resistance "L"	R_{DOL}	V1 = V2 = 1.8 V, V3 = 3.6 V, V6 = 0.5 V	5	10	20	kΩ	4
OUTPUT CURRENT							
AO pin sink current	I_{AOL}	V1 = V2 = 4.7 V, V4 = 0.5 V	10	–	–	μA	4
AO pin leak current	I_{AOH}	V4 = 10.0 V	–	–	0.1	μA	4

*1. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

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Table 7 (2 / 2)

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
DELAY TIME							
Overcharge detection delay time	t_{CU}	–	$t_{CU} \times 0.8$	t_{CU}	$t_{CU} \times 1.2$	–	5
Overcharge release delay time	t_{CL}	–	$t_{CL} \times 0.8$	t_{CL}	$t_{CL} \times 1.2$	–	5
Overcharge alarm detection delay time	t_{AU}	–	$t_{AU} \times 0.8$	t_{AU}	$t_{AU} \times 1.2$	–	5
Overcharge alarm release delay time	t_{AL}	–	$t_{AL} \times 0.8$	t_{AL}	$t_{AL} \times 1.2$	–	5
Overdischarge detection delay time	t_{DL}	–	$t_{DL} \times 0.8$	t_{DL}	$t_{DL} \times 1.2$	–	5
Discharge overcurrent 1 detection delay time	t_{DIOV1}	–	$t_{DIOV1} \times 0.8$	t_{DIOV1}	$t_{DIOV1} \times 1.2$	–	5
Discharge overcurrent 2 detection delay time	t_{DIOV2}		$t_{DIOV2} \times 0.8$	t_{DIOV2}	$t_{DIOV2} \times 1.2$	–	5
Load short-circuiting detection delay time	t_{SHORT}	–	$t_{SHORT} \times 0.8$	t_{SHORT}	$t_{SHORT} \times 1.2$	–	5
Charge overcurrent detection delay time	t_{CIOV}	–	$t_{CIOV} \times 0.8$	t_{CIOV}	$t_{CIOV} \times 1.2$	–	5

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2. Ta = –40°C to +85°C

Table 8 (1 / 2)

(Ta = –40°C to +85°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
DETECTION VOLTAGE							
Overcharge detection voltage n (n = 1, 2)	V_{CUn}	–	V_{CU} – 0.045	V_{CU}	V_{CU} + 0.030	V	1
Overcharge release voltage n (n = 1, 2)	V_{CLn}	–	V_{CL} – 0.070	V_{CL}	V_{CL} + 0.040	V	1
Overdischarge detection voltage n (n =1, 2)	V_{DLn}	–	V_{DL} – 0.085	V_{DL}	V_{DL} + 0.060	V	2
Overdischarge release voltage n (n =1, 2)	V_{DUn}	–	V_{DU} – 0.140	V_{DU}	V_{DU} + 0.110	V	2
Discharge overcurrent 1 detection voltage	V_{DIOV1}	–	V_{DIOV1} – 0.015	V_{DIOV1}	V_{DIOV1} + 0.015	V	2
Discharge overcurrent 2 detection voltage	V_{DIOV2}	–	V_{DIOV2} – 0.030	V_{DIOV2}	V_{DIOV2} + 0.030	V	2
Load short-circuiting detection voltage	V_{SHORT}	–	0.550	0.700	0.850	V	2
Charge overcurrent detection voltage	V_{CIOV}	–	V_{CIOV} – 0.030	V_{CIOV}	V_{CIOV} + 0.030	V	2
0 V BATTERY CHARGE FUNCTION							
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charge function "available"	0.0	0.7	1.5	V	2
0 V battery charge inhibition battery voltage	V_{0INH}	0 V battery charge function "unavailable"	0.3	0.8	1.3	V	2
INTERNAL RESISTANCE							
Resistance between VM pin and VDD pin	R_{VMD}	V1 = V2 = 1.8 V, V3 = 0 V	30	500	2190	kΩ	3
Resistance between VM pin and VSS pin	R_{VMS}	V1 = V2 = 3.5 V, V3 = 1.0 V	7.2	20	44	kΩ	3
INPUT VOLTAGE							
Operating voltage between VDD pin and VSS pin	V_{DSOP1}	–	1.5	–	10	V	–
DP pin voltage "H"	V_{DPH}	V1 = V2 = 3.5 V	V_{DS} × 0.55	–	V_{DS} × 0.95	V	4
DP pin voltage "L"	V_{DPL}	V1 = V2 = 3.5 V	V_{DS} × 0.05	–	V_{DS} × 0.45	V	4
INPUT CURRENT							
Current consumption during operation	I_{OPE}	V1 = V2 = 3.5 V, V3 = 0 V	–	4.0	8.5	µA	2
Current consumption during power-down	I_{PDN}	V1 = V2 = 1.5 V, V3 = 3.0 V	–	–	0.15	µA	2
VC pin current	I_{VC}	V1 = V2 = 3.5 V, V3 = 0 V	0.2	0.7	2.0	µA	2
OUTPUT RESISTANCE							
CO pin resistance "H"	R_{COH}	V1 = V2 = 3.5 V, V3 = 0 V, V5 = 6.5 V	1.2	5	15	kΩ	4
CO pin resistance "L"	R_{COL}	V1 = V2 = 4.7 V, V3 = 0 V, V5 = 0.5 V	1.2	5	15	kΩ	4
DO pin resistance "H"	R_{DOH}	V1 = V2 = 3.5 V, V3 = 0 V, V6 = 6.5 V	2.4	10	30	kΩ	4
DO pin resistance "L"	R_{DOL}	V1 = V2 = 1.8 V, V3 = 3.6 V, V6 = 0.5 V	2.4	10	30	kΩ	4
OUTPUT CURRENT							
AO pin sink current	I_{AOL}	V1 = V2 = 4.7 V, V4 = 0.5 V	10	–	–	µA	4
AO pin leak current	I_{AOH}	V4 = 10.0 V	–	–	0.15	µA	4

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Table 8 (2 / 2)

(Ta = −40°C to +85°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
DELAY TIME							
Overcharge detection delay time	t_{CU}	–	$t_{CU} \times 0.3$	t_{CU}	$t_{CU} \times 2.0$	–	5
Overcharge release delay time	t_{CL}	–	$t_{CL} \times 0.3$	t_{CL}	$t_{CL} \times 2.0$	–	5
Overcharge alarm detection delay time	t_{AU}	–	$t_{AU} \times 0.3$	t_{AU}	$t_{AU} \times 2.0$	–	5
Overcharge alarm release delay time	t_{AL}	–	$t_{AL} \times 0.3$	t_{AL}	$t_{AL} \times 2.0$	–	5
Overdischarge detection delay time	t_{DL}	–	$t_{DL} \times 0.3$	t_{DL}	$t_{DL} \times 2.0$	–	5
Discharge overcurrent 1 detection delay time	t_{DIOV1}	–	$t_{DIOV1} \times 0.3$	t_{DIOV1}	$t_{DIOV1} \times 2.0$	–	5
Discharge overcurrent 2 detection delay time	t_{DIOV2}	–	$t_{DIOV2} \times 0.3$	t_{DIOV2}	$t_{DIOV2} \times 2.0$	–	5
Load short-circuiting detection delay time	t_{SHORT}	–	$t_{SHORT} \times 0.3$	t_{SHORT}	$t_{SHORT} \times 2.0$	–	5
Charge overcurrent detection delay time	t_{CIOV}	–	$t_{CIOV} \times 0.3$	t_{CIOV}	$t_{CIOV} \times 2.0$	–	5

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■ Test Circuits

1. Overcharge detection voltage, overcharge release voltage (Test circuit 1)

Overcharge detection voltage (V_{CU1}) is defined as the voltage V1 at which V_{CO} goes from "H" to "L" when the voltage V1 is gradually increased from the set conditions of V1 = V2 = V_{CU} – 0.05 V, V3 = 0 V. After that, overcharge release voltage (V_{CL1}) is defined as the voltage V1 at which V_{CO} goes from "L" to "H" when the voltage V1 is gradually decreased after setting V2 = 3.5 V. Overcharge hysteresis voltage (V_{HC1}) is defined as the difference between V_{CU1} and V_{CL1}.
Overcharge detection voltage (V_{CU2}) is defined as the voltage V2 at which V_{CO} goes from "H" to "L" when the voltage V2 is gradually increased from the set conditions of V1 = V2 = V_{CU} – 0.05 V, V3 = 0 V. After that, overcharge release voltage (V_{CL2}) is defined as the voltage V2 at which V_{CO} goes from "L" to "H" when the voltage V2 is gradually decreased after setting V1 = 3.5 V. Overcharge hysteresis voltage (V_{HC2}) is defined as the difference between V_{CU2} and V_{CL2}.

2. Overdischarge detection voltage, overdischarge release voltage (Test circuit 2)

Overdischarge detection voltage (V_{DL1}) is defined as the voltage V1 at which V_{DO} goes from "H" to "L" when the voltage V1 is gradually decreased from the set conditions of V1 = V2 = 3.5 V, V3 = 0 V. After that, overdischarge release voltage (V_{DU1}) is defined as the voltage V1 at which V_{DO} goes from "L" to "H" when the voltage V1 is gradually increased. Overdischarge hysteresis voltage (V_{HD1}) is defined as the difference between V_{DU1} and V_{DL1}.
Overdischarge detection voltage (V_{DL2}) is defined as the voltage V2 at which V_{DO} goes from "H" to "L" when the voltage V2 is gradually decreased from the set conditions of V1 = V2 = 3.5 V, V3 = 0 V. After that, overdischarge release voltage (V_{DU2}) is defined as the voltage V2 at which V_{DO} goes from "L" to "H" when the voltage V2 is gradually increased. Overdischarge hysteresis voltage (V_{HD2}) is defined as the difference between V_{DU2} and V_{DL2}.

3. Discharge overcurrent 1 detection voltage (Test circuit 2)

Discharge overcurrent 1 detection voltage (V_{DIOV1}) is defined as the voltage V3 whose delay time for changing V_{DO} from "H" to "L" is discharge overcurrent 1 detection delay time (t_{DIOV1}) when the voltage V3 is increased from the set conditions of V1 = V2 = 3.5 V, V3 = 0 V.

4 Discharge overcurrent 2 detection voltage (Test circuit 2)

Discharge overcurrent 2 detection voltage (V_{DIOV2}) is defined as the voltage V3 whose delay time for changing V_{DO} from "H" to "L" is discharge overcurrent 2 detection delay time (t_{DIOV2}) when the voltage V3 is increased from the set conditions of V1 = V2 = 3.5 V, V3 = 0 V.

5. Load short-circuiting detection voltage (Test circuit 2)

Load short-circuiting detection voltage (V_{SHORT}) is defined as the voltage V3 whose delay time for changing V_{DO} from "H" to "L" is load short-circuiting delay time (t_{SHORT}) when the voltage V3 is increased from the set conditions of V1 = V2 = 3.5 V, V3 = 0 V.

6. Charge overcurrent detection voltage (Test circuit 2)

Charge overcurrent detection voltage (V_{CIOV}) is defined as the voltage V3 whose delay time for changing V_{CO} from "H" to "L" is charge overcurrent delay time (t_{CIOV}) when the voltage V3 is decreased from the set conditions of V1 = V2 = 3.5 V, V3 = 0 V.

7. Current consumption during operation (Test circuit 2)

Current consumption during operation (I_{OPE}) is the current that flows through the VDD pin (I_{DD}) under the set conditions of V1 = V2 = 3.5 V, V3 = 0 V.

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8. VC pin current (Test circuit 2)

The VC pin current (I_{VC}) is the current that flows through the VC pin (I_{VC}) under the set conditions of V1 = V2 = 3.5 V, V3 = 0 V.

9. Current consumption during power-down (Test circuit 2)

Current consumption during power-down (I_{PDN}) is the current that flows through the VSS pin (I_{SS}) under the set conditions of V1 = V2 = 1.5 V, V3 = 3.0 V.

10. Resistance between VM pin and VDD pin (Test circuit 3)

R_{VMD} is the resistance between VM pin and VDD pin under the set conditions of V1 = V2 = 1.8 V, V3 = 0 V.

11. Resistance between VM pin and VSS pin (Test circuit 3)

R_{VMS} is the resistance between VM pin and VSS pin under the set conditions of V1 = V2 = 3.5 V, V3 = 1.0 V.

12. CO pin resistance "H" (Test circuit 4)

The CO pin resistance "H" (R_{COH}) is the resistance between VDD pin and CO pin under the set conditions of V1 = V2 = 3.5 V, V3 = 0 V, V5 = 6.5 V.

13. CO pin resistance "L" (Test circuit 4)

The CO pin resistance "L" (R_{COL}) is the resistance between VM pin and CO pin under the set conditions of V1 = V2 = 4.7 V, V3 = 0 V, V5 = 0.5 V.

14. DO pin resistance "H" (Test circuit 4)

The DO pin resistance "H" (R_{DOH}) is the resistance between VDD pin and DO pin under the set conditions of V1 = V2 = 3.5 V, V3 = 0 V, V6 = 6.5 V

15. DO pin resistance "L" (Test circuit 4)

The DO pin resistance "L" (R_{DOL}) is the resistance between VSS pin and DO pin under the set conditions of V1 = V2 = 1.8 V, V3 = 0 V, V6 = 0.5 V.

16. AO pin sink current (Test circuit 4)

The AO pin sink current (I_{AOL}) is the current that flows through the AO pin (I_{AO}) under the set conditions of V1 = V2 = 4.7 V, V3 = 0 V, V4 = 0.5 V.

17. AO pin leak current

The AO pin leak current (I_{AOH}) is the current that flows through the AO pin (I_{AO}) under the set conditions of V1 = V2 = 3.5 V, V3 = 0 V, V4 = 10.0 V.

NOT RECOMMENDED FOR NEW DESIGN

18. Overcharge detection delay time, overcharge release delay time (Test circuit 5)

The overcharge detection delay time (t_{CU}) is the time needed for V_{CO} to go to "L" just after the voltage V1 increases and exceeds V_{CU} from the set conditions of V1 = V2 = 3.5 V, V3 = 0 V. After that, the overcharge release delay time (t_{CL}) is the time needed for V_{CO} to go to "H" after the voltage V1 decreases and falls below V_{CL}.

19. Overcharge alarm detection delay time, overcharge alarm release delay time (Test circuit 5)

The overcharge alarm detection delay time (t_{AU}) is the time needed for V_{AO} to go to "L" just after the voltage V1 increases and exceeds V_{CU} from the set conditions of V1 = V2 = 3.5 V, V3 = 0 V, V4 = V1 + V2. After that, the overcharge alarm release delay time (t_{AL}) is the time needed for V_{AO} to go to "H" after the voltage V1 decreases and falls below V_{CL} before V_{CO} goes to "L".

20. Overdischarge detection delay time (Test circuit 5)

The overdischarge detection delay time (t_{DL}) is the time needed for V_{DO} to go to "L" after the voltage V1 decreases and falls below V_{DL} from the set conditions of V1 = V2 = 3.5 V, V3 = 0 V.

21. Discharge overcurrent 1 detection delay time (Test circuit 5)

The discharge overcurrent 1 detection delay time (t_{DIOV1}) is the time needed for V_{DO} to go to "L" after the voltage V3 increases and exceeds V_{DIOV1} from the set conditions of V1 = V2 = 3.5 V, V3 = 0 V.

22. Discharge overcurrent 2 detection delay time (Test circuit 5)

The discharge overcurrent 2 detection delay time (t_{DIOV2}) is the time needed for V_{DO} to go to "L" after the voltage V3 increases and exceeds V_{DIOV2} from the set conditions of V1 = V2 = 3.5 V, V3 = 0 V.

23. Load short-circuiting detection delay time (Test circuit 5)

The load short-circuiting detection delay time (t_{SHORT}) is the time needed for V_{DO} to go to "L" after the voltage V3 increases and exceeds V_{SHORT} from the set conditions of V1 = V2 = 3.5 V, V3 = 0 V.

24. Charge overcurrent detection delay time (Test circuit 5)

The charge overcurrent detection delay time (t_{CIOV}) is the time needed for V_{CO} to go to "L" after the voltage V3 decreases and falls below V_{CIOV} from the set conditions of V1 = V2 = 3.5 V, V3 = 0 V.

25. 0 V battery charge starting charger voltage (0 V battery charge function "available") (Test circuit 2)

The 0 V battery charge starting charger voltage (V_{0CHA}) is defined as the voltage V3 at which V_{CO} goes to "H" (V_{CO} = V_{DD}) when the voltage V3 is gradually decreased under the set conditions of V1 = V2 = V3 = 0 V.

26. 0 V battery charge inhibition battery voltage (0 V battery charge function "unavailable") (Test circuit 2)

The 0 V battery charge inhibition battery voltage (V_{0INH}) is defined as the voltage V1 at which V_{CO} goes to "L" (V_{VM} + 0.1 V or lower) when the voltage V1 is gradually decreased from the set conditions of V1 = V2 = 1.5 V, V3 = –6.0 V.

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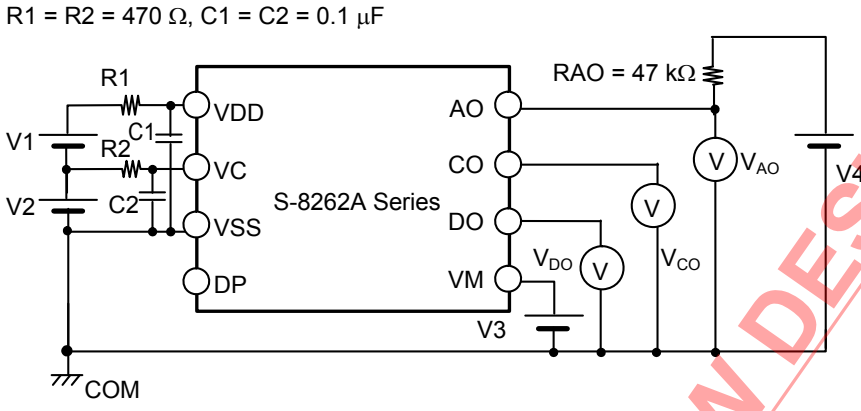


Figure 4 Test Circuit 1

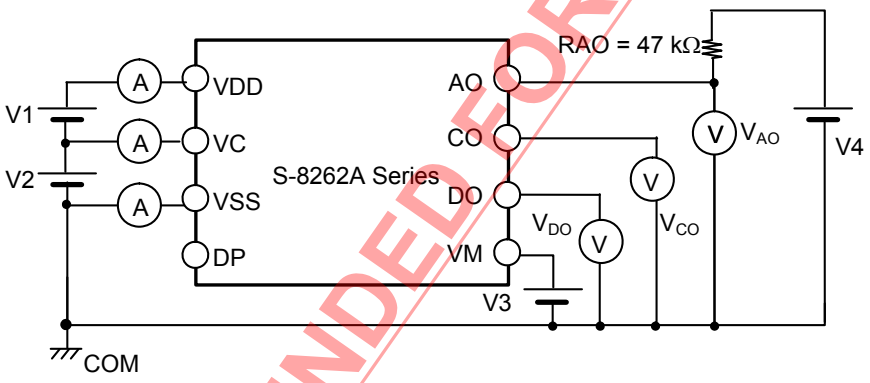


Figure 5 Test Circuit 2

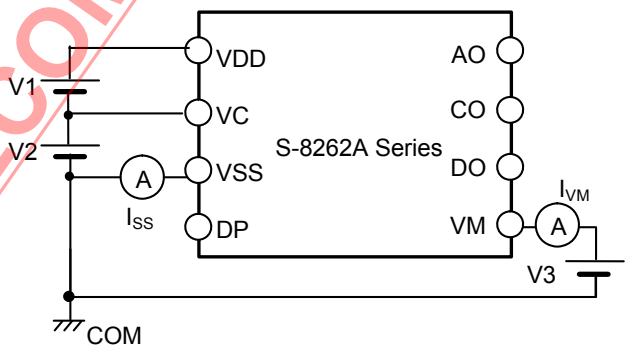


Figure 6 Test Circuit 3

NOT RECOMMENDED FOR NEW DESIGN

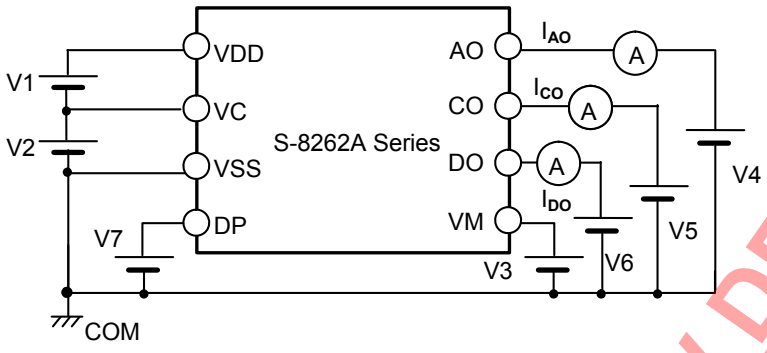


Figure 7 Test Circuit 4

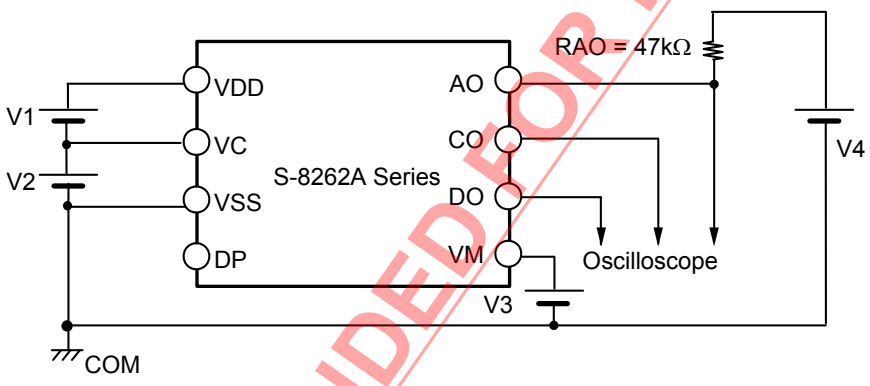


Figure 8 Test Circuit 5

NOT RECOMMENDED FOR NEW DESIGN

■ Operation

Remark Refer to "■ **Battery Protection IC Connection Example**".

1. Normal status

The S-8262A Series monitors the voltage of the battery connected between the VDD pin and VSS pin and the voltage difference between the VM pin and VSS pin to control charging and discharging. When the battery voltage is in the range from overdischarge detection voltage (V_{DL}) to overcharge detection voltage (V_{CU}), and the VM pin voltage is in the range from the charge overcurrent detection voltage (V_{CIOV}) to discharge overcurrent 1 detection voltage (V_{DIOV1}), the S-8262A Series turns both the charge and discharge control FETs on. This condition is called the normal status, and in this condition charging and discharging can be carried out freely. In the normal status the AO pin output becomes "High-Z". The resistance (R_{VMD}) between the VM pin and VDD pin, and the resistance (R_{VMS}) between the VM pin and VSS pin are not connected in the normal status.

Caution When the battery is connected for the first time, discharging may not be enabled. In this case,
Short the VM pin and VSS pin, or
Set the VM pin's voltage at the level of V_{CIOV} or more and V_{DIOV1} or less by connecting the charger
The IC returns to the normal status.

2. Overcharge status

When the battery voltage becomes higher than V_{CU} during charging in the normal status and detection continues for the overcharge alarm detection delay time (t_{AU}) or longer, the AO pin output becomes 'L". Moreover, when the detection continues for the detection delay time (t_{CU}) or longer, the S-8262A Series turns the charge control FET off to stop charging. This condition is called the overcharge status. In the overcharge status the AO pin output maintains "L", and R_{VMD} and R_{VMS} are not connected.

When the AO pin output is "L", the AO pin output becomes "High-Z" after the overcharge alarm release delay time (t_{AL}) if the battery voltage decreases and falls below V_{CU} during t_{CU}.

The overcharge status is released in the following two cases ((1) and (2)). The AO pin output becomes "High-Z" simultaneously with the release of the overcharge status.

(1) In the case that the VM pin voltage is lower than V_{DIOV2}, the S-8262A Series releases the overcharge status when the battery voltage falls below V_{CL}.
(2) In the case that the VM pin voltage is higher than or equal to V_{DIOV2}, the S-8262A Series releases the overcharge status when the battery voltage falls below V_{CU}.

When the discharge is started by connecting a load after the overcharge detection, the VM pin voltage rises more than the voltage at VSS pin due to the V_f voltage of the parasitic diode, because the discharge current flows through the parasitic diode in the charge control FET. If this VM pin voltage is higher than or equal to V_{DIOV2}, the S-8262A Series releases the overcharge status when the battery voltage is lower than or equal to V_{CU}.

Caution 1. If the battery is charged to a voltage higher than V_{CU} and the battery voltage does not fall to V_{CU} or lower even when a heavy load is connected, discharge overcurrent 1 detection, discharge overcurrent 2 detection and load short-circuiting detection do not function until the battery voltage falls below V_{CU}. However, since an actual battery has an internal impedance of tens of mΩ, the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and discharge overcurrent 1 detection, discharge overcurrent 2 detection and load short-circuiting detection function.
2. If a charger is connected after the overcharge detection, the overcharge status is not released even when the battery voltage falls below V_{CL}. The S-8262A Series releases the charge overcurrent status when the voltage at the VM pin returns to V_{CIOV} or higher by removing the charger.

NOT RECOMMENDED FOR NEW DESIGN

3. Overdischarge status

When the battery voltage falls below overdischarge detection voltage (V_{DL}) during discharging in the normal status and the detection continues for the overdischarge detection delay time (t_{DL}) or longer, the S-8262A Series turns the discharge control FET off to stop discharging. This condition is called the overdischarge status. In the overdischarge status the AO pin output becomes "High-Z".

Under the overdischarge status, the VM pin and VDD pin are shorted by R_{VMD} in the IC. The VM pin voltage is pulled up by R_{VMD}.

When a battery in the overdischarge status is connected to a charger and provided that the VM pin voltage is lower than −0.7 V typ., the S-8262A Series releases the overdischarge status when the battery voltage reaches V_{DL} or higher.

When VM pin voltage is not lower than −0.7 V typ., the S-8262A Series releases the overdischarge status when the battery voltage reaches V_{DU} or higher.

R_{VMS} is not connected in the overdischarge status.

3. 1 With power-down function

Under the overdischarge status, when voltage difference between the VM pin and VDD pin is 0.8 V typ. or lower, the current consumption is reduced to the power-down current consumption (I_{PDN}).

4. Discharge overcurrent status

(Discharge overcurrent 1, discharge overcurrent 2, load short-circuiting)

When a battery in the normal status is in the status where the voltage of the VM pin is equal to or higher than V_{DIOV1} because the discharge current is equal to or higher than the specified value and the status lasts for the discharge overcurrent 1 detection delay time (t_{DIOV1}) or longer, the discharge control FET is turned off and discharging is stopped. This status is called the discharge overcurrent status. In the discharge overcurrent status the AO pin output becomes "High-Z".

In the discharge overcurrent status, the VM pin and VSS pin are shorted by the R_{VMS} in the IC. However, the voltage of the VM pin is at the V_{DD} potential due to the load as long as the load is connected. When the load is disconnected, the VM pin returns to the V_{SS} potential.

If the voltage at the VM pin returns to V_{DIOV1} or lower, the S-8262A Series releases the discharge overcurrent status.

R_{VMD} is not connected in the discharge overcurrent detection status.

5. Charge overcurrent status

When a battery in the normal status is in the status where the voltage of the VM pin is equal to or lower than V_{CIOV} because the charge current is equal to or higher than the specified value and the status lasts for the charge overcurrent detection delay time (t_{CIOV}) or longer, the charge control FET is turned off and charging is stopped. This status is called the charge overcurrent status. In the charge overcurrent status the AO pin output becomes "High-Z".

The S-8262A Series releases the charge overcurrent status when the voltage at the VM pin returns to V_{CIOV} or higher by removing the charger.

The charge overcurrent detection function does not work in the overdischarge status.

R_{VMD} and R_{VMS} are not connected in the charge overcurrent status.

6. 0 V battery charge function "available"

This function is used to recharge a connected battery whose voltage is 0 V due to self-discharge. When the 0 V battery charge starting charger voltage (V_{0CHA}) or a higher voltage is applied between the EB+ and EB− pins by connecting a charger, the charge control FET gate is fixed to the V_{DD} potential.

When the voltage between the gate and source of the charge control FET becomes equal to or higher than the threshold voltage due to the charger voltage, the charge control FET is turned on to start charging. At this time, the discharge control FET is off and the charging current flows through the internal parasitic diode in the discharge control FET. When the battery voltage becomes equal to or higher than V_{DU}, the S-8262A Series enters the normal status.

Caution 1. Some battery providers do not recommend recharging for a completely self-discharged battery. Please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge function.

2. The 0 V battery charge function has higher priority than the charge overcurrent detection function. Consequently, a product in which use of the 0 V battery charge function is enabled charges a battery forcibly and the charge overcurrent cannot be detected when the battery voltage is lower than V_{DL}.

NOT RECOMMENDED FOR NEW DESIGN

7. 0 V battery charge function "unavailable"

This function inhibits charging when a battery that is internally short-circuited (0 V battery) is connected. When the battery voltage is the 0 V battery charge inhibition battery voltage (V_{0INH}) or lower, the charge control FET gate is fixed to the EB− pin voltage to inhibit charging. When the battery voltage is V_{0INH} or higher, charging can be performed.

Caution **Some battery providers do not recommend recharging for a completely self-discharged battery. Please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge function.**

8. Delay circuit

The detection delay times are determined by dividing a clock of approximately 4 kHz by the counter.

Remark t_{DIOV1} and t_{DIOV2} start when V_{DIOV1} is detected. Therefore, when V_{DIOV2} is detected over t_{DIOV2} after V_{DIOV1}, the S-8262A Series turns the discharge control FET off during $0 \leq t_D \leq t_{DIOV2}$ from the time of detecting V_{DIOV2}.

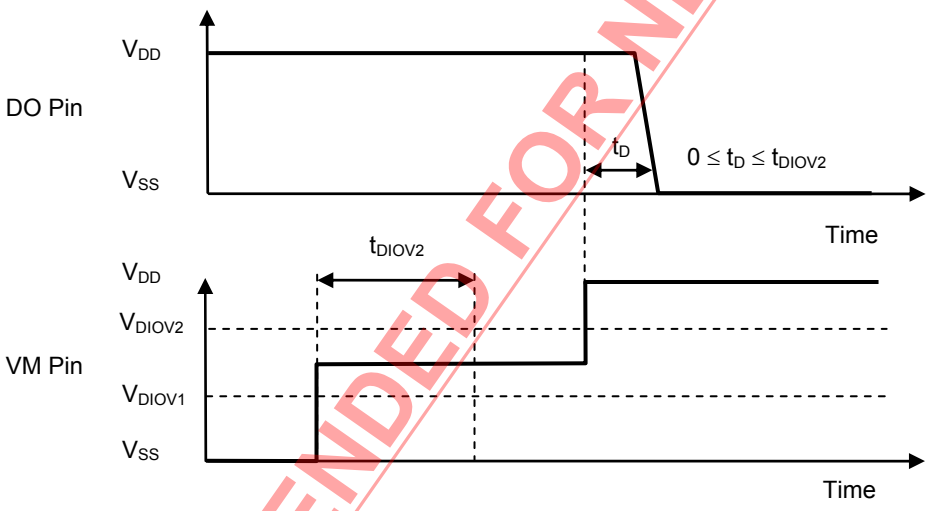


Figure 9

9. DP pin

The S-8262A Series has a DP pin (Test mode switching pin). The S-8262A Series becomes test mode by raising the voltage which is input to the DP pin to V_{DPH} or higher.

Table 9

DP Pin	Status
Open ($V_{DP} = V_{SS}$)	Normal operation mode
"H" ($V_{DP} \geq V_{DPH}$)	Test mode
"L" ($V_{DP} \leq V_{DPL}$)	Normal operation mode

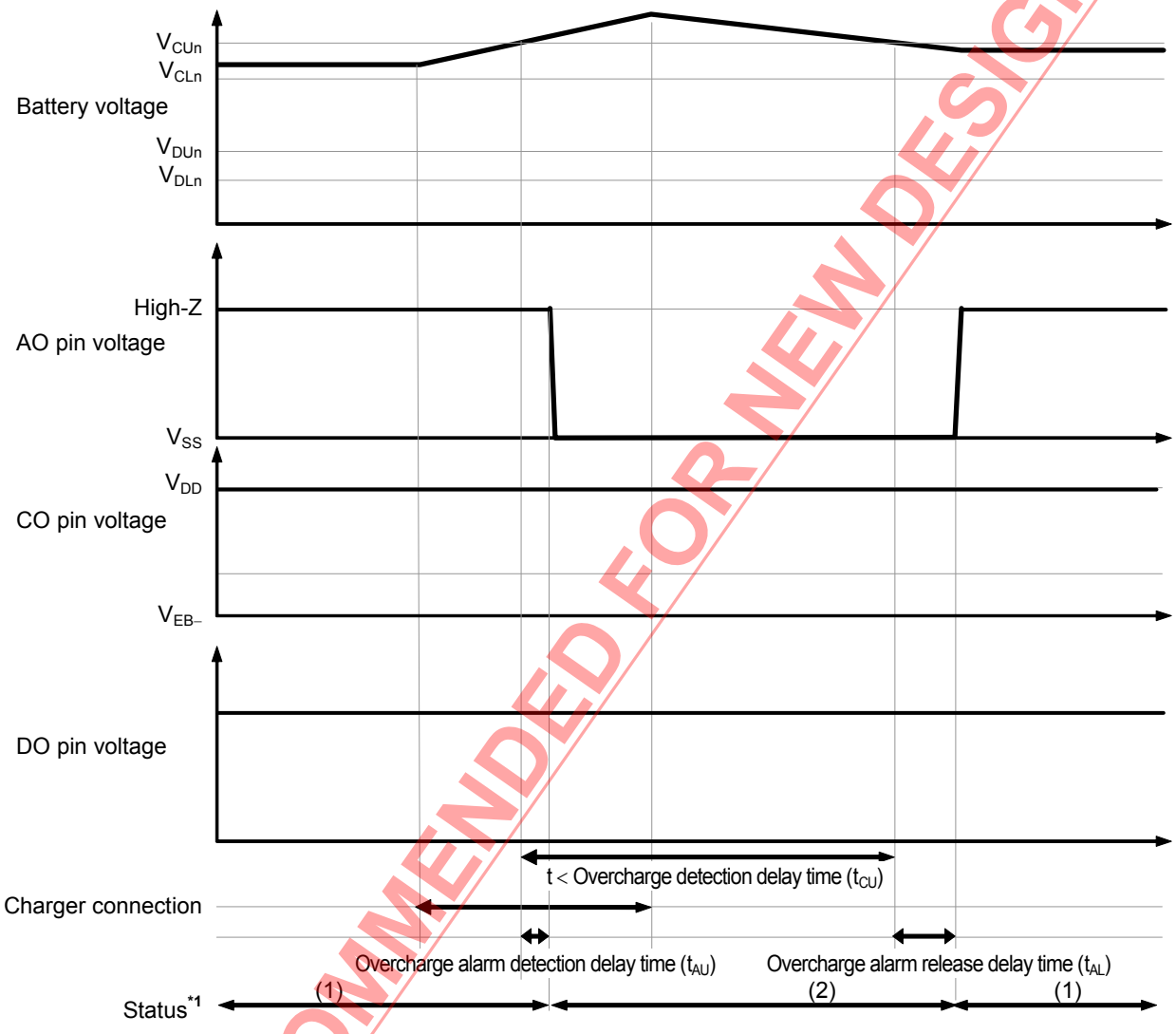
Under test mode, the overcharge detection delay time (t_{CU}) and the overcharge alarm release delay time (t_{AL}) are shortened to 1/128 of normal delay time.

Except during the above test of shortening delay time, set the DP pin OPEN or short-circuit it to V_{SS}. When the DP pin is OPEN, it is pulled down to V_{SS} by the internal resistance.

NOT RECOMMENDED FOR NEW DESIGN

■ Timing Charts

1. Overcharge alarm detection, overcharge alarm release



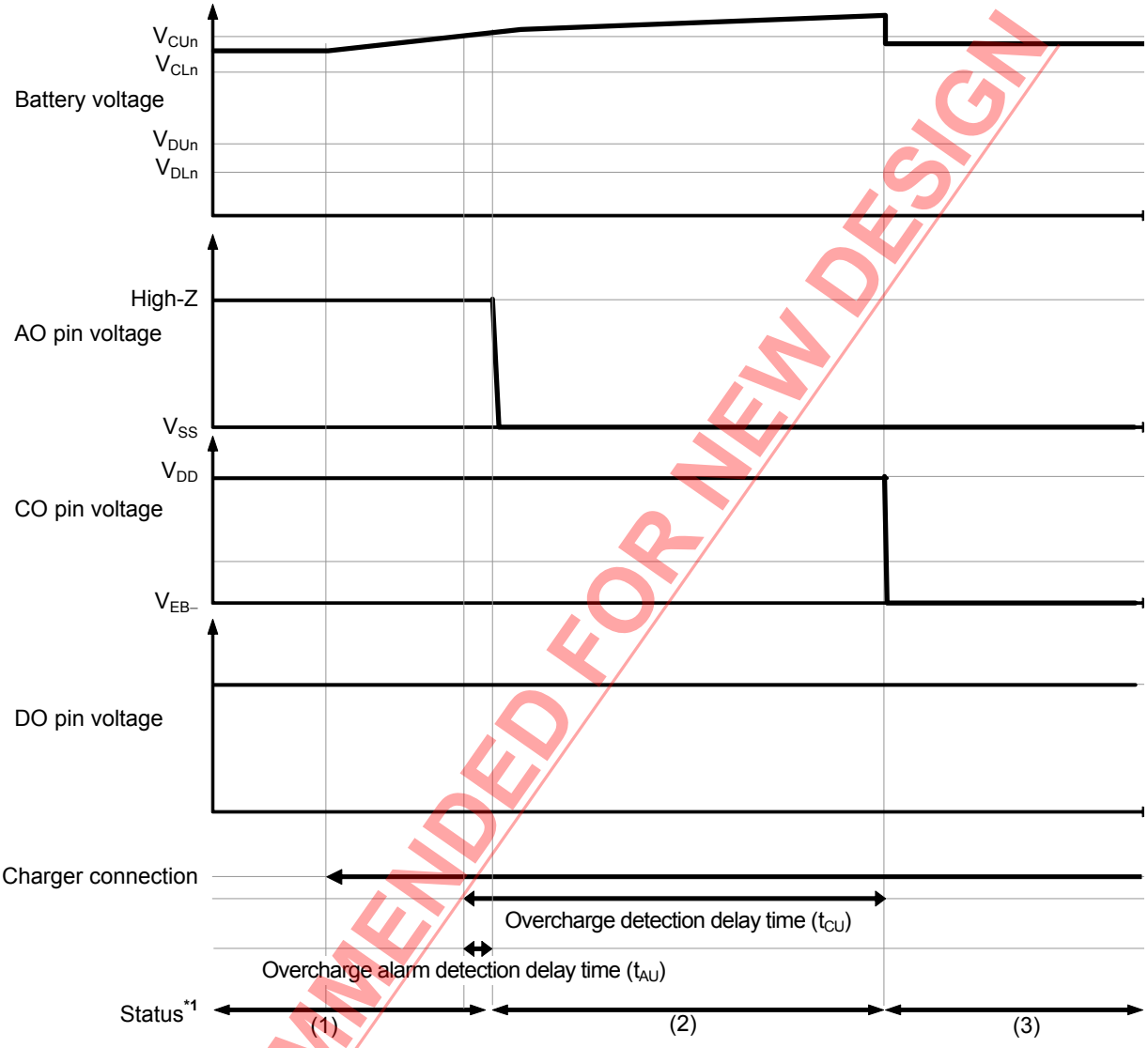
***1.** (1): Normal status
(2): Overcharge alarm status

Remark The charger is assumed to charge with a constant current.

Figure 10

NOT RECOMMENDED FOR NEW DESIGN

2. Overcharge detection, overcharge alarm detection



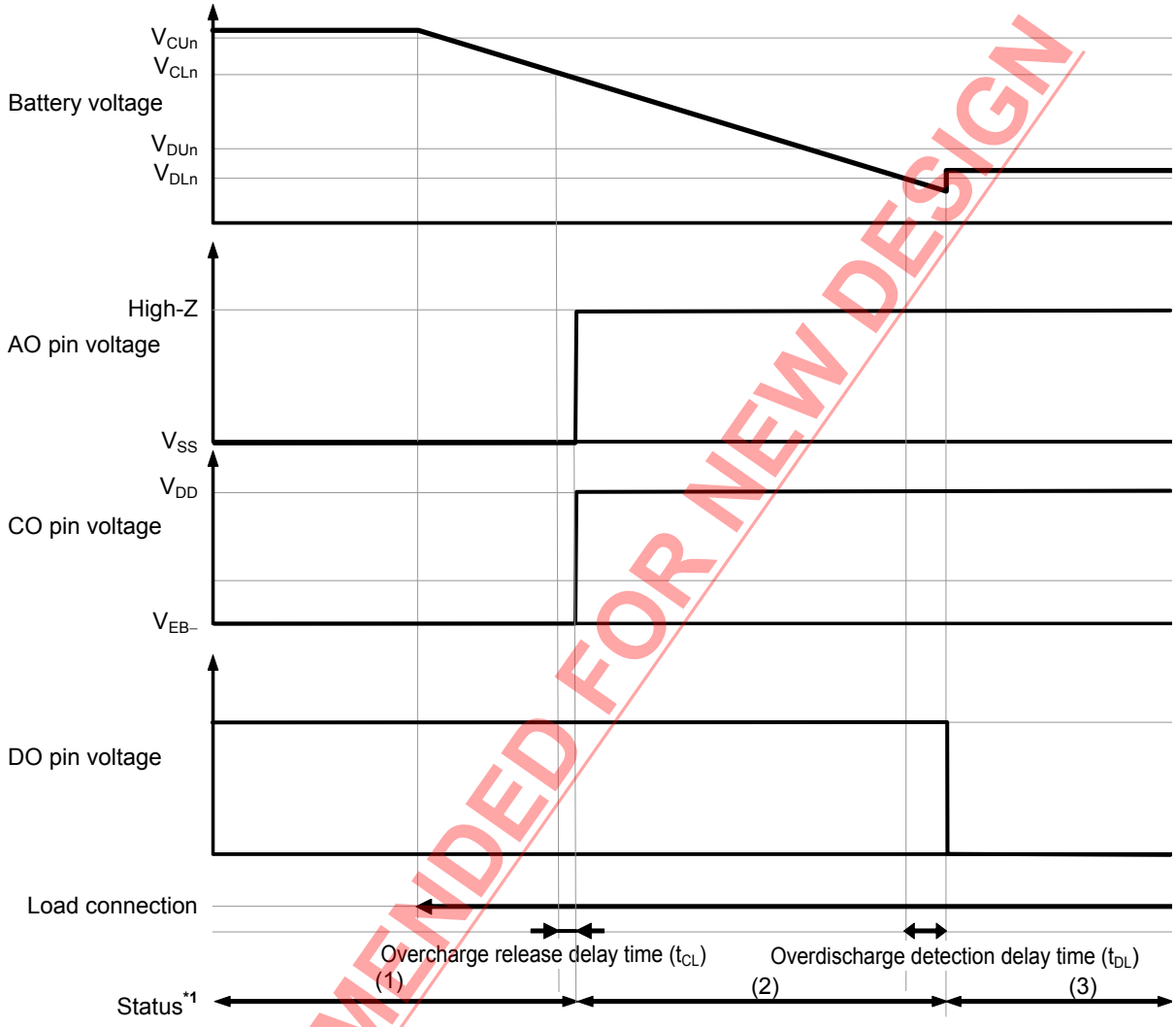
NOT RECOMMENDED FOR NEW DESIGN

***1.** (1): Normal status
(2): Overcharge alarm status
(3): Overcharge status

Remark The charger is assumed to charge with a constant current.

Figure 11

3. Overcharge release, overdischarge detection



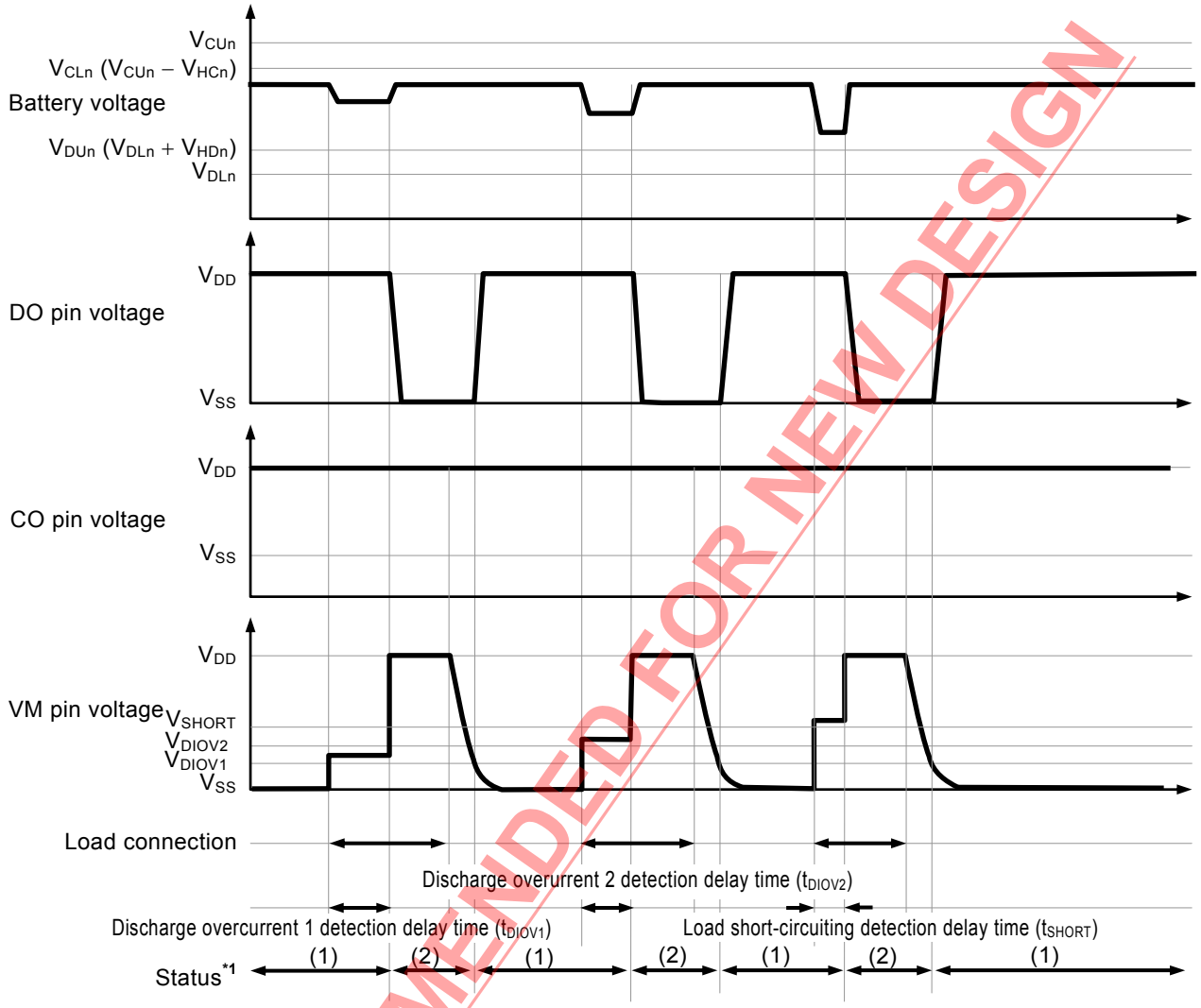
*1. (1): Overcharge status
(2): Normal status
(3): Overdischarge status

Remark The charger is assumed to charge with a constant current.

Figure 12

NOT RECOMMENDED FOR NEW DESIGN

4. Discharge overcurrent detection



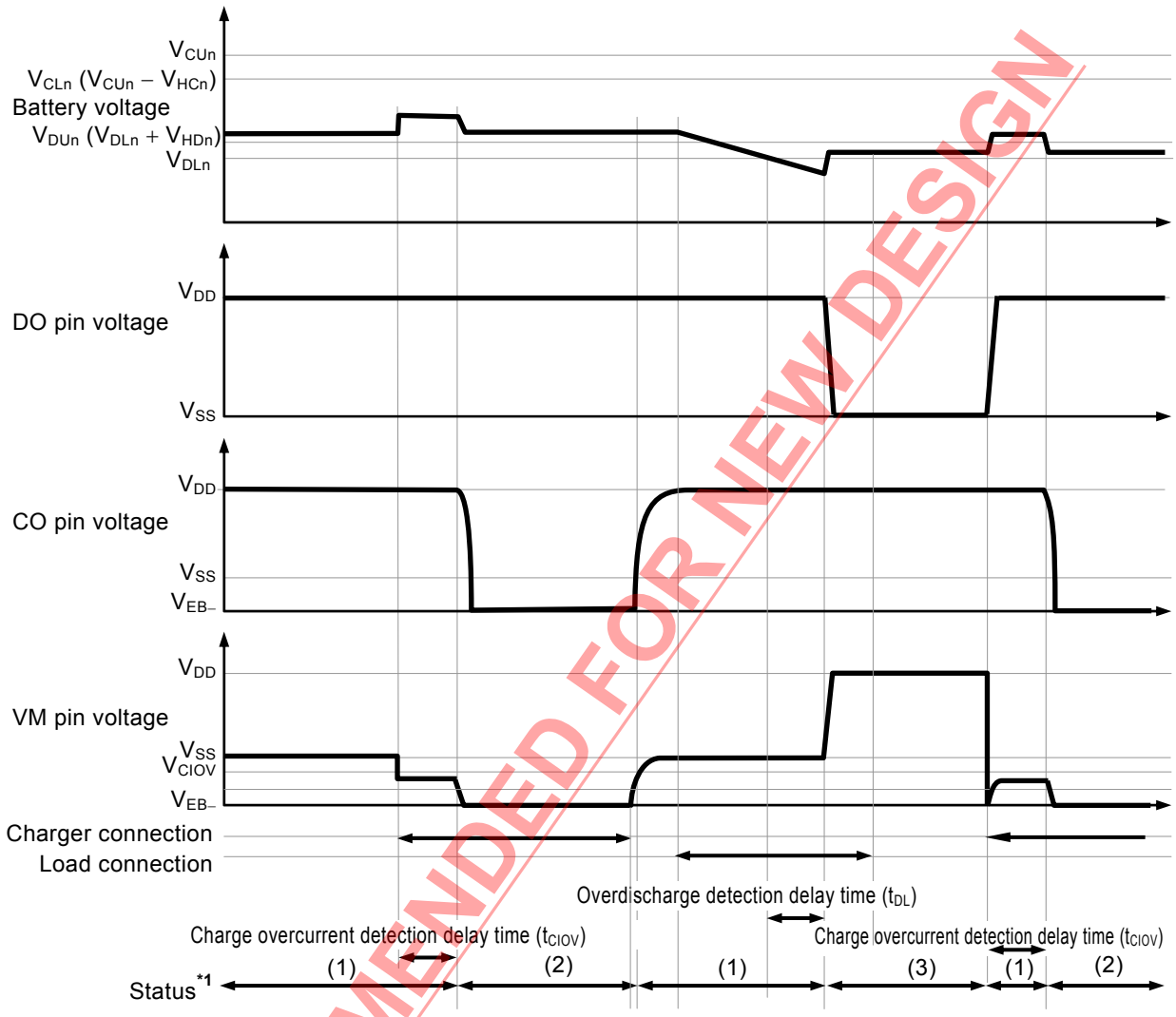
*1. (1): Normal status
(2): Discharge overcurrent status

Remark The charger is assumed to charge with a constant current.

Figure 13

NOT RECOMMENDED FOR NEW DESIGN

5. Charge overcurrent detection



***1.** (1): Normal status
(2): Charge overcurrent status
(3): Overdischarge status

Remark The charger is assumed to charge with a constant current.

Figure 14

NOT RECOMMENDED FOR NEW DESIGN

■ Battery Protection IC Connection Example

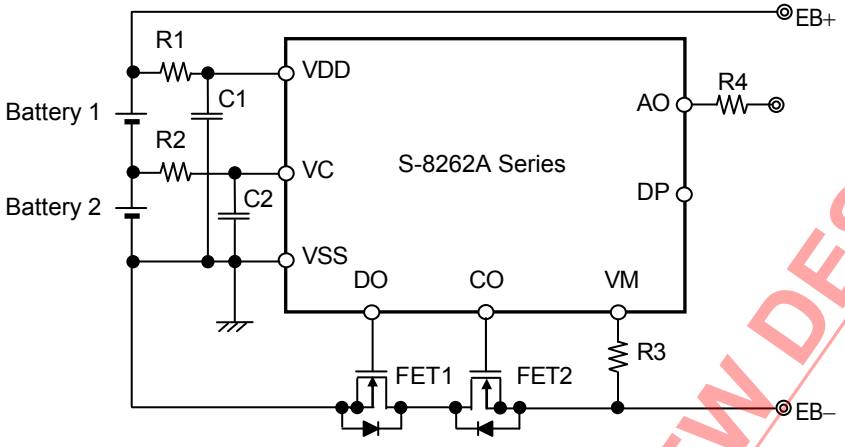


Figure 15

Table 10 Constants for External Components

Symbol	Part	Purpose	Typ.	Min.	Max.	Remark
FET1	Nch MOS FET	Discharge control	–	–	–	Threshold voltage ≤ Overdischarge detection voltage*2 Gate to source withstanding voltage ≥ Charger voltage*3
FET2	Nch MOS FET	Charge control	–	–	–	Threshold voltage ≤ Overdischarge detection voltage*2 Gate to source withstanding voltage ≥ Charger voltage*3
R1, R2	Resistor	ESD protection, For power fluctuation	470 Ω	150 Ω*1	1 kΩ*1	Resistance should be as small as possible to avoid lowering the overcharge detection accuracy due to current consumption.*4
C1, C2	Capacitor	For power fluctuation	0.1 μF	0.068 μF*1	1.0 μF*1	Connect a capacitor of 0.068 μF or higher between VDD pin and VSS pin.*5
R3	Resistor	Protection for reverse connection of a charger	2 kΩ	300 Ω*1	4 kΩ*1	Select as large a resistance as possible to prevent current when a charger is connected in reverse.*6
R4	Resistor	Pull up resistor	47 kΩ	–	–	–

*1. Please set up a filter constant to be R1 × C1 = R2 × C2.

*2. If the threshold voltage of a FET is low, the FET may not cut the charging current. If a FET with a threshold voltage equal to or higher than the overdischarge detection voltage is used, discharging may be stopped before overdischarge is detected.

*3. If the withstanding voltage between the gate and source is equal to or lower than the charger voltage, the FET may be destroyed.

*4. An accuracy of overcharge detection voltage is guaranteed by R1 = 470 Ω. Connecting resistors with other values worsen the accuracy. In case of connecting larger resistor to R1, the voltage between the VDD pin and VSS pin may exceed the absolute maximum rating because the current flows to the IC from the charger due to reverse connection of charger. Connect a resistor of 150 Ω or more to R1 for ESD protection.

*5. When connecting a resistor of 150 Ω or less to R1 or R2 or a capacitor of 0.068 μF or less to C1 or C2, the IC may malfunction when power dissipation is largely fluctuated.

*6. When a resistor of 4 kΩ or more is connected to R3, the charge current may not be cut.

Caution 1. The above constants may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.

3. Do not connect a resistor to the DP pin during normal use.

NOT RECOMMENDED FOR NEW DESIGN

■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

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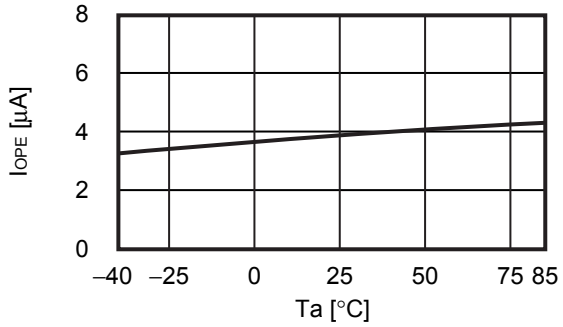
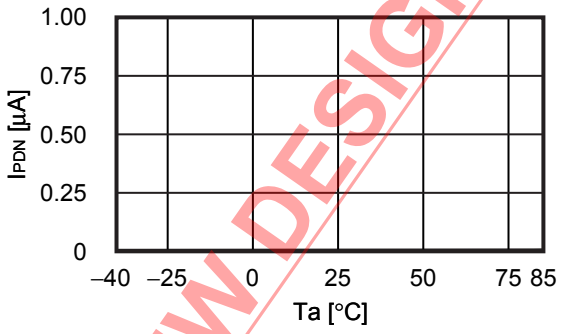
■ Characteristics (Typical Data)

1. Current consumption

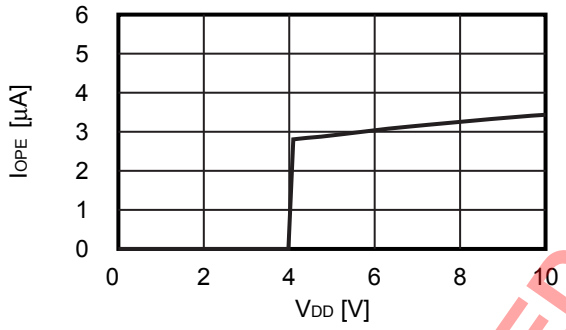
1. 1 I_{OPE} vs. Ta



1. 2 I_{PDN} vs. Ta



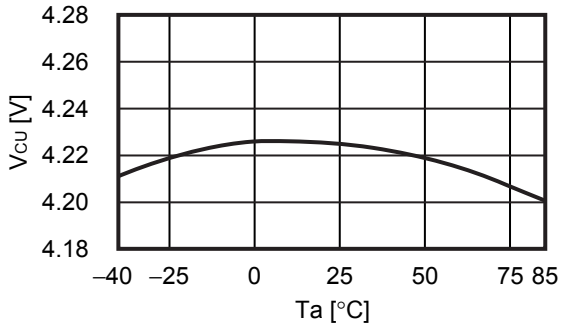
1. 3 I_{OPE} vs. V_{DD}



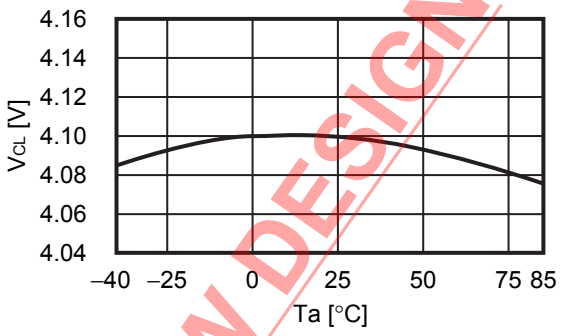
NOT RECOMMENDED FOR NEW DESIGN

2. Overcharge detection / release voltage, overdischarge detection / release voltage, overcurrent detection voltage, charge overcurrent detection voltage, and delay time

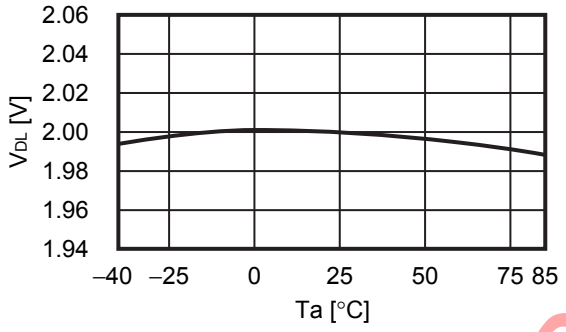
2. 1 V_{CU} vs. Ta



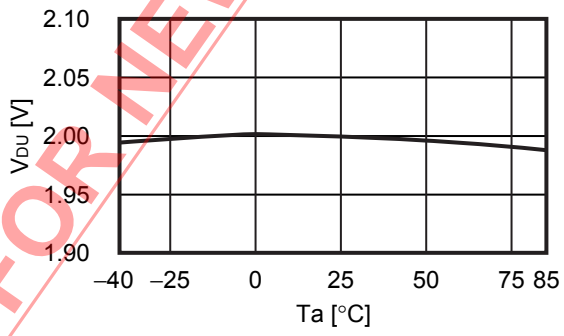
2. 2 V_{CL} vs. Ta



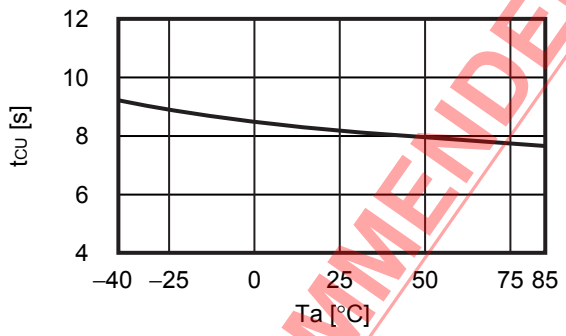
2. 3 V_{DL} vs. Ta



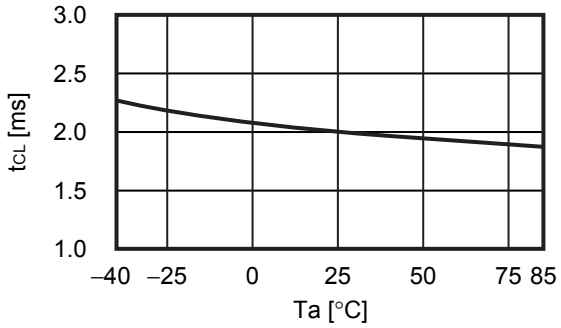
2. 4 V_{DU} vs. Ta



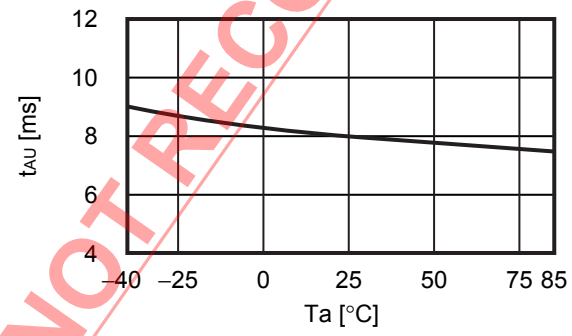
2. 5 t_{CU} vs. Ta



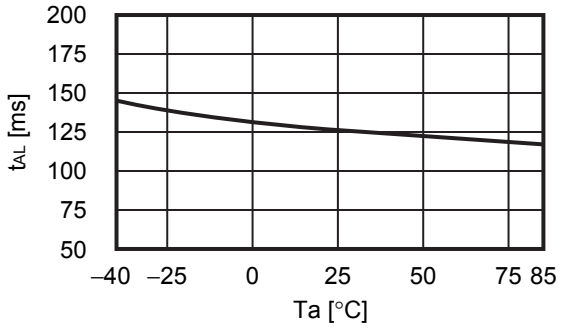
2. 6 t_{CL} vs. Ta



2. 7 t_{AU} vs. Ta

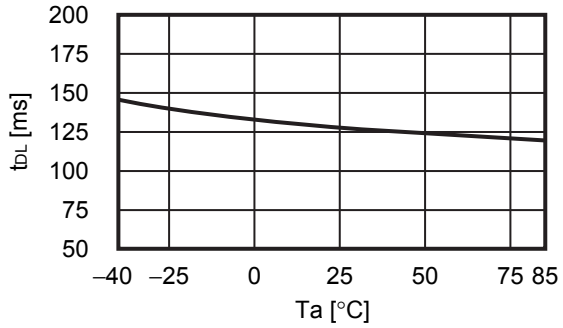


2. 8 t_{AL} vs. Ta

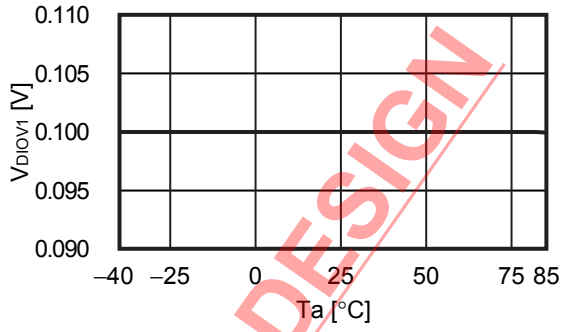


NOT RECOMMENDED FOR NEW DESIGN

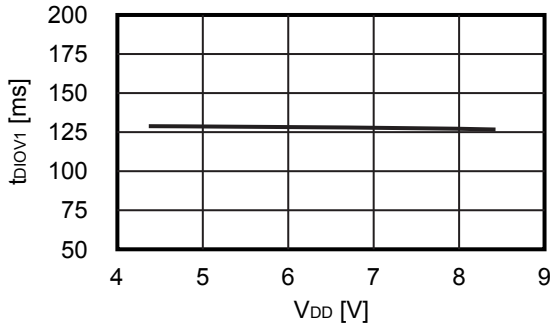
2. 9 t_{DL} vs. Ta



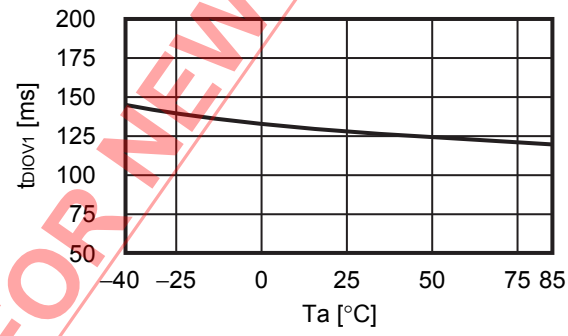
2. 10 V_{DIOV1} vs. Ta



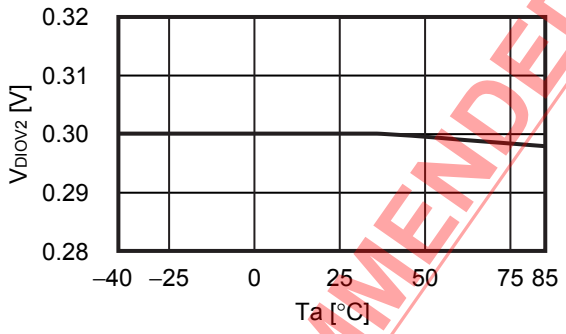
2. 11 t_{DIOV1} vs. V_{DD}



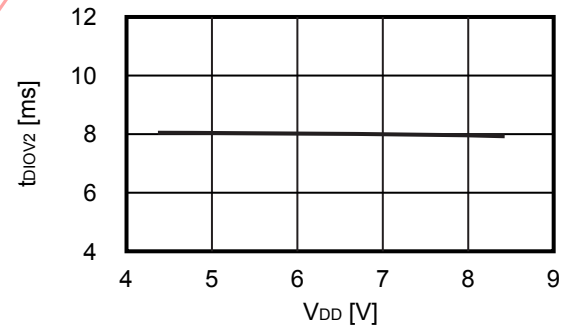
2. 12 t_{DIOV1} vs. Ta



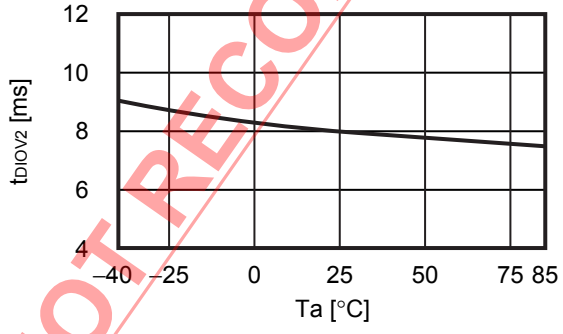
2. 13 V_{DIOV2} vs. Ta



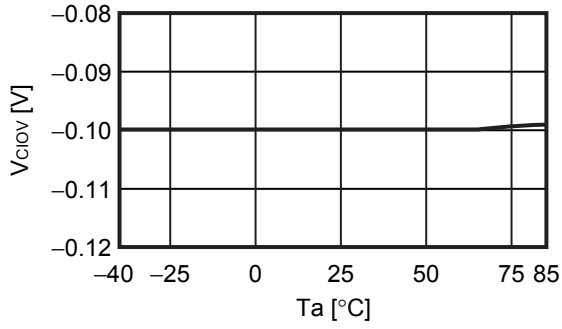
2. 14 t_{DIOV2} vs. V_{DD}



2. 15 t_{DIOV2} vs. Ta



2. 16 V_{CIOV} vs. Ta



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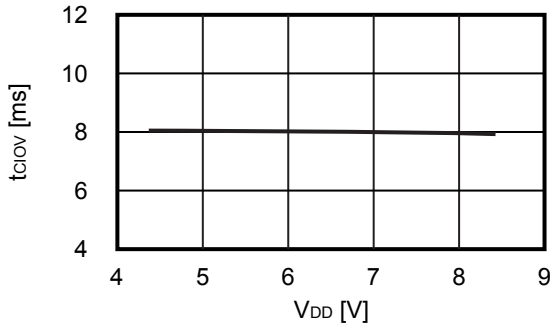
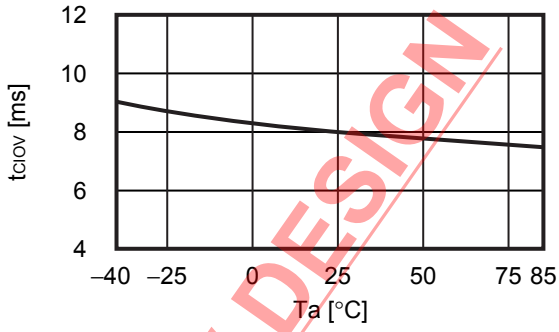
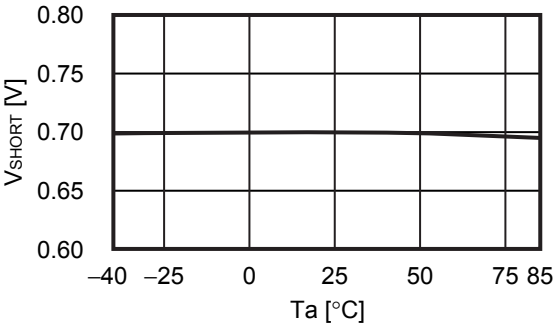
2. 17 t_{CIOV} vs. V_{DD}



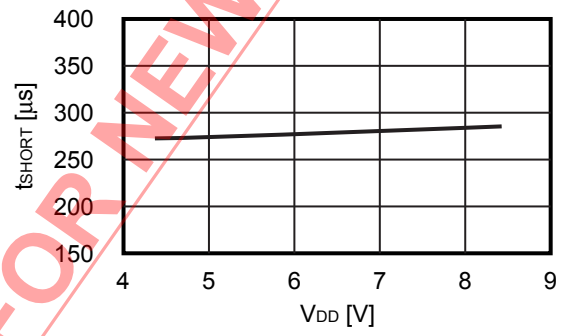
2. 18 t_{CIOV} vs. Ta



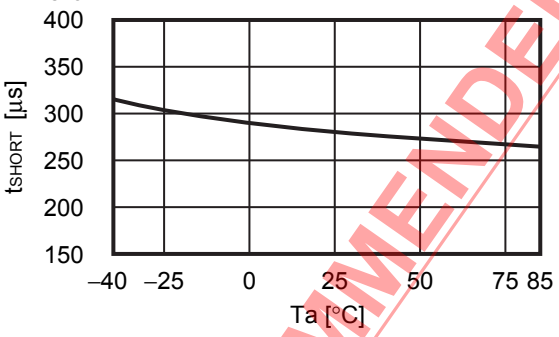
2. 19 V_{SHORT} vs. Ta



2. 20 t_{SHORT} vs. V_{DD}



2. 21 t_{SHORT} vs. Ta



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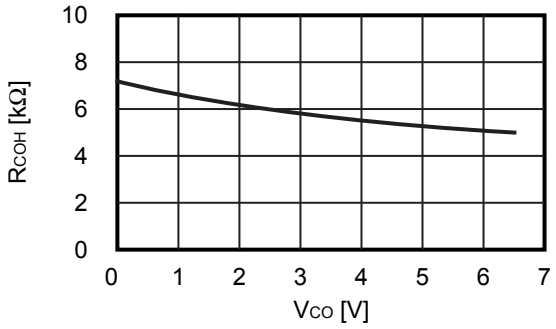
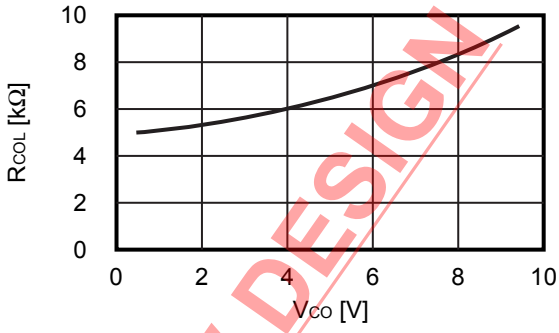
3. CO pin / DO pin

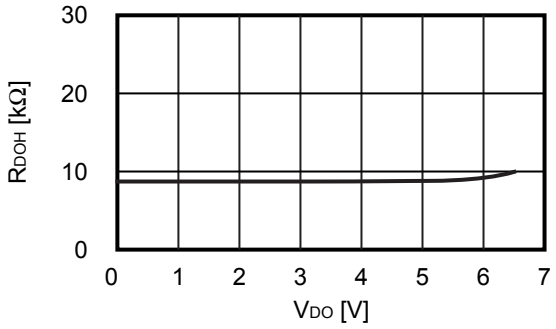
3. 1 R_{COH} vs. V_{CO}



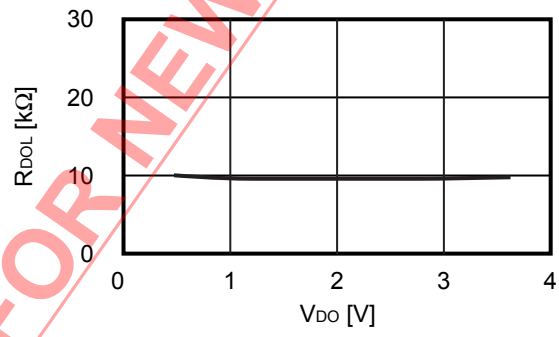
3. 2 R_{COL} vs. V_{CO}



3. 3 R_{DOH} vs. V_{DO}

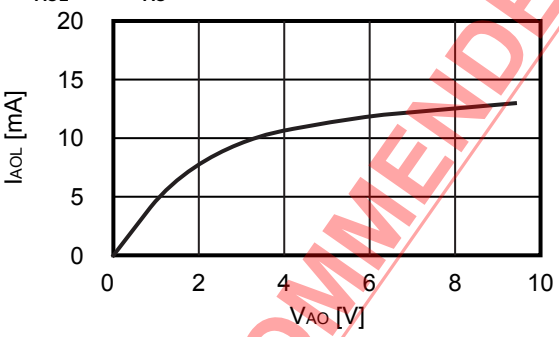


3. 4 R_{DOL} vs. V_{DO}

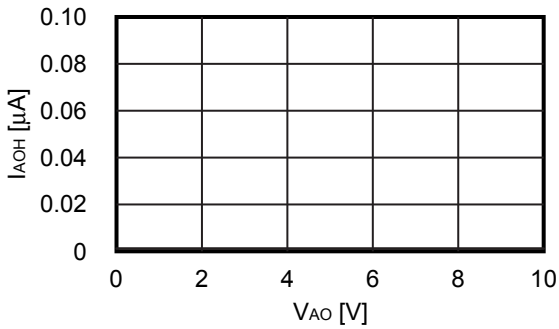


4. AO pin

4. 1 I_{AOL} vs. V_{AO}



4. 2 I_{AOH} vs. V_{AO}



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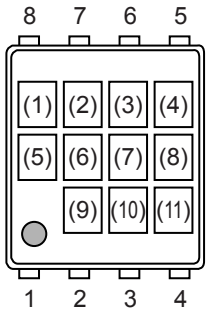
■ Marking Specification

1. SNT-8A

Top view



(1): Blank
(2) to (4): Product code (Refer to **Product name vs. Product code**)
(5), (6): Blank
(7) to (11): Lot number

Product name vs. Product code

Product Name	Product Code		
	(2)	(3)	(4)
S-8262AAA-I8T1U	W	9	A
S-8262AAB-I8T1U	W	9	B

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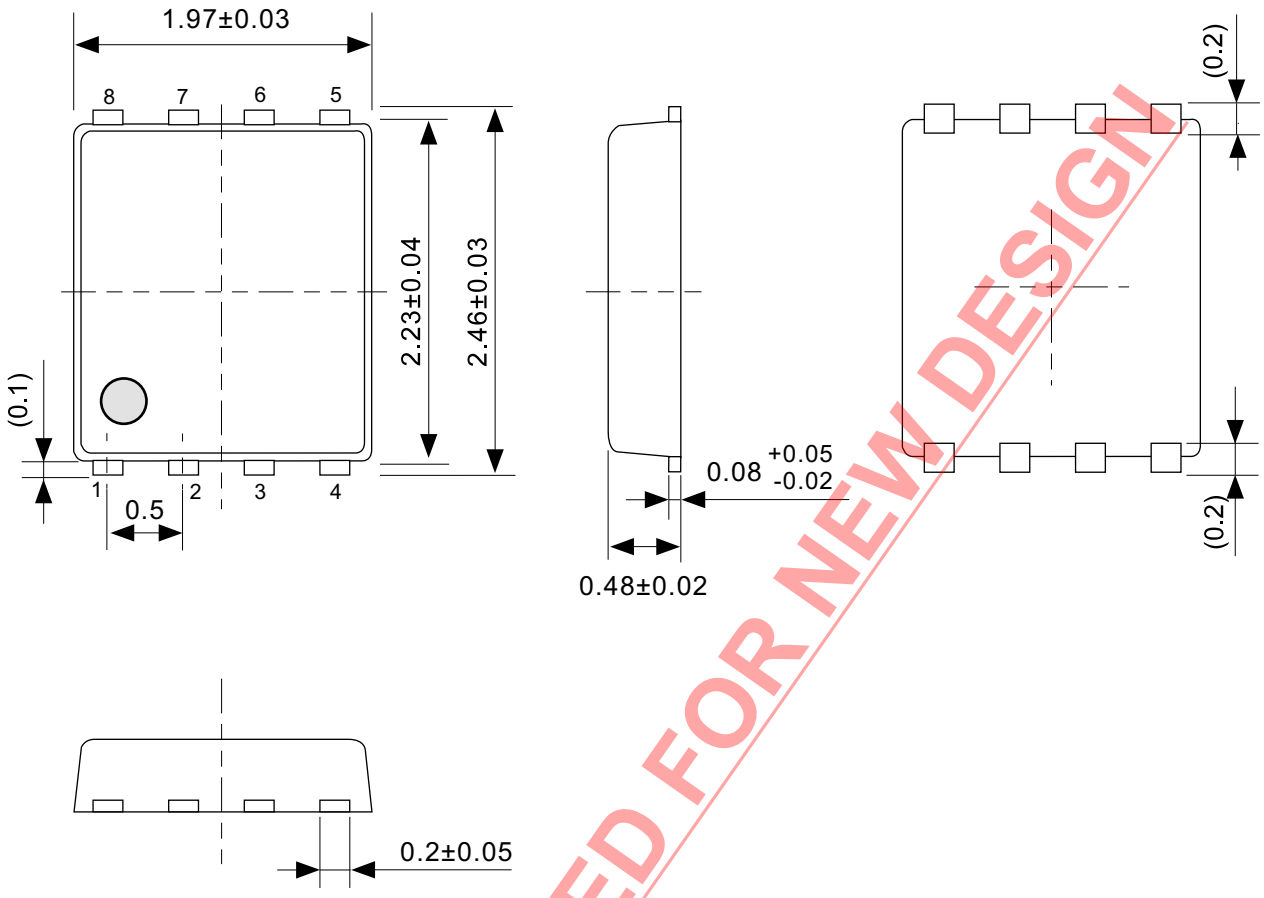
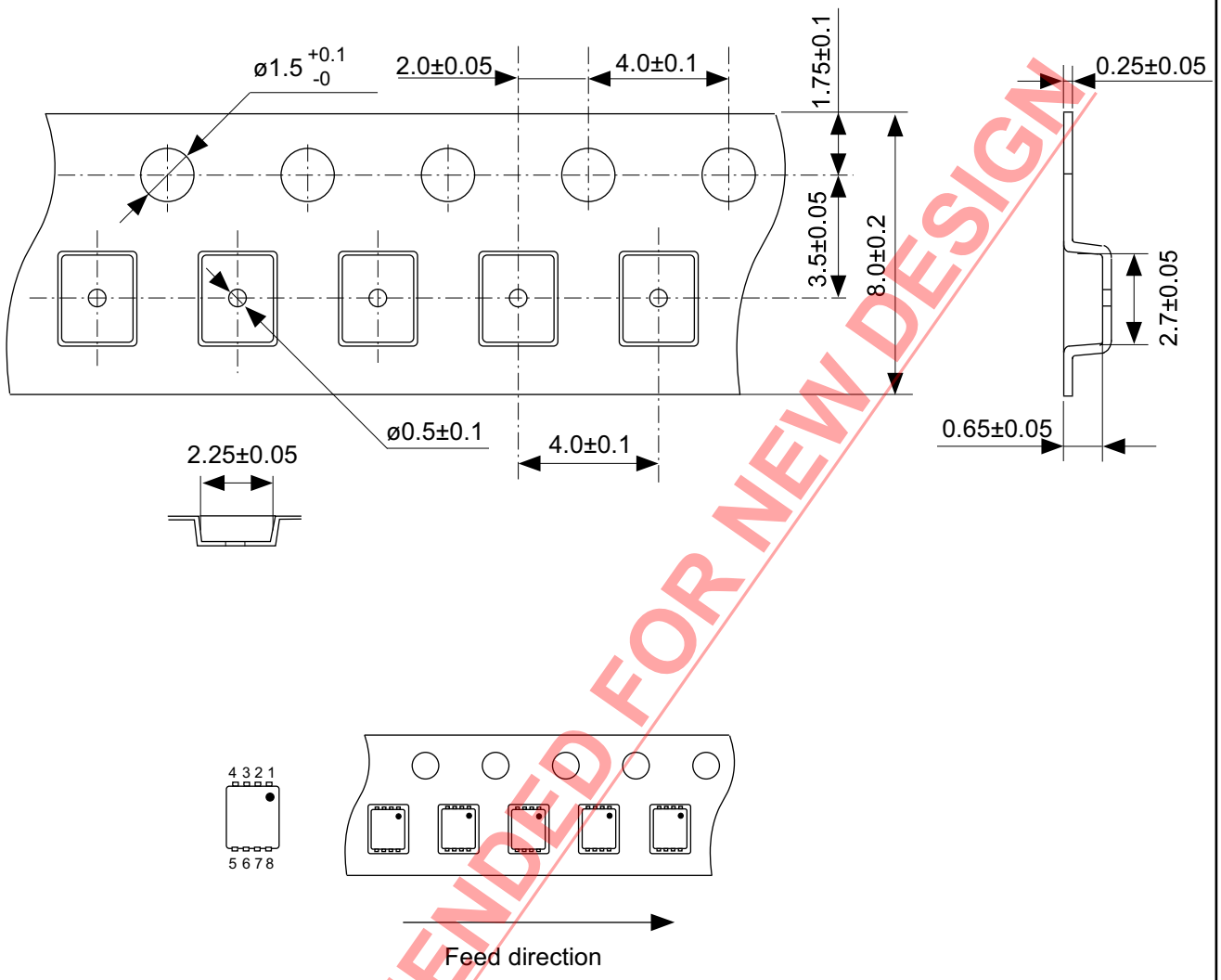


NOT RECOMMENDED FOR NEW DESIGN

No. PH008-A-P-SD-2.1

TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.1
ANGLE	
UNIT	mm

ABLIC Inc.

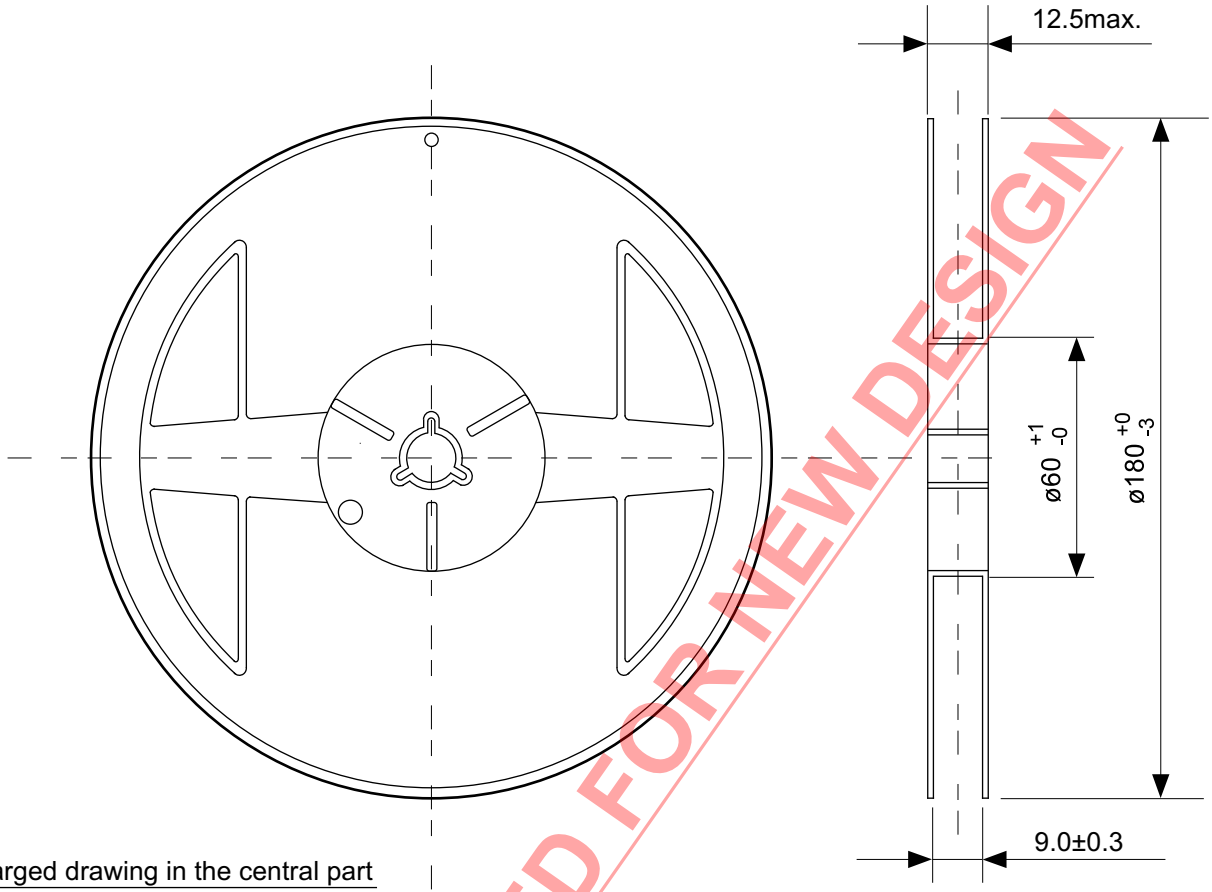


NOT RECOMMENDED FOR NEW DESIGN

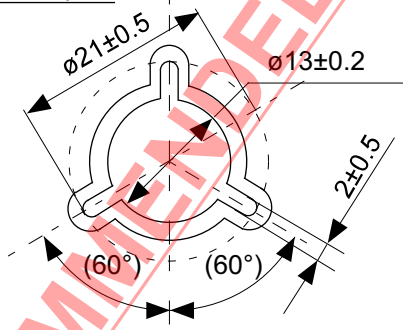
No. PH008-A-C-SD-2.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-2.0
ANGLE	
UNIT	mm

ABLIC Inc.



Enlarged drawing in the central part



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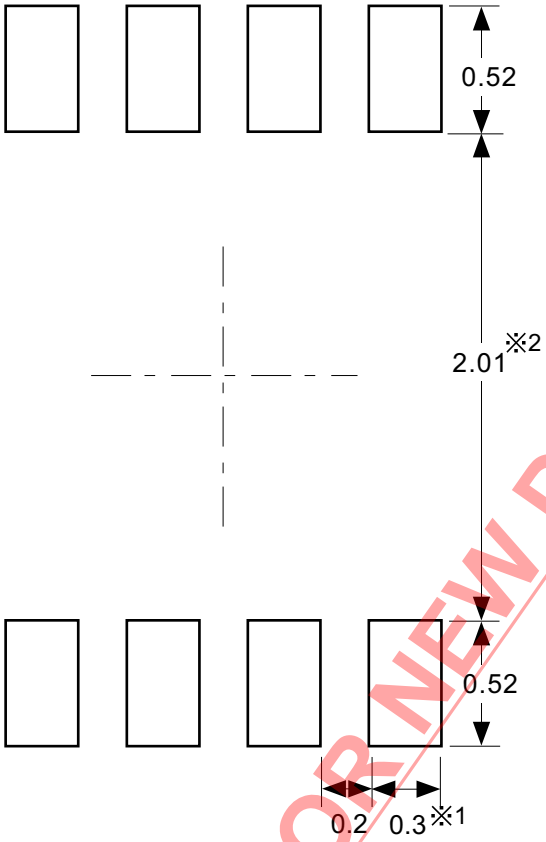
No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



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※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.96 mm ~ 2.06 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝SNTパッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.96 mm ~ 2.06 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PH008-A-L-SD-4.1

TITLE	SNT-8A-A -Land Recommendation
No.	PH008-A-L-SD-4.1
ANGLE	
UNIT	mm

ABLIC Inc.

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