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BATTERY PROTECTION IC FOR 3-SERIAL- OR 4-SERIAL-CELL PACK

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Rev.5.4_00

The S-8254A Series is a protection IC for 3-serial- or 4-serial-cell lithium-ion / lithium polymer rechargeable batteries and includes a high-accuracy voltage detector and delay circuit.
The S-8254A Series protects both 3-serial or 4-serial cells using the SEL pin for switching.

■ Features

(1) High-accuracy voltage detection function for each cell

• Overcharge detection voltage n (n = 1 to 4)	3.90 V to 4.45 V (50 mV step)	Accuracy ±25 mV
• Overcharge release voltage n (n = 1 to 4)	3.80 V to 4.45 V*1	Accuracy ±50 mV
• Overdischarge detection voltage n (n = 1 to 4)	2.0 V to 3.0 V (100 mV step)	Accuracy ±80 mV
• Overdischarge release voltage n (n = 1 to 4)	2.0 V to 3.4 V*2	Accuracy ±100 mV

(2) Three-level overcurrent protection

• Overcurrent detection voltage 1	0.05 V to 0.30 V (50 mV step)	Accuracy ±25 mV
• Overcurrent detection voltage 2	0.5 V	Accuracy ±100 mV
• Overcurrent detection voltage 3	V_{VC1} – 1.2 V	Accuracy ±300 mV

(3) Delay times for overcharge detection, overdischarge detection and overcurrent detection 1 can be set by external capacitors (delay times for overcurrent detection 2 and 3 are fixed internally).
(4) Switchable between a 3-serial cell and 4-serial cell using the SEL pin
(5) Charge/discharge operation can be controlled via the control pins.
(6) 0 V battery charge Enabled, inhibited
(7) Power-down function Available
(8) High-withstand voltage Absolute maximum rating : 26 V
(9) Wide operating voltage range 2 V to 24 V
(10) Wide operating temperature range –40°C to + 85°C
(11) Low current consumption
- During operation 30 µA max. (+25°C)
- During power-down 0.1 µA max. (+25°C)

(12) Lead-free, Sn100%, halogen-free*3

***1.** Overcharge hysteresis voltage n (n = 1 to 4) can be selected as 0 V or from a range of 0.1 V to 0.4 V in 50 mV steps.
(Overcharge hysteresis voltage = Overcharge detection voltage – Overcharge release voltage)
***2.** Overdischarge hysteresis voltage n (n = 1 to 4) can be selected as 0 V or from a range of 0.2 V to 0.7 V in 100 mV steps.
(Overdischarge hysteresis voltage = Overdischarge release voltage – Overdischarge detection voltage)
***3.** Refer to "■ **Product Name Structure**" for details.

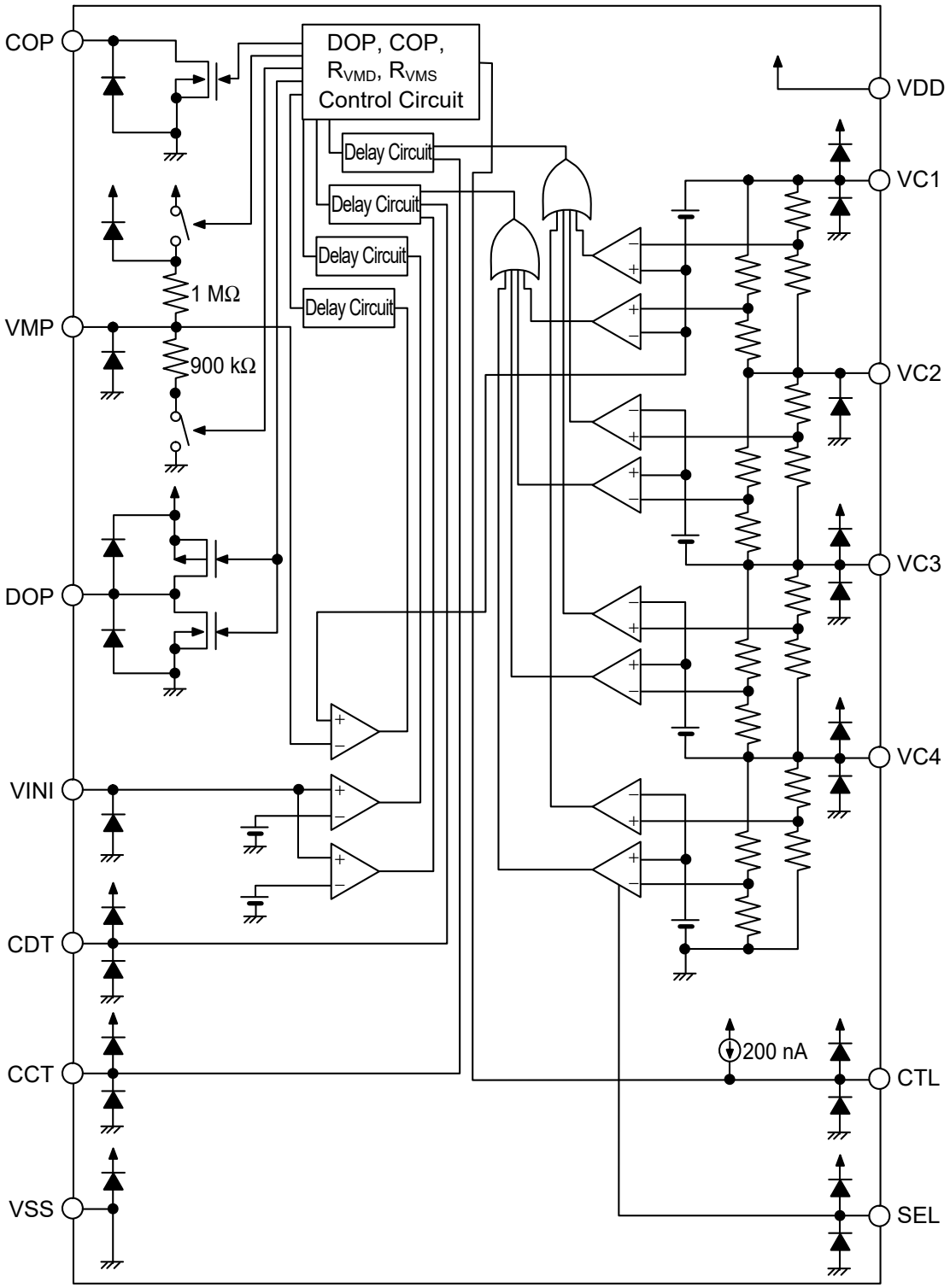
■ Applications

- Lithium-ion rechargeable battery packs
- Lithium polymer rechargeable battery packs

■ Package

- 16-Pin TSSOP

■ Block Diagram



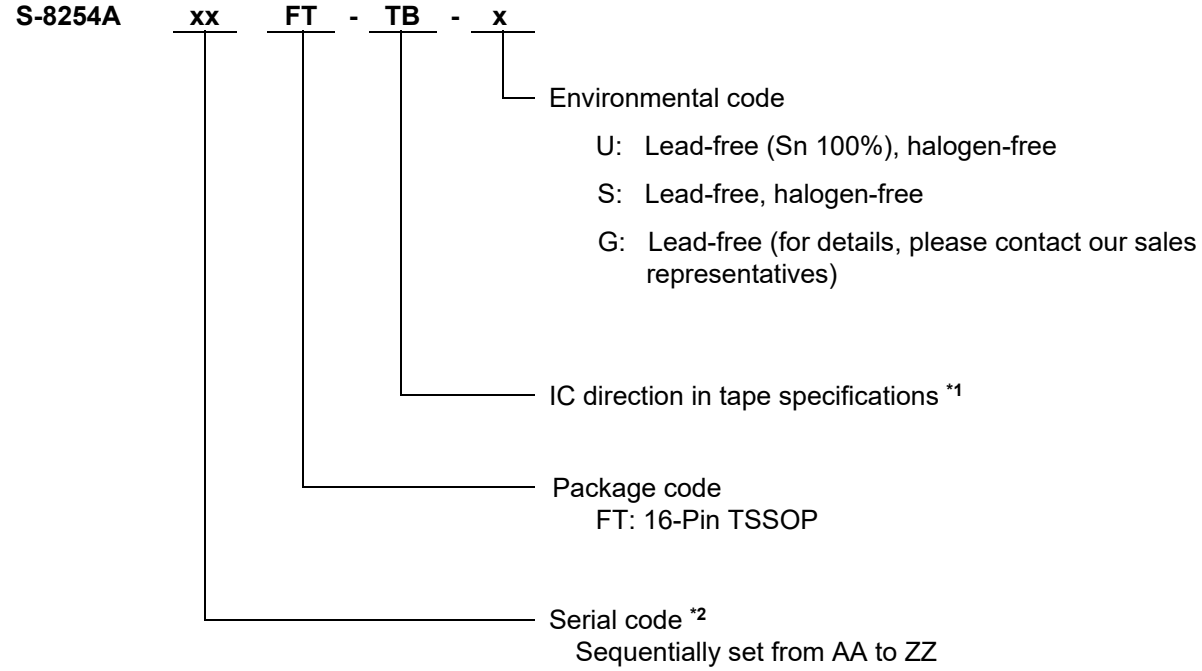
Remark **1.** Diodes in the figure are parasitic diodes.

2. Numerical values are typical values.

Figure 1

■ Product Name Structure

1. Product Name



***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product Name List**".

2. Package

Package name		Package	Tape	Reel
16-Pin TSSOP	Environmental code = G, S	FT016-A-P-SD	FT016-A-C-SD	FT016-A-R-SD
	Environmental code = U	FT016-A-P-SD	FT016-A-C-SD	FT016-A-R-S1

3. Product Name List

Table 1

Product name / Item	Overcharge detection voltage [V_{CU}]	Overcharge release voltage [V_{CL}]	Overdischarge detection voltage [V_{DL}]	Overdischarge release voltage [V_{DU}]	Overcurrent detection voltage 1 [V_{IOV1}]	0 V battery charge
S-8254AAAFT-TB-x	4.350 ± 0.025 V	4.150 ± 0.050 V	2.00 ± 0.080 V	2.70 ± 0.100 V	0.30 ± 0.025 V	Enabled
S-8254AABFT-TB-x	4.250 ± 0.025 V	4.250 ± 0.025 V	2.00 ± 0.080 V	2.70 ± 0.100 V	0.30 ± 0.025 V	Enabled
S-8254AAEFT-TB-x	4.350 ± 0.025 V	4.150 ± 0.050 V	2.00 ± 0.080 V	2.70 ± 0.100 V	0.20 ± 0.025 V	Enabled
S-8254AAFFT-TB-x	4.350 ± 0.025 V	4.150 ± 0.050 V	2.40 ± 0.080 V	3.00 ± 0.100 V	0.20 ± 0.025 V	Enabled
S-8254AAGFT-TB-x	4.275 ± 0.025 V	4.075 ± 0.050 V	2.30 ± 0.080 V	2.70 ± 0.100 V	0.13 ± 0.025 V	Enabled
S-8254AAHFT-TB-x	4.350 ± 0.025 V	4.150 ± 0.050 V	2.40 ± 0.080 V	2.70 ± 0.100 V	0.10 ± 0.025 V	Enabled
S-8254AAJFT-TB-x	4.350 ± 0.025 V	4.150 ± 0.050 V	2.40 ± 0.080 V	3.00 ± 0.100 V	0.15 ± 0.025 V	Enabled
S-8254AAKFT-TB-x	4.350 ± 0.025 V	4.150 ± 0.050 V	2.70 ± 0.080 V	3.00 ± 0.100 V	0.20 ± 0.025 V	Enabled
S-8254AALFT-TB-x	4.300 ± 0.025 V	4.150 ± 0.050 V	2.40 ± 0.080 V	3.00 ± 0.100 V	0.20 ± 0.025 V	Enabled
S-8254AAMFT-TB-x	4.200 ± 0.025 V	4.100 ± 0.050 V	2.50 ± 0.080 V	2.70 ± 0.100 V	0.30 ± 0.025 V	Enabled
S-8254AANFT-TB-x	4.250 ± 0.025 V	4.150 ± 0.050 V	2.50 ± 0.080 V	3.00 ± 0.100 V	0.10 ± 0.025 V	Enabled
S-8254AAOFT-TB-x	4.300 ± 0.025 V	4.080 ± 0.050 V	2.50 ± 0.080 V	3.00 ± 0.100 V	0.10 ± 0.025 V	Enabled
S-8254AAPFT-TB-x	4.280 ± 0.025 V	4.130 ± 0.050 V	3.00 ± 0.080 V	3.00 ± 0.080 V	0.15 ± 0.025 V	Enabled
S-8254AAQFT-TB-x	3.900 ± 0.025 V	3.800 ± 0.050 V	2.30 ± 0.080 V	2.70 ± 0.100 V	0.30 ± 0.025 V	Enabled
S-8254AARFT-TB-x	4.350 ± 0.025 V	4.150 ± 0.050 V	2.80 ± 0.080 V	3.00 ± 0.100 V	0.20 ± 0.025 V	Enabled
S-8254AASFT-TB-x	4.290 ± 0.025 V	4.090 ± 0.050 V	2.30 ± 0.080 V	3.00 ± 0.100 V	0.075 ± 0.025 V	Enabled
S-8254AATFT-TB-x	4.200 ± 0.025 V	4.200 ± 0.025 V	2.00 ± 0.080 V	2.70 ± 0.100 V	0.30 ± 0.025 V	Enabled
S-8254AAUFT-TB-x	4.350 ± 0.025 V	4.150 ± 0.050 V	2.40 ± 0.080 V	3.00 ± 0.100 V	0.20 ± 0.025 V	Inhibited
S-8254AAVFT-TB-x	4.250 ± 0.025 V	4.150 ± 0.050 V	2.70 ± 0.080 V	3.00 ± 0.100 V	0.20 ± 0.025 V	Enabled
S-8254AAWFT-TB-x	4.250 ± 0.025 V	4.100 ± 0.050 V	3.00 ± 0.080 V	3.20 ± 0.100 V	0.10 ± 0.025 V	Inhibited
S-8254AAYFT-TB-x	4.275 ± 0.025 V	4.125 ± 0.050 V	2.40 ± 0.080 V	2.70 ± 0.100 V	0.10 ± 0.025 V	Enabled
S-8254AAZFT-TB-x	4.250 ± 0.025 V	4.150 ± 0.050 V	2.00 ± 0.080 V	2.70 ± 0.100 V	0.13 ± 0.025 V	Enabled
S-8254ABAFT-TB-x	3.900 ± 0.025 V	3.800 ± 0.050 V	2.00 ± 0.080 V	2.50 ± 0.100 V	0.15 ± 0.025 V	Enabled
S-8254ABCFT-TB-x	4.175 ± 0.025 V	3.975 ± 0.050 V	2.75 ± 0.080 V	3.05 ± 0.100 V	0.10 ± 0.025 V	Enabled
S-8254ABDFT-TB-y	4.300 ± 0.025 V	4.100 ± 0.050 V	2.00 ± 0.080 V	2.00 ± 0.080 V	0.13 ± 0.025 V	Enabled
S-8254ABEFT-TB-y	4.200 ± 0.025 V	4.150 ± 0.050 V	2.50 ± 0.080 V	3.00 ± 0.100 V	0.15 ± 0.025 V	Enabled
S-8254ABFFT-TB-x	4.150 ± 0.025 V	4.050 ± 0.050 V	2.00 ± 0.080 V	2.70 ± 0.100 V	0.13 ± 0.025 V	Enabled
S-8254ABGFT-TB-x	4.180 ± 0.025 V	4.080 ± 0.050 V	2.00 ± 0.080 V	2.70 ± 0.100 V	0.13 ± 0.025 V	Enabled
S-8254ABHFT-TB-y	4.150 ± 0.025 V	4.050 ± 0.050 V	2.50 ± 0.080 V	2.80 ± 0.100 V	0.10 ± 0.025 V	Enabled
S-8254ABIFT-TB-x	4.215 ± 0.025 V	4.115 ± 0.050 V	2.40 ± 0.080 V	3.00 ± 0.100 V	0.20 ± 0.025 V	Inhibited
S-8254ABJFT-TB-U	4.225 ± 0.025 V	4.125 ± 0.050 V	2.50 ± 0.080 V	2.70 ± 0.100 V	0.10 ± 0.025 V	Enabled
S-8254ABKFT-TB-U	4.150 ± 0.025 V	4.150 ± 0.025 V	2.00 ± 0.080 V	2.70 ± 0.100 V	0.30 ± 0.025 V	Enabled
S-8254ABLFT-TB-U	4.250 ± 0.025 V	4.100 ± 0.050 V	2.40 ± 0.080 V	3.00 ± 0.100 V	0.20 ± 0.025 V	Inhibited
S-8254ABMFT-TB-U	4.425 ± 0.025 V	4.225 ± 0.050 V	2.50 ± 0.080 V	2.90 ± 0.100 V	0.15 ± 0.025 V	Enabled
S-8254ABNFT-TB-U	4.215 ± 0.025 V	4.115 ± 0.050 V	2.80 ± 0.080 V	3.00 ± 0.100 V	0.20 ± 0.025 V	Inhibited

Remark 1. Please contact our sales representatives for products other than the above.
2. x: G or U
y: S or U
3. Please select products of environmental code = U for Sn 100%, halogen-free products.

■ Pin Configuration

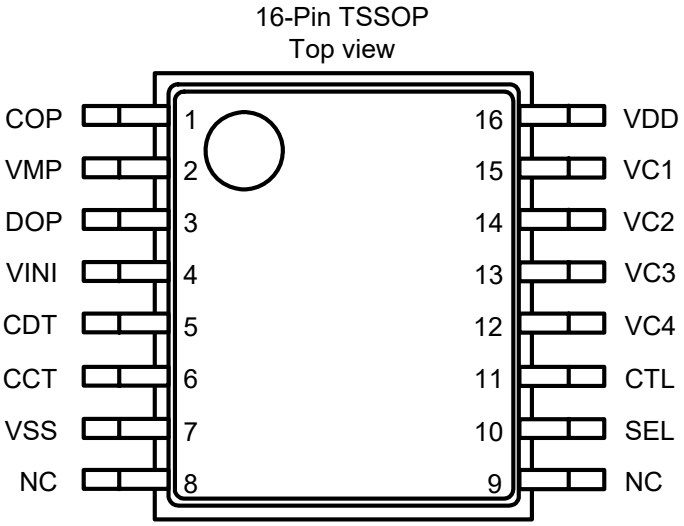


Figure 2

Table 2

Pin No.	Symbol	Description
1	COP	FET gate connection pin for charge control (Nch open drain output)
2	VMP	Pin for voltage detection between VC1 and VMP (Pin for overcurrent 3 detection)
3	DOP	FET gate connection pin for discharge control FET (CMOS output)
4	VINI	Pin for voltage detection between VSS and VINI (Pin for overcurrent detection 1,2)
5	CDT	Capacitor connection pin for delay for overdischarge detection, delay for overcurrent detection 1
6	CCT	Capacitor connection pin for delay for overcharge current
7	VSS	Input pin for negative power supply, Connection pin for battery 4's negative voltage
8	NC *1	No connection
9	NC *1	No connection
10	SEL	Pin for switching 3-series or 4-series cell V_{SS} level: 3-series cell, V_{DD} level : 4-series cell
11	CTL	Control of charge FET and discharge FET
12	VC4	Connection pin for battery 3's negative voltage, Connection pin for battery 4's positive voltage
13	VC3	Connection pin for battery 2's negative voltage, Connection pin for battery 3's positive voltage
14	VC2	Connection pin for battery 1's negative voltage, Connection pin for battery 2's positive voltage
15	VC1	Connection pin for battery 1's positive voltage
16	VDD	Input pin for positive power supply, Connection pin for battery 1's positive voltage

***1.** The NC pin is electrically open. The NC pin can be connected to VDD or VSS.

■ Absolute Maximum Ratings

Table 3

(Ta = 25°C unless otherwise specified)

Item	Symbol	Applied pin	Absolute Maximum Ratings	Unit
Input voltage between VDD and VSS	V_{DS}	—	V_{SS} − 0.3 to V_{SS} + 26	V
Input pin voltage	V_{IN}	VC1, VC2, VC3, VC4, CTL, SEL, CCT, CDT, VINI	V_{SS} − 0.3 to V_{DD} + 0.3	V
VMP pin input voltage	V_{VMP}	VMP	V_{SS} − 0.3 to V_{SS} + 26	V
DOP pin output voltage	V_{DOP}	DOP	V_{SS} − 0.3 to V_{DD} + 0.3	V
COP pin output voltage	V_{COP}	COP	V_{SS} − 0.3 to V_{SS} + 26	V
Power dissipation	P_D	—	400 (When not mounted on board)	mW
		—	1100*1	mW
Operating ambient temperature	T_{opr}	—	− 40 to + 85	°C
Storage temperature	T_{stg}	—	− 40 to + 125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size : 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name : JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

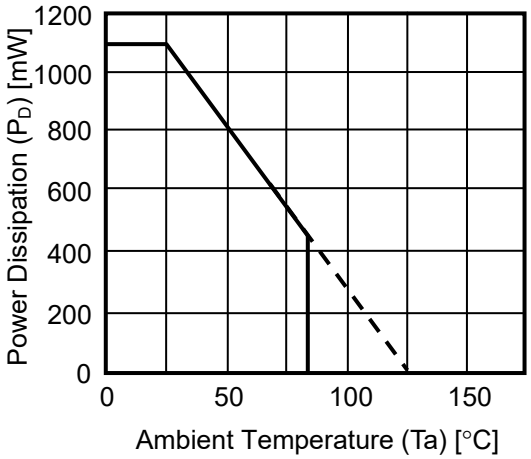


Figure 3 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

Table 4 (1 / 2)

(Ta = 25°C unless otherwise specified)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test circuit
[DETECTION VOLTAGE]								
Overcharge detection voltage n (n = 1, 2, 3, 4)	V_{CUn}	3.90 V to 4.45 V, Adjustable		V_{CUn} − 0.025	V_{CUn}	V_{CUn} + 0.025	V	2
Overcharge release voltage n (n = 1, 2, 3, 4)	V_{CLn}	3.80 V to 4.45 V, Adjustable	$V_{CL} \neq V_{CU}$	V_{CLn} − 0.05	V_{CLn}	V_{CLn} + 0.05	V	2
			$V_{CL} = V_{CU}$	V_{CLn} − 0.025	V_{CLn}	V_{CLn} + 0.025	V	2
Overdischarge detection voltage n (n = 1, 2, 3, 4)	V_{DLn}	2.0 V to 3.0 V, Adjustable		V_{DLn} − 0.08	V_{DLn}	V_{DLn} + 0.08	V	2
Overdischarge release voltage n (n = 1, 2, 3, 4)	V_{DUn}	2.0 V to 3.4 V, Adjustable	$V_{DL} \neq V_{DU}$	V_{DUn} − 0.10	V_{DUn}	V_{DUn} + 0.10	V	2
			$V_{DL} = V_{DU}$	V_{DUn} − 0.08	V_{DUn}	V_{DUn} + 0.08	V	2
Overcurrent detection voltage 1	V_{IOV1}	0.05 V to 0.3 V, Adjustable		V_{IOV1} − 0.025	V_{IOV1}	V_{IOV1} + 0.025	V	2
Overcurrent detection voltage 2	V_{IOV2}	—		0.4	0.5	0.6	V	2
Overcurrent detection voltage 3	V_{IOV3}	—		V_{VC1} − 1.5	V_{VC1} − 1.2	V_{VC1} − 0.9	V	2
Temperature coefficient 1 *1	T_{COE1}	Ta = 0°C to 50°C *3		− 1.0	0	1.0	mV / °C	2
Temperature coefficient 2 *2	T_{COE2}	Ta = 0°C to 50°C *3		− 0.5	0	0.5	mV / °C	2
[DELAY TIME]								
Overcharge detection delay time	t_{CU}	CCT pin capacitance = 0.1 μF		0.5	1.0	1.5	s	3
Overdischarge detection delay time	t_{DL}	CDT pin capacitance = 0.1 μF		50	100	150	ms	3
Overcurrent detection delay time 1	t_{IOV1}	CDT pin capacitance = 0.1 μF		5	10	15	ms	3
Overcurrent detection delay time 2	t_{IOV2}	—		0.4	1	1.6	ms	3
Overcurrent detection delay time 3	t_{IOV3}	FET gate capacitance = 2000 pF		100	300	600	μs	3
[0 V BATTERY CHARGE]								
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charge enabled		—	0.8	1.5	V	4
0 V battery charge inhibition battery voltage	V_{0INH}	0 V battery charge inhibited		0.4	0.7	1.1	V	4
[INTERNAL RESISTANCE]								
Resistance between VMP and VDD	R_{VMD}	—		0.5	1	1.5	MΩ	5
Resistance between VMP and VSS	R_{VMS}	—		450	900	1800	kΩ	5

Table 4 (2 / 2)

(Ta = 25°C unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test circuit
[INPUT VOLTAGE]							
Operating voltage between VDD and VSS	V_{DSOP}	Output voltage of DOP and COP fixed	2	—	24	V	2
CTL input voltage "H"	V_{CTLH}	—	V_{DD} × 0.8	—	—	V	2
CTL input voltage "L"	V_{CTLL}	—	—	—	V_{DD} × 0.2	V	2
SEL input voltage "H"	V_{SELH}	—	V_{DD} × 0.8	—	—	V	2
SEL input voltage "L"	V_{SELL}	—	—	—	V_{DD} × 0.2	V	2
[INPUT CURRENT]							
Current consumption during operation	I_{OPE}	V1 = V2 = V3 = V4 = 3.5 V	—	12	30	μA	1
Current consumption during power-down	I_{PDN}	V1 = V2 = V3 = V4 = 1.5 V	—	—	0.1	μA	1
VC1 pin current	I_{VC1}	V1 = V2 = V3 = V4 = 3.5 V	—	1.5	3	μA	5
VC2 pin current	I_{VC2}	V1 = V2 = V3 = V4 = 3.5 V	− 0.3	0	0.3	μA	5
VC3 pin current	I_{VC3}	V1 = V2 = V3 = V4 = 3.5 V	− 0.3	0	0.3	μA	5
VC4 pin current	I_{VC4}	V1 = V2 = V3 = V4 = 3.5 V	− 0.3	0	0.3	μA	5
CTL pin current "H"	I_{CTLH}	V1 = V2 = V3 = V4 = 3.5 V, $V_{CTL} = V_{DD}$	—	—	0.1	μA	5
CTL pin current "L"	I_{CTLL}	V1 = V2 = V3 = V4 = 3.5 V, $V_{CTL} = V_{SS}$	− 0.4	− 0.2	—	μA	5
SEL pin current "H"	I_{SELH}	V1 = V2 = V3 = V4 = 3.5 V, $V_{SEL} = V_{DD}$	—	—	0.1	μA	5
SEL pin current "L"	I_{SELL}	V1 = V2 = V3 = V4 = 3.5 V, $V_{SEL} = V_{SS}$	− 0.1	—	—	μA	5
[OUTPUT CURRENT]							
COP pin leakage current	I_{COH}	V_{COP} = 24 V	—	—	0.1	μA	5
COP pin sink current	I_{COL}	$V_{COP} = V_{SS} + 0.5$ V	10	—	—	μA	5
DOP pin source current	I_{DOH}	$V_{DOP} = V_{DD} - 0.5$ V	10	—	—	μA	5
DOP pin sink current	I_{DOL}	$V_{DOP} = V_{SS} + 0.5$ V	10	—	—	μA	5

***1.** Voltage temperature coefficient 1 : Overcharge detection voltage
***2.** Voltage temperature coefficient 2 : Overcurrent detection voltage 1
***3.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

■ Test Circuits

This chapter describes how to test the S-8254A Series when a 4-serial cell is selected by setting the SEL pin to the VDD level. When a 3-serial cell is selected by setting the SEL pin to the VSS level, short the power supply V4.

1. Current Consumption during Operation, Current Consumption during Power-down (Test circuit 1)

1. 1 Current Consumption during operation (I_{OPE})

The current at the VSS pin when V1 = V2 = V3 = V4 = 3.5 V and $V_{VMP} = V_{DD}$ is the current consumption during operation (I_{OPE}).

1. 2 Current Consumption during power-down (I_{PDN})

The current at the VSS pin when V1 = V2 = V3 = V4 = 1.5 V and $V_{VMP} = V_{SS}$ is the current consumption during power-down (I_{PDN}).

2. Overcharge Detection Voltage, Overcharge Release Voltage, Overdischarge Detection Voltage, Overdischarge Release Voltage, Overcurrent Detection Voltage 1, Overcurrent Detection Voltage 2, Overcurrent Detection Voltage 3, CTL Input Voltage "H", CTL Input Voltage "L", SEL Input Voltage "H", SEL Input Voltage "L" (Test circuit 2)

Confirm that the COP pin and DOP pin are low ($V_{DD} \times 0.1$ V or lower) when $V_{VMP} = V_{SEL} = V_{DD}$, $V_{INI} = V_{CTL} = V_{SS}$, the CCT pin is open, the CDT pin is open, and V1 = V2 = V3 = V4 = 3.5 V (this status is referred to as the initial status).

2. 1 Overcharge Detection Voltage (V_{CU1}), Overcharge Release Voltage (V_{CL1})

The overcharge detection voltage (V_{CU1}) is the voltage of V1 when the voltage of the COP pin is "H" ($V_{DD} \times 0.9$ V or more) after the V1 voltage has been gradually increased starting at the initial status. The overcharge release voltage (V_{CL1}) is the voltage of V1 when the voltage at the COP pin is "L" after the V1 voltage has been gradually decreased.

2. 2 Overdischarge Detection Voltage (V_{DL1}), Overdischarge Release Voltage (V_{DU1})

The overdischarge detection voltage (V_{DL1}) is the voltage of V1 when the voltage of the DOP pin is "H" after the V1 voltage has been gradually decreased starting at the initial status. The overdischarge release voltage (V_{DU1}) is the voltage of V1 when the voltage at the DOP pin is "L" after the V1 voltage has been gradually increased.
When the voltage of Vn (n = 2 to 4) is changed, the overcharge detection voltage (V_{CUn}), overcharge release voltage (V_{CLn}), overdischarge detection voltage (V_{DLn}), and overdischarge release voltage (V_{DUn}) can be determined in the same way as when n = 1.

2. 3 Overcurrent Detection Voltage 1 (V_{IOV1})

Overcurrent detection voltage 1 (V_{IOV1}) is the voltage of the VINI pin when the voltage of the DOP pin is "H" after the VINI pin voltage has been gradually increased starting at the initial status.

2. 4 Overcurrent Detection Voltage 2 (V_{IOV2})

Overcurrent detection voltage 2 (V_{IOV2}) is the voltage of the VINI pin when the voltage of the DOP pin is "H" after the voltage of the CDT pin was set to V_{SS} following the initial status and the voltage of the VINI pin has been gradually decreased.

2. 5 Overcurrent Detection Voltage 3 (V_{IOV3})

Overcurrent detection voltage 3 (V_{IOV3}) is the voltage difference between V_{VC1} and V_{VMP} ($V_{VC1} - V_{VMP}$) when the voltage of the DOP pin is "H" after the VMP voltage has been gradually decreased starting at the initial status.

2. 6 CTL Input Voltage "H" (V_{CTLH}), CTL Input Voltage "L" (V_{CTLL})

The CTL input voltage "H" (V_{CTLH}) is the voltage of CTL when the voltages at the COP and DOP pins are "H" after the CTL voltage has been gradually increased starting at the initial status. The CTL input voltage "L" (V_{CTLL}) is the voltage of CTL when the voltages at the COP and DOP pins are "L" after the CTL voltage has been gradually decreased.

2. 7 SEL Input Voltage "H" (V_{SELH}), SEL Input Voltage "L" (V_{SELL})

Apply 0 V to V4 in the initial status and confirm that the DOP pin is "H". The SEL input voltage "L" (V_{SELL}) is the voltage of the SEL pin when the voltage at the DOP pin is "L" after the SEL voltage has been gradually decreased. The SEL input voltage "H" (V_{SELH}) is the voltage of the SEL pin when the voltage of the DOP pin is "H" after the SEL voltage has been gradually increased.

3. Overcharge Detection Delay Time, Overdischarge Detection Delay Time, Overcurrent Detection Delay Time 1, Overcurrent Detection Delay Time 2, Overcurrent Detection Delay Time 3 (Test circuit 3)

Confirm that the COP pin and DOP pin are "L" when $V_{VMP} = V_{DD}$, $V_{INI} = V_{SS}$, and V1 = V2 = V3 = V4 = 3.5 V (this status is referred to as the initial status).

3. 1 Overcharge Detection Delay Time (t_{CU})

The overcharge detection delay time (t_{CU}) is the time it takes for the voltage of the COP pin to change from "L" to "H" after the voltage of V1 is instantaneously changed to 4.5 V from the initial status.

3. 2 Overdischarge Detection Delay Time (t_{DL})

The overdischarge detection delay time (t_{DL}) is the time it takes for the voltage of the DOP pin to change from "L" to "H" after the voltage of V1 is instantaneously changed to 1.5 V from the initial status

3. 3 Overcurrent Detection Delay Time 1 (t_{IOV1})

Overcurrent detection delay time 1 (t_{IOV1}) is the time it takes for the voltage of the DOP pin to change from "L" to "H" after the voltage of the VINI pin is instantaneously changed to 0.4 V from the initial status.

3. 4 Overcurrent Detection Delay Time 2 (t_{IOV2})

Overcurrent detection delay time 2 (t_{IOV2}) is the time it takes for the voltage of the DOP pin to change from "L" to "H" after the voltage of the VINI pin is instantaneously changed to V_{IOV2} max. + 0.2 V from the initial status.

3. 5 Overcurrent Detection Delay Time 3 (t_{IOV3})

Overcurrent detection delay time 3 (t_{IOV3}) is the time it takes for the voltage of the DOP pin to change from "L" to "H" after the voltage of the VMP pin is instantaneously changed to V_{IOV3} min. – 0.2 V from the initial status.

4. 0 V Battery Charge Starting Charger Voltage (0 V Battery Charge Enabled), 0 V Battery Charge Inhibition Battery Voltage (0 V Battery Charge Inhibited)
(Test circuit 4)

Either the 0 V battery charge starting charger voltage or the 0 V battery charge inhibition battery voltage is applied to each product according to the 0 V battery charge function.

4. 1 0 V Battery Charge Starting Charger Voltage (V_{0CHA}) (0 V Battery Charge Enabled)

For the 0 V battery charge starting charger voltage, the COP pin voltage should be lower than V_{0CHA} max. − 1 V when V1 = V2 = V3 = V4 = 0 V and $V_{VMP} = V_{0CHA}$ max.

4. 2 0 V Battery Charge Inhibition Battery Voltage (V_{0INH}) (0 V Battery Charge Inhibited)

For 0 V battery charge inhibition battery voltage, the COP pin voltage should be higher than V_{VMP} − 1 V when V1 = V2 = V3 = V4 = V_{0INH} min. and V_{VMP} = 24 V.

5. Resistance between VMP and VDD, Resistance between VMP and VSS, VC1 Pin Current, VC2 Pin Current, VC3 Pin Current, VC4 Pin Current, CTL pin Current "H", CTL Pin Current "L", SEL Pin Current "H", SEL Pin Current "L", COP Pin Leakage Current, COP Pin Sink Current, DOP Pin Source Current, DOP Pin Sink Current
(Test circuit 5)

$V_{VMP} = V_{SEL} = V_{DD}$, $V_{INI} = V_{CTL} = V_{SS}$, V1 = V2 = V3 = V4 = 3.5 V, and other pins left "open" (this status is referred to as the initial status).

5. 1 Resistance between VMP and VDD (R_{VMD})

The resistance between VMP and VDD (R_{VMD}) is obtained from $R_{VMD} = V_{DD} / I_{VMD}$ using the current value of the VMP pin (I_{VMD}) when V_{VMP} is V_{SS} after the initial status.

5. 2 Resistance between VMP and VSS (R_{VMS})

The resistance between VMP and VSS (R_{VMS}) is obtained from $R_{VMS} = V_{DD} / I_{VMS}$ using the current value of the VMP pin (I_{VMS}) when V1 = V2 = V3 = V4 = 1.8 V after the initial status.

5. 3 VC1 Pin Current (I_{VC1}), VC2 Pin Current (I_{VC2}), VC3 Pin Current (I_{VC3}), VC4 Pin Current (I_{VC4})

At the initial status, the current that flows through the VC1 pin is the VC1 pin current (I_{VC1}), the current that flows through the VC2 pin is the VC2 pin current (I_{VC2}), the current that flows through the VC3 pin is the VC3 pin current (I_{VC3}), and the current that flows through the VC4 pin is the VC4 pin current (I_{VC4}).

5. 4 CTL pin Current "H" (I_{CTLH}), CTL Pin Current "L" (I_{CTLL})

In the initial status, the current that flows through the CTL pin is the CTL pin current "L" (I_{CTLL}), after that, when $V_{CTL} = V_{DD}$, the current that flows through the CTL pin is the CTL pin current "H" (I_{CTLH}).

5. 5 SEL Pin Current "H" (I_{SELH}), SEL Pin Current "L" (I_{SELL})

In the initial status, the current that flows through the SEL pin is the SEL pin current "H" (I_{SELH}), after that, when $V_{SEL} = V_{SS}$, the current that flows through the SEL pin is the SEL pin current "L" (I_{SELL}).

5. 6 COP Pin Leakage Current (I_{COH}), COP Pin Sink Current (I_{COL})

The COP pin sink current (I_{COL}) is the current that flows through the COP pin when $V_{COP} = V_{SS} + 0.5$ V after the initial status. After that, the current that flows through the COP pin when V1 = V2 = V3 = V4 = 6 V and $V_{COP} = V_{DD}$ is the COP pin leakage current (I_{COH}).

5. 7 DOP Pin Source Current (I_{DOH}), DOP Pin Sink Current (I_{DOL})

The DOP pin sink current (I_{DOL}) is the current that flows through the DOP pin when $V_{DOP} = V_{SS} + 0.5$ V after the initial status. After that, the current that flows through the DOP pin when $V_{VMP} = V_{DD} - 2$ V and $V_{DOP} = V_{DD} - 0.5$ V is the DOP pin source current (I_{DOH}).

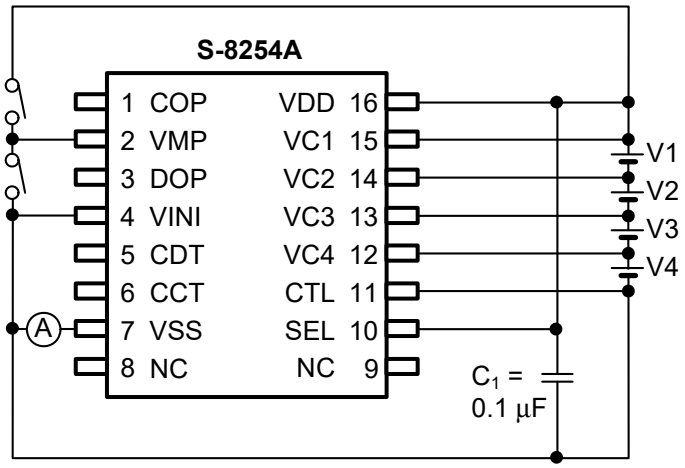


Figure 4 Test Circuit 1

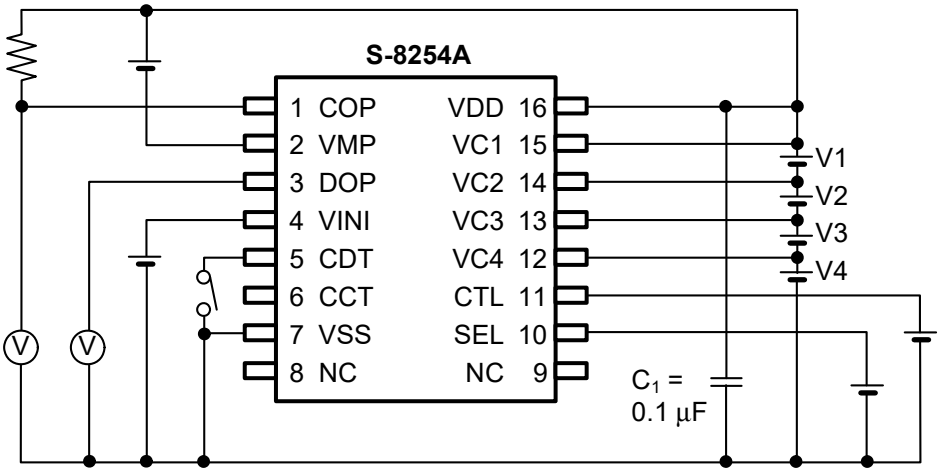


Figure 5 Test Circuit 2

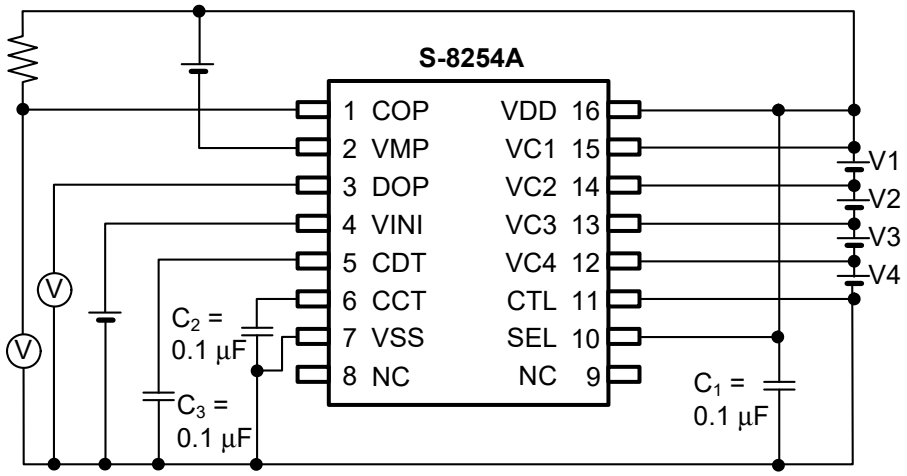


Figure 6 Test Circuit 3

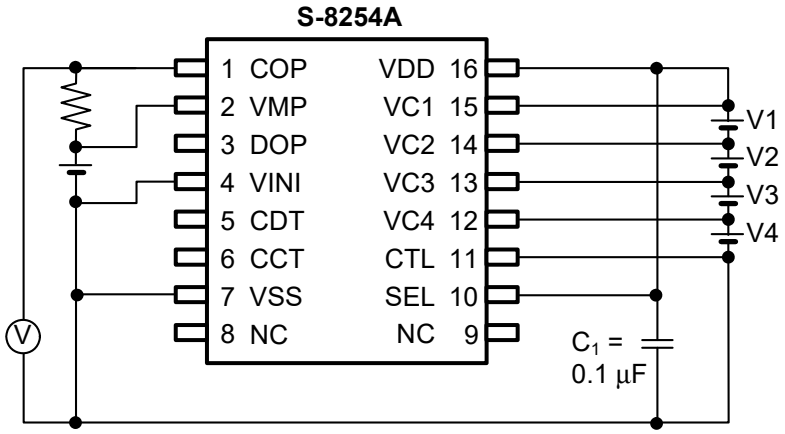


Figure 7 Test Circuit 4

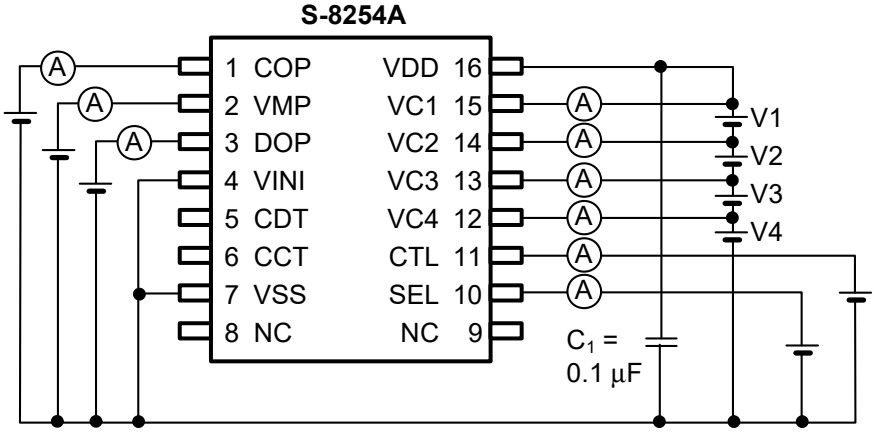


Figure 8 Test Circuit 5

■ Operation

Remark Refer to "■ **Battery Protection IC Connection Example**".

1. Normal Status

When the voltage of each of the batteries is in the range from V_{DLn} to V_{CUn} and the discharge current is lower than the specified value (the VINI pin voltage is lower than V_{IOV1} and V_{IOV2}, and the VMP pin voltage is higher than V_{IOV3}), the charging and discharging FETs are turned on.

2. Overcharge Status

When the voltage of one of the batteries becomes higher than V_{CUn} and the state continues for t_{CU} or longer, the COP pin becomes high impedance. The COP pin is pulled up to the EB_+ pin voltage by an external resistor, and the charging FET is turned off to stop charging. This is called the overcharge status. The overcharge status is released when one of the following two conditions holds.

(1) The voltage of each of the batteries becomes V_{CLn} or lower.
(2) The voltage of each of the batteries is V_{CUn} or lower, and the VMP pin voltage is 39 / 40 × V_{DD} or lower (a load is connected and discharging is started via the body diode of the charging FET).

3. Overdischarge Status

When the voltage of one of the batteries becomes lower than V_{DLn} and the state continues for t_{DL} or longer, the DOP pin voltage becomes V_{DD} level, and the discharging FET is turned off to stop discharging. This is called the overdischarge status.

3. 1 Power-down Function

When the overdischarge status is reached, the VMP pin is pulled down to the V_{SS} level by the internal R_{VMS} resistor of the IC. When the VMP pin voltage is V_{DD} / 2 or lower, the power-down function starts to operate and almost every circuit in the S-8254A Series stops working. The conditions of each output pin are as follows.

(1) COP pin : High-Z
(2) DOP pin : V_{DD}

The power-down function is released when the following condition holds.

(1) The VMP pin voltage is V_{DD} / 2 or higher.

The overdischarge status is released when either of the following two conditions is met.

(1) In case the VMP pin voltage is V_{DD} / 2 or higher and the VMP pin voltage is lower than V_{DD}, the overdischarge status is released when the voltage of each of the batteries is V_{DUn} or higher.
(2) In case a charger is connected, the overdischarge hysteresis is released. And the overdischarge status is released when the voltage of each of the batteries is V_{DLn} or higher.

4. Overcurrent Status

The S-8254A Series has three overcurrent detection levels (V_{IOV1}, V_{IOV2}, and V_{IOV3}) and three overcurrent detection delay times (t_{IOV1}, t_{IOV2}, and t_{IOV3}) corresponding to each overcurrent detection level. When the discharging current becomes higher than the specified value (the voltage between V_{SS} and V_{INI} is greater than V_{IOV1}) and the state continues for t_{IOV1} or longer, the S-8254A Series enters the overcurrent status, in which the DOP pin voltage becomes V_{DD} level to turn off the discharging FET to stop discharging, the COP pin becomes high impedance and is pulled up to the EB+ pin voltage to turn off the charging FET to stop charging, and the VMP pin is pulled up to the V_{DD} voltage by the internal resistor (R_{VMD}). Operation of overcurrent detection level 2 (V_{IOV2}) and overcurrent detection delay time 2 (t_{IOV2}) is the same as for V_{IOV1} and t_{IOV1}.
In the overcurrent status, the VMP pin is pulled up to the V_{DD} level by the internal resistor in the IC (R_{VMD} resistor). The overcurrent status is released when the following condition holds.

(1) The VMP pin voltage is V_{IOV3} or higher because a charger is connected or the load (30 MΩ or more) is released.

5. 0 V Battery Charge

Regarding the charging of a self-discharged battery (0 V battery), the S-8254A Series has two functions from which one should be selected.

(1) 0 V battery charging is allowed (0 V battery charge enabled)
When the charger voltage is higher than V_{0CHA}, the 0 V battery can be charged.

(2) 0 V battery charging is prohibited (0 V battery charge inhibited)
When the battery voltage is V_{0INH} or lower, the 0 V battery cannot be charged.

Caution When the VDD pin voltage is lower than the minimum value of V_{DSOP}, the operation of the S-8254A Series is not guaranteed.

6. Delay Time Setting

The overcharge detection delay time (t_{CU}) is determined by the external capacitor connected to the CCT pin. The overdischarge detection delay time (t_{DL}) and overcurrent detection delay time 1 (t_{IOV1}) are determined by the external capacitor connected to the CDT pin. Overcurrent detection delay times 2 and 3 (t_{IOV2}, t_{IOV3}) are fixed internally.

	min.	typ.	max.	
t_{CU} [s] =	(5.00,	10.0,	15.0)	× C_{CCT} [μF]
t_{DL} [s] =	(0.50,	1.00,	1.50)	× C_{CDT} [μF]
t_{IOV1} [s] =	(0.05,	0.10,	0.15)	× C_{CDT} [μF]

7. CTL Pin

The S-8254A Series has control pins. The CTL pin is used for controlling the COP and DOP pin output voltages. CTL pin takes precedence over the battery protection circuit.

Table 5 Conditions Set by CTL Pin

CTL Pin	COP Pin	DOP Pin
High	High-Z	V_{DD}
Open	High-Z	V_{DD}
Low	Normal status *1	Normal status *1

***1.** The status is controlled by the voltage detector.

Caution Please note unexpected behavior might occur when electrical potential difference between the CTL pin ('L' level) and VSS is generated through the external filter (R_{VSS} and C_{VSS}) as a result of input voltage fluctuations.

8. SEL pin

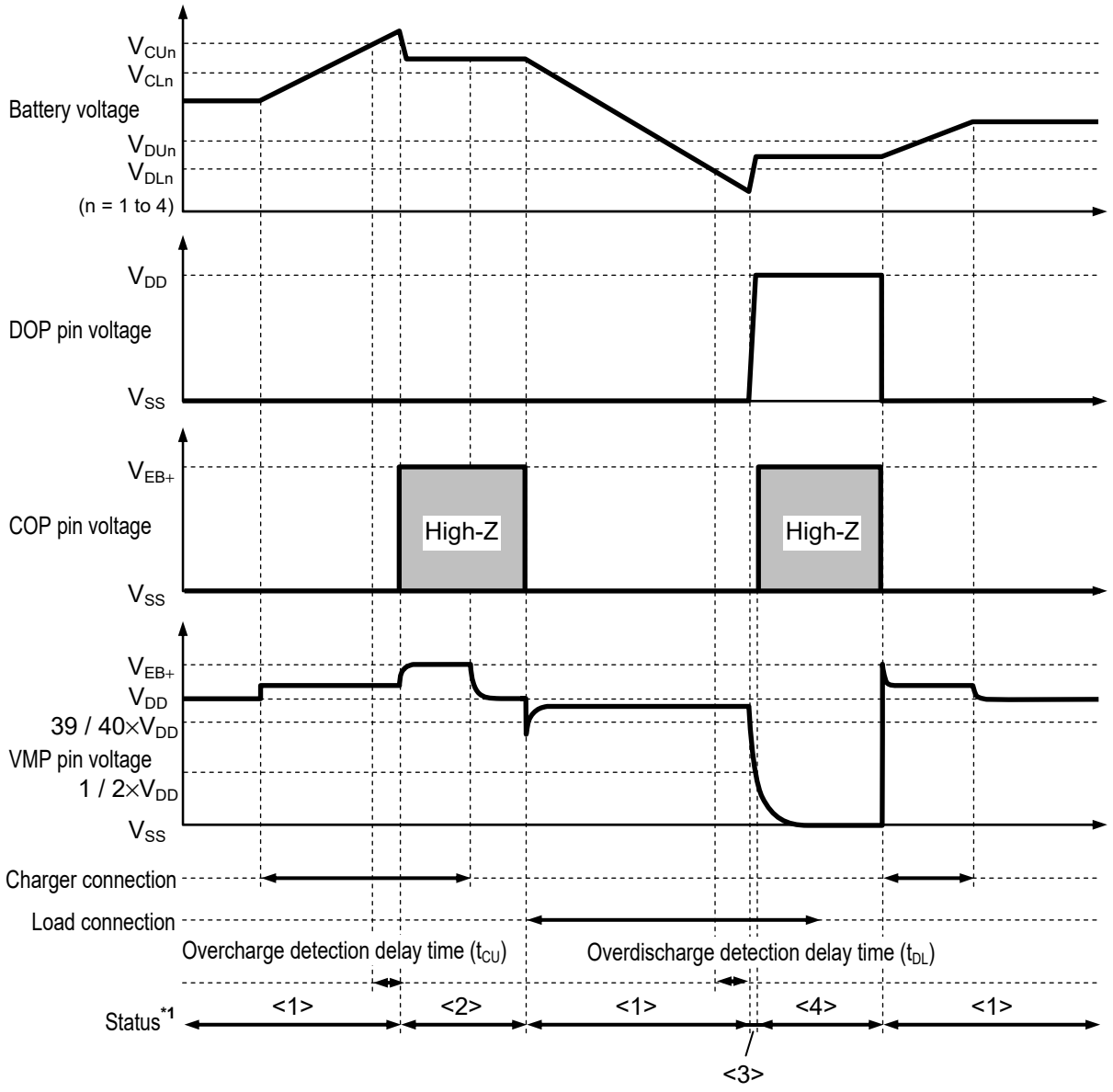
The S-8254A Series has control pins. The SEL pin is used for switching between 3-cell and 4-cell protection. When the SEL pin is low, overdischarge detection of the V4 cell is prohibited and an overdischarge is not detected even if the V4 cell is shorted, therefore, this IC can be used for 3-cell protection. The SEL pin takes precedence over the battery protection circuit. Use the SEL pin at high or low.

Table 6 Conditions Set by SEL Pin

SEL Pin	Condition
High	4-cell protection
Open	Undefined
Low	3-cell protection

■ Timing Chart

1. Overcharge Detection and Overdischarge Detection

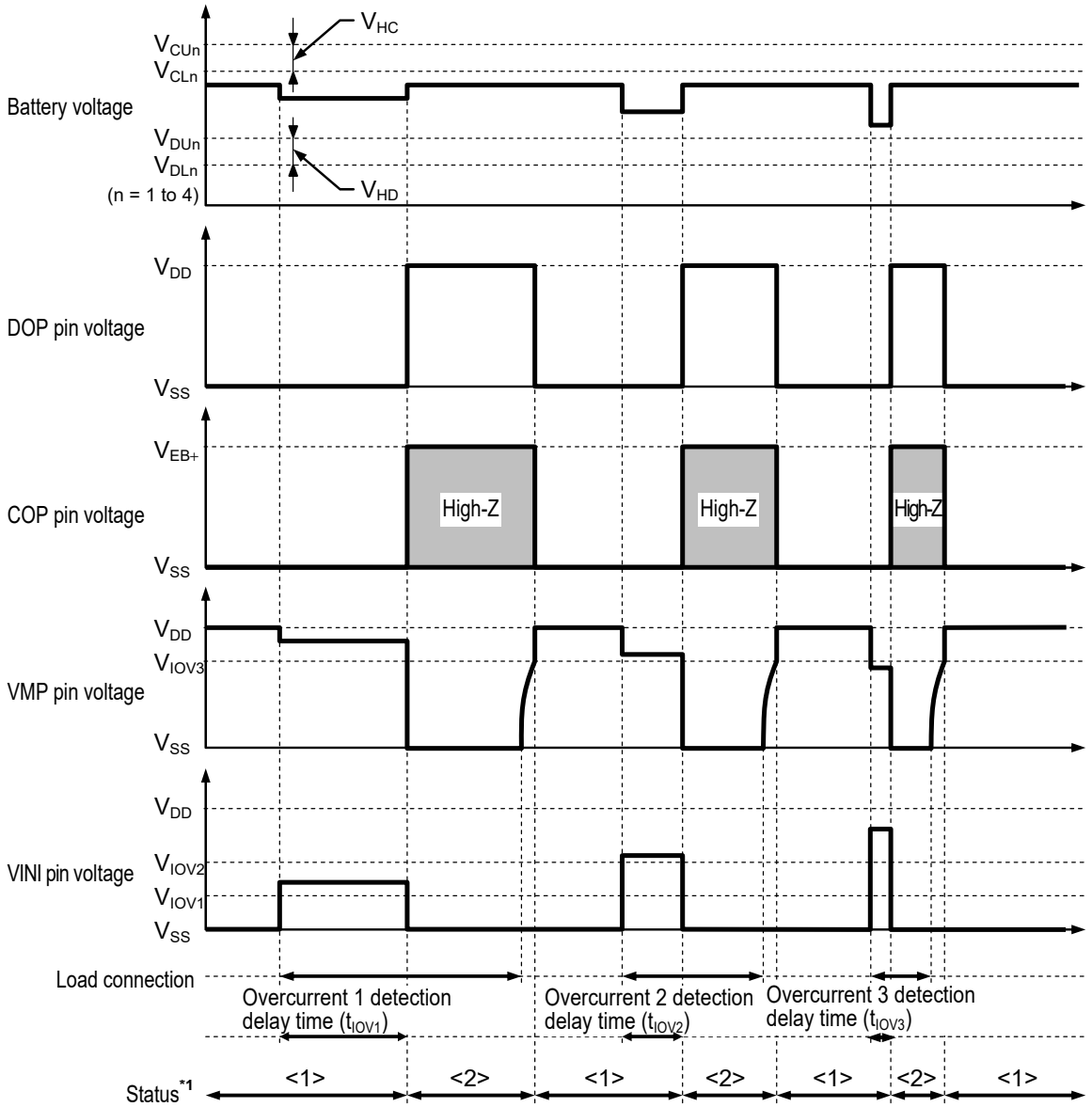


***1.** < 1 > : Normal status
< 2 > : Overcharge status
< 3 > : Overdischarge status
< 4 > : Power-down status

Remark The charger is assumed to charge with a constant current. V_{EB+} indicates the open voltage of the charger.

Figure 9

2. Overcurrent detection



***1.** < 1 > : Normal status
< 2 > : Overcurrent status

Remark The charger is assumed to charge with a constant current. V_{EB+} indicates the open voltage of the charger.

Figure 10

■ Battery Protection IC Connection Example

1. 3-serial Cell

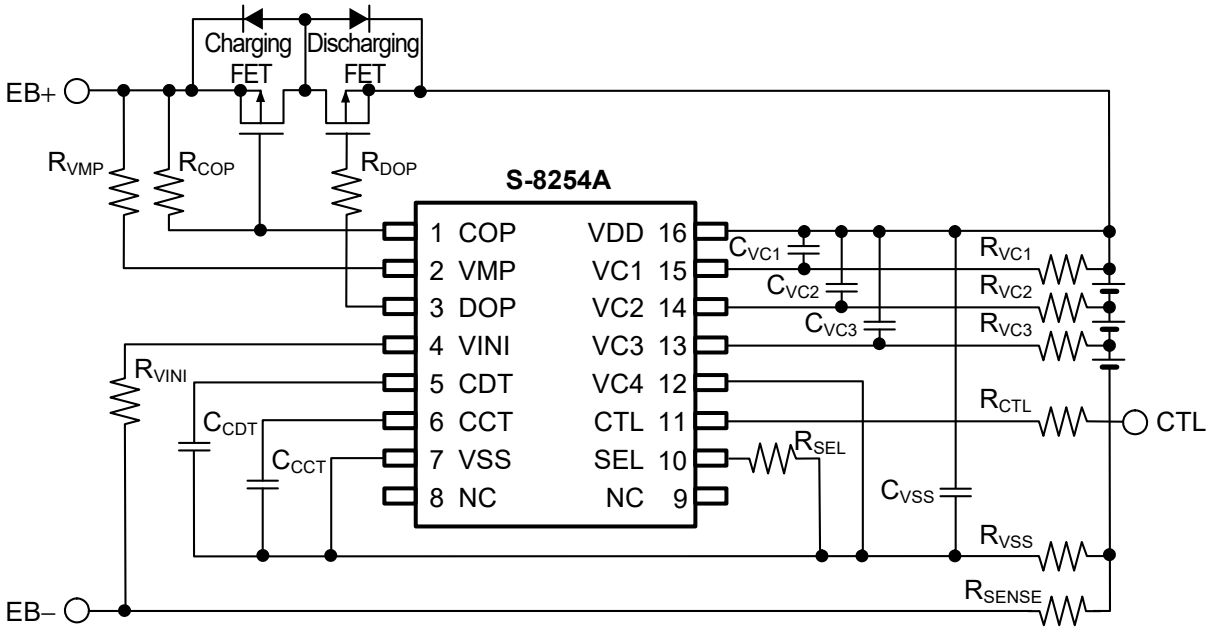


Figure 11

2. 4-serial Cell

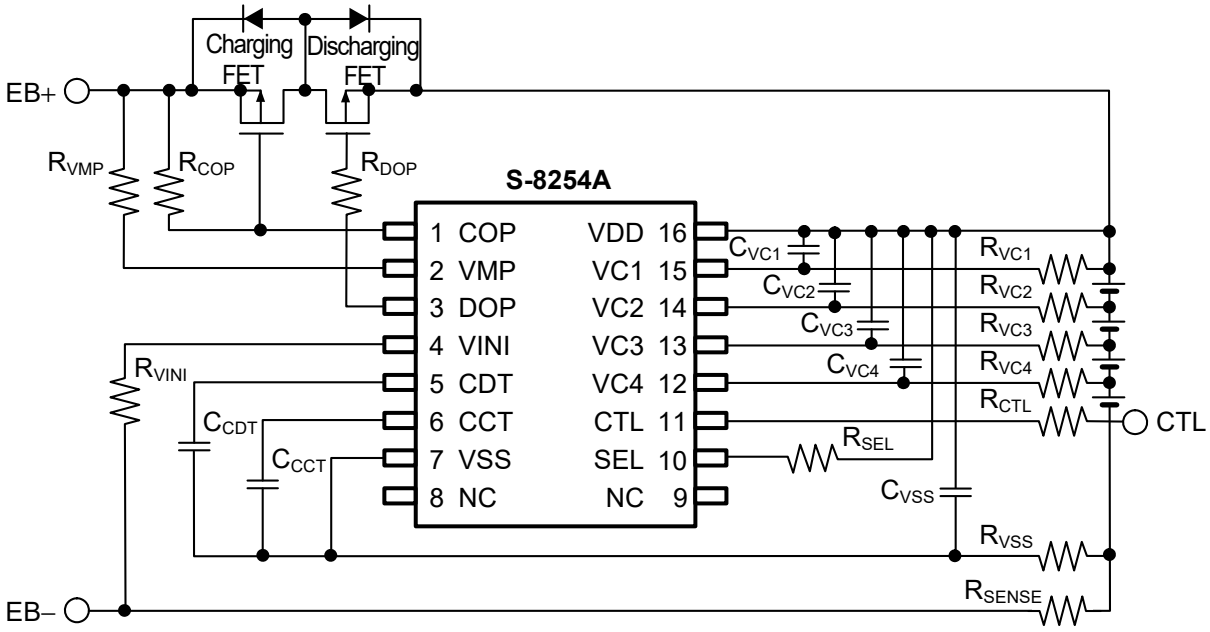


Figure 12

Table 7 Constants for External Components

Symbol	Min.	Typ.	Max.	Unit
R_{VC1}*1	0	1	1	kΩ
R_{VC2}*1	0	1	1	kΩ
R_{VC3}*1	0	1	1	kΩ
R_{VC4}*1	0	1	1	kΩ
R_{DOP}	2	5.1	10	kΩ
R_{COP}	0.1	1	1	MΩ
R_{VMP}	1	5.1	10	kΩ
R_{CTL}	1	1	100	kΩ
R_{VINI}	1	1	100	kΩ
R_{SEL}	1	1	100	kΩ
R_{SENSE}	0	—	—	mΩ
R_{VSS}*1	10	10	51	Ω
C_{VC1}*1	0	0.1	0.33	μF
C_{VC2}*1	0	0.1	0.33	μF
C_{VC3}*1	0	0.1	0.33	μF
C_{VC4}*1	0	0.1	0.33	μF
C_{CCT}	0.01	0.1	—	μF
C_{CDT}	0.07	0.1	—	μF
C_{VSS}*1	2.2	10	10	μF

***1.** Please set up a filter constant to be $R_{VSS} \times C_{VSS} \geq 51\ \mu F \bullet \Omega$ and to be $R_{VC1} \times C_{VC1} = R_{VC2} \times C_{VC2} = R_{VC3} \times C_{VC3} = R_{VC4} \times C_{VC4} = R_{VSS} \times C_{VSS}$.

Caution 1. The constants may be changed without notice.

2. It is recommended that filter constants between VDD and VSS should be set approximately to 100 μF • Ω.

e.g. $C_{VSS} \times R_{VSS} = 10\ \mu F \times 10\ \Omega = 100\ \mu F \bullet \Omega$

Enough evaluation of transient power supply variation and overcurrent protection function in the actual application is needed to determine the proper constants. Contact our sales representatives in case the constants should be set to other than 100 μF • Ω or so.

3. It has not been confirmed whether the operation is normal or not in circuits other than the connection examples. In addition, the connection examples and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.

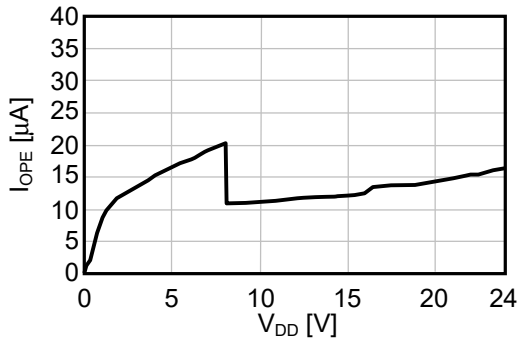
■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Batteries can be connected in any order, however, there may be cases when discharging cannot be performed when a battery is connected. In this case, short the VMP pin and VDD pin or connect the battery charger to return to the normal status.
- When an overcharged battery and an overdischarged battery intermix, the circuit is in both the overcharge and overdischarge statuses, so charging and discharging are not possible.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

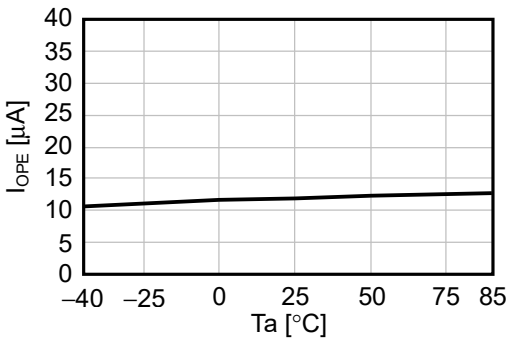
■ Characteristics (Typical Data)

1. Current Consumption

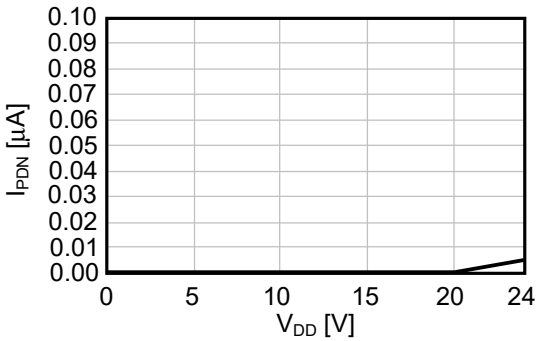
1. 1 I_{OPE} vs. V_{DD}



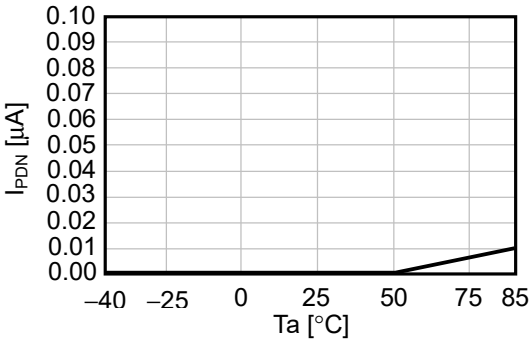
1. 2 I_{OPE} vs. Ta



1. 3 I_{PDN} vs. V_{DD}

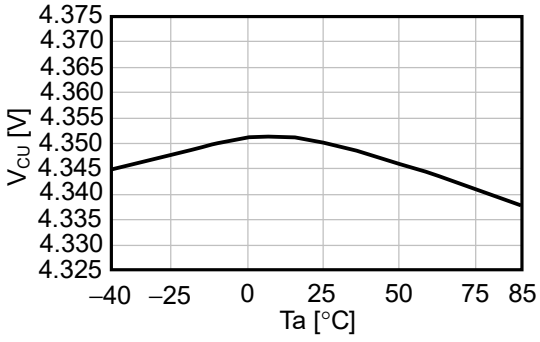


1. 4 I_{PDN} vs. Ta

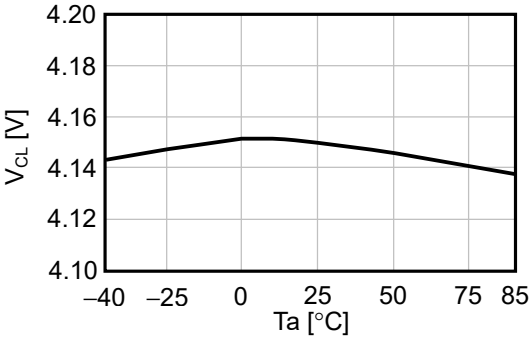


2. Overcharge Detection / Release Voltage, Overdischarge Detection / Release Voltage, Overcurrent Detection Voltage, and Delay Times

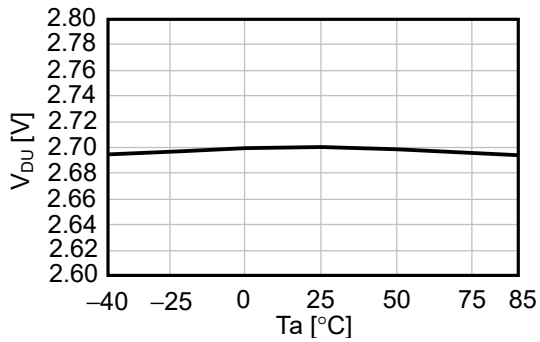
2. 1 V_{CU} vs. Ta



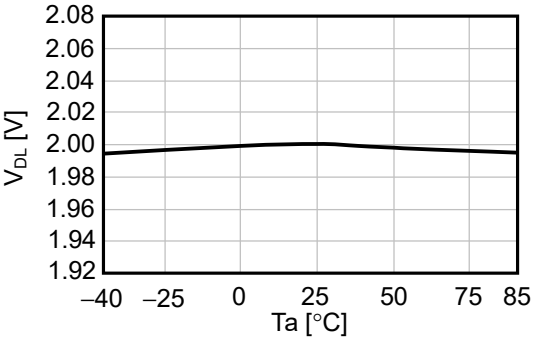
2. 2 V_{CL} vs. Ta



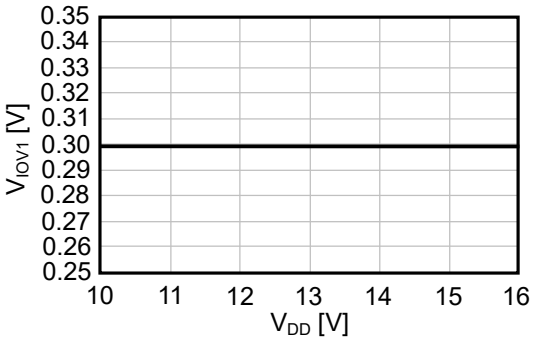
2. 3 V_{DU} vs. Ta



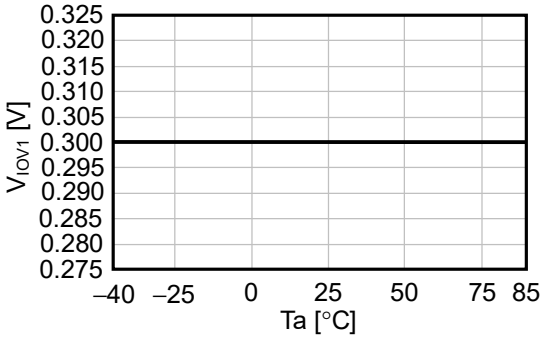
2. 4 V_{DL} vs. Ta



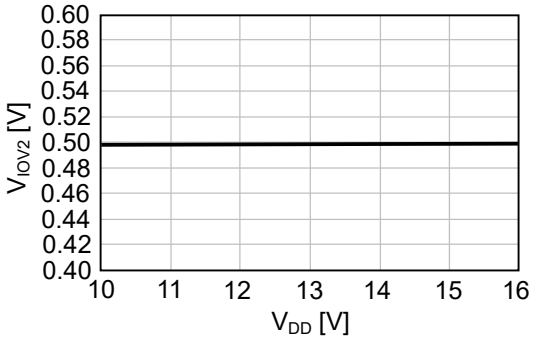
2. 5 V_{IOV1} vs. V_{DD}



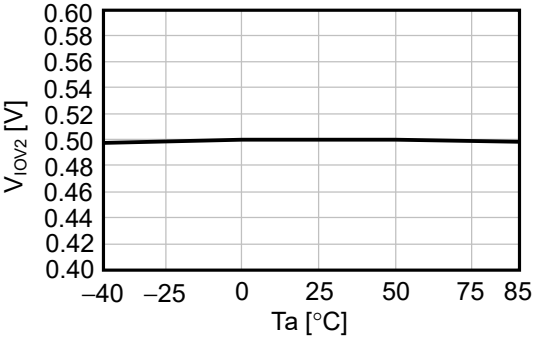
2. 6 V_{IOV1} vs. Ta



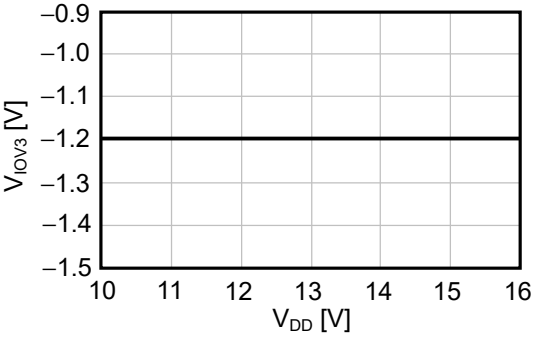
2. 7 V_{IOV2} vs. V_{DD}



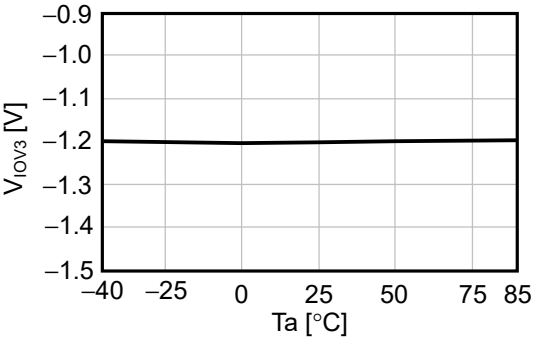
2. 8 V_{IOV2} vs. Ta



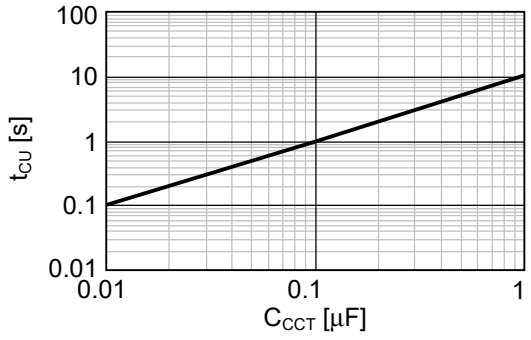
2. 9 V_{IOV3} vs. V_{DD}



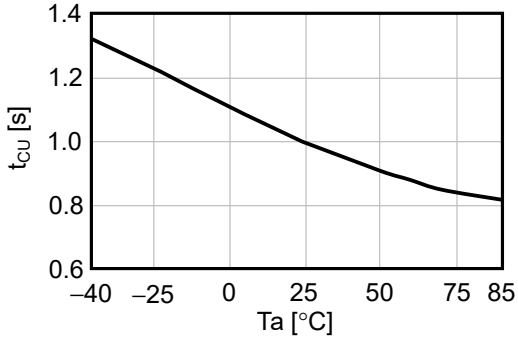
2. 10 V_{IOV3} vs. Ta



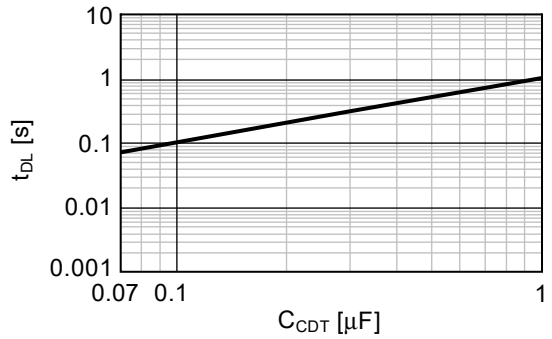
2. 11 t_{CU} vs. C_{CCT}



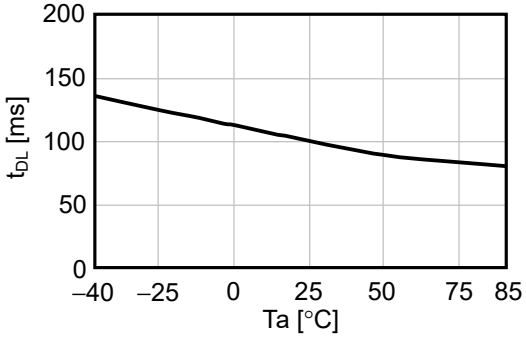
2. 12 t_{CU} vs. Ta



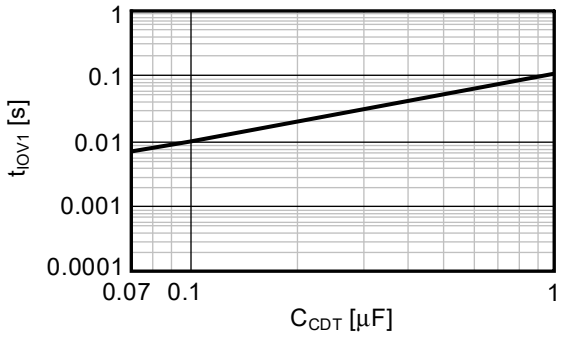
2. 13 t_{DL} vs. C_{CDT}



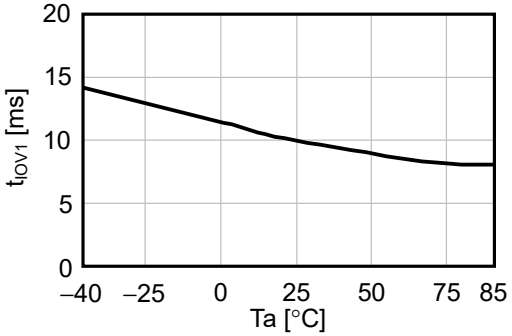
2. 14 t_{DL} vs. Ta



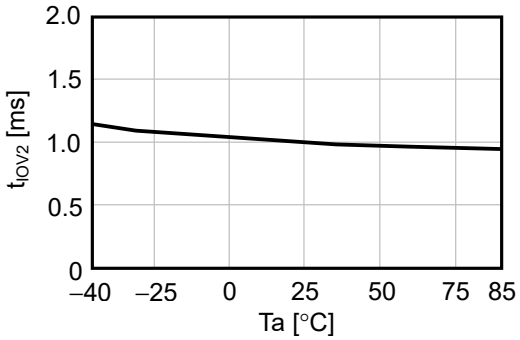
2. 15 t_{IOV1} vs. C_{CDT}



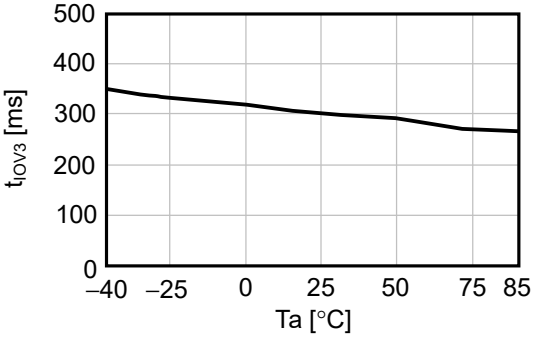
2. 16 t_{IOV1} vs. Ta



2. 17 t_{IOV2} vs. Ta

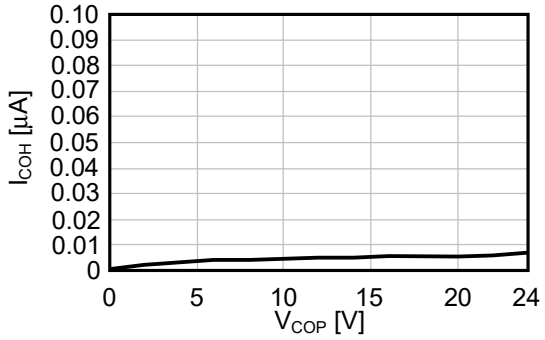


2. 18 t_{IOV3} vs. Ta

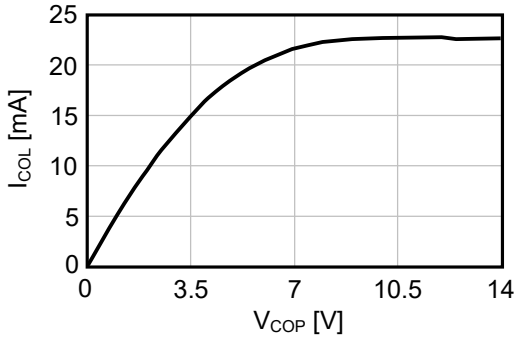


3. COP / DOP Pin

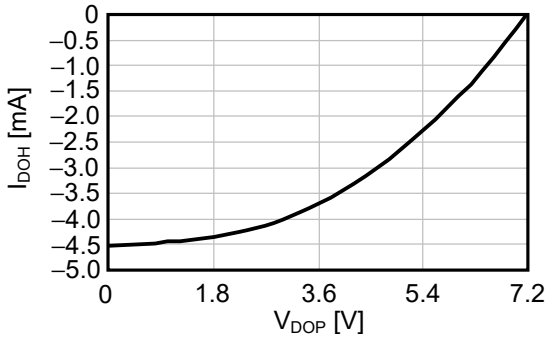
3. 1 I_{COH} vs. V_{COP}



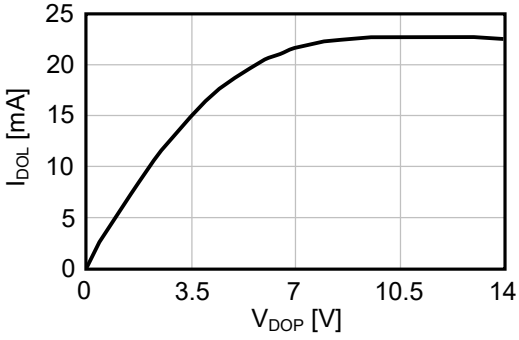
3. 2 I_{COL} vs. V_{COP}

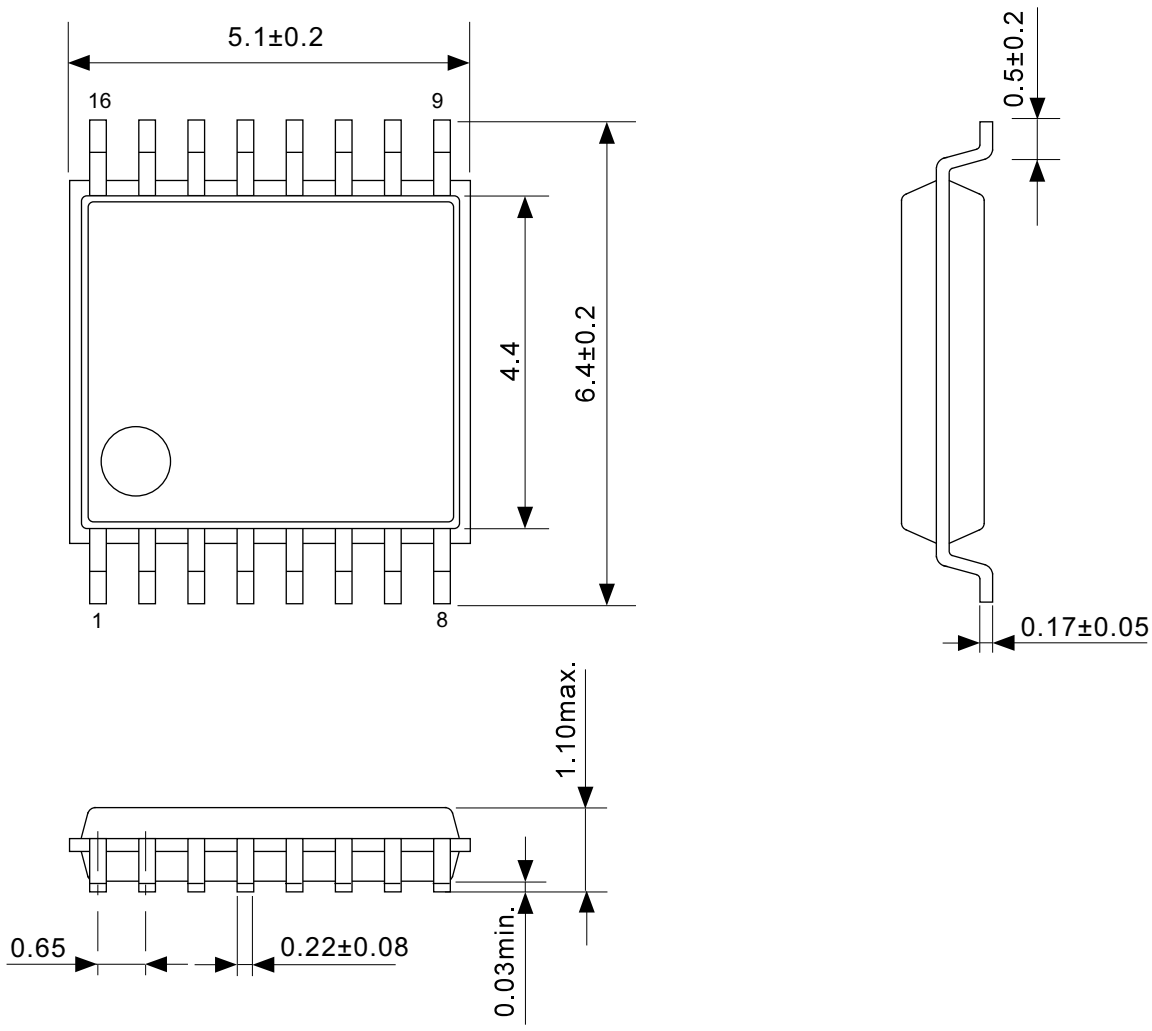


3. 3 I_{DOH} vs. V_{DOP}



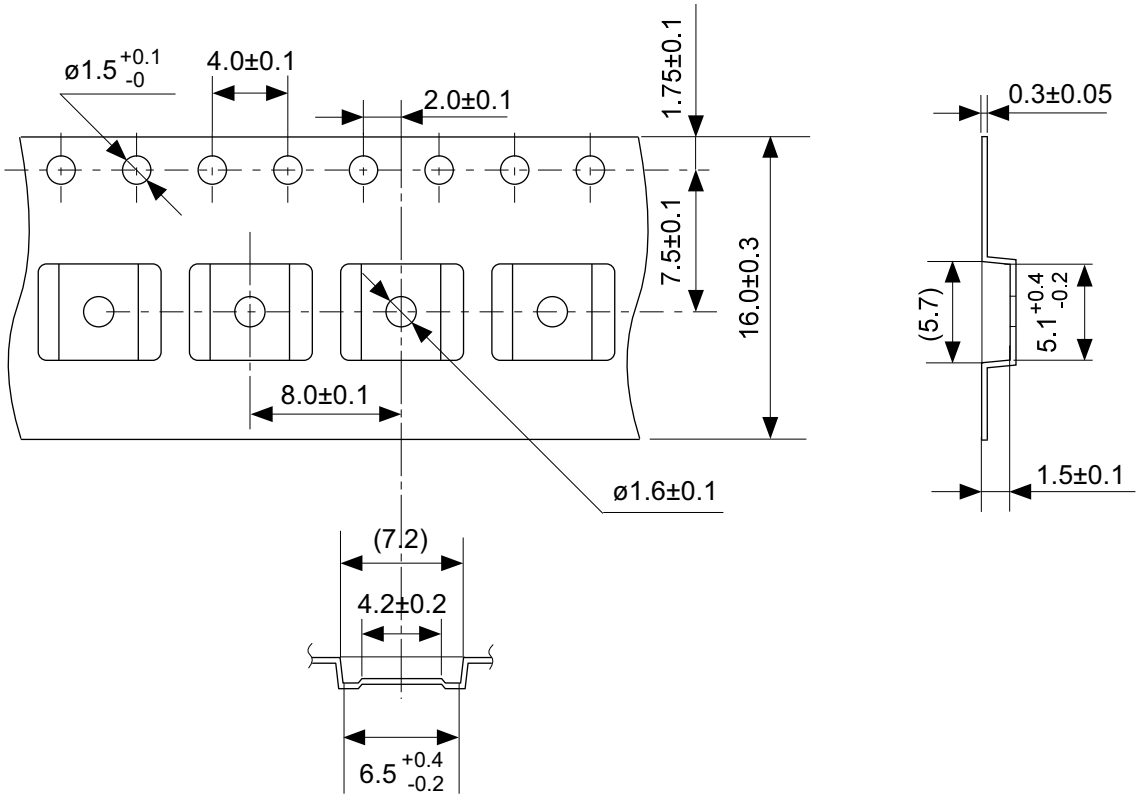
3. 4 I_{DOL} vs. V_{DOP}

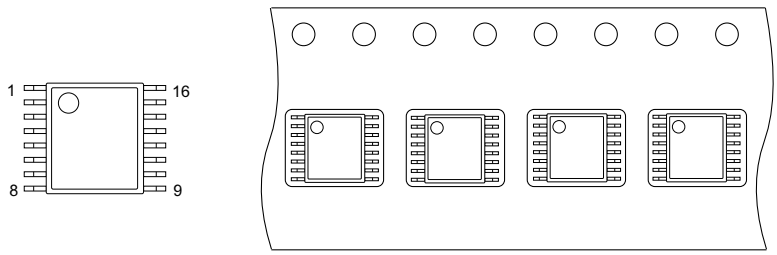




No. FT016-A-P-SD-1.2

TITLE	TSSOP16-A-PKG Dimensions
No.	FT016-A-P-SD-1.2
ANGLE	
UNIT	mm
ABLIC Inc.	

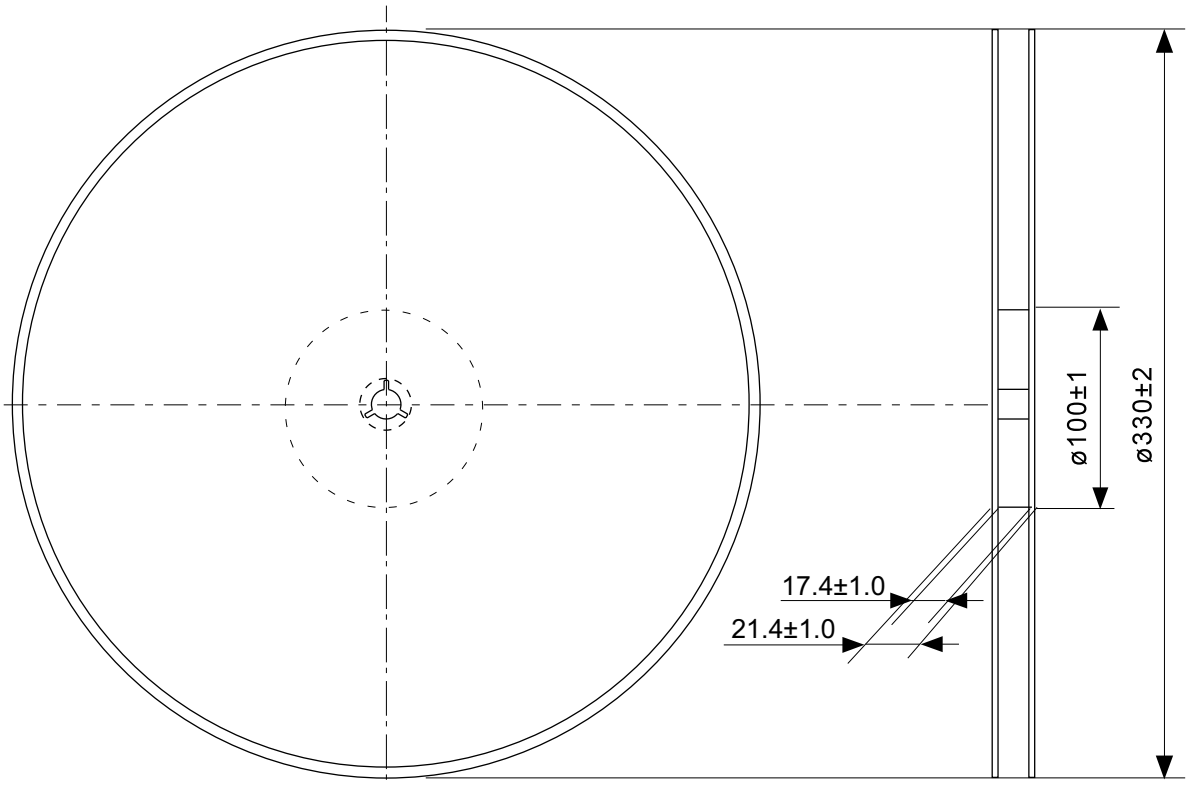




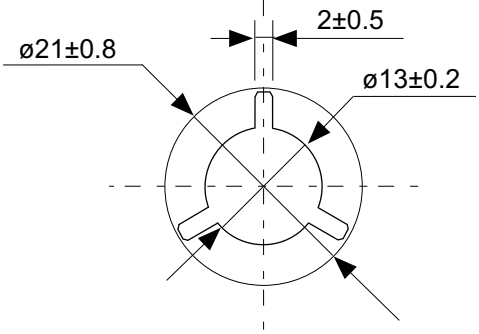
No. FT016-A-C-SD-1.1

TITLE	TSSOP16-A-Carrier Tape
No.	FT016-A-C-SD-1.1
ANGLE	
UNIT	mm

ABLIC Inc.

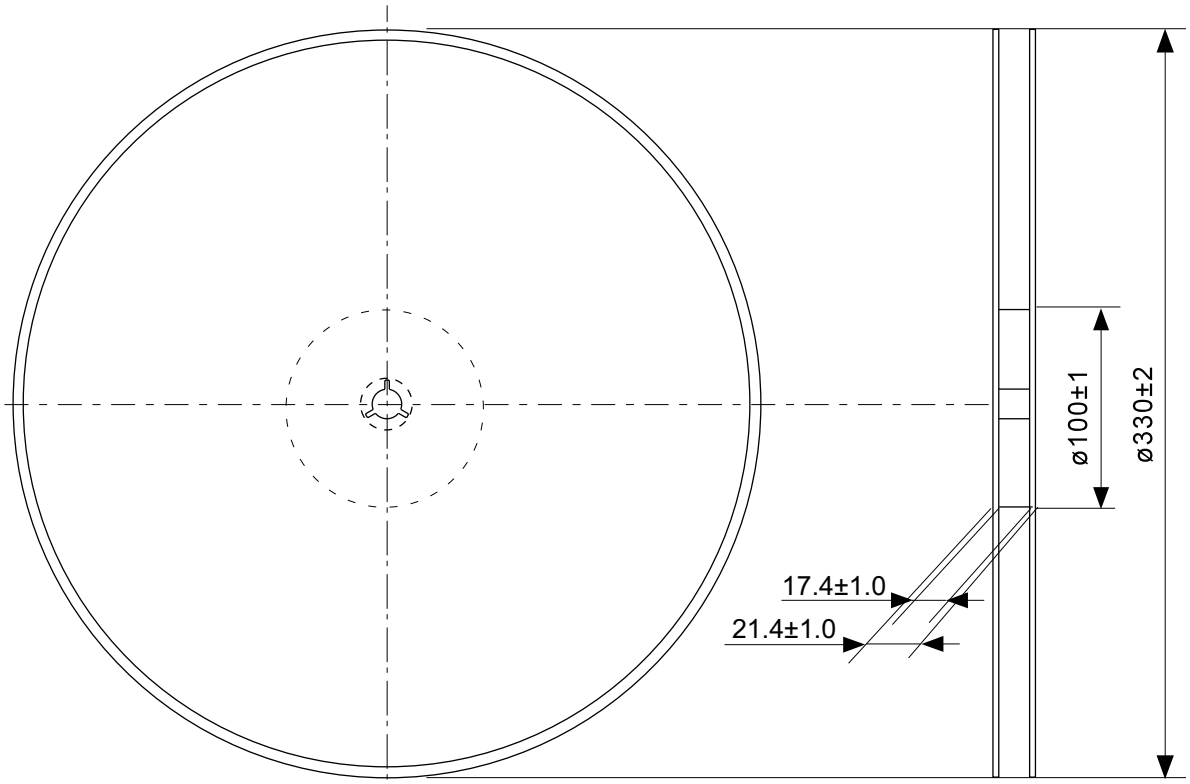


Enlarged drawing in the central part

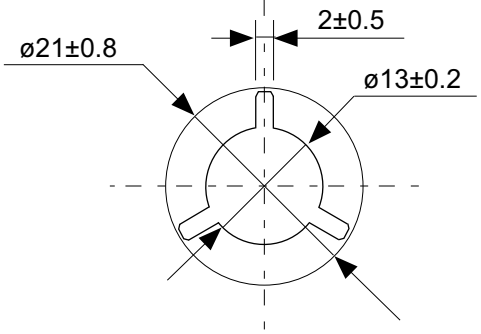


No. FT016-A-R-SD-3.0

TITLE	TSSOP16-A- Reel		
No.	FT016-A-R-SD-3.0		
ANGLE		QTY.	2,000
UNIT	mm		
	ABLIC Inc.		



Enlarged drawing in the central part



No. FT016-A-R-S1-2.0

TITLE	TSSOP16-A- Reel		
No.	FT016-A-R-S1-2.0		
ANGLE		QTY.	4,000
UNIT	mm		
	ABLIC Inc.		

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2.4-2019.07

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