www.ablic.com

BATTERY MONITORING IC FOR 3-SERIAL TO 5-SERIAL CELL PACK

© ABLIC Inc., 2012-2020

Rev.2.1_00

The S-8225A Series includes high-accuracy voltage detection circuits and delay circuits, and can monitor the status of 3-serial to 5-serial cell lithium-ion rechargeable battery in single use. By switching the voltage level which is applied to the SEL1 pin and SEL2 pin, users are able to use the S-8225A Series for 3-serial to 5-serial cell pack.
By cascade connection using the S-8225A Series, it is also possible to protect 6-serial or more cells lithium-ion rechargeable battery pack.

■ Features

- High-accuracy voltage detection function for each cell
  - Overcharge detection voltage n (n = 1 to 5): 3.500 V to 4.400 V (50 mV step), Accuracy ±20 mV (Ta = +25°C), ±30 mV (Ta = 0°C to +60°C)
  - Overcharge release voltage n (n = 1 to 5): 3.300 V to 4.400 V*1, Accuracy ±50 mV
  - Overdischarge detection voltage n (n = 1 to 5): 2.000 V to 3.200 V (100 mV step), Accuracy ±80 mV
  - Overdischarge release voltage n (n = 1 to 5): 2.100 V to 3.400 V*2, Accuracy ±100 mV
- Overcharge detection delay time and overdischarge detection delay time can be set by external capacitor.
- Switchable between 3-serial to 5-serial cell by using the SEL1 pin and the SEL2 pin
- Cascade connection is available.
- The CO pin and the DO pin are controlled by the CTLC pin and the CTLD pin, respectively.
- Output voltage of the CO pin and the DO pin is limited to 12 V max.
- High-withstand voltage: Absolute maximum rating: 28 V
- Wide operation voltage range: 4 V to 26 V
- Wide operation temperature range: Ta = −40°C to +85°C
- Low current consumption
  - During operation (V1 = V2 = V3 = V4 = V5 = 3.4 V): 22 μA max. (Ta = +25°C)
  - During power-down (V1 = V2 = V3 = V4 = V5 = 1.6 V): 4.5 μA max. (Ta = +25°C)
- Lead-free (Sn 100%), halogen-free

***1.** Overcharge hysteresis voltage n (n = 1 to 5) is selectable in 0 V, or in 0.1 V to 0.4 V in 50 mV step.
(Overcharge hysteresis voltage = Overcharge detection voltage − Overcharge release voltage)

***2.** Overdischarge hysteresis voltage n (n = 1 to 5) is selectable in 0 V to 0.7 V in 100 mV step.
(Overdischarge hysteresis voltage = Overdischarge release voltage − Overdischarge detection voltage)

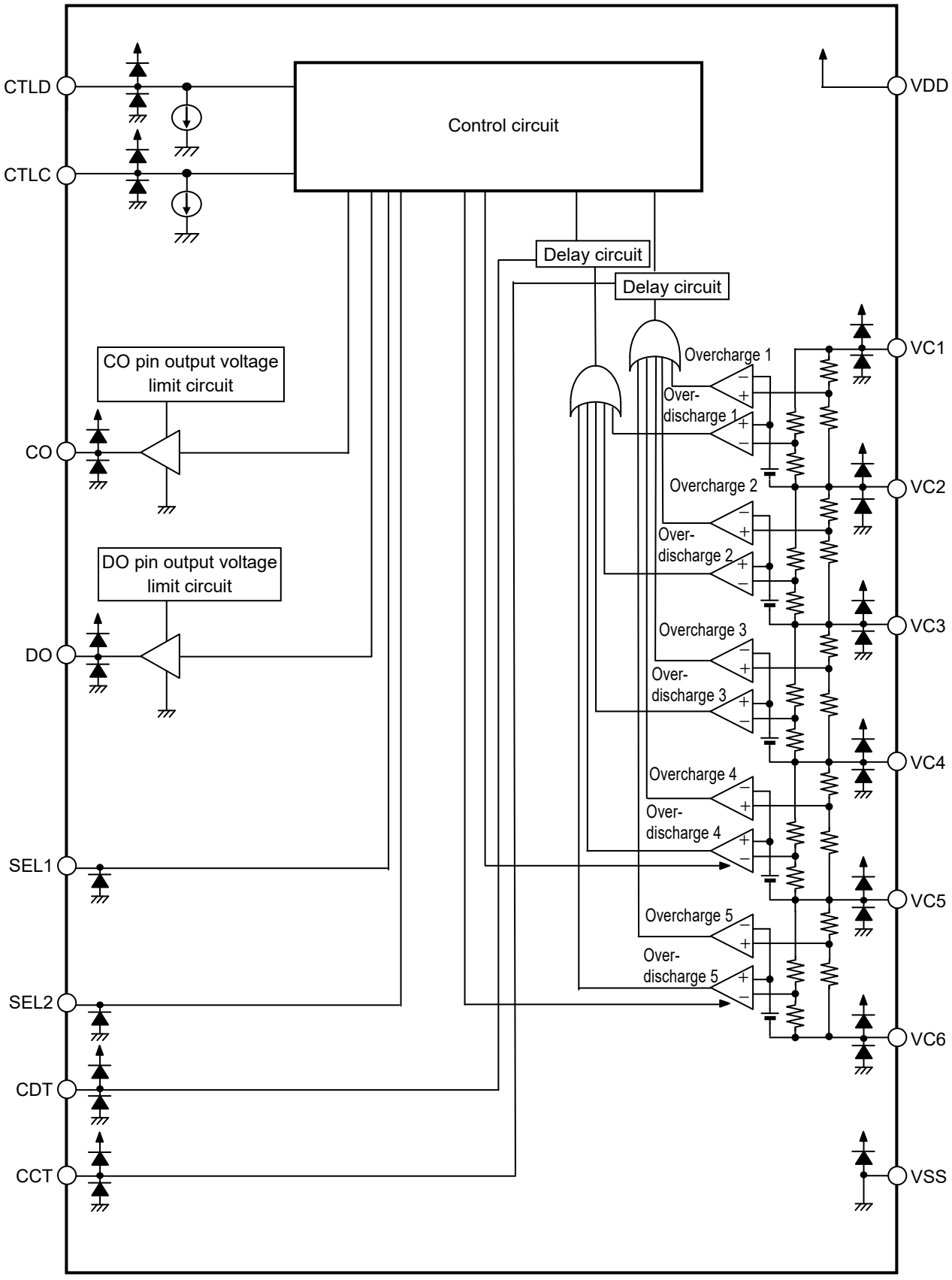
■ Application

- Lithium-ion rechargeable battery pack

■ Package

- 16-Pin TSSOP

■ Block Diagram



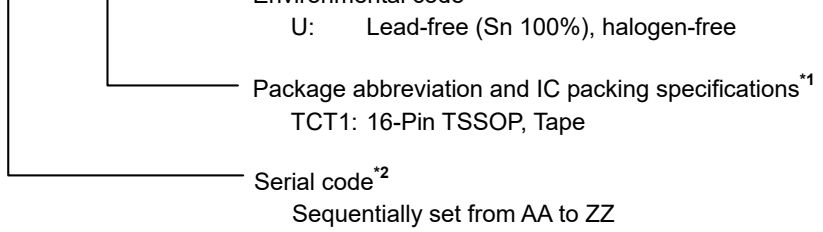
Remark Diodes in the figure are parasitic diodes.

Figure 1

■ Product Name Structure

1. Product name

S-8225A xx - TCT1 U



***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel
16-Pin TSSOP	FT016-A-P-SD	FT016-A-C-SD	FT016-A-R-S1

3. Product name list

Table 2

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Overdischarge Detection Voltage [V_{DL}]	Overdischarge Release Voltage [V_{DU}]	0 V Battery Detection Function
S-8225AAA-TCT1U	4.225 V	4.125 V	2.300 V	2.500 V	Available
S-8225AAB-TCT1U	4.400 V	4.300 V	2.300 V	2.500 V	Available
S-8225AAC-TCT1U	4.250 V	4.150 V	2.500 V	3.000 V	Unavailable
S-8225AAD-TCT1U	4.350 V	4.350 V	2.500 V	2.700 V	Unavailable
S-8225AAE-TCT1U	4.225 V	4.125 V	2.300 V	3.000 V	Unavailable
S-8225AAF-TCT1U	4.215 V	4.155 V	2.800 V	3.000 V	Available
S-8225AAG-TCT1U	4.250 V	4.250 V	2.500 V	2.700 V	Unavailable
S-8225AAH-TCT1U	4.150 V	4.000 V	2.500V	3.000 V	Available
S-8225AAI-TCT1U	4.200 V	4.150 V	2.500V	2.550 V	Available
S-8225AAJ-TCT1U	3.900 V	3.500 V	2.000 V	2.700 V	Available
S-8225AAK-TCT1U	4.275 V	4.175 V	2.600 V	2.800 V	Available
S-8225AAM-TCT1U	4.220 V	4.120 V	2.500 V	3.000 V	Available
S-8225AAN-TCT1U	4.300 V	4.200 V	2.300 V	2.800 V	Unavailable

Remark Please contact our sales representatives for products other than the above.

■ Pin Configuration

1. 16-Pin TSSOP

Top view

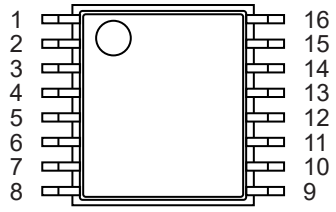


Figure 2

Table 3

Pin No.	Symbol	Description
1	CTLD	DO control pin
2	CTLC	CO control pin
3	CO	Output pin for overcharge detection
4	DO	Output pin for overdischarge detection
5	SEL1	Switching pins for 3-serial to 5-serial cell*1
6	SEL2	
7	CDT	Capacitor connection pin for delay for overdischarge detection voltage
8	CCT	Capacitor connection pin for delay for overcharge detection voltage
9	VSS	Input pin for negative power supply, connection pin for negative voltage of battery 5
10	VC6	Connection pin for negative voltage of battery 5
11	VC5	Connection pin for negative voltage of battery 4, connection pin for positive voltage of battery 5
12	VC4	Connection pin for negative voltage of battery 3, connection pin for positive voltage of battery 4
13	VC3	Connection pin for negative voltage of battery 2, connection pin for positive voltage of battery 3
14	VC2	Connection pin for negative voltage of battery 1, connection pin for positive voltage of battery 2
15	VC1	Connection pin for positive voltage of battery 1
16	VDD	Input pin for positive power supply, connection pin for positive voltage of battery 1

***1.** Refer to "**7. SEL pin**" in "**■ Operation**" for setting of the SEL1 pin and the SEL2 pin.

■ Absolute Maximum Ratings

Table 4

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin	V_{DS}	VDD	V_{SS} – 0.3 to V_{SS} + 28	V
Input pin voltage	V_{IN}	VC1, VC2, VC3, VC4, VC5, VC6, SEL1, SEL2, CTLC, CTLD, CCT, CDT	V_{SS} – 0.3 to V_{DD} + 0.3	V
Output pin voltage	V_{OUT}	DO, CO	V_{SS} – 0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	–	1100*1	mW
Operation ambient temperature	T_{opr}	–	–40 to +85	°C
Storage temperature	T_{stg}	–	–40 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

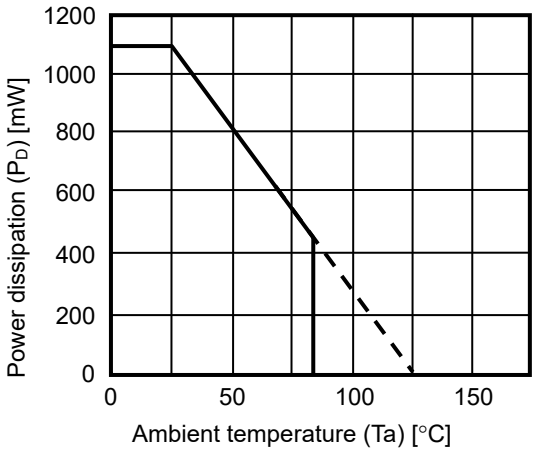


Figure 3 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

Table 5 (1 / 2)

(Ta = +25°C, $V_{DS} = V_{DD} - V_{SS} = V1 + V2 + V3 + V4 + V5$ unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage n (n = 1, 2, 3, 4, 5)	V_{CUn}	Ta = +25°C V1 = V2 = V3 = V4 = V5 = V_{CU} – 0.05 V	V_{CUn} – 0.020	V_{CUn}	V_{CUn} + 0.020	V	1
		Ta = 0°C to +60°C*1 V1 = V2 = V3 = V4 = V5 = V_{CU} – 0.05 V	V_{CUn} – 0.030	V_{CUn}	V_{CUn} + 0.030	V	1
Overcharge release voltage n (n = 1, 2, 3, 4, 5)	V_{CLn}	–	V_{CLn} – 0.050	V_{CLn}	V_{CLn} + 0.050	V	1
Overdischarge detection voltage n (n = 1, 2, 3, 4, 5)	V_{DLn}	–	V_{DLn} – 0.080	V_{DLn}	V_{DLn} + 0.080	V	1
Overdischarge release voltage n (n = 1, 2, 3, 4, 5)	V_{DUn}	–	V_{DUn} – 0.100	V_{DUn}	V_{DUn} + 0.100	V	1
0 V battery detection voltage n (n = 1, 2, 3, 4, 5)	V_{0INHn}	With 0 V battery detection function	0.4	0.7	1.1	V	1
Delay Time Function*2							
Overcharge detection delay time	t_{CU}	C_{CCT} = 0.1 µF	0.67	1.00	1.33	s	2
Overdischarge detection delay time	t_{DL}	C_{CDT} = 0.1 µF	0.67	1.00	1.33	s	2
CCT pin voltage	V_{CCT}	–	–	1.5	5.0	V	2
CDT pin voltage	V_{CDT}	–	–	1.5	5.0	V	2
Input Voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP}	Fixed output voltage of CO pin and DO pin	4	–	26	V	–
CTLC pin voltage "H"	V_{CTLCH}	–	–	–	V_{DS} – 0.8	V	3
CTLC pin voltage "L"	V_{CTLCL}	–	V_{DS} – 4.0	–	–	V	3
CTLD pin voltage "H"	V_{CTLDH}	–	–	–	V_{DS} – 0.8	V	3
CTLD pin voltage "L"	V_{CTLDL}	–	V_{DS} – 4.0	–	–	V	3
SEL1 pin voltage "H"	V_{SELH1}	–	$V_{DS} \times 0.8$	–	–	V	3
SEL2 pin voltage "H"	V_{SELH2}	–	$V_{DS} \times 0.8$	–	–	V	3
SEL1 pin voltage "L"	V_{SELL1}	–	–	–	$V_{DS} \times 0.2$	V	3
SEL2 pin voltage "L"	V_{SELL2}	–	–	–	$V_{DS} \times 0.2$	V	3
Output Voltage		–					
CO pin voltage "H"	V_{COH}	–	5.0	8.0	12.0	V	4
DO pin voltage "H"	V_{DOH}	–	5.0	8.0	12.0	V	4
Input Current							
Current consumption during operation	I_{OPE}	V1 = V2 = V3 = V4 = V5 = 3.4 V	–	13	22	µA	5
Current consumption during power-down	I_{PDN}	V1 = V2 = V3 = V4 = V5 = 1.6 V	–	2.6	4.5	µA	5
VC1 pin current	I_{VC1}	V1 = V2 = V3 = V4 = V5 = 3.4 V, V6 = V7 = V_{DS}, V8 = V9 = 0 V	–	0.4	0.8	µA	6
VC2 to VC5 pins current	I_{VC2} to I_{VC5}	V1 = V2 = V3 = V4 = V5 = 3.4 V, V6 = V7 = V_{DS}, V8 = V9 = 0 V	–1.0	–	1.0	µA	6
VC6 pin current	I_{VC6}	V1 = V2 = V3 = V4 = V5 = 3.4 V, V6 = V7 = V_{DS}, V8 = V9 = 0 V	–3.0	–1.0	–	µA	6
CTLC pin current "H"	I_{CTLCH}	V1 = V2 = V3 = V4 = V5 = 3.4 V, V6 = V7 = V_{DS}, V8 = V9 = 0 V	0.4	0.6	0.8	µA	6
CTLD pin current "H"	I_{CTLDH}	V1 = V2 = V3 = V4 = V5 = 3.4 V, V6 = V7 = V_{DS}, V8 = V9 = 0 V	0.4	0.6	0.8	µA	6

Table 5 (2 / 2)

(Ta = +25°C, $V_{DS} = V_{DD} - V_{SS} = V1 + V2 + V3 + V4 + V5$ unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
SEL1 pin current "H"	I_{SELH1}	V1 = V2 = V3 = V4 = V5 = 3.4 V, V6 = V7 = V8 = V_{DS}, V9 = 0 V	–	–	0.1	µA	6
SEL2 pin current "H"	I_{SELH2}	V1 = V2 = V3 = V4 = V5 = 3.4 V, V6 = V7 = V9 = V_{DS}, V8 = 0 V	–	–	0.1	µA	6
SEL1 pin current "L"	I_{SELL1}	V1 = V2 = V3 = V4 = V5 = 3.4 V, V6 = V7 = V_{DS}, V8 = V9 = 0 V	–0.1	–	–	µA	6
SEL1 pin current "L"	I_{SELL2}	V1 = V2 = V3 = V4 = V5 = 3.4 V, V6 = V7 = V_{DS}, V8 = V9 = 0 V	–0.1	–	–	µA	6
Output Current							
CO pin source current	I_{COH}	–	–	–	–10	µA	7
CO pin sink current	I_{COL}	–	10	–	–	µA	7
DO pin source current	I_{DOH}	–	–	–	–10	µA	7
DO pin sink current	I_{DOL}	–	10	–	–	µA	7

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

***2.** Refer to "**6. Delay time setting**" in "**■ Operation**" for details of the delay time function.

■ Test Circuits

1. Overcharge detection voltage (V_{CUn}), overcharge release voltage (V_{CLn}), overdischarge detection voltage (V_{DLn}), overdischarge release voltage (V_{DUn}) (Test circuit 1)

V_{CU1} is defined as the voltage V1 when V1 is gradually increased and the CO pin output becomes detection status after setting V1 = V2 = V3 = V4 = V5 = V_{CU} – 0.05 V. After that, V_{CL1} is defined as the voltage V1 when V1 is gradually decreased and the CO pin output becomes release status after setting V2 = V3 = V4 = V5 = 3.2 V. Moreover, V_{DL1} is defined as the voltage V1 when V1 is gradually decreased and the DO pin output becomes detection status after setting V1 = V2 = V3 = V4 = V5 = 3.5 V. After that, V_{DU1} is defined as the voltage V1 when V1 is gradually increased and the DO pin output becomes release status.
Similarly, V_{CUn}, V_{CLn}, V_{DLn} and V_{DUn} can be defined by changing Vn (n = 2 to 5).

2. 0 V battery detection voltage (V_{0INHn}) (With 0 V battery detection function) (Test circuit 1)

V_{0INH1} is defined as the voltage V1 when V1 is gradually decreased and the CO pin output becomes detection status after setting V1 = V2 = V3 = V4 = V5 = 3.4 V.
Similarly, V_{0INHn} can be defined by changing Vn (n = 2 to 5).

3. Overcharge detection delay time (t_{CU}), overdischarge detection delay time (t_{DL}) (Test circuit 2)

t_{CU} is defined as the time period from when V1 changes from 3.4 V to 4.5 V to when the CO pin output becomes detection status after setting V1 = V2 = V3 = V4 = V5 = 3.4 V.
Moreover, t_{DL} is defined as the time period from when V1 changes from 3.4 V to 1.6 V to when the DO pin output becomes detection status after setting V1 = V2 = V3 = V4 = V5 = 3.4 V.

4. CCT pin voltage (V_{CCT}), CDT pin voltage (V_{CDT}) (Test circuit 2)

V_{CCT} is defined as the voltage between the CCT pin and the VSS pin during the time period when V1 changes from 3.4 V to 4.5 V to when the CO pin output becomes detection status after setting V1 = V2 = V3 = V4 = V5 = 3.4 V.
Moreover, V_{CDT} is defined as the voltage between the CDT pin and the VSS pin during the time period when V1 changes from 3.4 V to 1.6 V to when the DO pin output becomes detection status after setting V1 = V2 = V3 = V4 = V5 = 3.4 V.

5. CTLC pin voltage "H" (V_{CTLCH}), CTLC pin voltage "L" (V_{CTLCL}), CTLD pin voltage "H" (V_{CTLDH}), CTLD pin voltage "L" (V_{CTLDL}) (Test circuit 3)

V_{CTLCL} is defined as the voltage V6 when V6 is gradually decreased and the CO pin output becomes detection status after setting V1 = V2 = V3 = V4 = V5 = 3.4 V, V6 = V7 = V_{DS} (= V1 + V2 + V3 + V4 + V5), V8 = V9 = 0 V. After that, V_{CTLCH} is defined as the voltage V6 when V6 is gradually increased and the CO pin output becomes release status. Moreover, V_{CTLDL} is defined as the voltage V7 when V7 is gradually decreased and the DO pin output becomes detection status after setting V1 = V2 = V3 = V4 = V5 = 3.4 V, V6 = V7 = V_{DS} (= V1 + V2 + V3 + V4 + V5), V8 = V9 = 0 V. After that, V_{CTLDH} is defined as the voltage V7 when V7 is gradually increased and the DO pin output becomes release status.

6. SEL1 pin voltage "H" (V_{SELH1}), SEL2 pin voltage "H" (V_{SELH2}), SEL1 pin voltage "L" (V_{SELL1}), SEL2 pin voltage "L" (V_{SELL2})
(Test circuit 3)

V_{SELH1} is defined as the voltage V8 when V8 is gradually increased and the DO pin output becomes release status after setting V1 = V2 = V3 = V5 = 3.5 V, V4 = 0 V, V6 = V7 = V_{DS} (= V1 + V2 + V3 + V4 + V5), V8 = V9 = 0 V. After that, V_{SELL1} is defined as the voltage V8 when V8 is gradually decreased and the DO pin output becomes detection status.
Moreover, V_{SELH2} is defined as the voltage V9 when V9 is gradually increased and the DO pin output becomes release status after setting V1 = V2 = V3 = V4 = 3.5 V, V5 = 0 V, V6 = V7 = V_{DS} (= V1 + V2 + V3 + V4 + V5), V8 = V9 = 0 V. After that, V_{SELL2} is defined as the voltage V9 when V9 is gradually decreased and the DO pin output becomes detection status.

7. CO pin voltage "H" (V_{COH}), DO pin voltage "H" (V_{DOH})
(Test circuit 4)

V_{COH} is defined as the voltage between the CO pin and the VSS pin when V1 = V2 = V3 = V4 = V5 = 3.4 V.
V_{DOH} is defined as the voltage between the DO pin and the VSS pin when V1 = V2 = V3 = V4 = V5 = 3.4 V.

8. CO pin source current (I_{COH}), CO pin sink current (I_{COL}), DO pin source current (I_{DOH}), DO pin sink current (I_{DOL})
(Test circuit 7)

I_{COH} is defined as the CO pin current when V1 = V2 = V3 = V4 = V5 = 3.4 V, V6 = V_{COH} – 0.5 V.
I_{COL} is defined as the CO pin current when V1 = 6.8 V, V2 = 0 V, V3 = V4 = V5 = 3.4 V, V6 = 0.5 V.
I_{DOH} is defined as the DO pin current when V1 = V2 = V3 = V4 = V5 = 3.4 V, V7 = V_{DOH} – 0.5 V.
I_{DOL} is defined as the DO pin current when V1 = 6.8 V, V2 = 0 V, V3 = V4 = V5 = 3.4 V, V7 = 0.5 V.

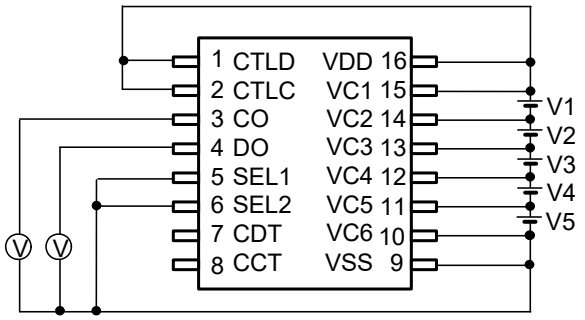


Figure 4 Test Circuit 1

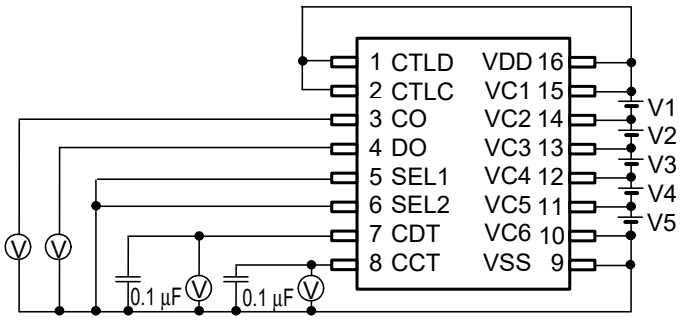


Figure 5 Test Circuit 2

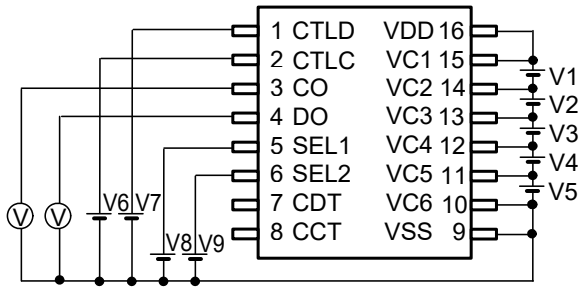


Figure 6 Test Circuit 3

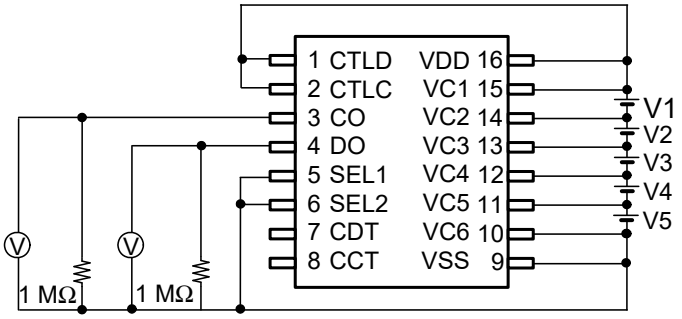


Figure 7 Test Circuit 4

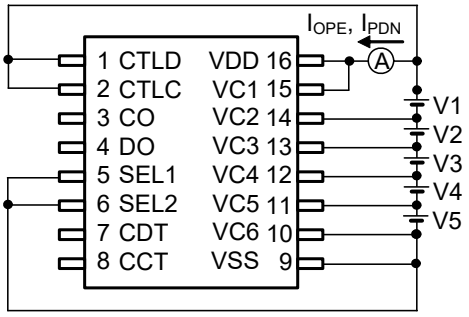


Figure 8 Test Circuit 5

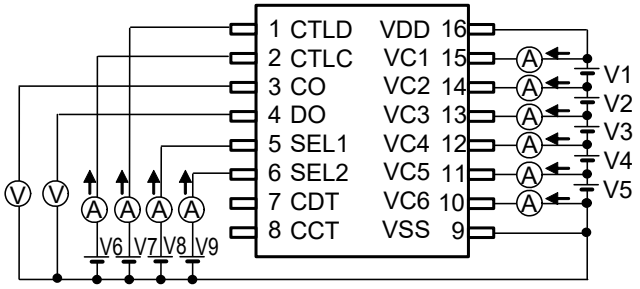


Figure 9 Test Circuit 6

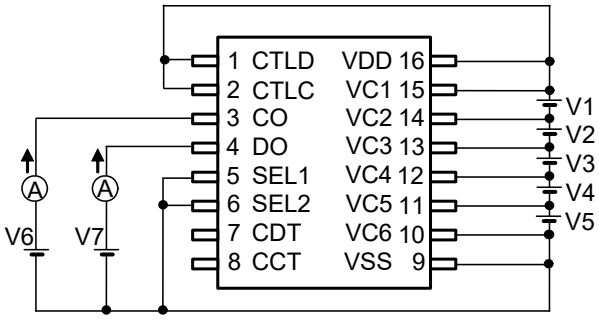


Figure 10 Test Circuit 7

■ Operation

Remark Refer to "■ **Connection Examples of Battery Monitoring IC**".

1. Normal status

When the voltage of each of the batteries is in the range from overcharge detection voltage (V_{CUn}) to overdischarge detection voltage (V_{DLn}), and the CTLC pin input voltage (V_{CTLC}) and the CTLD pin input voltage (V_{CTLD}) are higher than the CTLC pin voltage "H" (V_{CTLCH}) and the CTLD pin voltage "H" (V_{CTLDH}), respectively, the S-8225A Series defines each of the CO pin output voltage (V_{CO}) and the DO pin output voltage (V_{DO}) as "H". This is called normal status.
V_{CO} is defined as the CO pin voltage "H" (V_{COH}) when it is "H". Similarly, V_{DO} is defined as the DO pin voltage "H" (V_{DOH}) when it is "H".

Caution When the battery is connected for the first time, the S-8225A Series returns to normal status if the voltage of each of the batteries is in the range from overcharge release voltage (V_{CLn}) to overdischarge release voltage (V_{DUn}).

2. Overcharge status

When the voltage of one of the batteries becomes V_{CUn} or higher, the CO pin output inverts and the S-8225A Series becomes detection status. This is called overcharge status.
When the voltage of each of the batteries becomes overcharge release voltage (V_{CLn}) or lower, the overcharge status is released and the S-8225A Series returns to normal status.

3. Overdischarge status

When the voltage of one of the batteries becomes V_{DLn} or lower, the DO pin output inverts and the S-8225A Series becomes detection status. This is called overdischarge status.
When the voltage of each of the batteries becomes overdischarge release voltage (V_{DUn}) or higher, the overdischarge status is released and the S-8225A Series returns to normal status.

4. CTLC pin and CTLD pin

The S-8225A Series has two pins to control.
The CTLC pin controls the output voltage from the CO pin; the CTLD pin controls the output voltage from the DO pin. Thus it is possible for users to control the output voltages from the CO pin and DO pin, respectively. These controls precede the battery protection circuit.

Table 6 Status Set by CTLC Pin

CTLC Pin	CO Pin
"H"*1	Normal status*4
Open*2	V_{SS}
"L"*3	V_{SS}

***1.** "H": CTLC ≥ V_{CTLCH}
***2.** Pulled down by I_{CTLCH}
***3.** "L": CTLC ≤ V_{CTLCL}
***4.** The status is controlled by the voltage detection circuit.

Table 7 Status Set by CTLD Pin

CTLD Pin	DO Pin
"H"*1	Normal status*4
Open*2	V_{SS}
"L"*3	V_{SS}

***1.** "H": CTLD ≥ V_{CTLDH}
***2.** Pulled down by I_{CTLDH}
***3.** "L": CTLD ≤ V_{CTLDL}
***4.** The status is controlled by the voltage detection circuit.

Caution When the power supply fluctuates, unexpected behavior might occur if an electrical potential is generated between the potentials of "H" level input to the CTLC / CTLD pins and IC's V_{DD} by external filters.

5. 0 V battery detection function

In the S-8225A Series, users are able to select a 0 V battery detection function.
If this optional function is selected, the CO pin becomes detection status when the voltage of one of the batteries becomes 0 V battery detection voltage (V_{0INHn}) or lower.

6. Delay time setting

When the voltage of one of the batteries becomes V_{CUn} or higher, the S-8225A Series charges the capacitor connected to the CCT pin rapidly up to the CCT pin voltage (V_{CCT}). After that, The S-8225A Series discharges the capacitor with the constant current of 100 nA, and the CO pin output is defined as detection status at the time when the CCT pin voltage falls to a certain level or lower. The overcharge detection delay time (t_{CU}) changes depending on the capacitor connected to the CCT pin.
t_{CU} is calculated by the following formula.

Min. Typ. Max.

$$t_{CU}\ [s] = (6.7, 10, 13.3) \times C_{CCT}\ [\mu F]$$

Similarly, the overdischarge detection delay time (t_{DL}) changes depending on the capacitor connected to the CDT pin.
t_{DL} is calculated by the following formula.

Min. Typ. Max.

$$t_{DL}\ [s] = (6.7, 10, 13.3) \times C_{CDT}\ [\mu F]$$

Since the S-8225A Series charges the capacitor for delay rapidly, the voltage of the CCT pin and the CDT pin becomes large if the capacitance value is small. As a result, a variation between the calculated value of the delay time and the actual delay time is generated.
If the capacitance value is so large that the rapid charging can not be finished within the internal delay time, the output pin becomes detection status simultaneously with the end of internal delay time.
In addition, the charging current to the capacitor for delay passes through the VDD pin. Therefore, a large resistor connected to the VDD pin results in a big drop of the power supply voltage at the time of rapid charging which causes malfunction.
Regarding the recommended values for external components, refer to "**Table 9 Constants for External Components**".

7. SEL pin

In the S-8225A Series, switchable monitoring control between 3-cell to 5-cell is possible by using the SEL1 pin and the SEL2 pin. For example, since the overdischarge detection of V4 or V5 is prohibited and the overdischarge is not detected even if V4 or V5 is shorted when the SEL1 pin is "H" and the SEL2 pin is "L", the S-8225A Series can be used for 3-cell monitoring.
Be sure to use the SEL1 pin and the SEL2 pin at "H" or "L" potential.

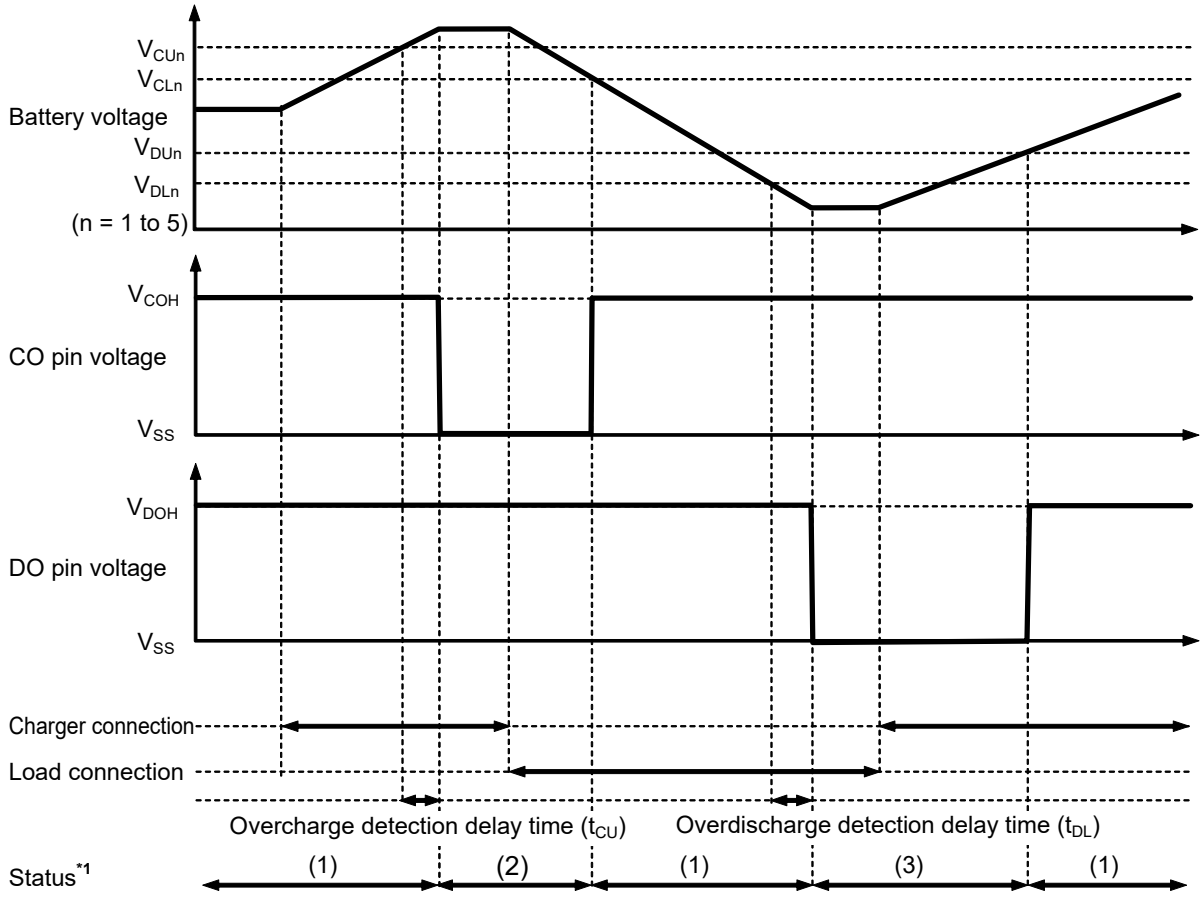
Table 8 Settings of SEL1 Pin and SEL2 Pin

SEL1 pin	SEL2 pin	Setting
"H"*1	"H"*1	Prohibition
"H"*1	"L"*2	3-cell monitoring
"L"*2	"H"*1	4-cell monitoring
"L"*2	"L"*2	5-cell monitoring

***1.** "H": SEL1 ≥ V_{SELH1} and SEL2 ≥ V_{SELH2}
***2.** "L": SEL1 ≤ V_{SELL1} and SEL2 ≤ V_{SELL2}

■ Timing Charts

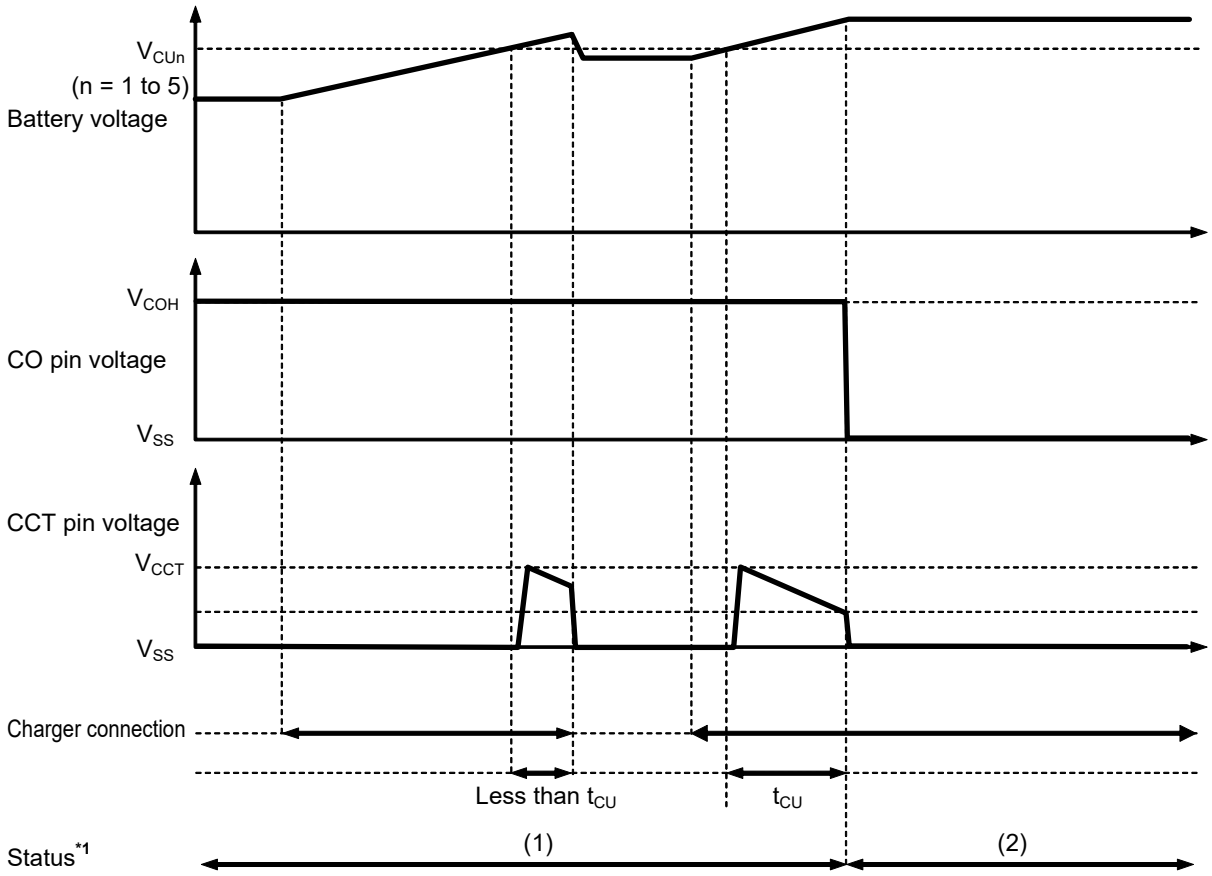
1. Overcharge detection and overdischarge detection



***1.** (1): Normal status
(2): Overcharge status
(3): Overdischarge status

Figure 11

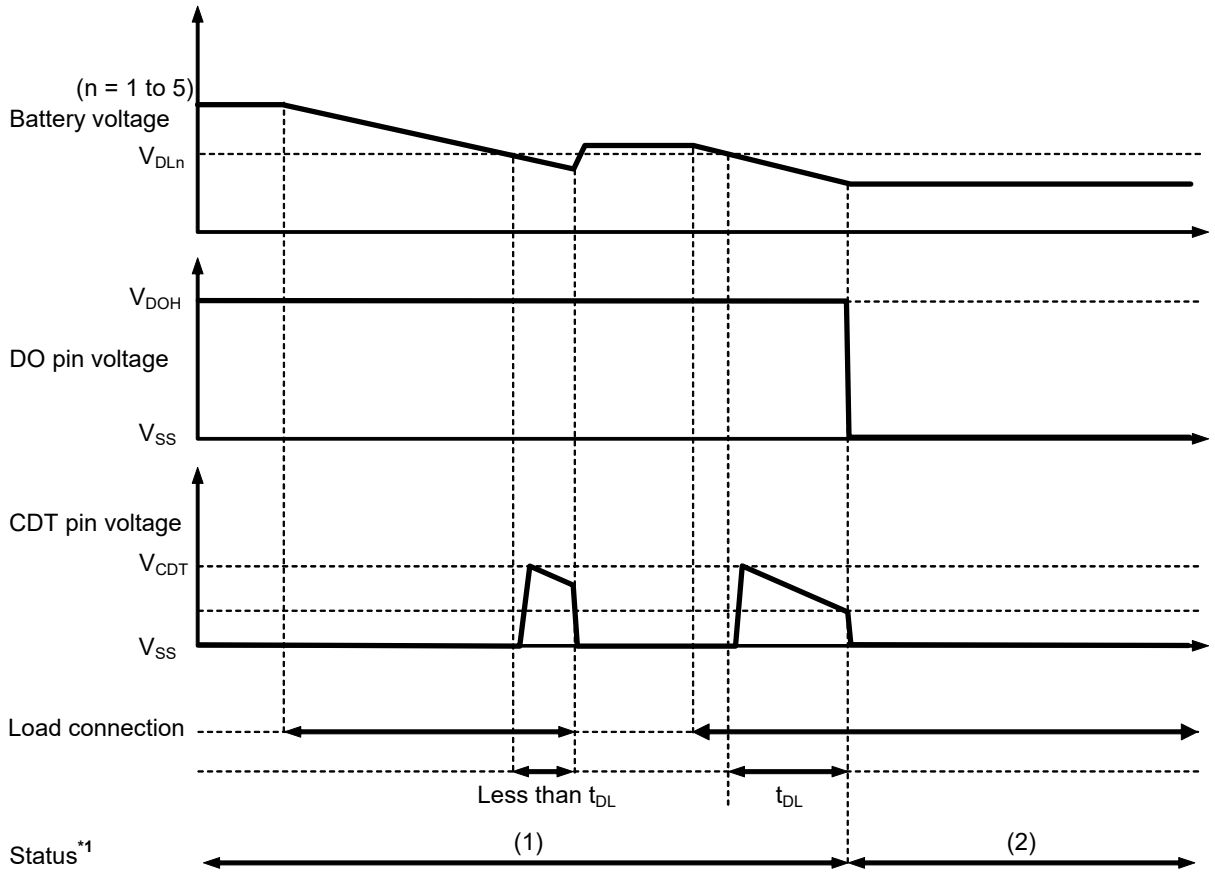
2. Overcharge detection delay



***1.** (1): Normal status
(2): Overcharge status

Figure 12

3. Overdischarge detection delay

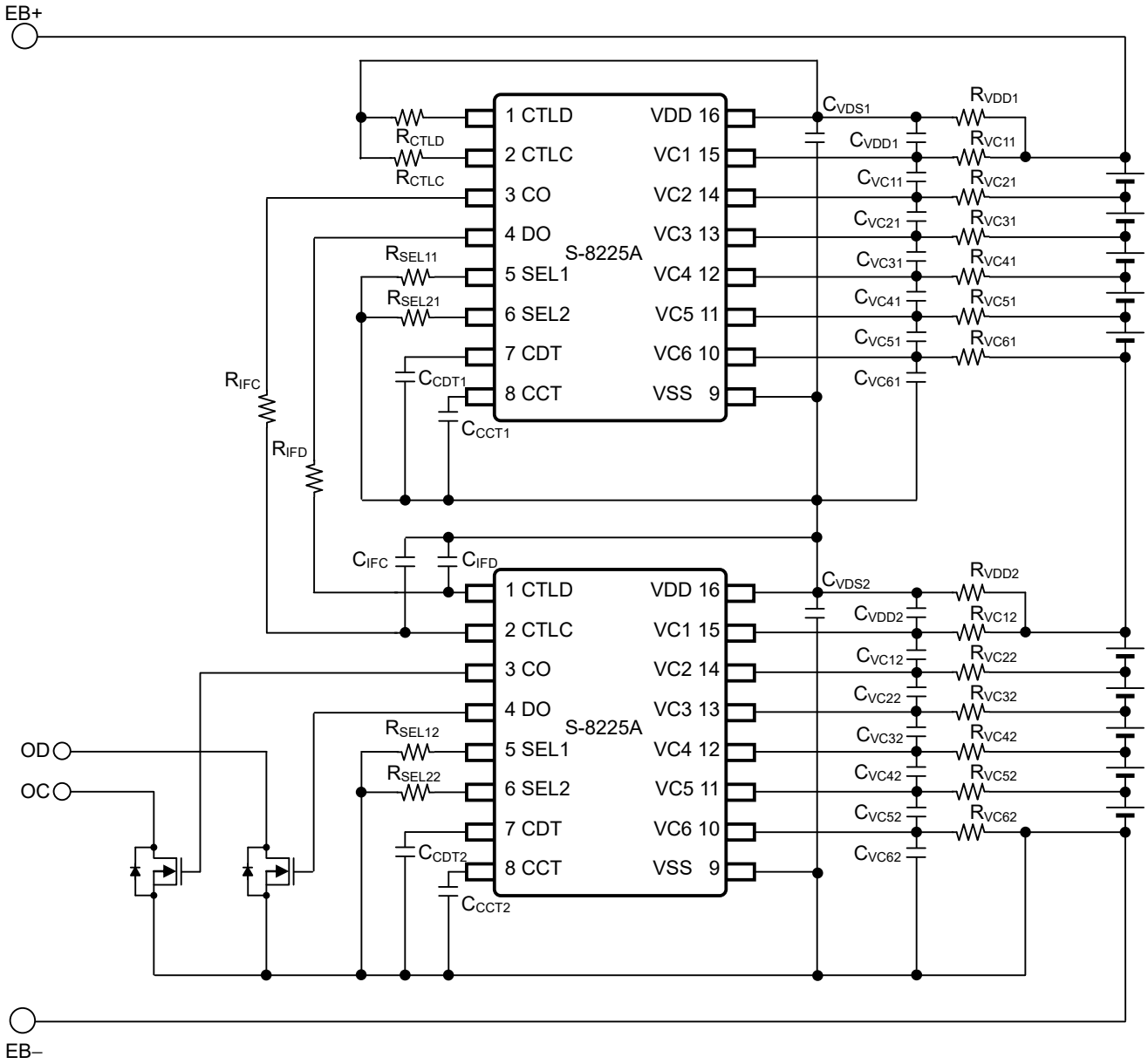


***1.** (1): Normal status
(2): Overdischarge status

Figure 13

■ Connection Examples of Battery Monitoring IC

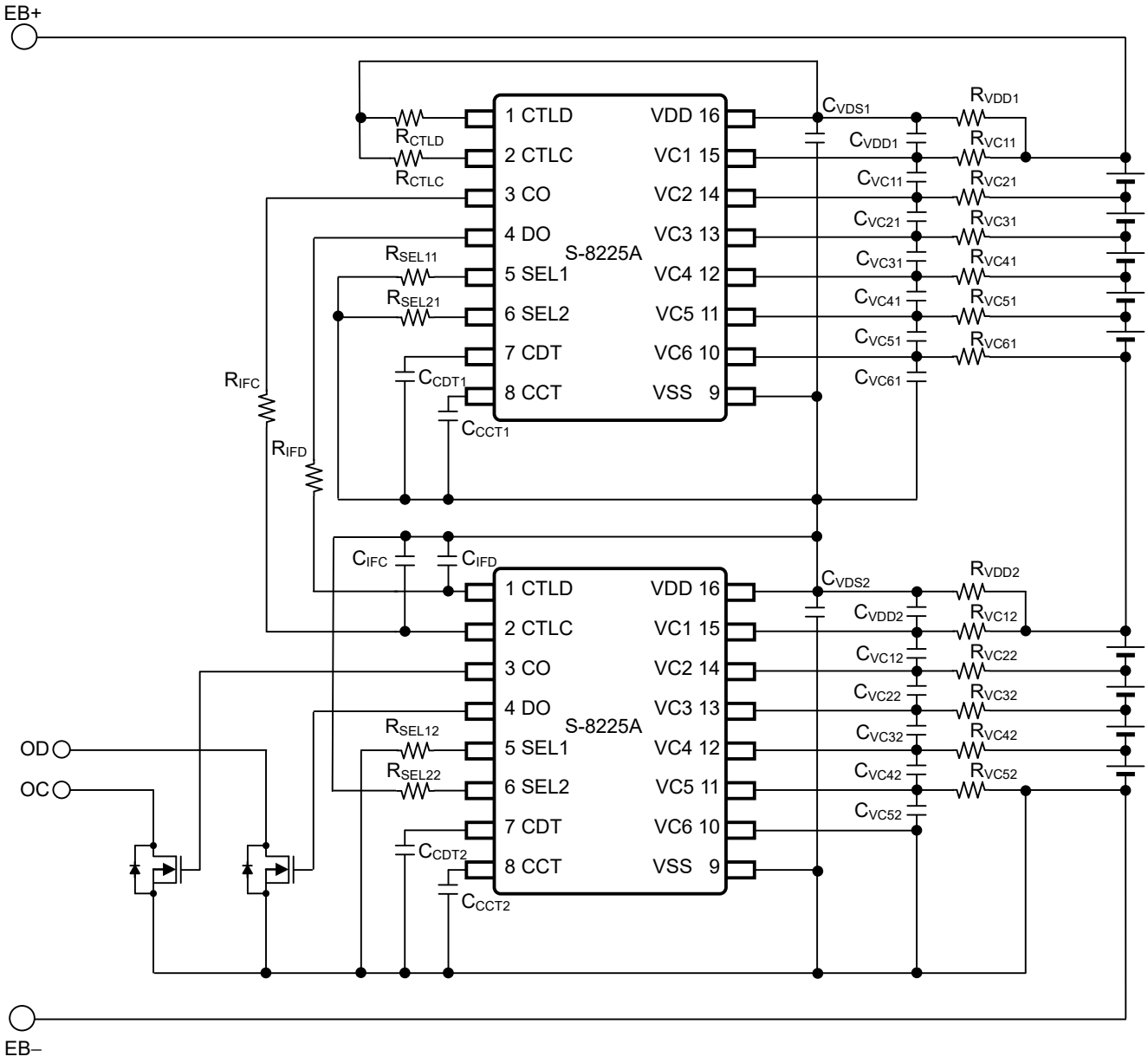
1. 10-serial cell



Remark Regarding the recommended values for external components, refer to "**Table 9 Constants for External Components**".

Figure 14

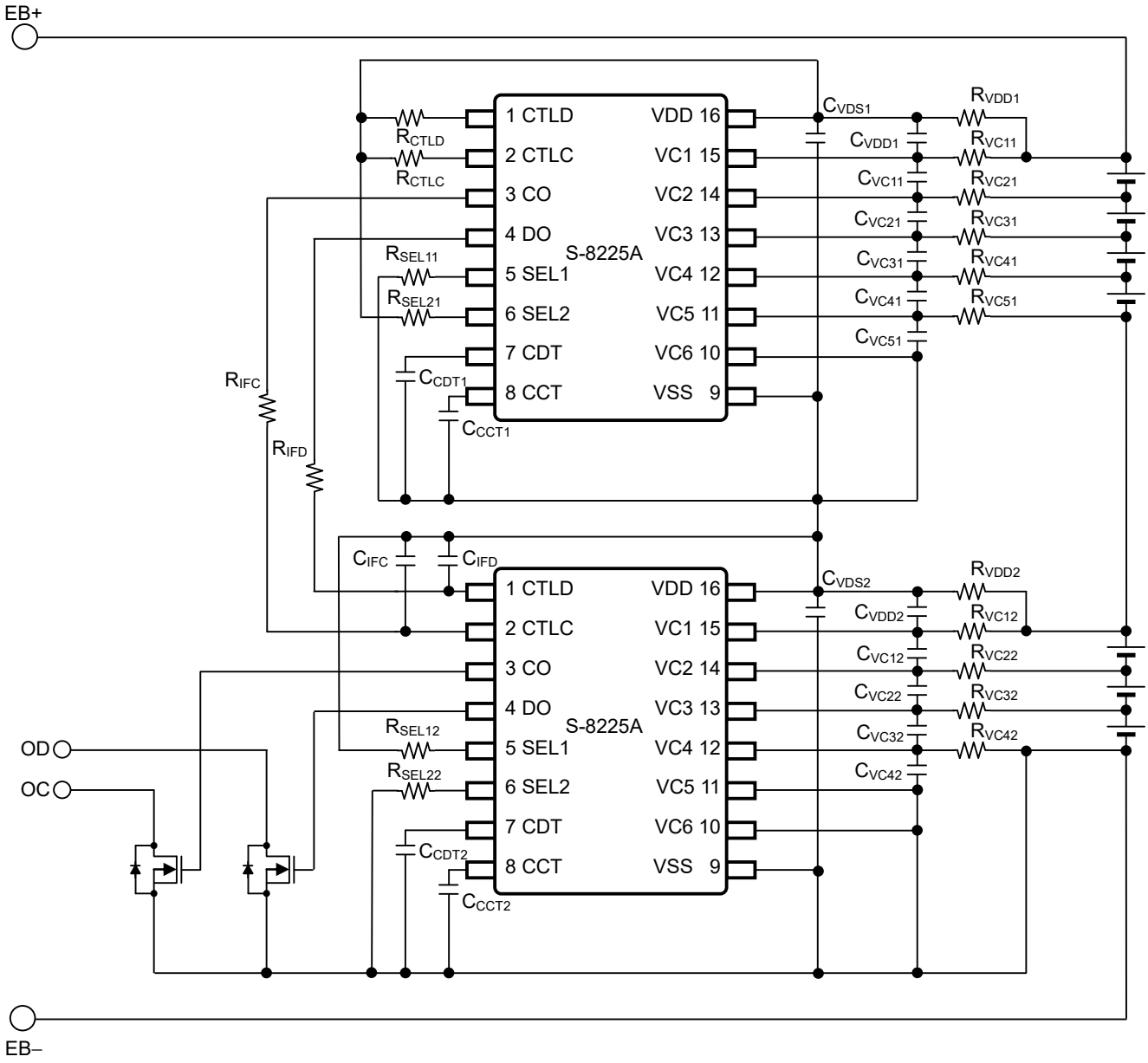
2. 9-serial cell



Remark Regarding the recommended values for external components, refer to "**Table 9 Constants for External Components**".

Figure 15

3. 7-serial cell



Remark Regarding the recommended values for external components, refer to "**Table 9 Constants for External Components**".

Figure 16

Table 9 Constants for External Components

Symbol	Min.	Typ.	Max.	Unit
R_{VDD1}, R_{VDD2}	50	100	1000	Ω
R_{VCn1}, R_{VCn2}	0.5	1	2	kΩ
C_{VDS1}, C_{VDS2}	0.01	0.1	1	μF
C_{VDD1}, C_{VDD2}	–	0	1	μF
C_{VCn1}, C_{VCn2}	0.01	0.1	1	μF
C_{CCT1}, C_{CCT2}	0.001	0.1	0.22	μF
C_{CDT1}, C_{CDT2}	0.001	0.1	0.22	μF
R_{IFC}, R_{IFD}	–	5.1	–	MΩ
C_{IFC}, C_{IFD}	–	1000	–	pF
R_{CTLC}, R_{CTLD}	–	1	–	kΩ
R_{SEL11}, R_{SEL21}	0.5	1	–	kΩ
R_{SEL12}, R_{SEL22}	0.5	1	–	kΩ

Caution 1. The constants may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the connection examples. In addition, the connection examples and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.

3. R_{VC1} to R_{VC6} and C_{VC1} to C_{VC6} should be the same constant, respectively.

4. Set up R_{VCn} and C_{VCn} as $R_{VCn} \times C_{VCn} \geq 50 \times 10^{-6}$.

5. Set up R_{VDD} and C_{VDS} as $5 \times 10^{-6} \leq R_{VDD} \times C_{VDS} \leq 100 \times 10^{-6}$.

6. Set $(R_{VDD} \times C_{VDS}) / (R_{VCn} \times C_{VCn}) = 0.1$.

Remark n = 1 to 6

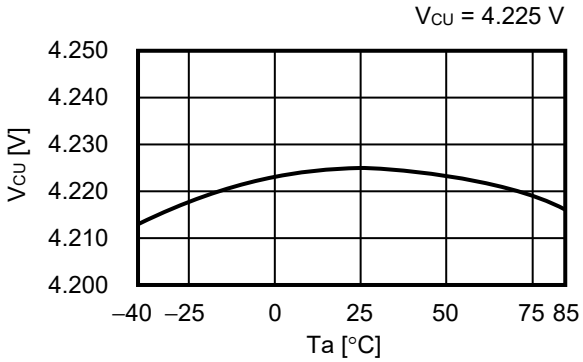
■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- If both an overcharge battery and an overdischarge battery are included among the whole batteries, the condition is set in overcharge status and overdischarge status. Therefore either charging or discharging is impossible.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

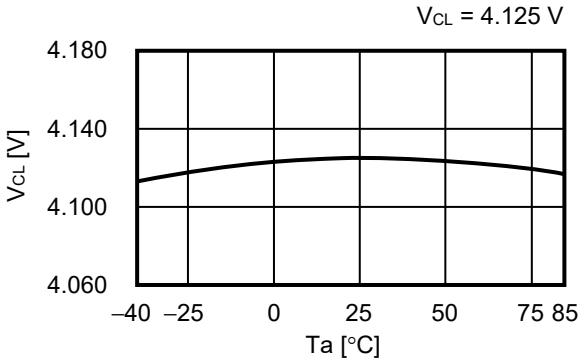
■ Characteristics (Typical Data)

1. Detection voltage

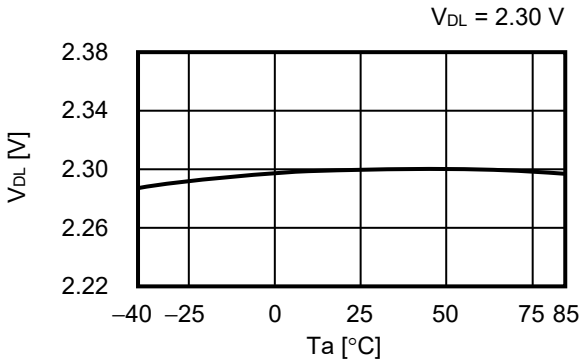
1. 1 V_{CU} vs. Ta



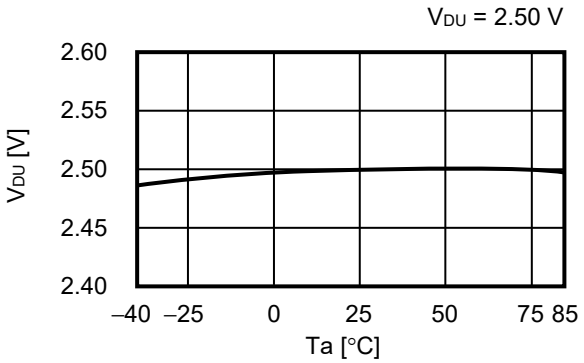
1. 2 V_{CL} vs. Ta



1. 3 V_{DL} vs. Ta

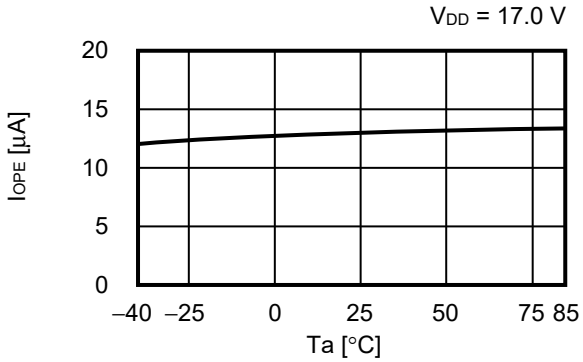


1. 4 V_{DU} vs. Ta

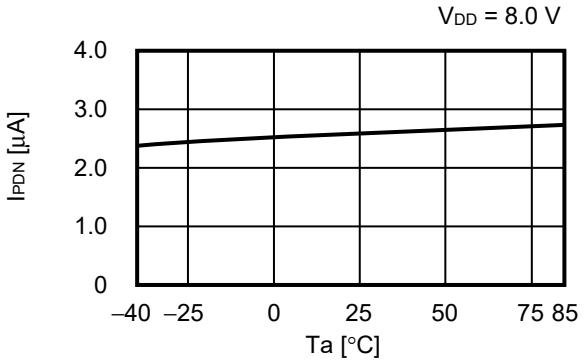


2. Current consumption

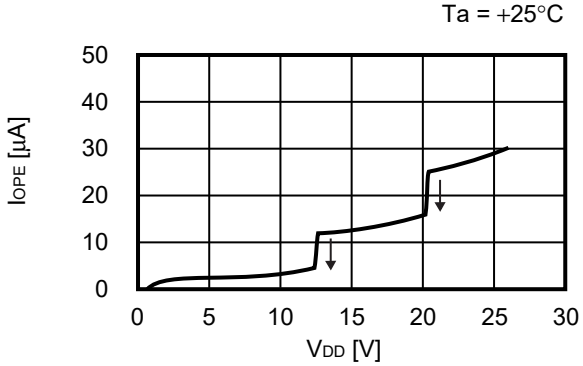
2. 1 I_{OPE} vs. Ta



2. 2 I_{PDN} vs. Ta

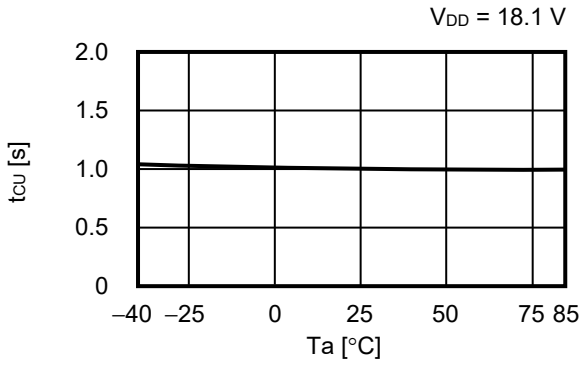


2. 3 I_{OPE} vs. V_{DD}

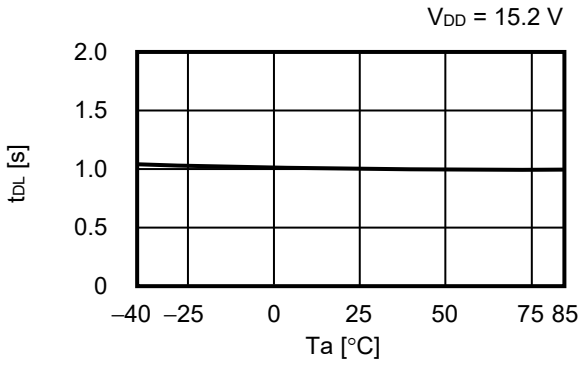


3. Delay time

3. 1 t_{CU} vs. Ta

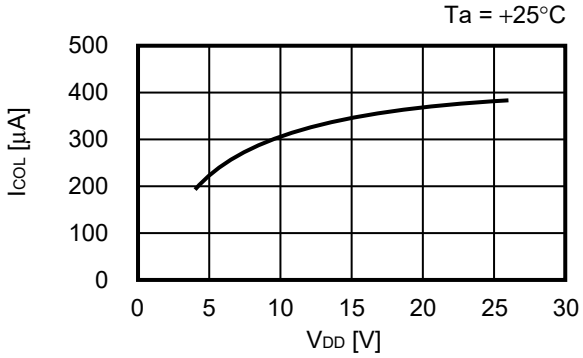


3. 2 t_{DL} vs. Ta

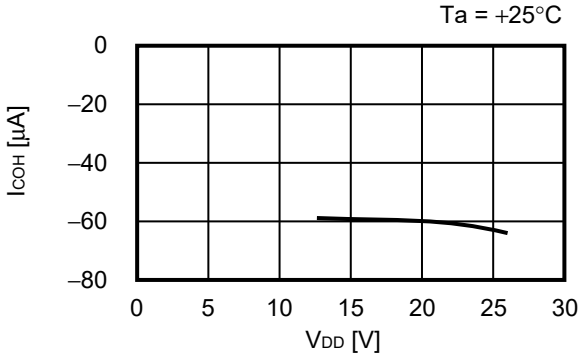


4. Output current

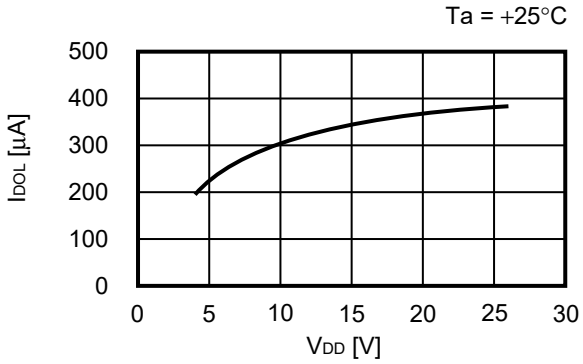
4. 1 I_{COL} vs. V_{DD}



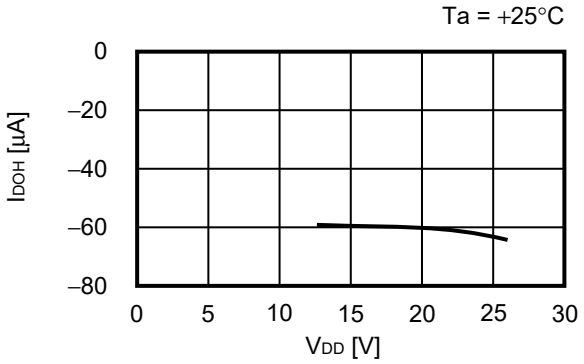
4. 2 I_{COH} vs. V_{DD}



4. 3 I_{DOL} vs. V_{DD}

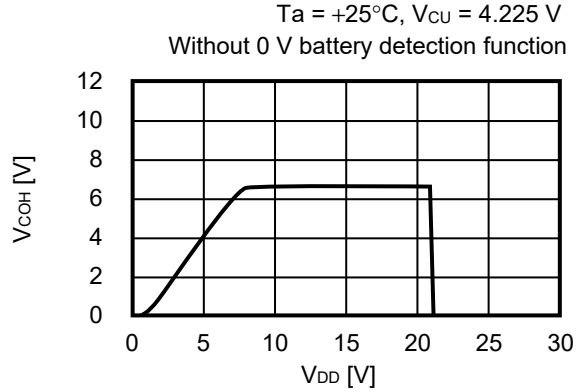


4. 4 I_{DOH} vs. V_{DD}

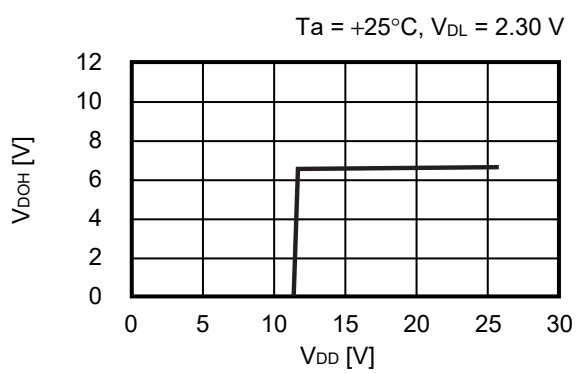


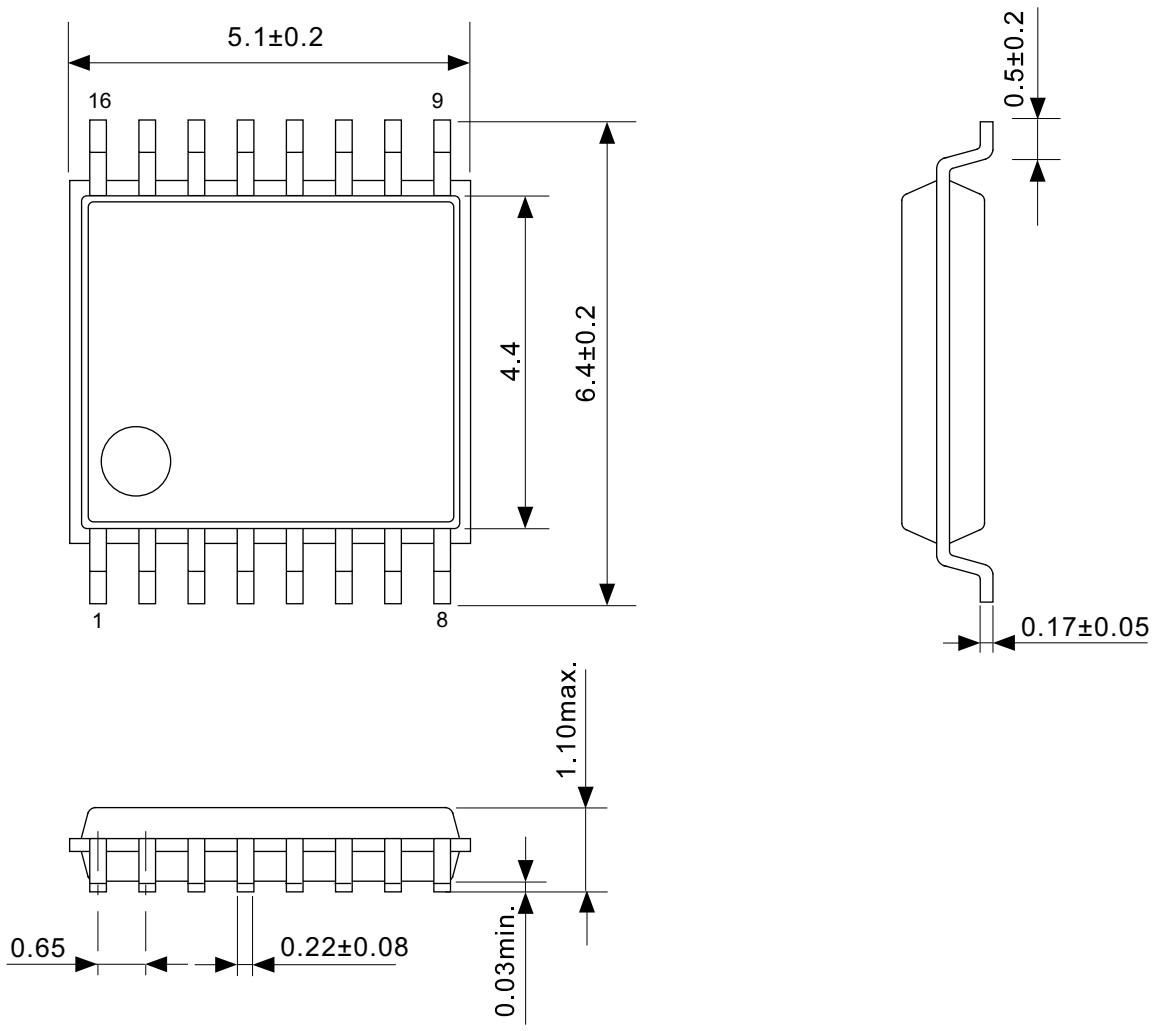
5. Output voltage

5. 1 V_{COH} vs. V_{DD}



5. 2 V_{DOH} vs. V_{DD}

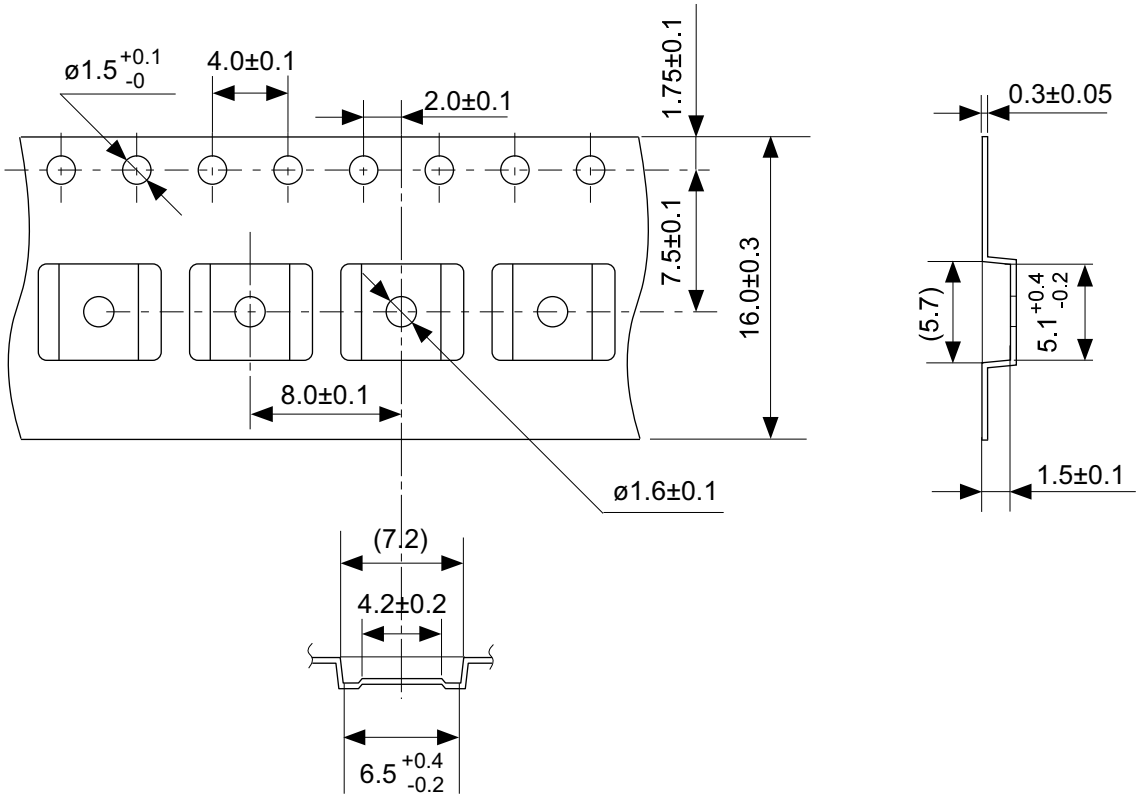


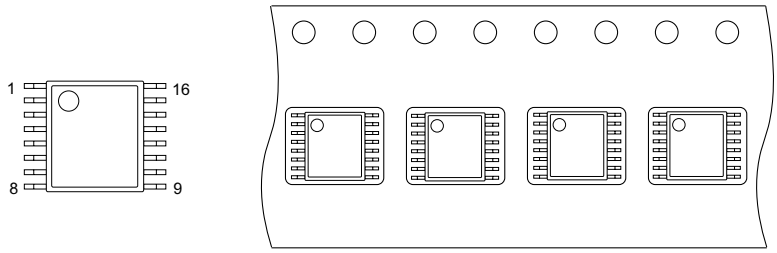


No. FT016-A-P-SD-1.2

TITLE	TSSOP16-A-PKG Dimensions
No.	FT016-A-P-SD-1.2
ANGLE	
UNIT	mm

ABLIC Inc.



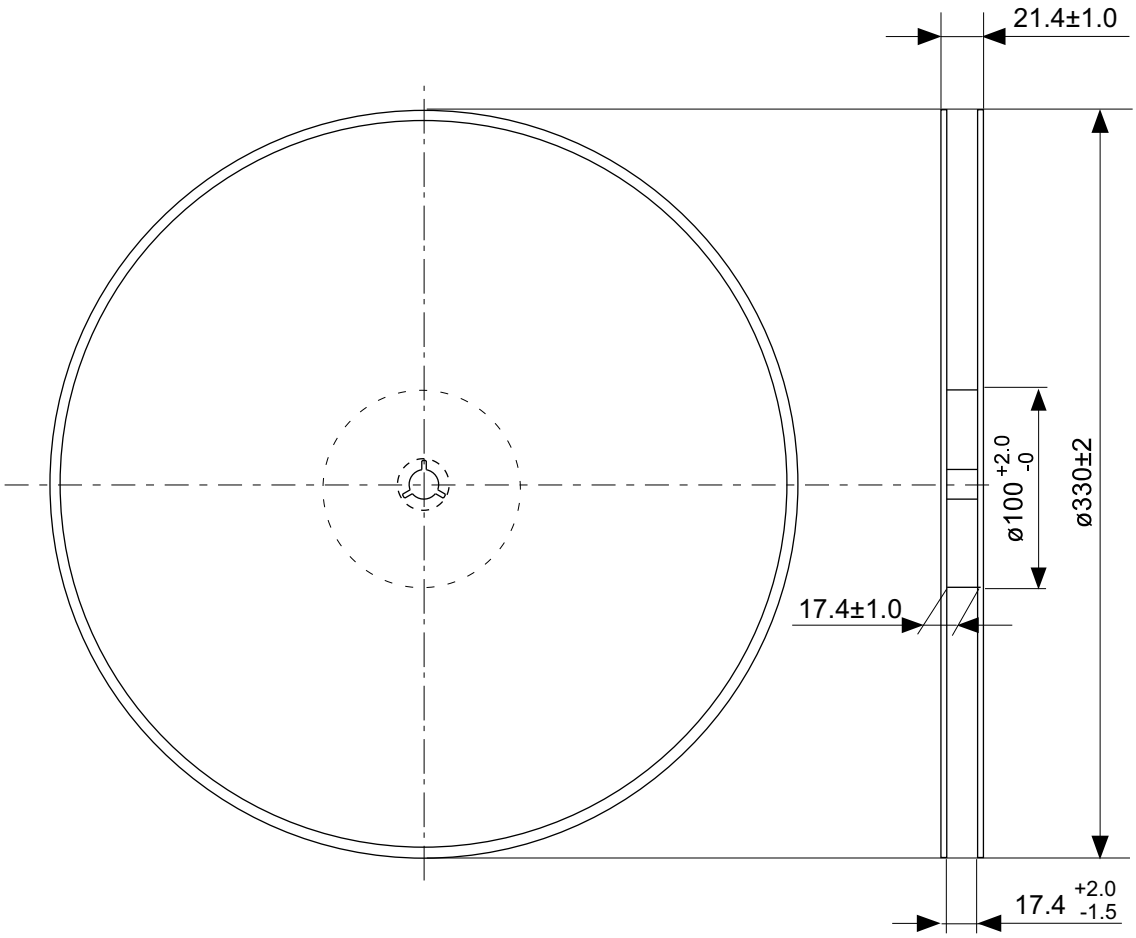


Feed direction

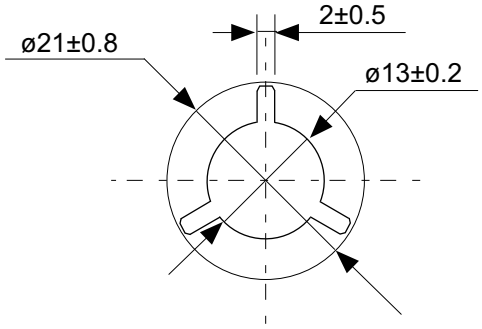
No. FT016-A-C-SD-1.1

TITLE	TSSOP16-A-Carrier Tape
No.	FT016-A-C-SD-1.1
ANGLE	
UNIT	mm

ABLIC Inc.



Enlarged drawing in the central part



No. FT016-A-R-S1-1.0

TITLE	TSSOP16-A- Reel		
No.	FT016-A-R-S1-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
	ABLIC Inc.		

Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the incorrect information described herein.
4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.
5. Before using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc. The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party is strictly prohibited without the express permission of ABLIC Inc.
14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

2.4-2019.07

ENTEGRECİ

Bu belge www.entegreci.com üzerinden sunulmaktadır.

Elektronik komponent tedarikinde Entegreci

Entegreci, Eskişehir merkezli, Türkiye geneline satış yapan bir elektronik komponent mağazasıdır. Entegreler (IC), mikrodenetleyiciler, transistörler, diyotlar, pasif elemanlar, konnektörler, modüller ve geliştirme kartları tek adetten seri üretim adetlerine kadar satılır. Ürün sayfalarında güncel stok durumunu, fiyatı ve datasheet bağlantısını bulabilirsiniz.

Parça koduyla arama

Üretici parça numarasını yazın; stok ve fiyatı hemen görün.

www.entegreci.com

Ürün kategorileri

Entegreden kapasitöre tüm elektronik komponent kategorileri.

Kategorilere göz atın

Üreticiler

Aradığınız üreticinin ürünlerini tek sayfada inceleyin.

Üreticileri görün

Toplu alım ve teklif

Listede olmayan ya da yüksek adetli parçalar için teklif isteyin.

Teklif isteyin

www.entegreci.com | **destek@entegreci.com** | **0850 305 90 34**

Entegreci is an online electronic components store based in Türkiye. Search by manufacturer part number to see stock, prices and datasheets for integrated circuits, microcontrollers, transistors, passive components and connectors, or request a quote for parts that are not listed.

Bu sayfa Entegreci tarafından eklenmiştir. Belgenin önceki sayfaları asıl yayıncısına aittir ve içeriği değiştirilmemiştir; en güncel sürüm için belgenin yayıncısına başvurun.