S-8211D Series

BATTERY PROTECTION IC FOR 1-CELL PACK

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The S-8211D Series is a protection IC for 1-cell lithium-ion / lithium-polymer rechargeable battery and includes high-accuracy voltage detection circuits and delay circuits.
The S-8211D Series is suitable for protecting 1-cell rechargeable lithium-ion / lithium-polymer battery packs from overcharge, overdischarge, and overcurrent.

NOT RECOMMENDED FOR NEW DESIGN

■ Features

- High-accuracy voltage detection circuit

Overcharge detection voltage	3.6 V to 4.5 V (5 mV step)	Accuracy ±25 mV (Ta = +25°C) Accuracy ±30 mV (Ta = –5°C to +55°C)
Overcharge release voltage	3.5 V to 4.4 V*1	Accuracy ±50 mV
Overdischarge detection voltage	2.0 V to 3.0 V (10 mV step)	Accuracy ±50 mV
Overdischarge release voltage	2.0 V to 3.4 V*2	Accuracy ±100 mV
Discharge overcurrent detection voltage	0.05 V to 0.30 V (10 mV step)	Accuracy ±15 mV
Load short-circuiting detection voltage	0.5 V (fixed)	Accuracy ±200 mV

- Detection delay times are generated only by an internal circuit (external capacitors are unnecessary). Accuracy ±20%
- High-withstand voltage (VM pin and CO pin: Absolute maximum rating = 28 V)
- 0 V battery charge function "available" / "unavailable" is selectable.
- Power-down function "available" / "unavailable" is selectable.
- Wide operation temperature range Ta = –40°C to +85°C
- Low current consumption

During operation	3.0 µA typ., 5.5 µA max. (Ta = +25°C)
During power-down	0.2 µA max. (Ta = +25°C)

- Lead-free, Sn 100%, halogen-free*3

*1. Overcharge release voltage = Overcharge detection voltage – Overcharge hysteresis voltage
(Overcharge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.4 V in 50 mV step.)
*2. Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage
(Overdischarge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.7 V in 100 mV step.)
*3. Refer to "■ **Product Name Structure**" for details.

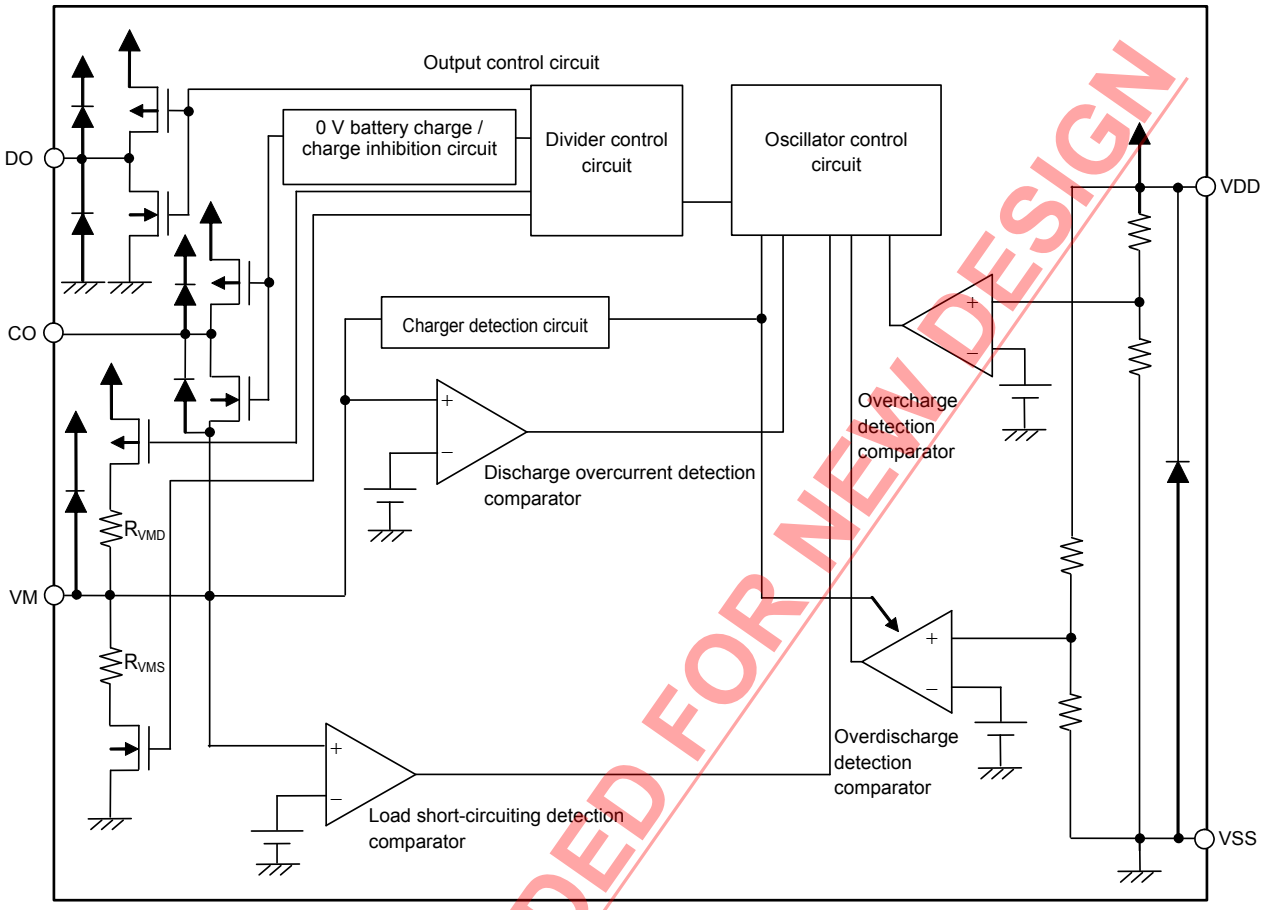
■ Applications

- Lithium-ion rechargeable battery pack
- Lithium-polymer rechargeable battery pack

■ Packages

- SOT-23-5
- SNT-6A

■ Block Diagram



Remark All diodes shown in figure are parasitic diodes.

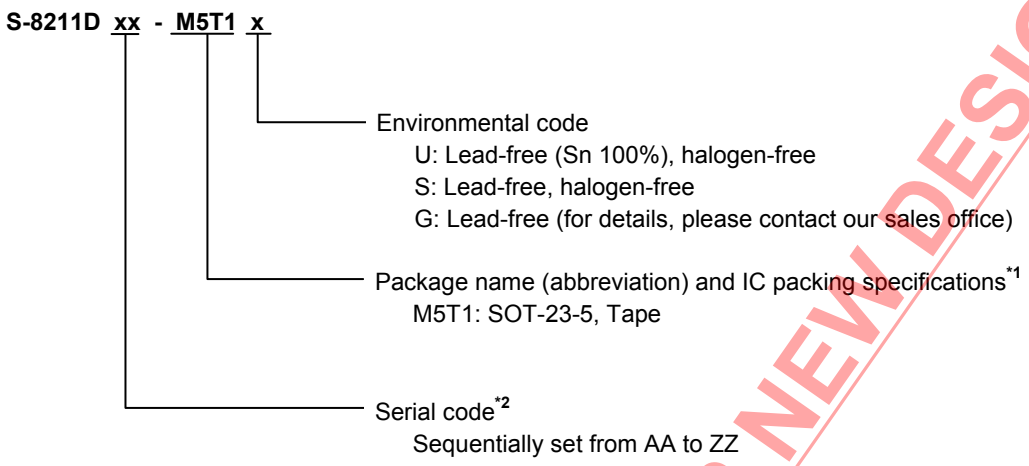
Figure 1

NOT RECOMMENDED FOR NEW DESIGN

■ Product Name Structure

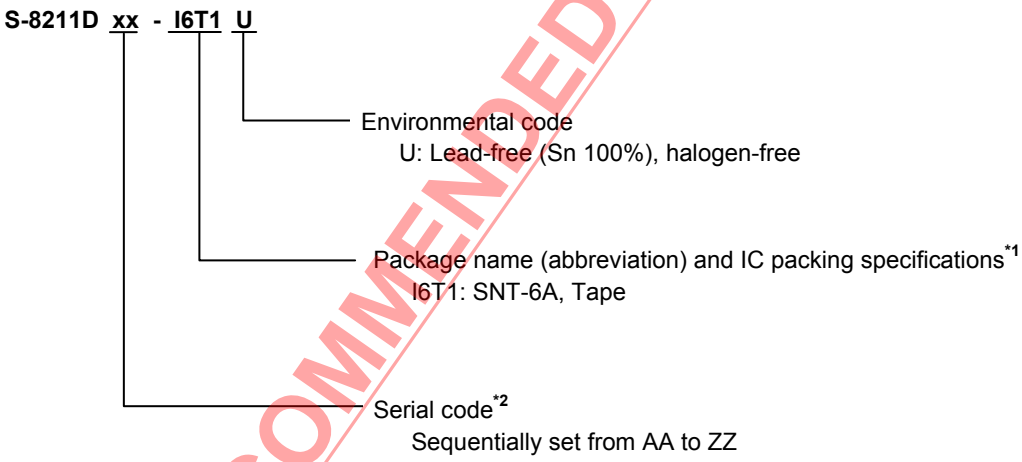
1. Product name

1. 1 SOT-23-5



***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

1. 2 SNT-6A



***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

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2. Packages

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SOT-23-5	MP005-A-P-SD	MP005-A-C-SD	MP005-A-R-SD	–
SNT-6A	PG006-A-P-SD	PG006-A-C-SD	PG006-A-R-SD	PG006-A-L-SD

3. Product name list

3. 1 SOT-23-5

Table 2

Product Name	Over-charge Detection Voltage [V_{CU}]	Over-charge Release Voltage [V_{CL}]	Over-discharge Detection Voltage [V_{DL}]	Over-discharge Release Voltage [V_{DU}]	Discharge Overcurrent Detection Voltage [V_{DIOV}]	0 V Battery Charge Function	Delay Time Combination*1	Power-down Function
S-8211DAD-M5T1x	4.280 V	4.180 V	2.50 V	2.80 V	0.19 V	Unavailable	(1)	Available
S-8211DAE-M5T1x	4.280 V	4.180 V	2.50 V	2.70 V	0.19 V	Unavailable	(1)	Available
S-8211DAH-M5T1x	4.275 V	4.175 V	2.30 V	2.40 V	0.10 V	Available	(1)	Available
S-8211DAI-M5T1x	4.325 V	4.075 V	2.50 V	2.90 V	0.15 V	Unavailable	(1)	Available
S-8211DAJ-M5T1x	4.280 V	4.080 V	3.00 V	3.00 V	0.08 V	Available	(1)	Available
S-8211DAK-M5T1x	4.280 V	4.080 V	2.30 V	2.30 V	0.13 V	Unavailable	(1)	Available
S-8211DAL-M5T1x	4.280 V	4.080 V	2.80 V	2.80 V	0.10 V	Available	(1)	Available
S-8211DAM-M5T1x	4.275 V	4.075 V	2.50 V	2.90 V	0.15 V	Unavailable	(1)	Available
S-8211DAR-M5T1x	3.600 V	3.600 V	2.00 V	2.30 V	0.15 V	Available	(1)	Available
S-8211DAS-M5T1x	3.600 V	3.500 V	2.50 V	2.80 V	0.10 V	Available	(1)	Available
S-8211DAU-M5T1y	3.650 V	3.550 V	2.50 V	2.80 V	0.15 V	Available	(1)	Available
S-8211DAV-M5T1y	3.700 V	3.600 V	2.50 V	2.80 V	0.05 V	Available	(1)	Available
S-8211DAW-M5T1y	3.800 V	3.700 V	2.50 V	2.80 V	0.10 V	Available	(1)	Available
S-8211DBB-M5T1U	4.350 V	4.150 V	2.10 V	2.20 V	0.26 V	Unavailable	(1)	Available
S-8211DBD-M5T1U	4.350 V	4.150 V	2.10 V	2.20 V	0.11 V	Unavailable	(1)	Available
S-8211DBE-M5T1U	4.350 V	4.150 V	2.10 V	2.20 V	0.14 V	Unavailable	(1)	Available
S-8211DBF-M5T1U	4.230 V	4.080 V	3.00 V	3.10 V	0.15 V	Unavailable	(1)	Available
S-8211DBG-M5T1U	4.250 V	4.050 V	2.70 V	3.00 V	0.20 V	Unavailable	(1)	Available

***1.** Refer to **Table 4** about the details of the delay time combinations (1).

Remark 1. Please contact our sales office for the products with detection voltage value other than those specified above.
2. x: G or U
y: S or U
3. Please select products of environmental code = U for Sn 100%, halogen-free products.

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3. 2 SNT-6A

Table 3

Product Name	Over-charge Detection Voltage [V_{CU}]	Over-charge Release Voltage [V_{CL}]	Over-discharge Detection Voltage [V_{DL}]	Over-discharge Release Voltage [V_{DU}]	Discharge Overcurrent Detection Voltage [V_{DIOV}]	0 V Battery Charge Function	Delay Time Combination *1	Power-down Function
S-8211DAD-I6T1U	4.280 V	4.180 V	2.50 V	2.80 V	0.19 V	Unavailable	(1)	Available
S-8211DAE-I6T1U	4.280 V	4.180 V	2.50 V	2.70 V	0.19 V	Unavailable	(1)	Available
S-8211DAF-I6T1U	4.250 V	4.050 V	2.40 V	2.90 V	0.10 V	Available	(2)	Unavailable
S-8211DAG-I6T1U	4.280 V	4.080 V	2.30 V	2.30 V	0.08 V	Available	(1)	Unavailable
S-8211DAI-I6T1U	4.325 V	4.075 V	2.50 V	2.90 V	0.15 V	Unavailable	(1)	Available
S-8211DAN-I6T1U	4.280 V	4.080 V	2.30 V	3.00 V	0.10 V	Unavailable	(3)	Available
S-8211DAQ-I6T1U	4.280 V	4.080 V	2.30 V	2.30 V	0.10 V	Unavailable	(3)	Available
S-8211DAT-I6T1U	4.280 V	4.080 V	2.70 V	2.70 V	0.08 V	Unavailable	(3)	Available
S-8211DAX-I6T1U	4.280 V	4.080 V	2.00 V	2.00 V	0.11 V	Unavailable	(3)	Available
S-8211DAY-I6T1U	3.900 V	3.900 V	2.00 V	2.30 V	0.15 V	Available	(1)	Available
S-8211DAZ-I6T1U	3.800 V	3.500 V	2.40 V	2.70 V	0.07 V	Available	(1)	Available
S-8211DBA-I6T1U	4.000 V	3.900 V	2.35 V	2.65 V	0.10 V	Available	(1)	Available
S-8211DBC-I6T1U	4.250 V	4.150 V	3.00 V	3.10 V	0.20 V	Unavailable	(1)	Available

***1.** Refer to **Table 4** about the details of the delay time combinations (1) to (3).

Remark Please contact our sales office for the products with detection voltage value other than those specified above.

Table 4

Delay Time Combination	Overcharge Detection Delay Time [t_{CU}]	Overdischarge Detection Delay Time [t_{DL}]	Discharge Overcurrent Detection Delay Time [t_{DIOV}]	Load Short-circuiting Detection Delay Time [t_{SHORT}]
(1)	1.2 s	150 ms	9 ms	300 µs
(2)	1.2 s	75 ms	9 ms	300 µs
(3)	1.2 s	150 ms	18 ms	300 µs

Remark The delay times can be changed within the range listed **Table 5**. For details, please contact our sales office.

Table 5

Delay Time	Symbol	Selection Range			Remark
Overcharge detection delay time	t_{CU}	143 ms	573 ms	1.2 s *1	Select a value from the left.
Overdischarge detection delay time	t_{DL}	38 ms	150 ms *1	300 ms	Select a value from the left.
Discharge overcurrent detection delay time	t_{DIOV}	4.5 ms	9 ms *1	18 ms	Select a value from the left.
Load short-circuiting detection delay time	t_{SHORT}	–	300 µs *1	560 µs	Select a value from the left.

***1.** The value is the delay time of the standard products.

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■ Pin Configurations

1. SOT-23-5

Top view

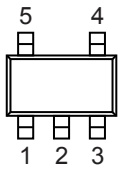

Figure 2

Table 6

Pin No.	Symbol	Description
1	VM	Voltage detection pin between VM pin and VSS pin (Overcurrent / charger detection pin)
2	VDD	Input pin for positive power supply
3	VSS	Input pin for negative power supply
4	DO	Connection pin of discharge control FET gate (CMOS output)
5	CO	Connection pin of charge control FET gate (CMOS output)

2. SNT-6A

Top view



Figure 3

Table 7

Pin No.	Symbol	Description
1	NC*1	No connection
2	CO	Connection pin of charge control FET gate (CMOS output)
3	DO	Connection pin of discharge control FET gate (CMOS output)
4	VSS	Input pin for negative power supply
5	VDD	Input pin for positive power supply
6	VM	Voltage detection pin between VM pin and VSS pin (Overcurrent / charger detection pin)

***1.** The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.

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■ Absolute Maximum Ratings

Table 8

(Ta = +25°C unless otherwise specified)

Item		Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin		V_{DS}	VDD	V_{SS} − 0.3 to V_{SS} + 12	V
VM pin input voltage		V_{VM}	VM	V_{DD} − 28 to V_{DD} + 0.3	V
DO pin output voltage		V_{DO}	DO	V_{SS} − 0.3 to V_{DD} + 0.3	V
CO pin output voltage		V_{CO}	CO	V_{VM} − 0.3 to V_{DD} + 0.3	V
Power dissipation	SOT-23-5	P_D	–	250 (When not mounted on board)	mW
			–	600[*1]	mW
	SNT-6A		–	400[*1]	mW
Operation ambient temperature		T_{opr}	–	−40 to +85	°C
Storage temperature		T_{stg}	–	−55 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name: JEDEC STANDARD51-7

Caution **The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

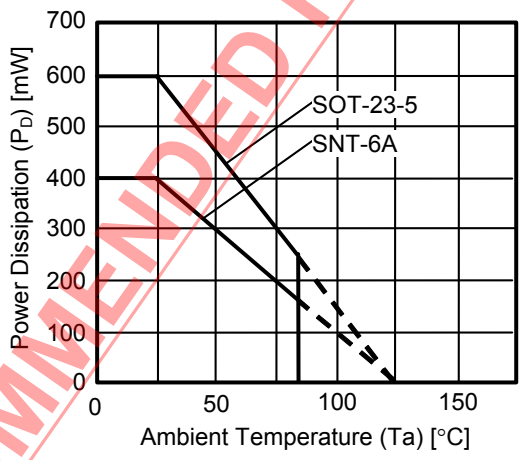

Figure 4 Power Dissipation of Package (When Mounted on Board)

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■ Electrical Characteristics

1. Except detection delay time (Ta = +25°C)

Table 9

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DETECTION VOLTAGE									
Overcharge detection voltage	V_{CU}	3.60 V to 4.50 V, adjustable		V_{CU} − 0.025	V_{CU}	V_{CU} + 0.025	V	1	1
		3.60 V to 4.50 V, adjustable, Ta = −5°C to +55°C*1		V_{CU} − 0.03	V_{CU}	V_{CU} + 0.03	V	1	1
Overcharge release voltage	V_{CL}	3.50 V to 4.40 V, adjustable	$V_{CL} \neq V_{CU}$	V_{CL} − 0.05	V_{CL}	V_{CL} + 0.05	V	1	1
			$V_{CL} = V_{CU}$	V_{CL} − 0.05	V_{CL}	V_{CL} + 0.025	V	1	1
Overdischarge detection voltage	V_{DL}	2.00 V to 3.00 V, adjustable		V_{DL} − 0.05	V_{DL}	V_{DL}+ 0.05	V	2	2
Overdischarge release voltage	V_{DU}	2.00 V to 3.40 V, Adjustable	$V_{DU} \neq V_{DL}$	V_{DU} − 0.10	V_{DU}	V_{DU} + 0.10	V	2	2
			$V_{DU} = V_{DL}$	V_{DU} − 0.05	V_{DU}	V_{DU} + 0.05	V	2	2
Discharge overcurrent detection voltage	V_{DIOV}	0.05 V to 0.30 V, adjustable		V_{DIOV} − 0.015	V_{DIOV}	V_{DIOV} + 0.015	V	3	2
Load short-circuiting detection voltage*2	V_{SHORT}	–		0.30	0.50	0.70	V	3	2
Charger detection voltage	V_{CHA}	–		−1.0	−0.7	−0.4	V	4	2
0 V BATTERY CHARGE FUNCTION									
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charge function "available"		1.2	–	–	V	10	2
0 V battery charge inhibition battery voltage	V_{0INH}	0 V battery charge function "unavailable"		–	–	0.5	V	11	2
INTERNAL RESISTANCE									
Resistance between VM pin and VDD pin	R_{VMD}	V_{DD} = 1.8 V, V_{VM} = 0 V		100	300	900	kΩ	5	3
Resistance between VM pin and VSS pin	R_{VMS}	V_{DD} = 3.5 V, V_{VM} = 1.0 V		10	20	40	kΩ	5	3
INPUT VOLTAGE									
Operation voltage between VDD pin and VSS pin	V_{DSOP1}	–		1.5	–	8	V	–	–
Operation voltage between VDD pin and VM pin	V_{DSOP2}	–		1.5	–	28	V	–	–
INPUT CURRENT (WITH POWER-DOWN FUNTION)									
Current consumption during operation	I_{OPE}	V_{DD} = 3.5 V, V_{VM} = 0 V		1.0	3.0	5.5	μA	4	2
Current consumption during power-down	I_{PDN}	V_{DD} = V_{VM} = 1.5 V		–	–	0.2	μA	4	2
INPUT CURRENT (WITHOUT POWER-DOWN FUNTION)									
Current consumption during operation	I_{OPE}	V_{DD} = 3.5 V, V_{VM} = 0 V		1.0	3.0	5.5	μA	4	2
Current consumption during overdischarge	I_{OPED}	V_{DD} = V_{VM} = 1.5 V		0.3	2.0	3.5	μA	4	2
OUTPUT RESISTANCE									
CO pin resistance "H"	R_{COH}	V_{CO} = 3.0 V, V_{DD} = 3.5 V, V_{VM} = 0 V		2.5	5	10	kΩ	6	4
CO pin resistance "L"	R_{COL}	V_{CO} = 0.5 V, V_{DD} = 4.5 V, V_{VM} = 0 V		2.5	5	10	kΩ	6	4
DO pin resistance "H"	R_{DOH}	V_{DO} = 3.0 V, V_{DD} = 3.5 V, V_{VM} = 0 V		2.5	5	10	kΩ	7	4
DO pin resistance "L"	R_{DOL}	V_{DO} = 0.5 V, V_{DD} = V_{VM} = 1.8 V		2.5	5	10	kΩ	7	4

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*1. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

*2. In any conditions, load short-circuiting detection voltage (V_{SHORT}) is higher than discharge overcurrent detection voltage (V_{DIOV}).

2. Except detection delay time (Ta = –40°C to +85°C[*1])

Table 10

(Ta = –40°C to +85°C[*1] unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DETECTION VOLTAGE									
Overcharge detection voltage	V_{CU}	3.60 V to 4.50 V, adjustable		V_{CU} – 0.060	V_{CU}	V_{CU} + 0.040	V	1	1
Overcharge release voltage	V_{CL}	3.50 V to 4.40 V, adjustable	$V_{CL} \neq V_{CU}$	V_{CL} – 0.08	V_{CL}	V_{CL} + 0.065	V	1	1
			$V_{CL} = V_{CU}$	V_{CL} – 0.08	V_{CL}	V_{CL} + 0.04	V	1	1
Overdischarge detection voltage	V_{DL}	2.00 V to 3.00 V, adjustable		V_{DL} – 0.11	V_{DL}	V_{DL} + 0.13	V	2	2
Overdischarge release voltage	V_{DU}	2.00 V to 3.40 V, adjustable	$V_{DU} \neq V_{DL}$	V_{DU} – 0.15	V_{DU}	V_{DU} + 0.19	V	2	2
			$V_{DU} = V_{DL}$	V_{DU} – 0.11	V_{DU}	V_{DU} + 0.13	V	2	2
Discharge overcurrent detection voltage	V_{DIOV}	0.05 V to 0.30 V, adjustable		V_{DIOV} – 0.021	V_{DIOV}	V_{DIOV} + 0.024	V	3	2
Load short-circuiting detection voltage[*2]	V_{SHORT}	–		0.16	0.50	0.84	V	3	2
Charger detection voltage	V_{CHA}	–		–1.2	–0.7	–0.2	V	4	2
0 V BATTERY CHARGE FUNCTION									
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charge function "available"		1.7	–	–	V	10	2
0 V battery charge inhibition battery voltage	V_{0INH}	0 V battery charge function "unavailable"		–	–	0.3	V	11	2
INTERNAL RESISTANCE									
Resistance between VM pin and VDD pin	R_{VMD}	V_{DD} = 1.8 V, V_{VM} = 0 V		78	300	1310	kΩ	5	3
Resistance between VM pin and VSS pin	R_{VMS}	V_{DD} = 3.5 V, V_{VM} = 1.0 V		7.2	20	44	kΩ	5	3
INPUT VOLTAGE									
Operation voltage between VDD pin and VSS pin	V_{DSOP1}	–		1.5	–	8	V	–	–
Operation voltage between VDD pin and VM pin	V_{DSOP2}	–		1.5	–	28	V	–	–
INPUT CURRENT (WITH POWER-DOWN FUNTION)									
Current consumption during operation	I_{OPE}	V_{DD} = 3.5 V, V_{VM} = 0 V		0.7	3.0	6.0	μA	4	2
Current consumption during power-down	I_{PDN}	V_{DD} = V_{VM} = 1.5 V		–	–	0.3	μA	4	2
INPUT CURRENT (WITHOUT POWER-DOWN FUNTION)									
Current consumption during operation	I_{OPE}	V_{DD} = 3.5 V, V_{VM} = 0 V		0.7	3.0	6.0	μA	4	2
Current consumption during overdischarge	I_{OPED}	V_{DD} = V_{VM} = 1.5 V		0.2	2.0	3.8	μA	4	2
OUTPUT RESISTANCE									
CO pin resistance "H"	R_{COH}	V_{CO} = 3.0 V, V_{DD} = 3.5 V, V_{VM} = 0 V		1.2	5	15	kΩ	6	4
CO pin resistance "L"	R_{COL}	V_{CO} = 0.5 V, V_{DD} = 4.5 V, V_{VM} = 0 V		1.2	5	15	kΩ	6	4
DO pin resistance "H"	R_{DOH}	V_{DO} = 3.0 V, V_{DD} = 3.5 V, V_{VM} = 0 V		1.2	5	15	kΩ	7	4
DO pin resistance "L"	R_{DOL}	V_{DO} = 0.5 V, V_{DD} = V_{VM} = 1.8 V		1.2	5	15	kΩ	7	4

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

***2.** In any conditions, load short-circuiting detection voltage (V_{SHORT}) is higher than discharge overcurrent detection voltage (V_{DIOV}).

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3. Detection delay time

3. 1 S-8211DAD, S-8211DAE, S-8211DAG, S-8211DAH, S-8211DAI, S-8211DAJ, S-8211DAK, S-8211DAL, S-8211DAM, S-8211DAR, S-8211DAS, S-8211DAU, S-8211DAV, S-8211DAW, S-8211DAY, S-8211DAZ, S-8211DBA, S-8211DBB, S-8211DBC, S-8211DBD, S-8211DBE, S-8211DBF, S-8211DBG

Table 11

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DELAY TIME (Ta = +25°C)								
Overcharge detection delay time	t_{CU}	–	0.96	1.2	1.4	s	8	5
Overdischarge detection delay time	t_{DL}	–	120	150	180	ms	8	5
Discharge overcurrent detection delay time	t_{DIOV}	–	7.2	9	11	ms	9	5
Load short-circuiting detection delay time	t_{SHORT}	–	240	300	360	µs	9	5
DELAY TIME (Ta = –40°C to +85°C)*1								
Overcharge detection delay time	t_{CU}	–	0.7	1.2	2.0	s	8	5
Overdischarge detection delay time	t_{DL}	–	83	150	255	ms	8	5
Discharge overcurrent detection delay time	t_{DIOV}	–	5	9	15	ms	9	5
Load short-circuiting detection delay time	t_{SHORT}	–	150	300	540	µs	9	5

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

3. 2 S-8211DAF

Table 12

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DELAY TIME (Ta = +25°C)								
Overcharge detection delay time	t_{CU}	–	0.96	1.2	1.4	s	8	5
Overdischarge detection delay time	t_{DL}	–	61	75	90	ms	8	5
Discharge overcurrent detection delay time	t_{DIOV}	–	7.2	9	11	ms	9	5
Load short-circuiting detection delay time	t_{SHORT}	–	240	300	360	µs	9	5
DELAY TIME (Ta = –40°C to +85°C)*1								
Overcharge detection delay time	t_{CU}	–	0.7	1.2	2.0	s	8	5
Overdischarge detection delay time	t_{DL}	–	41	75	128	ms	8	5
Discharge overcurrent detection delay time	t_{DIOV}	–	5	9	15	ms	9	5
Load short-circuiting detection delay time	t_{SHORT}	–	150	300	540	µs	9	5

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

NOT RECOMMENDED FOR NEW DESIGN

3. 3 S-8211DAN, S-8211DAQ, S-8211DAT, S-8211DAX

Table 13

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condi-tion	Test Circuit
DELAY TIME (Ta = +25°C)								
Overcharge detection delay time	t_{CU}	–	0.96	1.2	1.4	s	8	5
Overdischarge detection delay time	t_{DL}	–	120	150	180	ms	8	5
Discharge overcurrent detection delay time	t_{DIOV}	–	14.5	18	22	ms	9	5
Load short-circuiting detection delay time	t_{SHORT}	–	240	300	360	µs	9	5
DELAY TIME (Ta = –40°C to +85°C)*1								
Overcharge detection delay time	t_{CU}	–	0.7	1.2	2.0	s	8	5
Overdischarge detection delay time	t_{DL}	–	83	150	255	ms	8	5
Discharge overcurrent detection delay time	t_{DIOV}	–	10	18	30	ms	9	5
Load short-circuiting detection delay time	t_{SHORT}	–	150	300	540	µs	9	5

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

NOT RECOMMENDED FOR NEW DESIGN

■ Test Circuits

Caution Unless otherwise specified, the output voltage levels "H" and "L" at the CO pin (V_{CO}) and the DO pin (V_{DO}) are judged by the threshold voltage (1.0 V) of the N-channel FET. Judge the CO pin level with respect to V_{VM} and the DO pin level with respect to V_{SS}.

1. Overcharge detection voltage, overcharge release voltage (Test condition 1, test circuit 1)

Overcharge detection voltage (V_{CU}) is defined as the voltage between the VDD pin and the VSS pin at which V_{CO} goes from "H" to "L" when the voltage V1 is gradually increased from the starting condition of V1 = 3.5 V. Overcharge release voltage (V_{CL}) is defined as the voltage between the VDD pin and the VSS pin at which V_{CO} goes from "L" to "H" when the voltage V1 is then gradually decreased. Overcharge hysteresis voltage (V_{HC}) is defined as the difference between overcharge detection voltage (V_{CU}) and overcharge release voltage (V_{CL}).

2. Overdischarge detection voltage, overdischarge release voltage (Test condition 2, test circuit 2)

Overdischarge detection voltage (V_{DL}) is defined as the voltage between the VDD pin and the VSS pin at which V_{DO} goes from "H" to "L" when the voltage V1 is gradually decreased from the starting condition of V1 = 3.5 V, V2 = 0 V. Overdischarge release voltage (V_{DU}) is defined as the voltage between the VDD pin and the VSS pin at which V_{DO} goes from "L" to "H" when the voltage V1 is then gradually increased. Overdischarge hysteresis voltage (V_{HD}) is defined as the difference between overdischarge release voltage (V_{DU}) and overdischarge detection voltage (V_{DL}).

3. Discharge overcurrent detection voltage (Test condition 3, test circuit 2)

Discharge overcurrent detection voltage (V_{DIOV}) is defined as the voltage between the VM pin and the VSS pin whose delay time for changing V_{DO} from "H" to "L" lies between the minimum and the maximum value of discharge overcurrent delay time when the voltage V2 is increased rapidly (within 10 μs) from the starting condition of V1 = 3.5 V, V2 = 0 V.

4. Load short-circuiting detection voltage (Test condition 3, test circuit 2)

Load short-circuiting detection voltage (V_{SHORT}) is defined as the voltage between the VM pin and the VSS pin whose delay time for changing V_{DO} from "H" to "L" lies between the minimum and the maximum value of load short-circuiting delay time when the voltage V2 is increased rapidly (within 10 μs) from the starting condition of V1 = 3.5 V, V2 = 0 V.

5. Current consumption during operation (Test condition 4, test circuit 2)

The current consumption during operation (I_{OPE}) is the current that flows through the VDD pin (I_{DD}) under the set conditions of V1 = 3.5 V and V2 = 0 V (normal status).

6. Charger detection voltage (= abnormal charge current detection voltage) (Test condition 4, test circuit 2)

The charger detection voltage (V_{CHA}) is the voltage between the VM pin and the VSS pin; when gradually increasing V1 at V1 = 1.8 V, V2 = 0 V to set V1 = V_{DL} + (V_{HD}/2), after that, decreasing V2 gradually from 0 V so that V_{DO} goes "L" to "H".
Measurement of the charger detection voltage is available for the product with overdischarge hysteresis $V_{HD} \neq 0$ only.
The abnormal charge current detection voltage is the voltage between the VM pin and the VSS pin; when gradually decreasing V2 at V1 = 3.5 V, V2 = 0 V and V_{CO} goes "H" to "L".
The value of the abnormal charge current detection voltage is equal to the charger detection voltage (V_{CHA}).

NOT RECOMMENDED FOR NEW DESIGN

7. Current consumption during power-down, current consumption during overdischarge (Test condition 4, test circuit 2)

7. 1 With power-down function

The current consumption during power-down (I_{PDN}) is the current that flows through the VDD pin (I_{DD}) under the set conditions of V1 = V2 = 1.5 V (overdischarge status).

7. 2 Without power-down function

The current consumption during overdischarge (I_{OPED}) is the current that flows through the VDD pin (I_{DD}) under the set conditions of V1 = V2 = 1.5 V (overdischarge status).

8. Resistance between VM pin and VDD pin (Test condition 5, test circuit 3)

The resistance between the VM pin and the VDD pin (R_{VMD}) is the resistance between the VM pin and the VDD pin under the set conditions of V1 = 1.8 V, V2 = 0 V.

9. Resistance between VM pin and VSS pin (Test condition 5, test circuit 3)

The resistance between the VM pin and the VSS pin (R_{VMS}) is the resistance between the VM pin and the VSS pin under the set conditions of V1 = 3.5 V, V2 = 1.0 V.

10. CO pin resistance "H" (Test condition 6, test circuit 4)

The CO pin resistance "H" (R_{COH}) is the resistance at the CO pin under the set conditions of V1 = 3.5 V, V2 = 0 V, V3 = 3.0 V.

11. CO pin resistance "L" (Test condition 6, test circuit 4)

The CO pin resistance "L" (R_{COL}) is the resistance at the CO pin under the set conditions of V1 = 4.5 V, V2 = 0 V, V3 = 0.5 V.

12. DO pin resistance "H" (Test condition 7, test circuit 4)

The DO pin resistance "H" (R_{DOH}) is the resistance at the DO pin under the set conditions of V1 = 3.5 V, V2 = 0 V, V4 = 3.0 V.

13. DO pin resistance "L" (Test condition 7, test circuit 4)

The DO pin resistance "L" (R_{DOL}) is the resistance at the DO pin under the set conditions of V1 = 1.8 V, V2 = 0 V, V4 = 0.5 V.

14. Overcharge detection delay time (Test condition 8, test circuit 5)

The overcharge detection delay time (t_{CU}) is the time needed for V_{CO} to change from "H" to "L" just after the voltage V1 momentarily increases (within 10 μs) from overcharge detection voltage (V_{CU}) − 0.2 V to overcharge detection voltage (V_{CU}) + 0.2 V under the set conditions of V2 = 0 V.

15. Overdischarge detection delay tme (Test condition 8, test circuit 5)

The overdischarge detection delay time (t_{DL}) is the time needed for V_{DO} to change from "H" to "L" just after the voltage V1 momentarily decreases (within 10 μs) from overdischarge detection voltage (V_{DL}) + 0.2 V to overdischarge detection voltage (V_{DL}) − 0.2 V under the set condition of V2 = 0 V.

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16. Discharge overcurrent detection delay time (Test condition 9, test circuit 5)

Discharge overcurrent detection delay time (t_{DIOV}) is the time needed for V_{DO} to go to "L" after the voltage V2 momentarily increases (within 10 μs) from 0 V to 0.35 V under the set conditions of V1 = 3.5 V, V2 = 0 V.

17. Load short-circuiting detection delay time (Test condition 9, test circuit 5)

Load short-circuiting detection delay time (t_{SHORT}) is the time needed for V_{DO} to go to "L" after the voltage V2 momentarily increases (within 10 μs) from 0 V to 1.6 V under the set conditions of V1 = 3.5 V, V2 = 0 V.

18. 0 V battery charge starting charger voltage (0 V battery charge function "available") (Test condition 10, test circuit 2)

The 0 V battery charge starting charger voltage (V_{0CHA}) is defined as the voltage between the VDD pin and the VM pin at which V_{CO} goes to "H" (V_{VM} + 0.1 V or higher) when the voltage V2 is gradually decreased from the starting condition of V1 = V2 = 0 V.

19. 0 V battery charge inhibition battery voltage (0 V battery charge function "unavailable") (Test condition 11, test circuit 2)

The 0 V battery charge inhibition battery voltage (V_{0INH}) is defined as the voltage between the VDD pin and the VSS pin at which V_{CO} goes to "H" (V_{VM} + 0.1 V or higher) when the voltage V1 is gradually increased from the starting condition of V1 = 0 V, V2 = −4 V.

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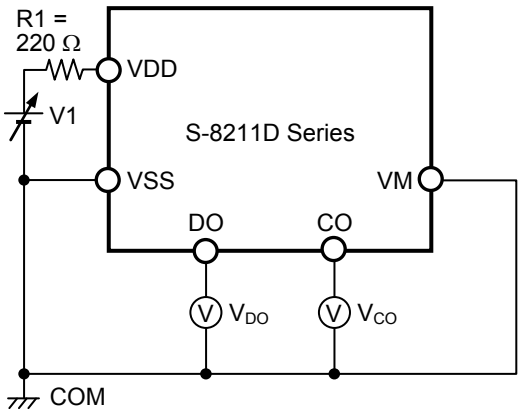

Figure 5 Test Circuit 1

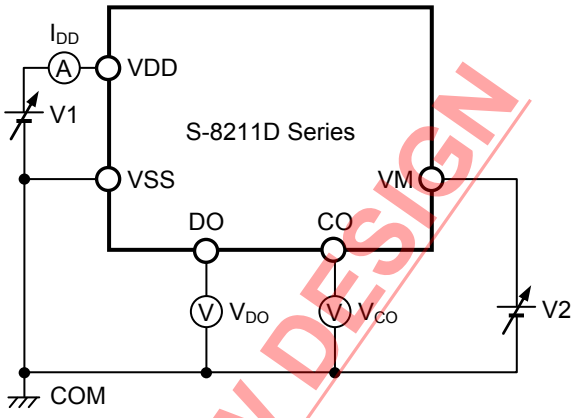

Figure 6 Test Circuit 2

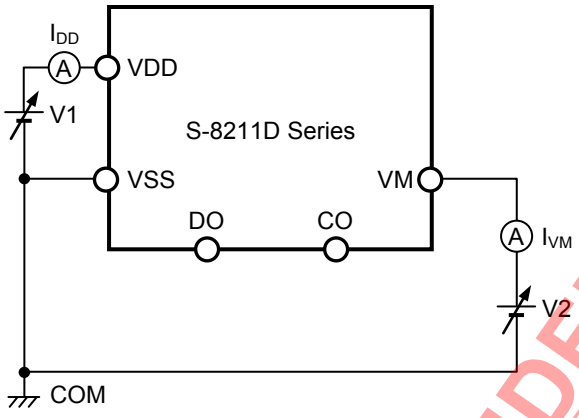

Figure 7 Test Circuit 3

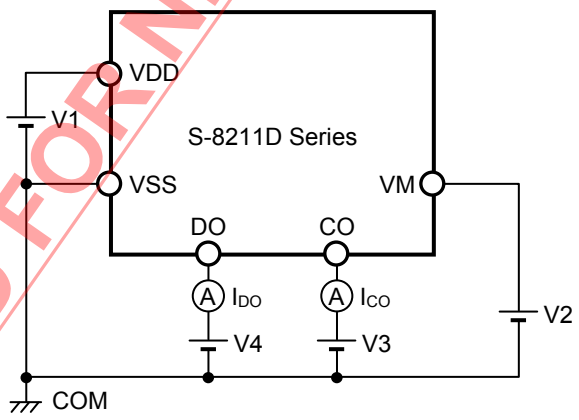

Figure 8 Test Circuit 4

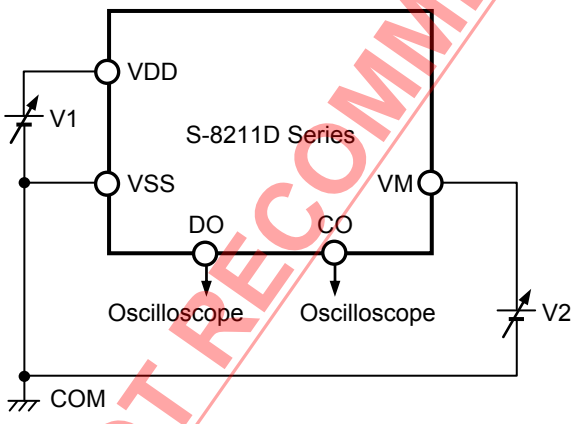

Figure 9 Test Circuit 5

NOT RECOMMENDED FOR NEW DESIGN

■ Operation

Remark Refer to the "■ **Battery Protection IC Connection Example**".

1. Normal status

The S-8211D Series monitors the voltage of the battery connected between the VDD pin and the VSS pin and the voltage difference between the VM pin and the VSS pin to control charging and discharging. When the battery voltage is in the range from overdischarge detection voltage (V_{DL}) to overcharge detection voltage (V_{CU}), and the VM pin voltage is not more than the discharge overcurrent detection voltage (V_{DIOV}), the S-8211D Series turns both the charging and discharging control FETs on. This condition is called the normal status, and in this condition charging and discharging can be carried out freely.
The resistance (R_{VMD}) between the VM pin and the VDD pin, and the resistance (R_{VMS}) between the VM pin and the VSS pin are not connected in the normal status.

Caution When the battery is connected for the first time, discharging may not be enabled. In this case, short the VM pin and the VSS pin, or set the VM pin's voltage at the level of the charger detection voltage (V_{CHA}) or more and the discharge overcurrent detection voltage (V_{DIOV}) or less by connecting the charger. The S-8211D Series then returns to the normal status.

2. Overcharge status

When the battery voltage becomes higher than overcharge detection voltage (V_{CU}) during charging in the normal status and detection continues for the overcharge detection delay time (t_{CU}) or longer, the S-8211D Series turns the charging control FET off to stop charging. This condition is called the overcharge status.
The resistance (R_{VMD}) between the VM pin and the VDD pin, and the resistance (R_{VMS}) between the VM pin and the VSS pin are not connected in the overcharge status.
The overcharge status is released in the following two cases ((1) and (2)).

(1) In the case that the VM pin voltage is higher than or equal to charger detection voltage (V_{CHA}), and is lower than the discharge overcurrent detection voltage (V_{DIOV}), the S-8211D Series releases the overcharge status when the battery voltage falls below the overcharge release voltage (V_{CL}).
(2) In the case that the VM pin voltage is higher than or equal to the discharge overcurrent detection voltage (V_{DIOV}), the S-8211D Series releases the overcharge status when the battery voltage falls below the overcharge detection voltage (V_{CU}).

When the discharge is started by connecting a load after the overcharge detection, the VM pin voltage rises more than the voltage at the VSS pin due to the V_f voltage of the parasitic diode. This is because the discharge current flows through the parasitic diode in the charging control FET. If the VM pin voltage is higher than or equal to the discharge overcurrent detection voltage (V_{DIOV}), the S-8211D Series releases the overcharge status when the battery voltage is lower than or equal to the overcharge detection voltage (V_{CU}).

Caution 1. If the battery is charged to a voltage higher than overcharge detection voltage (V_{CU}) and the battery voltage does not fall below overcharge detection voltage (V_{CU}) even when a heavy load is connected, discharge overcurrent detection and load short-circuiting detection do not function until the battery voltage falls below overcharge detection voltage (V_{CU}). Since an actual battery has an internal impedance of tens of mΩ, the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and discharge overcurrent detection and load short-circuiting detection function.
2. When a charger is connected after overcharge detection, the overcharge status is not released even if the battery voltage is below overcharge release voltage (V_{CL}). The overcharge status is released when the VM pin voltage goes over charger detection voltage (V_{CHA}) by removing the charger.

NOT RECOMMENDED FOR NEW DESIGN

3. Overdischarge status

3. 1 With power-down function

When the battery voltage falls below overdischarge detection voltage (V_{DL}) during discharging in the normal status and the detection continues for the overdischarge detection delay time (t_{DL}) or longer, the S-8211D Series turns the discharging control FET off to stop discharging. This condition is called the overdischarge status. Under the overdischarge status, the VM pin voltage is pulled up by the resistor between the VM pin and the VDD pin in the S-8211D Series (R_{VMD}). When voltage difference between the VM pin and the VDD pin then is 1.3 V typ. or lower, the current consumption is reduced to the power-down current consumption (I_{PDN}). This condition is called the power-down status.

The resistance (R_{VMS}) between the VM pin and the VSS pin is not connected in the power-down status and the overdischarge status.

The power-down status is released when a charger is connected and the voltage difference between the VM pin and the VDD pin becomes 1.3 V typ. or higher.

When a battery in the overdischarge status is connected to a charger and provided that the VM pin voltage is lower than charger detection voltage (V_{CHA}), the S-8211D Series releases the overdischarge status and turns the discharging FET on when the battery voltage reaches overdischarge detection voltage (V_{DL}) or higher.

When a battery in the overdischarge status is connected to a charger and provided that the VM pin voltage is not lower than charger detection voltage (V_{CHA}), the S-8211D Series releases the overdischarge status when the battery voltage reaches overdischarge release voltage (V_{DU}) or higher.

3. 2 Without power-down function

When the battery voltage falls below overdischarge detection voltage (V_{DL}) during discharging in the normal status and the detection continues for the overdischarge detection delay time (t_{DL}) or longer, the S-8211D Series turns the discharging control FET off to stop discharging. This condition is called the overdischarge status. Under the overdischarge status, the VM pin voltage is pulled up by the resistor between the VM pin and the VDD pin in the S-8211D Series (R_{VMD}).

The resistance (R_{VMS}) between the VM pin and the VSS pin is not connected in the overdischarge status.

When a battery in the overdischarge status is connected to a charger and provided that the VM pin voltage is lower than charger detection voltage (V_{CHA}), the S-8211D Series releases the overdischarge status and turns the discharging FET on when the battery voltage reaches overdischarge detection voltage (V_{DL}) or higher.

When a battery in the overdischarge status is connected to a charger and provided that the VM pin voltage is not lower than charger detection voltage (V_{CHA}), the S-8211D Series releases the overdischarge status when the battery voltage reaches overdischarge release voltage (V_{DU}) or higher.

4. Discharge overcurrent status (discharge overcurrent, load short-circuiting)

When a battery in the normal status is in the status where the voltage of the VM pin is equal to or higher than the discharge overcurrent detection voltage because the discharge current is higher than the specified value and the status lasts for the discharge overcurrent detection delay time, the discharge control FET is turned off and discharging is stopped. This status is called the discharge overcurrent status.

In the discharge overcurrent status, the VM pin and the VSS pin are shorted by the resistor between the VM pin and the VSS pin (R_{VMS}) in the S-8211D Series. However, the voltage of the VM pin is at the V_{DD} potential due to the load as long as the load is connected. When the load is disconnected completely, the VM pin returns to the V_{SS} potential.

If the S-8211D Series detects that the voltage of the VM pin returns to discharge overcurrent detection voltage (V_{DIOV}) or lower, the discharge overcurrent status is restored to the normal status.

The S-8211D Series will be restored to the normal status from discharge overcurrent detection status even when the voltage of the VM pin becomes the discharge overcurrent detection voltage (V_{DIOV}) or lower by connecting the charger.

The resistance (R_{VMD}) between the VM pin and the VDD pin is not connected in the discharge overcurrent status.

NOT RECOMMENDED FOR NEW DESIGN

5. Abnormal charge current detection

During charging a battery which is in the normal status, if the VM pin voltage becomes lower than the charger detection voltage (V_{CHA}) and this status is held longer than the overcharge detection delay time (t_{CU}), the S-8211D Series turns off the charge-control FET to stop charging. This is abnormal charge current detection.
This function works in the case that the DO pin voltage is in "H", and the VM pin voltage becomes lower than the charger detection voltage (V_{CHA}). Thus if the abnormal charge current flows in the battery in the overdischarge status, the S-8211D Series turns off the charge-control FET to stop charging; the DO pin voltage goes in "H" so that the battery voltage becomes higher than the overdischarge detection voltage (V_{DL}), and after the overcharge detection delay time (t_{cu}).
The status of abnormal charge current detection is released by the lower potential difference between the VM pin and the VSS pin than the charger detection voltage (V_{CHA}).

6. 0 V battery charge function "available"

This function is used to recharge a connected battery whose voltage is 0 V due to self-discharge. When the 0 V battery charge starting charger voltage (V_{0CHA}) or a higher voltage is applied between the EB+ pin and EB− pin by connecting a charger, the charging control FET gate is fixed to the VDD pin voltage.
When the voltage between the gate and source of the charging control FET becomes equal to or higher than the turn-on voltage due to the charger voltage, the charging control FET is turned on to start charging. At this time, the discharging control FET is off and the charging current flows through the internal parasitic diode in the discharging control FET. When the battery voltage becomes equal to or higher than overdischarge release voltage (V_{DU}), the S-8211D Series enters the normal status.

Caution Some battery providers do not recommend charging for a completely self-discharged battery. Please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge function.

7. 0 V battery charge function "unavailable"

This function inhibits recharging when a battery that is internally short-circuited (0 V battery) is connected. When the battery voltage is the 0 V battery charge inhibition battery voltage (V_{0INH}) or lower, the charging control FET gate is fixed to the EB− pin voltage to inhibit charging. When the battery voltage is the 0 V battery charge inhibition battery voltage (V_{0INH}) or higher, charging can be performed.

Caution Some battery providers do not recommend charging for a completely self-discharged battery. Please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge function.

NOT RECOMMENDED FOR NEW DESIGN

8. Delay circuit

The detection delay times are determined by dividing a clock of approximately 3.5 kHz by the counter.

Remark1. The discharge overcurrent detection delay time (t_{DIOV}) and the load short-circuiting detection delay time (t_{SHORT}) start when the discharge overcurrent detection voltage (V_{DIOV}) is detected. When the load short-circuiting detection voltage (V_{SHORT}) is detected over the load short-circuiting detection delay time (t_{SHORT}) after the detection of discharge overcurrent detection voltage (V_{DIOV}), the S-8211D Series turns the discharging control FET off within t_{SHORT} from the time of detecting V_{SHORT}.

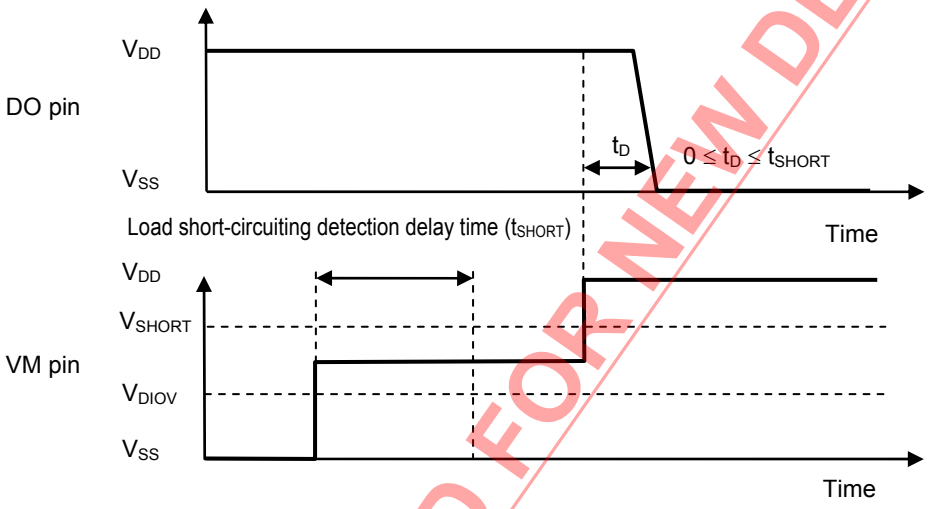

Figure 10

2. With power-down function

When any overcurrent is detected and the overcurrent continues for longer than the overdischarge detection delay time (t_{DL}) without the load being released, the status changes to the power-down status at the point where the battery voltage falls below overdischarge detection voltage (V_{DL}).
When the battery voltage falls below overdischarge detection voltage (V_{DL}) due to overcurrent, the S-8211D Series turns the discharging control FET off via overcurrent detection. In this case, if the recovery of the battery voltage is so slow that the battery voltage after the overdischarge detection delay time (t_{DL}) is still lower than the overdischarge detection voltage (V_{DL}), the S-8211D Series shifts to the power-down status.

Without power-down function

When any overcurrent is detected and the overcurrent continues for longer than the overdischarge detection delay time (t_{DL}) without the load being released, the status changes to the overdischarge status at the point where the battery voltage falls below overdischarge detection voltage (V_{DL}).
When the battery voltage falls below overdischarge detection voltage (V_{DL}) due to overcurrent, the S-8211D Series turns the discharging control FET off via overcurrent detection. In this case, if the recovery of the battery voltage is so slow that the battery voltage after the overdischarge detection delay time (t_{DL}) is still lower than the overdischarge detection voltage (V_{DL}), the S-8211D Series shifts to the overdischarge status.

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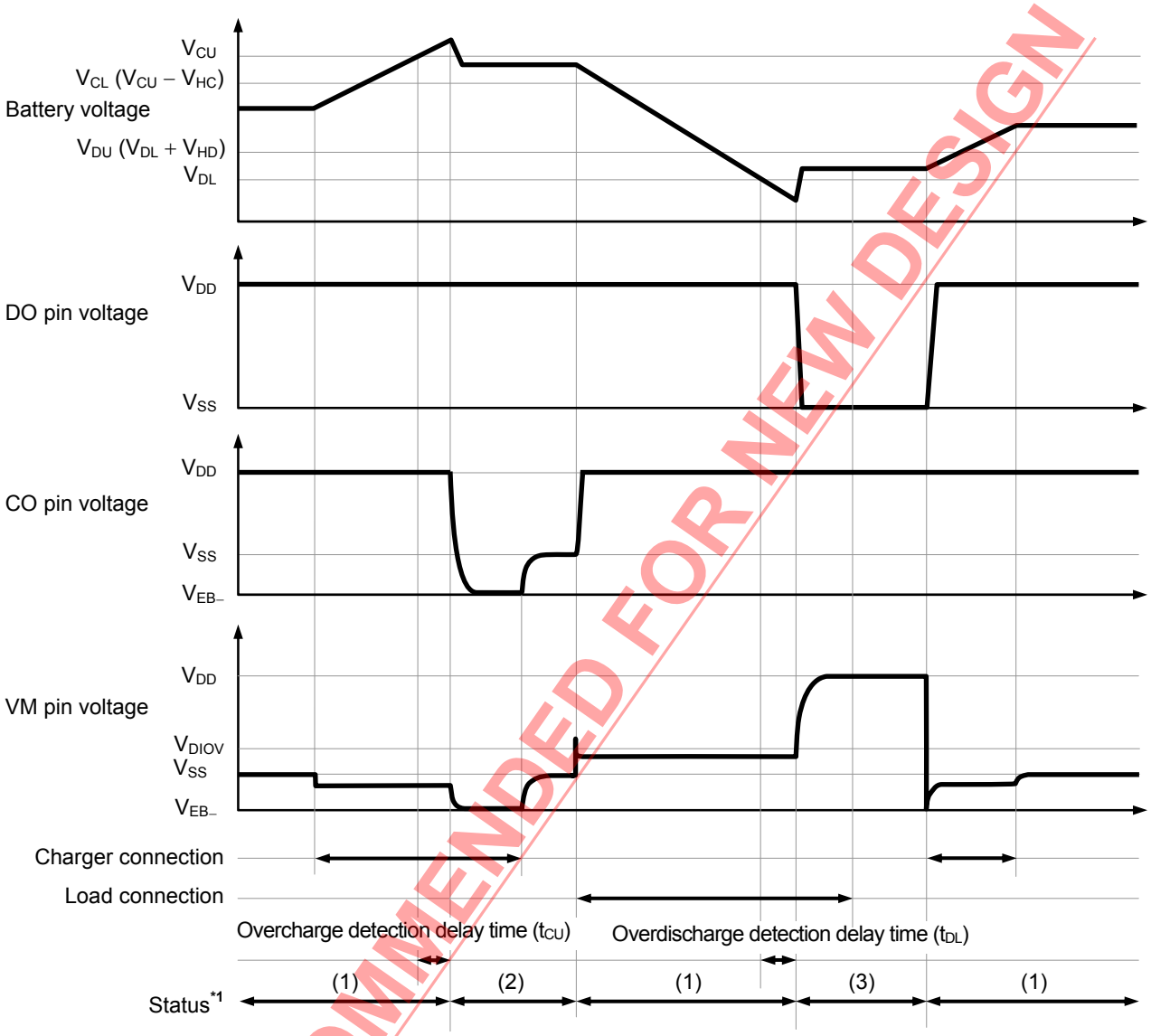
■ Timing Chart

1. Overcharge detection, overdischarge detection



***1.** (1): Normal status
(2): Overcharge status
(3): Overdischarge status

Remark The charger is assumed to charge with a constant current.

Figure 11

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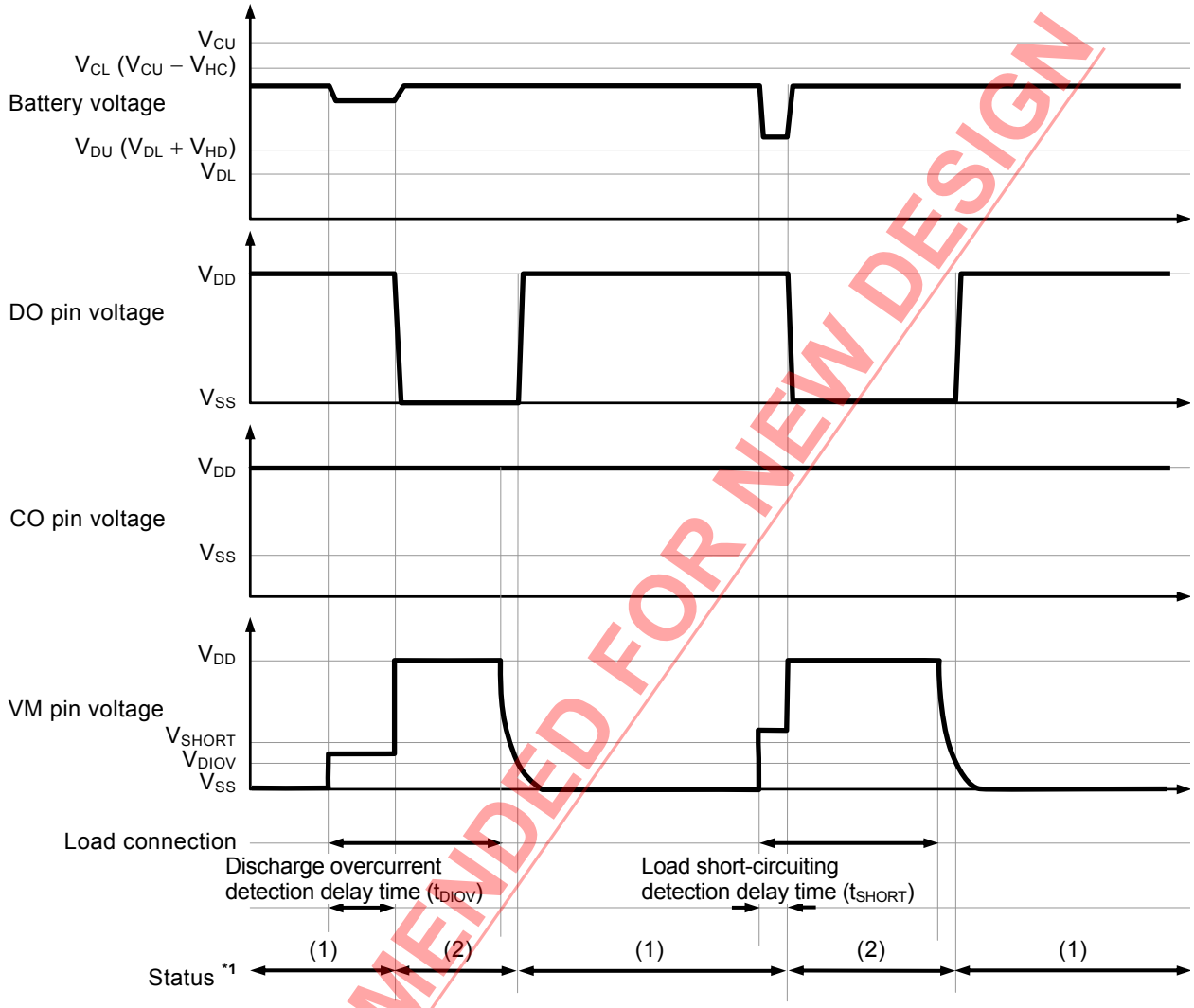
2. Discharge overcurrent detection



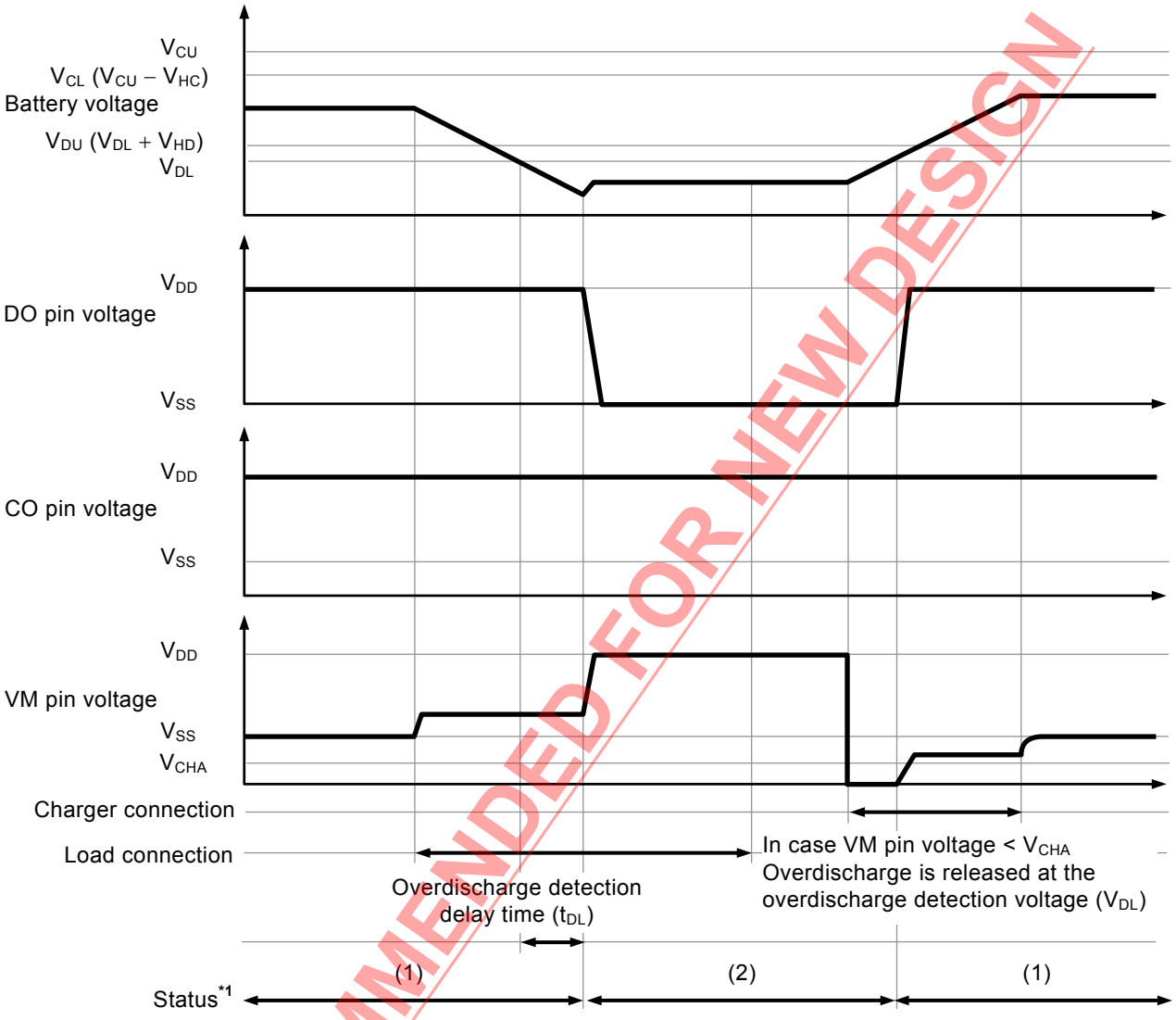
***1.** (1): Normal status
(2): Discharge overcurrent status

Remark The charger is assumed to charge with a constant current.

Figure 12

NOT RECOMMENDED FOR NEW DESIGN

3. Charger detection



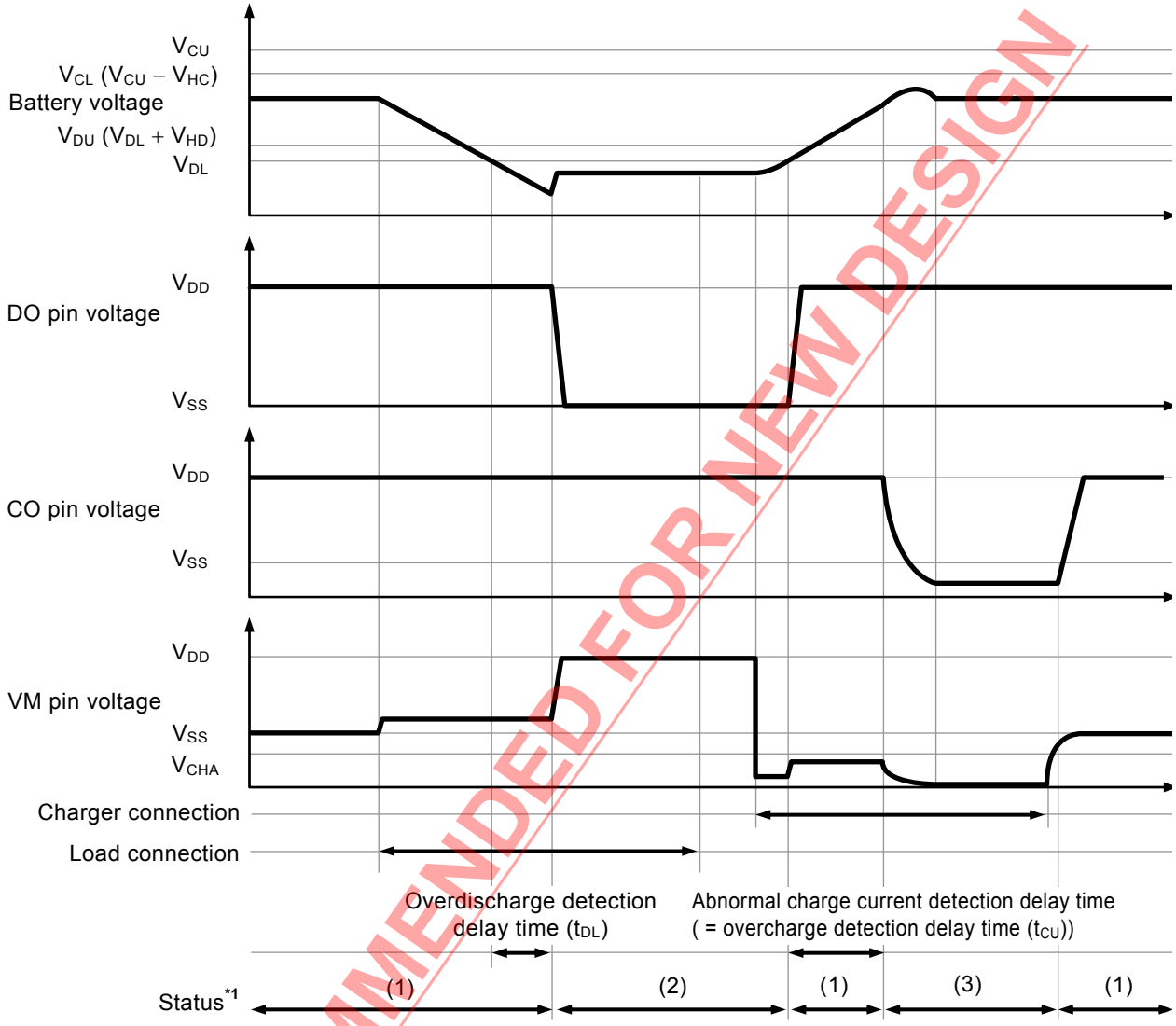
***1.** (1): Normal status
(2): Overdischarge status

Remark The charger is assumed to charge with a constant current.

Figure 13

NOT RECOMMENDED FOR NEW DESIGN

4. Abnormal charge current detection



***1.** (1): Normal status
(2): Overdischarge status
(3): Overcharge status

Remark The charger is assumed to charge with a constant current.

Figure 14

NOT RECOMMENDED FOR NEW DESIGN

■ Battery Protection IC Connection Example

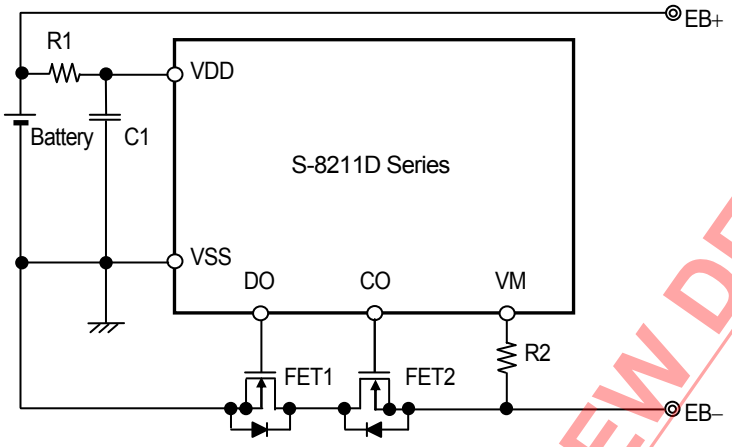


Figure 15

Table 14 Constants for External Components

Symbol	Part	Purpose	Min.	Typ.	Max.	Remark
FET1	N-channel MOS FET	Discharge control	–	–	–	Threshold voltage ≤ Overdischarge detection voltage*1 Gate to source withstand voltage ≥ Charger voltage*2
FET2	N-channel MOS FET	Charge control	–	–	–	Threshold voltage ≤ Overdischarge detection voltage*1 Gate to source withstand voltage ≥ Charger voltage*2
R1	Resistor	ESD protection, For power fluctuation	100 Ω	220 Ω	330 Ω	Resistance should be as small as possible to avoid lowering the overcharge detection accuracy due to current consumption.*3
C1	Capacitor	For power fluctuation	0.022 μF	0.1 μF	1.0 μF	Connect a capacitor of 0.022 μF or higher between VDD pin and VSS pin.*4
R2	Resistor	Protection for reverse connection of a charger	300 Ω	2 kΩ	4 kΩ	Select as large a resistance as possible to prevent current when a charger is connected in reverse.*5

***1.** If the threshold voltage of a FET is low, the FET may not cut the charge current. If a FET with a threshold voltage equal to or higher than the overdischarge detection voltage is used, discharging may be stopped before overdischarge is detected.

***2.** If the withstand voltage between the gate and source is lower than the charger voltage, the FET may be destroyed.

***3.** If a high resistor is connected to R1, the voltage between the VDD pin and the VSS pin may exceed the absolute maximum rating when a charger is connected in reverse since the current flows from the charger to the IC. Insert a resistor of 100 Ω or higher as R1 for ESD protection.

***4.** If a capacitor of less than 0.022 μF is connected to C1, the DO pin may oscillate when load short-circuiting is detected. Be sure to connect a capacitor of 0.022 μF or higher to C1.

***5.** If a resistor of 4 kΩ or higher is connected to R2, the charging current may not be cut when a high-voltage charger is connected.

Caution 1. The above constants may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.

NOT RECOMMENDED FOR NEW DESIGN

■ Precautions

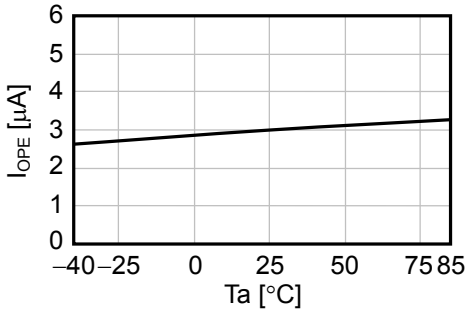
- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

NOT RECOMMENDED FOR NEW DESIGN

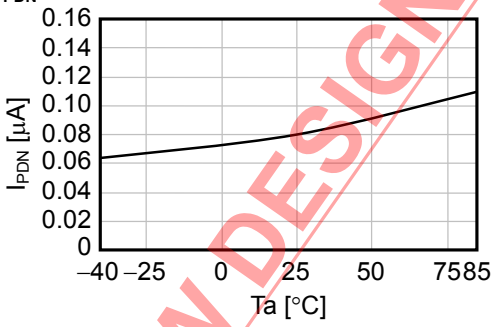
■ Characteristics (Typical Data)

1. Current consumption

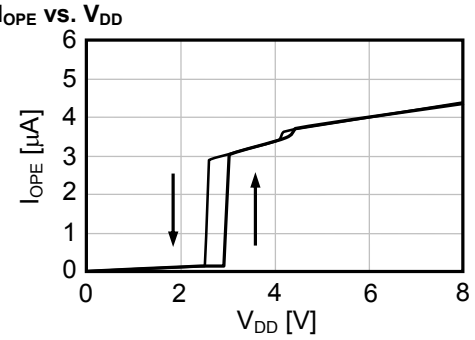
1. 1 I_{OPE} vs. Ta



1. 2 I_{PDN} vs. Ta

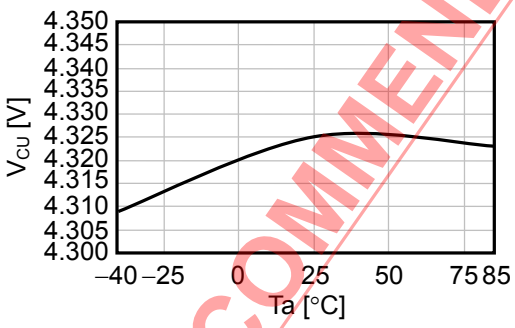


1. 3 I_{OPE} vs. V_{DD}

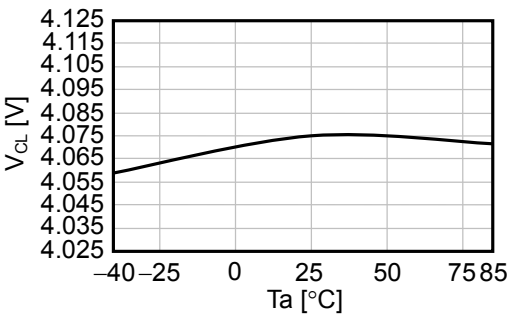


2. Overcharge detection / release voltage, overdischarge detection / release voltage, overcurrent detection voltage, and delay time

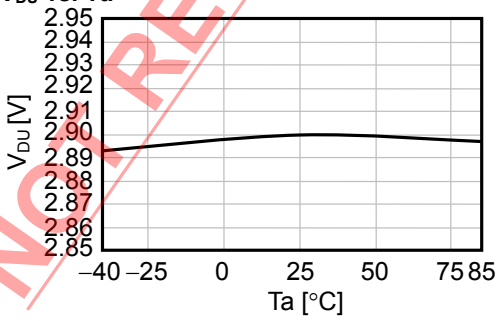
2. 1 V_{CU} vs. Ta



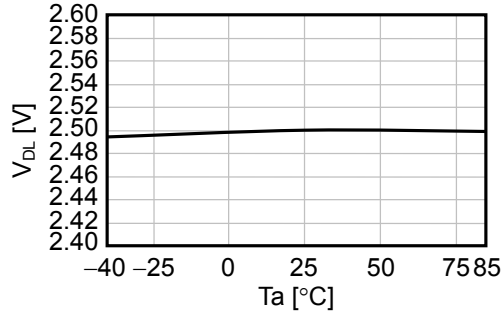
2. 2 V_{CL} vs. Ta



2. 3 V_{DU} vs. Ta



2. 4 V_{DL} vs. Ta



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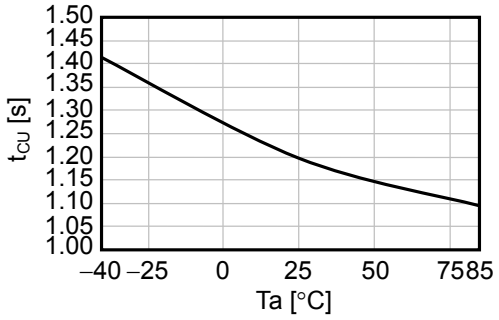
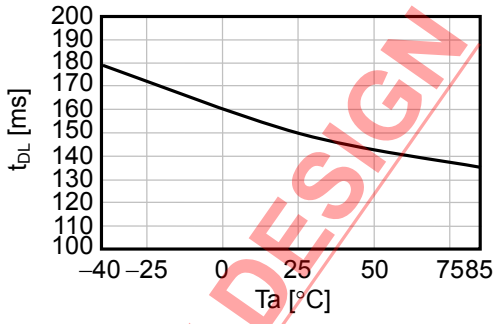
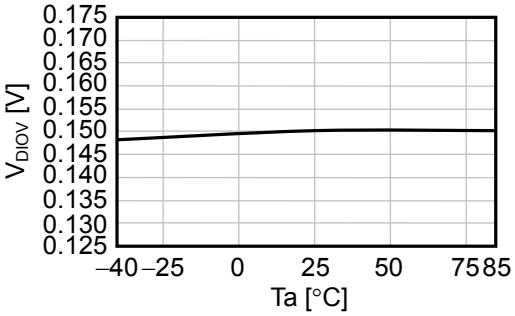
2. 5 t_{CU} vs. Ta



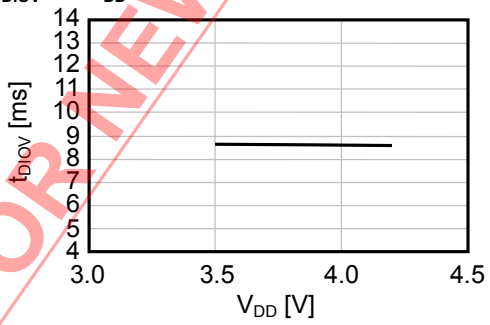
2. 6 t_{DL} vs. Ta



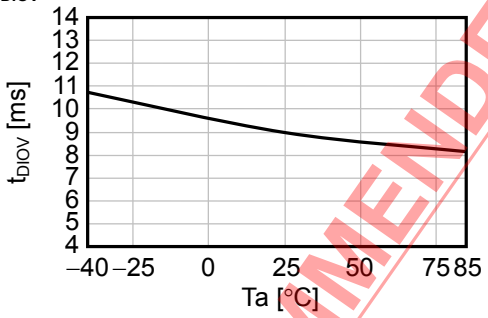
2. 7 V_{DIOV} vs. Ta



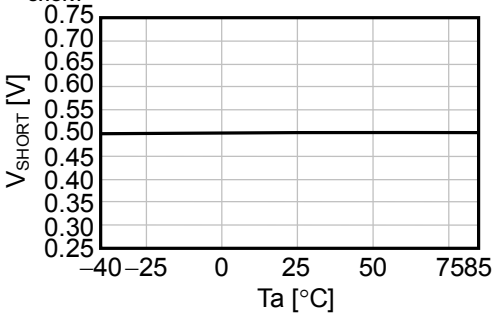
2. 8 t_{DIOV} vs. V_{DD}



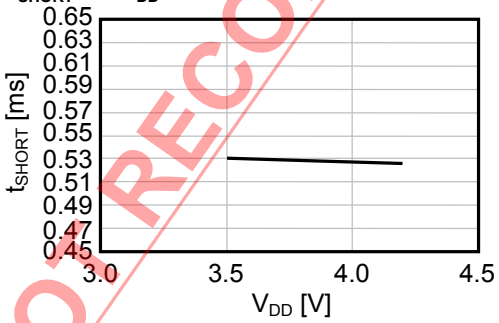
2. 9 t_{DIOV} vs. Ta



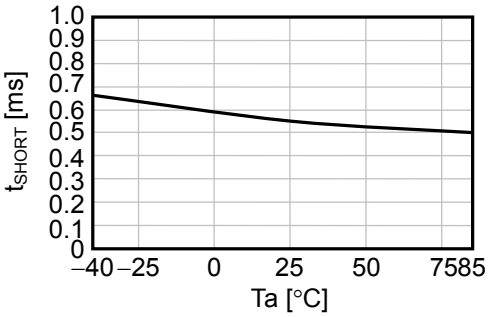
2. 10 V_{SHORT} vs. Ta



2. 11 t_{SHORT} vs. V_{DD}



2. 12 t_{SHORT} vs. Ta



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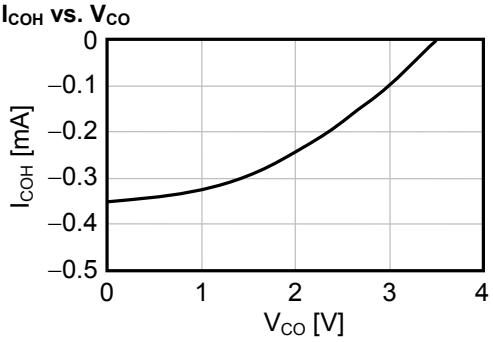
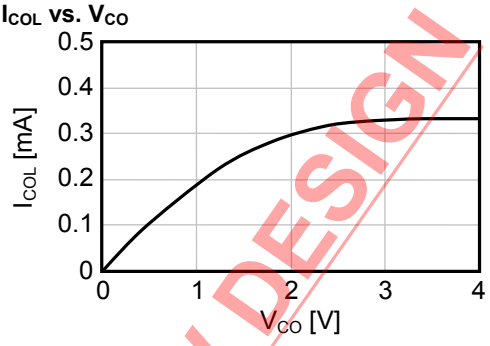
3. CO pin / DO pin

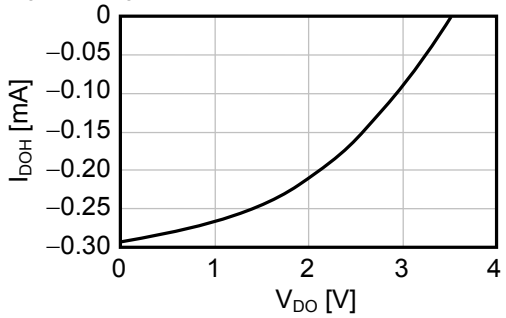
3. 1 I_{COH} vs. V_{CO}



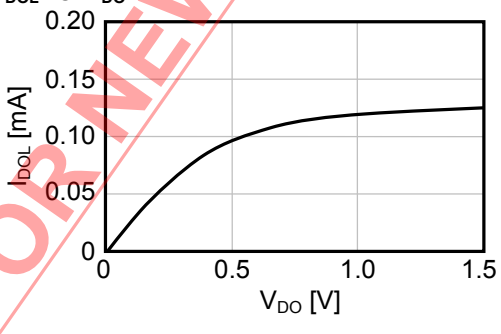
3. 2 I_{COL} vs. V_{CO}



3. 3 I_{DOH} vs. V_{DO}



3. 4 I_{DOL} vs. V_{DO}



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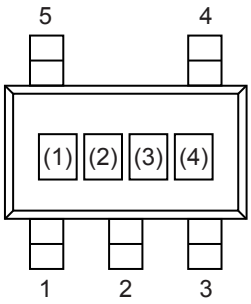
■ Marking Specifications

1. SOT-23-5

Top view



(1) to (3): Product code (refer to **Product name vs. Product code**)
(4): Lot number

Product name vs. Product code

Product Name	Product Code		
	(1)	(2)	(3)
S-8211DAD-M5T1x	R	2	D
S-8211DAE-M5T1x	R	2	E
S-8211DAH-M5T1x	R	2	H
S-8211DAI-M5T1x	R	2	I
S-8211DAJ-M5T1x	R	2	J
S-8211DAK-M5T1x	R	2	K
S-8211DAL-M5T1x	R	2	L
S-8211DAM-M5T1x	R	2	M
S-8211DAR-M5T1x	R	2	R
S-8211DAS-M5T1x	R	2	S
S-8211DAU-M5T1y	R	2	U
S-8211DAV-M5T1y	R	2	V
S-8211DAW-M5T1y	R	2	W
S-8211DBB-M5T1U	R	9	B
S-8211DBD-M5T1U	R	9	D
S-8211DBE-M5T1U	R	9	E
S-8211DBF-M5T1U	R	9	F
S-8211DBG-M5T1U	R	9	G

Remark 1. x: G or U
y: S or U
2. Please select products of environmental code = U for Sn 100%, halogen-free products.

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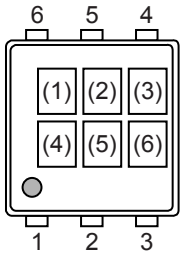
2. SNT-6A

Top view



(1) to (3): Product code (refer to **Product name vs. Product code**)
(4) to (6): Lot number

Product name vs. Product code

Product Name	Product Code		
	(1)	(2)	(3)
S-8211DAD-I6T1U	R	2	D
S-8211DAE-I6T1U	R	2	E
S-8211DAF-I6T1U	R	2	F
S-8211DAG-I6T1U	R	2	G
S-8211DAI-I6T1U	R	2	I
S-8211DAN-I6T1U	R	2	N
S-8211DAQ-I6T1U	R	2	Q
S-8211DAT-I6T1U	R	2	T
S-8211DAX-I6T1U	R	2	X
S-8211DAY-I6T1U	R	2	Y
S-8211DAZ-I6T1U	R	2	Z
S-8211DBA-I6T1U	R	9	A
S-8211DBC-I6T1U	R	9	C

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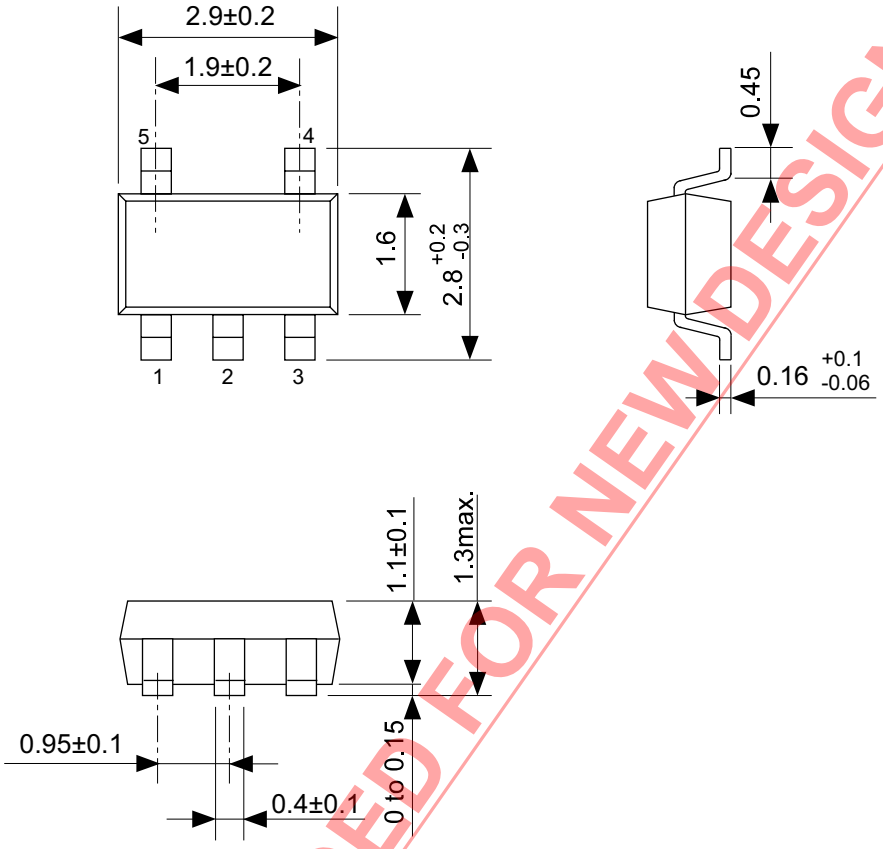

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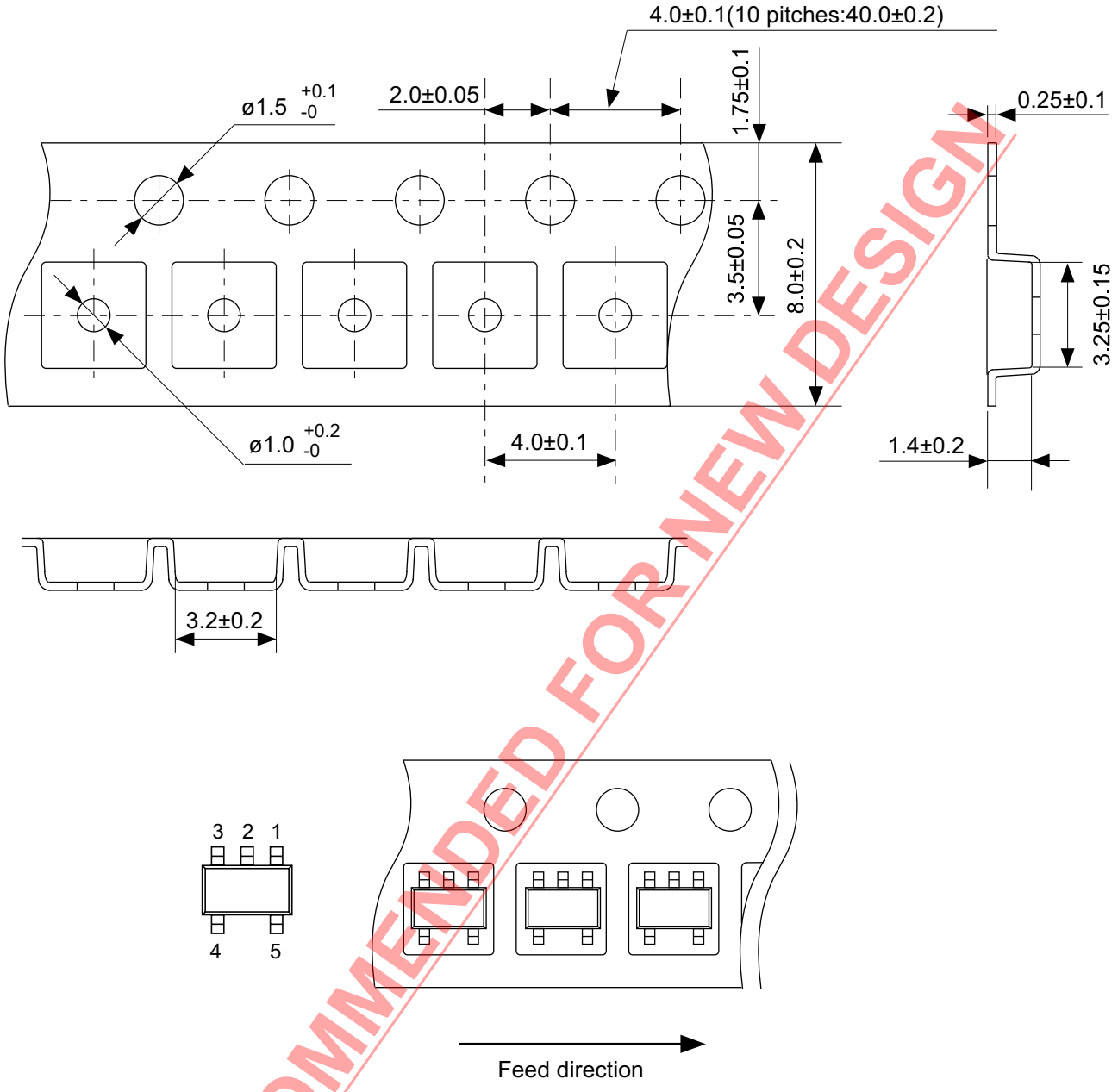
No. MP005-A-P-SD-1.3

TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.3
ANGLE	
UNIT	mm

ABLIC Inc.

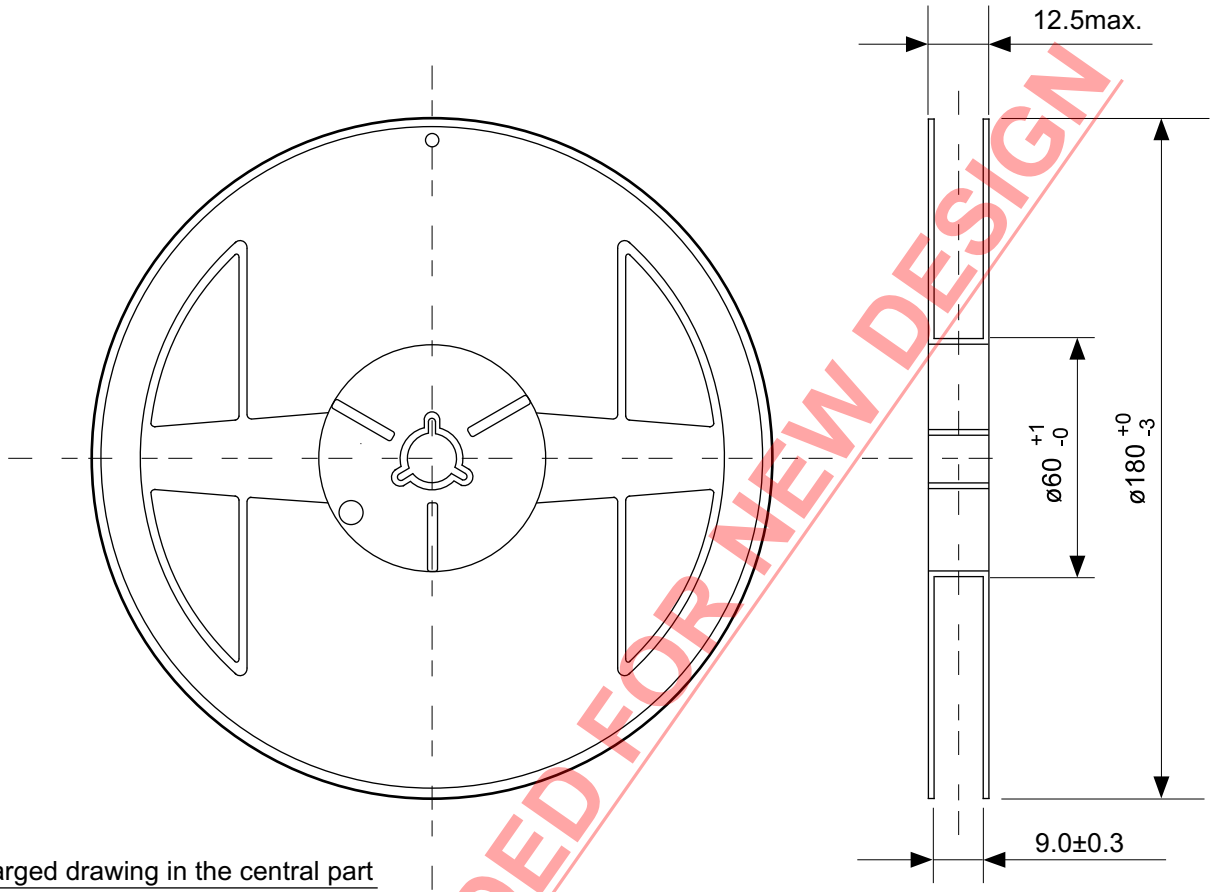


NOT RECOMMENDED FOR NEW DESIGN

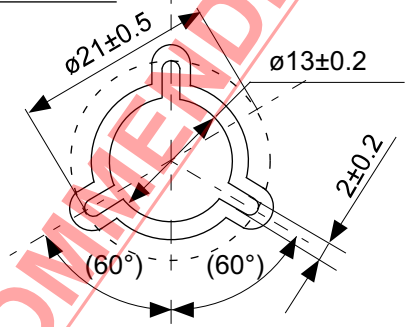
No. MP005-A-C-SD-2.1

TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
ANGLE	
UNIT	mm

ABLIC Inc.



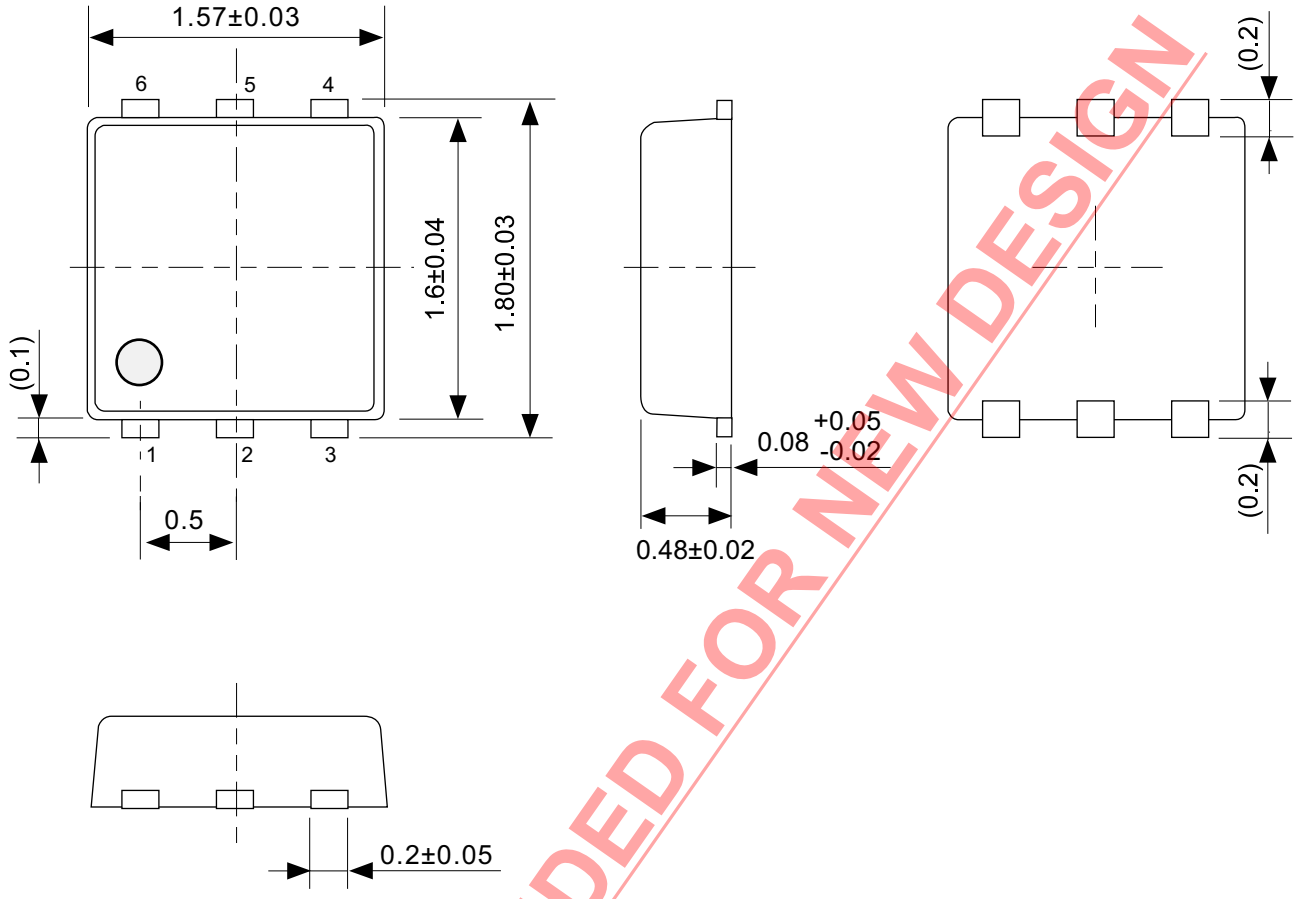
Enlarged drawing in the central part



NOT RECOMMENDED FOR NEW DESIGN

No. MP005-A-R-SD-1.1

TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-1.1		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			

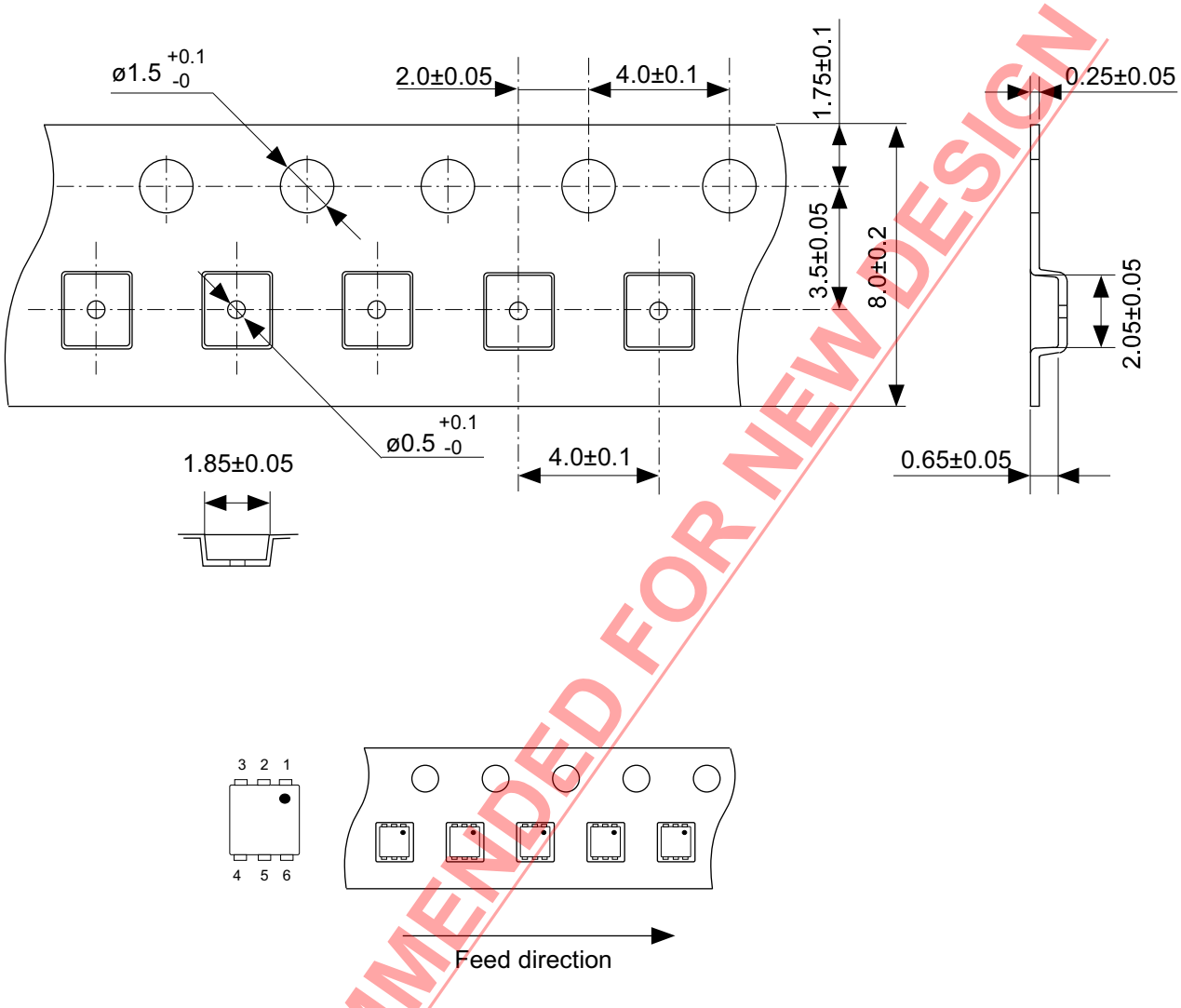


NOT RECOMMENDED FOR NEW DESIGN

No. PG006-A-P-SD-2.1

TITLE	SNT-6A-A-PKG Dimensions
No.	PG006-A-P-SD-2.1
ANGLE	
UNIT	mm

ABLIC Inc.

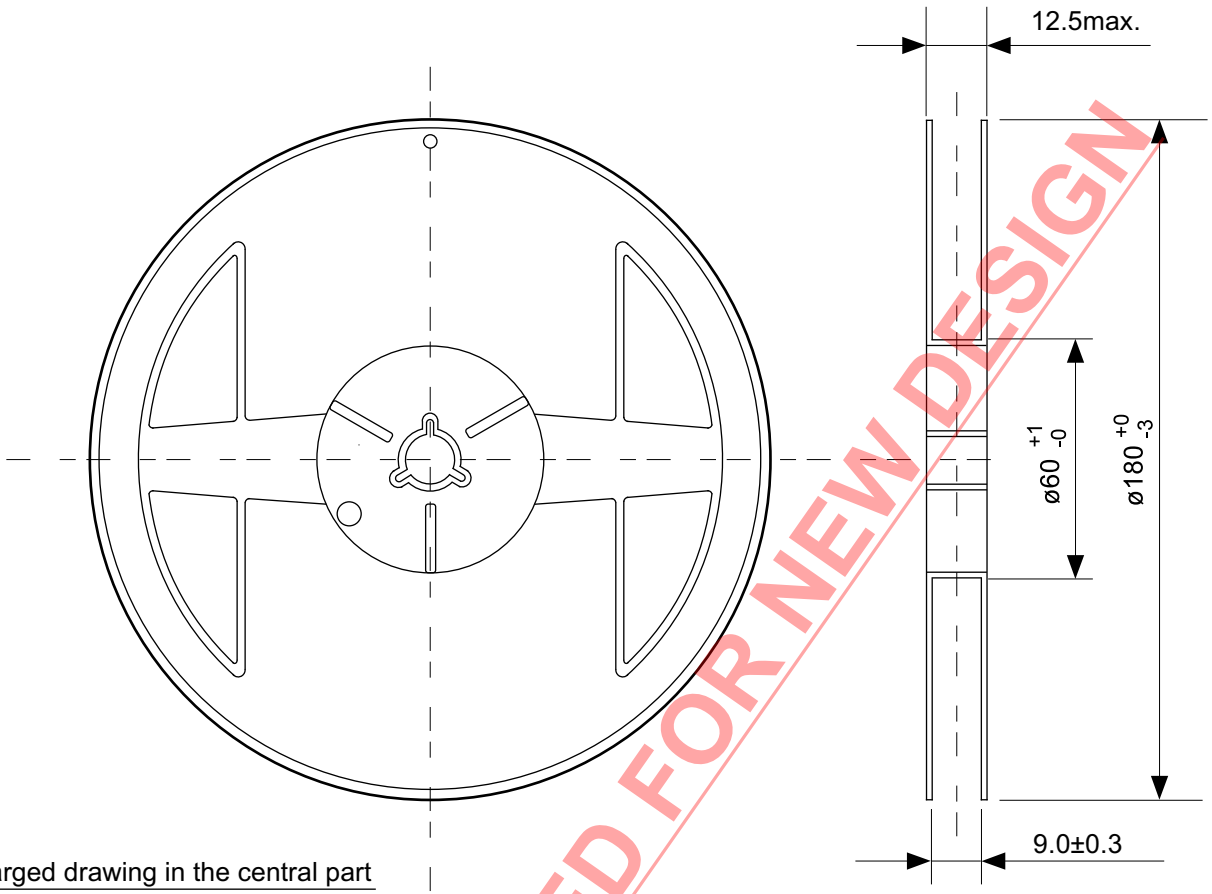


NOT RECOMMENDED FOR NEW DESIGN

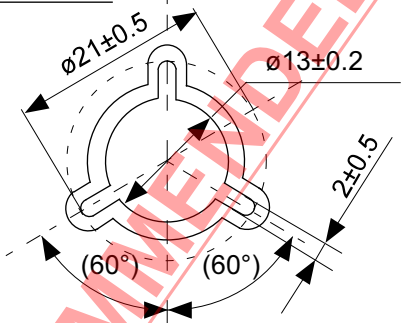
No. PG006-A-C-SD-2.0

TITLE	SNT-6A-A-Carrier Tape
No.	PG006-A-C-SD-2.0
ANGLE	
UNIT	mm

ABLIC Inc.



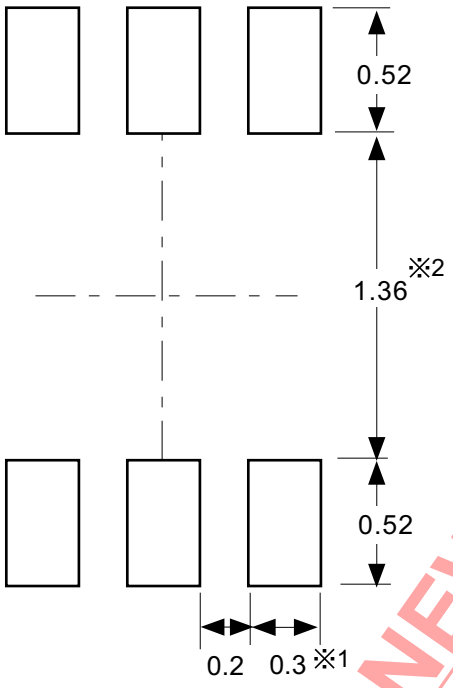
Enlarged drawing in the central part



No. PG006-A-R-SD-1.0

NOT RECOMMENDED FOR NEW DESIGN

TITLE	SNT-6A-A-Reel		
No.	PG006-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.30 mm ~ 1.40 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝SNTパッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.30 mm ~ 1.40 mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.30 mm ~ 1.40 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

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No. PG006-A-L-SD-4.1

TITLE	SNT-6A-A -Land Recommendation
No.	PG006-A-L-SD-4.1
ANGLE	
UNIT	mm

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   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
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