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5.5 V INPUT, 100 mA VOLTAGE REGULATOR WITH SUPPLY VOLTAGE DIVIDED OUTPUT

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The S-1740/1741 Series, developed using CMOS technology, is a positive voltage regulator with the supply voltage divided output, which features super low current consumption and low dropout voltage.
The regulator block has low current consumption of 0.35 μA typ. and high-accuracy output voltage of ±1.0%.
The function of the supply voltage divided output is prepared in the S-1740/1741 Series. The supply voltage divided output is a function that divides the input voltage (V_{IN}) of the regulator into $V_{IN}/2$ or $V_{IN}/3$ and outputs the voltage. For example, this function makes it possible that the IC connects to a low voltage microcontroller A/D converter directly and the microcontroller monitors a battery voltage.

■ Features

Regulator block

- Output voltage: V_{OUT} = 1.0 V to 3.5 V, selectable in 0.05 V step
- Input voltage: V_{IN} = 1.5 V to 5.5 V
- Output voltage accuracy: ±1.0% (1.0 V to 1.45 V output product: ±15 mV) (Ta = +25°C)
- Dropout voltage: 20 mV typ. (2.5 V output product, at I_{OUT} = 10 mA) (Ta = +25°C)
- Current consumption during operation: I_{SS1} = 0.35 μA typ. (Ta = +25°C)
- Output current: Possible to output 100 mA (at $V_{IN} \geq V_{OUT(S)} + 1.0$ V)*1
- Input capacitor: A ceramic capacitor can be used. (1.0 μF or more)
- Output capacitor: A ceramic capacitor can be used. (1.0 μF to 100 μF)
- Built-in overcurrent protection circuit: Limits overcurrent of output transistor.

Supply voltage divider block

- Output voltage: $V_{PMOUT} = V_{IN}/2$ (S-1740 Series)
  $V_{PMOUT} = V_{IN}/3$ (S-1741 Series)
- Current consumption during operation: I_{SS1P} = 0.15 μA typ. (Ta = +25°C)
- Output capacitor: A ceramic capacitor can be used. (100 nF to 220 nF)
- Built-in enable circuit: Ensures long battery life.

Overall

- Operation temperature range: Ta = –40°C to +85°C
- Lead-free (Sn 100%), halogen-free

***1.** Please make sure that the loss of the IC will not exceed the power dissipation when the output current is large.

■ Applications

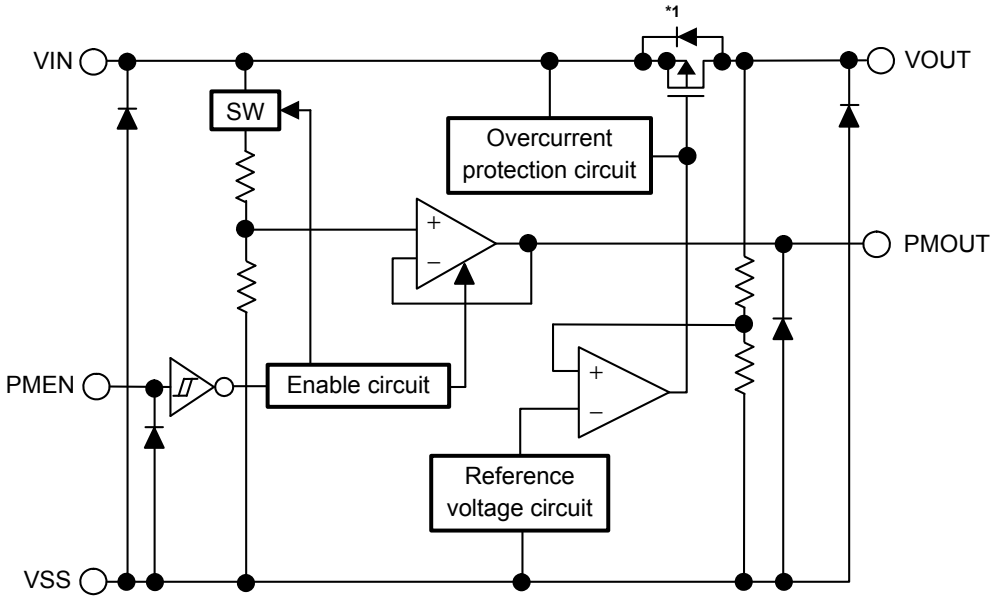
- Constant-voltage power supply and battery voltage monitoring support for battery-powered device
- Constant-voltage power supply for portable communication device, digital camera, and digital audio player
- Constant-voltage power supply for home electric appliance

■ Packages

- SOT-23-5
- HSNT-6(1212)
- HSNT-4(1010)

■ Block Diagram

1. S-1740/1741 Series A / C type (SOT-23-5, HSNT-6(1212))

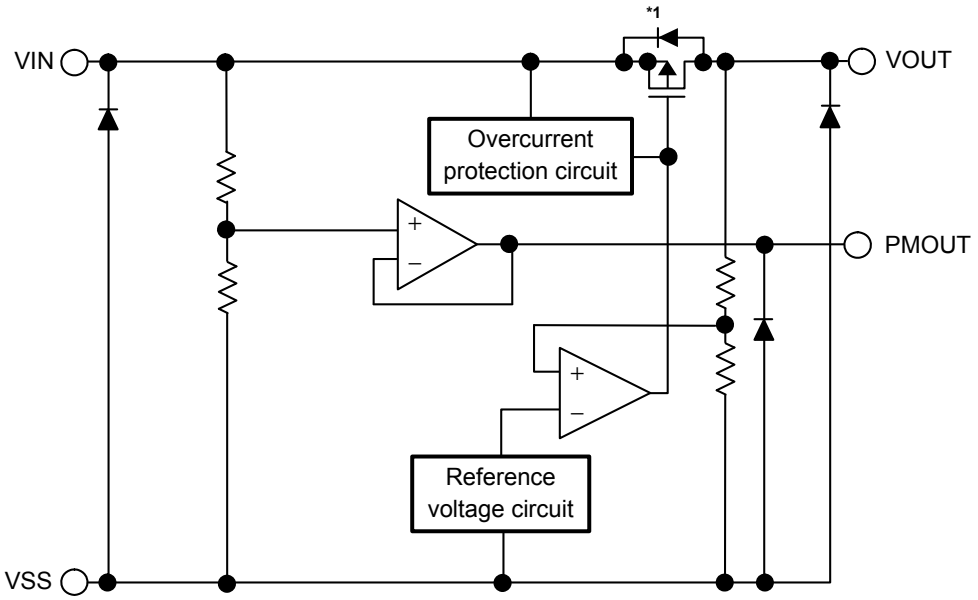


Product Type	Output Voltage (V_{PMOUT})	PMEN Pin Logic
S-1740 Series A type	$V_{IN}/2$	Active "H"
S-1740 Series C type		Active "L"
S-1741 Series A type	$V_{IN}/3$	Active "H"
S-1741 Series C type		Active "L"

***1.** Parasitic diode

Figure 1

2. S-1740/1741 Series G type (HSNT-4(1010))



Product Type	Output Voltage (V_{PMOUT})	PMEN Pin Logic
S-1740 Series G type	$V_{IN}/2$	Without PMEN pin
S-1741 Series G type	$V_{IN}/3$	

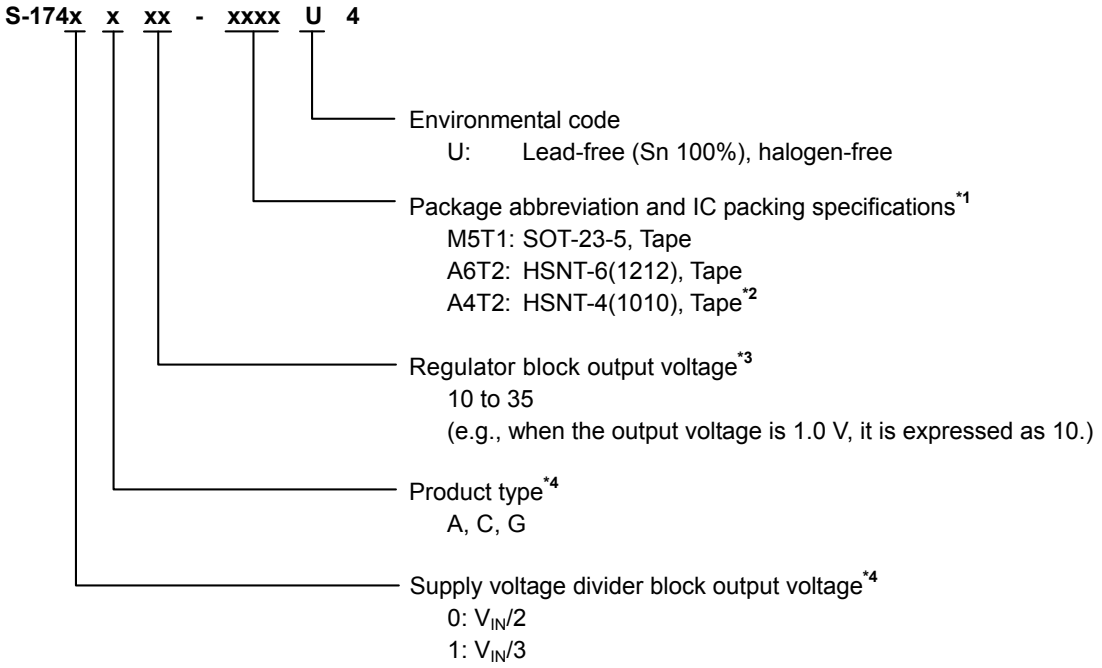
***1.** Parasitic diode

Figure 2

■ Product Name Structure

Users can select supply voltage divider block output voltage, product type, regulator block output voltage, and package type for the S-1740/1741 Series. Refer to "**1. Product name**" regarding the contents of product name, "**2. Function list of product type**" regarding the product type, "**3. Packages**" regarding the package drawings and "**4. Product name list**" for details of product names.

1. Product name



***1.** Refer to the tape drawing.
***2.** Only S-1740/1741 Series G type
***2.** Contact our sales office when the product which has 0.05 V step is necessary.
***3.** Refer to "**2. Function list of product type**" and "**2. 2 PMEN pin**" in "**2. Supply voltage divider block**" in "**■ Operation**".

2. Function list of product type

Table 1

Product Type	Output Voltage (V_{PMOUT})	PMEN Pin Logic	Package
S-1740 Series A type	$V_{IN}/2$	Active "H"	HSNT-6(1212), SOT-23-5
S-1740 Series C type		Active "L"	
S-1740 Series G type		Without PMEN pin	HSNT-4(1010)
S-1741 Series A type	$V_{IN}/3$	Active "H"	HSNT-6(1212), SOT-23-5
S-1741 Series C type		Active "L"	
S-1741 Series G type		Without PMEN pin	HSNT-4(1010)

3. Packages

Table 2 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SOT-23-5	MP005-A-P-SD	MP005-A-C-SD	MP005-A-R-SD	–
HSNT-6(1212)	PM006-A-P-SD	PM006-A-C-SD	PM006-A-R-SD	PM006-A-L-SD
HSNT-4(1010)	PL004-A-P-SD	PL004-A-C-SD	PL004-A-R-SD	PL004-A-L-SD

4. Product name list

4. 1 S-1740 Series

4. 1. 1 A type

PMEN pin logic: Active "H" Output Voltage (V_{PMOUT}): $V_{IN}/2$

Table 3

Output Voltage (V_{OUT})	SOT-23-5	HSNT-6(1212)
1.0 V ± 15 mV	S-1740A10-M5T1U4	S-1740A10-A6T2U4
1.7 V ± 1.0%	S-1740A17-M5T1U4	S-1740A17-A6T2U4
1.8 V ± 1.0%	S-1740A18-M5T1U4	S-1740A18-A6T2U4
2.0 V ± 1.0%	S-1740A20-M5T1U4	S-1740A20-A6T2U4
2.1 V ± 1.0%	S-1740A21-M5T1U4	S-1740A21-A6T2U4
3.0 V ± 1.0%	S-1740A30-M5T1U4	S-1740A30-A6T2U4

Remark Please contact our sales office for products with specifications other than the above.

4. 1. 2 C type

PMEN pin logic: Active "L" Output Voltage (V_{PMOUT}): $V_{IN}/2$

Table 4

Output Voltage (V_{OUT})	SOT-23-5	HSNT-6(1212)
1.0 V ± 15 mV	S-1740C10-M5T1U4	S-1740C10-A6T2U4
1.7 V ± 1.0%	S-1740C17-M5T1U4	S-1740C17-A6T2U4
1.8 V ± 1.0%	S-1740C18-M5T1U4	S-1740C18-A6T2U4
2.0 V ± 1.0%	S-1740C20-M5T1U4	S-1740C20-A6T2U4
2.1 V ± 1.0%	S-1740C21-M5T1U4	S-1740C21-A6T2U4
3.0 V ± 1.0%	S-1740C30-M5T1U4	S-1740C30-A6T2U4

Remark Please contact our sales office for products with specifications other than the above.

4. 1. 3 G type

PMEN pin logic: Without PMEN pin Output Voltage (V_{PMOUT}): $V_{IN}/2$

Table 5

Output Voltage (V_{OUT})	HSNT-4(1010)
1.0 V ± 15 mV	S-1740G10-A4T2U4
1.7 V ± 1.0%	S-1740G17-A4T2U4
1.8 V ± 1.0%	S-1740G18-A4T2U4
2.0 V ± 1.0%	S-1740G20-A4T2U4
2.1 V ± 1.0%	S-1740G21-A4T2U4
3.0 V ± 1.0%	S-1740G30-A4T2U4

Remark Please contact our sales office for products with specifications other than the above.

4. 2 S-1741 Series

4. 2. 1 A type

PMEN pin logic: Active "H" Output Voltage (V_{PMOUT}): $V_{IN}/3$

Table 6

Output Voltage (V_{OUT})	SOT-23-5	HSNT-6(1212)
1.0 V ± 15 mV	S-1741A10-M5T1U4	S-1741A10-A6T2U4
1.7 V ± 1.0%	S-1741A17-M5T1U4	S-1741A17-A6T2U4
1.8 V ± 1.0%	S-1741A18-M5T1U4	S-1741A18-A6T2U4
2.0 V ± 1.0%	S-1741A20-M5T1U4	S-1741A20-A6T2U4
2.1 V ± 1.0%	S-1741A21-M5T1U4	S-1741A21-A6T2U4
3.0 V ± 1.0%	S-1741A30-M5T1U4	S-1741A30-A6T2U4

Remark Please contact our sales office for products with specifications other than the above.

4. 2. 2 C type

PMEN pin logic: Active "L" Output Voltage (V_{PMOUT}): $V_{IN}/3$

Table 7

Output Voltage (V_{OUT})	SOT-23-5	HSNT-6(1212)
1.0 V ± 15 mV	S-1741C10-M5T1U4	S-1741C10-A6T2U4
1.7 V ± 1.0%	S-1741C17-M5T1U4	S-1741C17-A6T2U4
1.8 V ± 1.0%	S-1741C18-M5T1U4	S-1741C18-A6T2U4
2.0 V ± 1.0%	S-1741C20-M5T1U4	S-1741C20-A6T2U4
2.1 V ± 1.0%	S-1741C21-M5T1U4	S-1741C21-A6T2U4
3.0 V ± 1.0%	S-1741C30-M5T1U4	S-1741C30-A6T2U4

Remark Please contact our sales office for products with specifications other than the above.

4. 2. 3 G type

PMEN pin logic: Without PMEN pin Output Voltage (V_{PMOUT}): $V_{IN}/3$

Table 8

Output Voltage (V_{OUT})	HSNT-4(1010)
1.0 V ± 15 mV	S-1741G10-A4T2U4
1.7 V ± 1.0%	S-1741G17-A4T2U4
1.8 V ± 1.0%	S-1741G18-A4T2U4
2.0 V ± 1.0%	S-1741G20-A4T2U4
2.1 V ± 1.0%	S-1741G21-A4T2U4
3.0 V ± 1.0%	S-1741G30-A4T2U4

Remark Please contact our sales office for products with specifications other than the above.

■ Pin Configurations

1. SOT-23-5

Top view

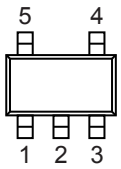


Figure 3

Table 9 S-1740/1741 Series A / C type

Pin No.	Symbol	Description
1	VIN	Input voltage pin
2	VSS	GND pin
3	PMEN	Supply voltage divided output enable pin
4	PMOUT	Supply voltage divided output pin
5	VOUT	Output voltage pin

2. HSNT-6(1212)

Top view



Bottom view

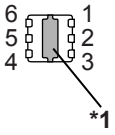


Figure 4

Table 10 S-1740/1741 Series A / C type

Pin No.	Symbol	Description
1	VOUT	Output voltage pin
2	VSS	GND pin
3	PMOUT	Supply voltage divided output pin
4	PMEN	Supply voltage divided output enable pin
5	NC*2	No connection
6	VIN	Input voltage pin

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential GND.
However, do not use it as the function of electrode.
***2.** The NC pin is electrically open.
The NC pin can be connected to the VIN pin or the VSS pin.

3. HSNT-4(1010)

Top view



Bottom view

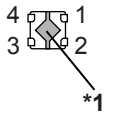


Figure 5

Table 11 S-1740/1741 Series G type

Pin No.	Symbol	Description
1	VOUT	Output voltage pin
2	VSS	GND pin
3	PMOUT	Supply voltage divided output pin
4	VIN	Input voltage pin

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential GND.
However, do not use it as the function of electrode.

■ Absolute Maximum Ratings

Table 12

(Ta = +25°C unless otherwise specified)

Item		Symbol	Absolute Maximum Rating	Unit
Input voltage	Regulator block	V_{IN}	V_{SS} – 0.3 to V_{SS} + 6.0	V
	Supply voltage divider block	V_{PMEN}	V_{SS} – 0.3 to V_{SS} + 6.0	V
Output voltage	Regulator block	V_{OUT}	V_{SS} – 0.3 to V_{IN} + 0.3	V
	Supply voltage divider block	V_{PMOUT}	V_{SS} – 0.3 to V_{IN} + 0.3	V
Output current		I_{OUT}	120	mA
Operation ambient temperature		T_{opr}	–40 to +85	°C
Storage temperature		T_{stg}	–40 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 13

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	SOT-23-5	Board A	–	192	–	°C/W
			Board B	–	160	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W
		HSNT-6(1212)	Board A	–	234	–	°C/W
			Board B	–	193	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W
		HSNT-4(1010)	Board A	–	378	–	°C/W
			Board B	–	317	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

1. Regulator block

Table 14

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Output voltage*1	$V_{OUT(E)}$	$V_{IN} = V_{OUT(S)} + 1.0$ V, I_{OUT} = 10 mA	1.0 V ≤ $V_{OUT(S)}$ < 1.5 V	$V_{OUT(S)} - 0.015$	$V_{OUT(S)}$	$V_{OUT(S)} + 0.015$	V	1
			1.5 V ≤ $V_{OUT(S)}$ ≤ 3.5 V	$V_{OUT(S)} \times 0.99$	$V_{OUT(S)}$	$V_{OUT(S)} \times 1.01$	V	1
Output current*2	I_{OUT}	$V_{IN} \geq V_{OUT(S)} + 1.0$ V		100*5	–	–	mA	3
Dropout voltage*3	V_{drop}	I_{OUT} = 10 mA	1.0 V ≤ $V_{OUT(S)}$ < 1.1 V	0.50	–	–	V	1
			1.1 V ≤ $V_{OUT(S)}$ < 1.2 V	0.40	–	–	V	1
			1.2 V ≤ $V_{OUT(S)}$ < 1.3 V	0.30	–	–	V	1
			1.3 V ≤ $V_{OUT(S)}$ < 1.4 V	0.20	–	–	V	1
			1.4 V ≤ $V_{OUT(S)}$ < 1.5 V	0.10	–	–	V	1
			1.5 V ≤ $V_{OUT(S)}$ < 1.7 V	–	0.050	0.080	V	1
			1.7 V ≤ $V_{OUT(S)}$ < 1.8 V	–	0.040	0.060	V	1
			1.8 V ≤ $V_{OUT(S)}$ < 2.0 V	–	0.040	0.050	V	1
			2.0 V ≤ $V_{OUT(S)}$ < 2.5 V	–	0.030	0.040	V	1
			2.5 V ≤ $V_{OUT(S)}$ < 2.8 V	–	0.020	0.030	V	1
			2.8 V ≤ $V_{OUT(S)}$ < 3.0 V	–	0.019	0.021	V	1
			3.0 V ≤ $V_{OUT(S)}$ ≤ 3.5 V	–	0.018	0.020	V	1
Line regulation	$\frac{\Delta V_{OUT1}}{\Delta V_{IN} \bullet V_{OUT}}$	$V_{OUT(S)} + 0.5$ V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 10 mA		–	0.05	0.2	%/V	1
Load regulation	ΔV_{OUT2}	$V_{IN} = V_{OUT(S)} + 1.0$ V, 1 μA ≤ I_{OUT} ≤ 50 mA		–	20	40	mV	1
Output voltage temperature coefficient*4	$\frac{\Delta V_{OUT}}{\Delta Ta \bullet V_{OUT}}$	$V_{IN} = V_{OUT(S)} + 1.0$ V, I_{OUT} = 10 mA, −40°C ≤ Ta ≤ +85°C		–	±130	–	ppm/°C	1
Current consumption during operation	I_{SS1}	$V_{IN} = V_{OUT(S)} + 1.0$ V, no load		–	0.35	0.53	μA	2
Input voltage	V_{IN}	–		1.5	–	5.5	V	–
Short-circuit current	I_{short}	$V_{IN} = V_{OUT(S)} + 1.0$ V, V_{OUT} = 0 V		–	60	–	mA	3

***1.** $V_{OUT(S)}$: Set output voltage
$V_{OUT(E)}$: Actual output voltage
Output voltage when fixing I_{OUT} (= 10 mA) and inputting $V_{OUT(S)} + 1.0$ V

***2.** The output current at which the output voltage becomes 95% of $V_{OUT(E)}$ after gradually increasing the output current.

***3.** $V_{drop} = V_{IN1} - (V_{OUT3} \times 0.98)$
V_{IN1} is the input voltage at which the output voltage becomes 98% of V_{OUT3} after gradually decreasing the input voltage.
V_{OUT3} is the output voltage when $V_{IN} = V_{OUT(S)} + 1.0$ V and I_{OUT} = 10 mA.

***4.** A change in the temperature of the output voltage [mV/°C] is calculated using the following equation.

$$\frac{\Delta V_{OUT}}{\Delta Ta}\ [\text{mV/°C}]^{*1} = V_{OUT(S)}\ [\text{V}]^{*2} \times \frac{\Delta V_{OUT}}{\Delta Ta \bullet V_{OUT}}\ [\text{ppm/°C}]^{*3} \div 1000$$

***1.** Change in temperature of output voltage
***2.** Set output voltage
***3.** Output voltage temperature coefficient

***5.** Due to limitation of the power dissipation, this value may not be satisfied. Attention should be paid to the power dissipation when the output current is large.
This specification is guaranteed by design.

2. Supply voltage divider block

Table 15

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Output voltage*1	$V_{PMOUT(S)}$	V_{IN} = 3.6 V, −10 μA ≤ I_{PMOUT} ≤ 10 μA	S-1740 Series	–	V_{IN}/2	–	V	4
			S-1741 Series	–	V_{IN}/3	–	V	4
Load current	I_{PMOUT}	V_{IN} = 3.6 V		−10	–	10	μA	–
Output offset voltage	V_{POF}	V_{IN} = 3.6 V, −10 μA ≤ I_{PMOUT} ≤ 10 μA		−30	–	30	mV	4
Output impedance	R_{PS}	V_{IN} = 3.6 V, −10 μA ≤ I_{PMOUT} ≤ 10 μA		–	–	1000	Ω	4
Set-up time	t_{PU}	S-1740/1741 Series A / C type, V_{IN} = 3.6 V, C_{PM} = 220 nF, no load		–	5	10	ms	4
Current consumption during operation*2	I_{SS1P}	V_{IN} = 3.6 V, when supply voltage divided output is enabled, no load		–	0.15	0.23	μA	5
Input voltage	V_{IN}	–		1.5	–	5.5	V	–
PMEN pin input voltage "H"	V_{PSH}	S-1740/1741 Series A / C type	V_{IN} = 3.6 V, determined by V_{PMOUT} output level	1.0	–	–	V	6
PMEN pin input voltage "L"	V_{PSL}		V_{IN} = 3.6 V, determined by V_{PMOUT} output level	–	–	0.25	V	6
PMEN pin input current "H"	I_{PSH}		V_{IN} = 3.6 V, V_{PMEN} = V_{IN}	−0.1	–	0.1	μA	6
PMEN pin input current "L"	I_{PSL}		V_{IN} = 3.6 V, V_{PMEN} = 0 V	−0.1	–	0.1	μA	6
Discharge shunt resistance during power-off	R_{PLOW}	S-1740/1741 Series A / C type, V_{IN} = 3.6 V, when supply voltage divided output is disabled, V_{PMOUT} = 0.1 V		–	2.8	–	kΩ	7

***1.** $V_{PMOUT(S)}$: Set output voltage
$V_{PMOUT(S)} + V_{POF}$: Actual output voltage

***2.** Increased current value from the current consumption during operation (I_{SS1}) of the regulator block when the supply voltage divided output is enabled.

■ Test Circuits

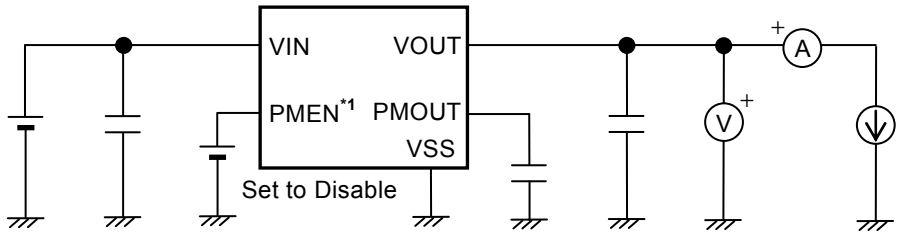


Figure 6 Test Circuit 1

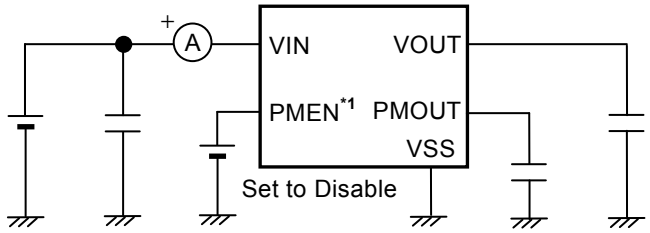


Figure 7 Test Circuit 2

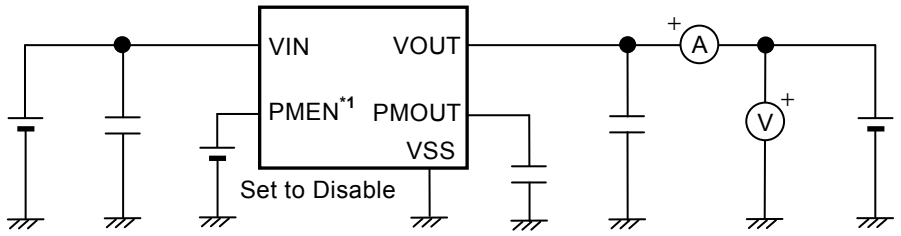


Figure 8 Test Circuit 3

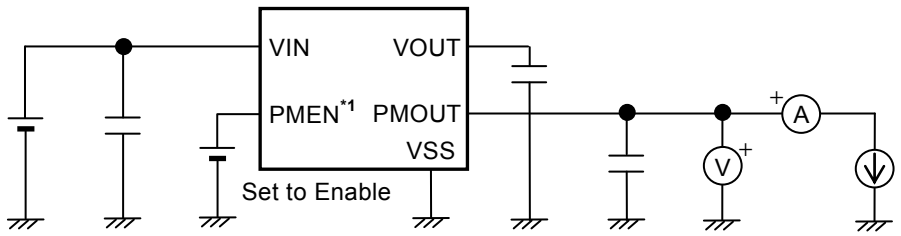


Figure 9 Test Circuit 4

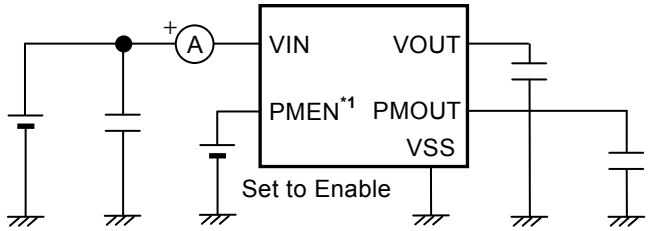


Figure 10 Test Circuit 5

***1.** Only S-1740/1741 Series A / C type

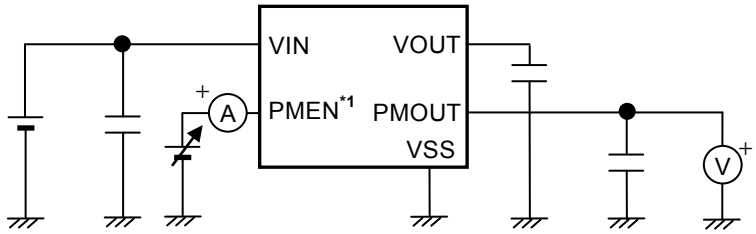


Figure 11 Test Circuit 6

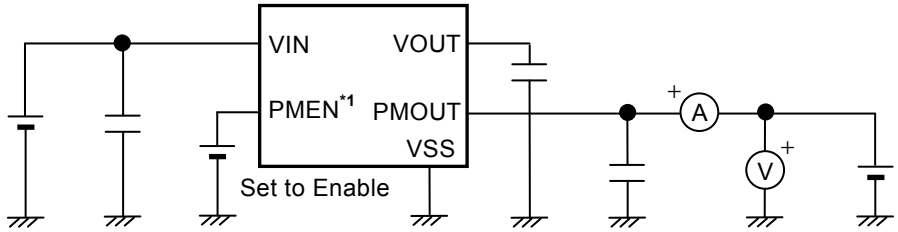
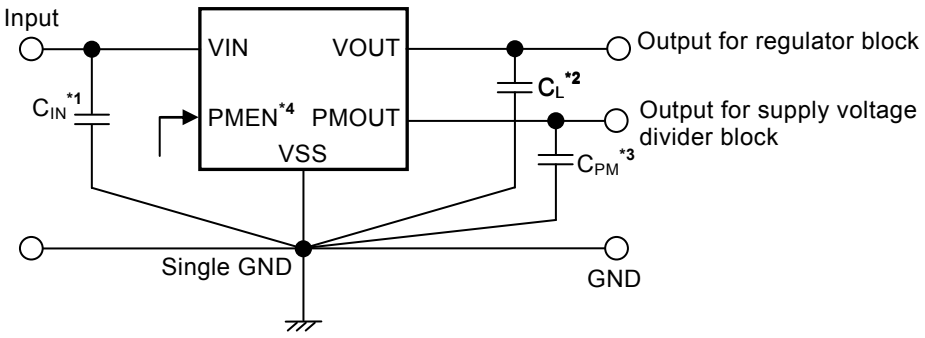


Figure 12 Test Circuit 7

1. Only S-1740/1741 Series A / C type

■ Standard Circuit



1. C_{IN} is a capacitor for stabilizing the input.
2. C_L is a capacitor for stabilizing the output.
3. C_{PM} is a capacitor for stabilizing the output.
4. Only S-1740/1741 Series A / C type

Figure 13

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics with an actual application to set the constants.

■ Condition of Application

Input capacitor (C_{IN}):	A ceramic capacitor with capacitance of 1.0 μF or more is recommended.
Output capacitor (C_L):	A ceramic capacitor with capacitance of 1.0 μF to 100 μF is recommended.
Output capacitor (C_{PM}):	A ceramic capacitor with capacitance of 100 nF to 220 nF is recommended.

Caution Generally, in a voltage regulator, an oscillation may occur depending on the selection of the external parts. Perform thorough evaluation including the temperature characteristics with an actual application using the above capacitors to confirm no oscillation occurs.

■ Selection of Regulator Block Input Capacitor (C_{IN}) and Output Capacitor (C_L)

The S-1740/1741 Series requires C_L between the VOUT pin and the VSS pin for regulator phase compensation.
The operation is stabilized by a ceramic capacitor with capacitance of 1.0 μF to 100 μF. When using an OS capacitor, a tantalum capacitor or an aluminum electrolytic capacitor, the capacitance must also be 1.0 μF to 100 μF. However, an oscillation may occur depending on the equivalent series resistance (ESR).
Moreover, the S-1740/1741 Series requires C_{IN} between the VIN pin and the VSS pin for a stable operation.
Generally, an oscillaiton may occur when a voltage regulator is used under the conditon that the impedance of the power supply is high. Note that the output voltage transient characteristics vary depending on the capacitance of C_{IN} and C_L and the value of ESR.

Caution Perform thorough evaluation including the temperature characteristics with an actual application to select C_{IN}, C_L.

■ Selection of Supply Voltage Divider Block Output Capacitor (C_{PM})

The S-1740/1741 Series requires C_{PM} between the PMOUT pin and the VSS pin for supply voltage divider phase compensation.
The operation is stabilized by a ceramic capacitor with capacitance of 100 nF to 220 nF. When using an OS capacitor, a tantalum capacitor or an aluminum electrolytic capacitor, the capacitance must also be 100 nF to 220 nF. However, an oscillation may occur depending on ESR.
Note that the output voltage transient characteristics vary depending on the capacitance of C_{PM} and the value of ESR.

Caution Perform thorough evaluation including the temperature characteristics with an actual application to select C_{PM}.

■ Explanation of Terms

1. Regulator block

1. 1 Output voltage (V_{OUT})

This voltage is output at an accuracy of ±1.0% or ±15 mV[*2] when the input voltage, the output current and the temperature are in a certain condition[*1].

***1.** Differs depending on the product.
***2.** When V_{OUT} < 1.5 V: ±15 mV, when V_{OUT} ≥ 1.5 V: ±1.0%

Caution If the certain condition is not satisfied, the output voltage may exceed the accuracy range of ±1.0% or ±15 mV. Refer to Table 14 in "■ Electrical Characteristics" for details.

1. 2 Line regulation $\left(\frac{\Delta V_{OUT1}}{\Delta V_{IN} \bullet V_{OUT}}\right)$

Indicates the dependency of the output voltage against the input voltage. The value shows how much the output voltage changes due to a change in the input voltage after fixing output current constant.

1. 3 Load regulation (ΔV_{OUT2})

Indicates the dependency of the output voltage against the output current. The value shows how much the output voltage changes due to a change in the output current after fixing input voltage constant.

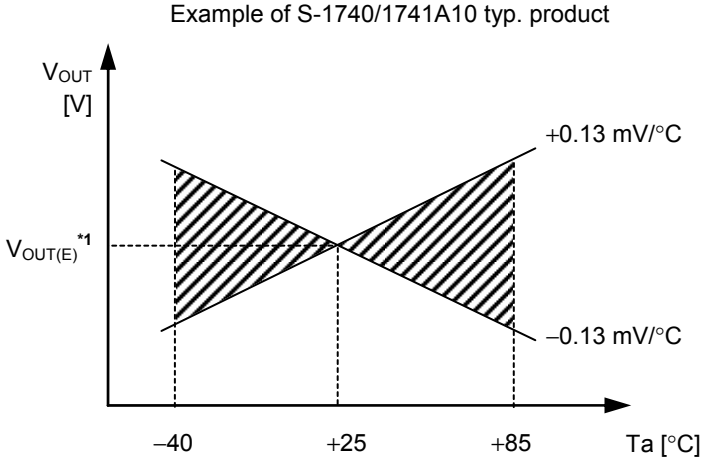
1. 4 Dropout voltage (V_{drop})

Indicates the difference between input voltage (V_{IN1}) and the output voltage when the output voltage becomes 98% of the output voltage value (V_{OUT3}) at V_{IN} = $V_{OUT(S)}$ + 1.0 V after the input voltage (V_{IN}) is decreased gradually.

$V_{drop} = V_{IN1} - (V_{OUT3} \times 0.98)$

1. 5 Output voltage temperature coefficient $\left(\frac{\Delta V_{OUT}}{\Delta Ta \bullet V_{OUT}}\right)$

The shaded area in **Figure 14** is the range where V_{OUT} varies in the operation temperature range when the output voltage temperature coefficient is ±130 ppm/°C.



***1.** $V_{OUT(E)}$ is the value of the output voltage measured at Ta = +25°C.

Figure 14

A change in the temperature of the output voltage [mV/°C] is calculated using the following equation.

$$\frac{\Delta V_{OUT}}{\Delta Ta}\ [mV/°C]^{*1} = V_{OUT(S)}\ [V]^{*2} \times \frac{\Delta V_{OUT}}{\Delta Ta \bullet V_{OUT}}\ [ppm/°C]^{*3} \div 1000$$

***1.** Change in temperature of output voltage
***2.** Set output voltage
***3.** Output voltage temperature coefficient

2. Supply voltage divider block

2. 1 Supply voltage divided output

This is a function that divides the input voltage (V_{IN}) of the regulator into $V_{IN}/2$ or $V_{IN}/3$ and outputs the voltage.
For example, a microcontroller can monitor a battery voltage by inputting output voltage (V_{PMOUT}) to the microcontroller A/D converter.

2. 2 Output voltage (V_{PMOUT})

This is the voltage of the divided V_{IN}, which is $V_{IN}/2$ in the S-1740 Series and $V_{IN}/3$ in the S-1741 Series.

2. 3 Output offset voltage (V_{POF})

This is the supply voltage divider block offset voltage when V_{IN}, the load current and the temperature are in a certain condition.

Caution If the certain condition is not satisfied, the output voltage may exceed the accuracy range of ±30 mV. Refer to "■ Electrical Characteristics" for details.

2. 4 Output impedance (R_{PS})

This is the supply voltage divider block impedance. It shows how much V_{PMOUT} changes when the load current changes.
For example, the output impedance can be used in sampling rate calculation as signal source impedance when V_{PMOUT} from the PMOUT pin is input to the A/D converter as a microcontroller input signal.

2. 5 Set-up time (t_{PU}) (S-1740/1741 Series A / C type)

This is the time from when the supply voltage divided output is enabled until V_{PMOUT} stabilizes.
V_{PMOUT}, V_{POF} and R_{PS} are not guaranteed until the set-up time elapses.

2. 6 Discharge shunt resistance during power-off (R_{PLOW}) (S-1740/1741 Series A / C type)

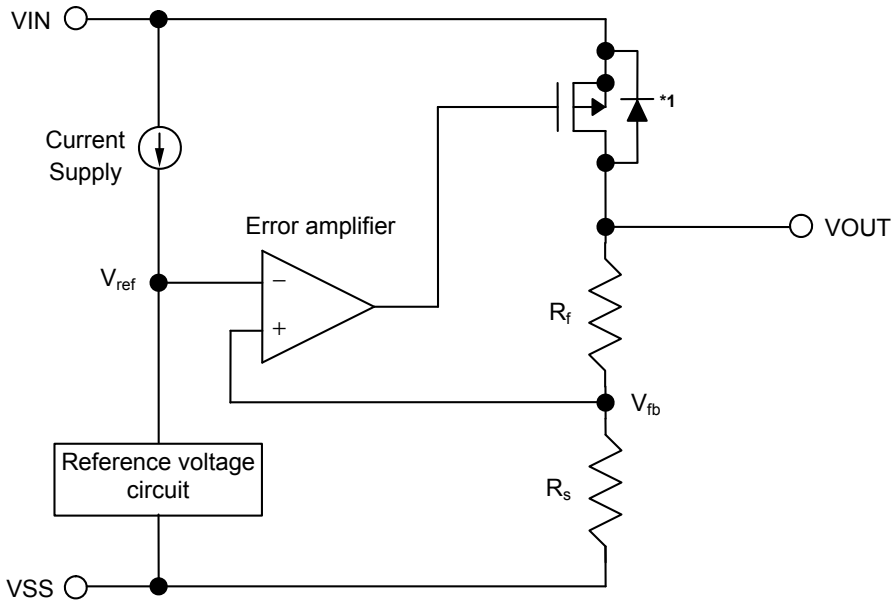
The ON resistance of the N-channel transistor built into the supply voltage divider block.
When the supply voltage divided output is disabled, V_{PMOUT} is set to the V_{SS} level by the built-in N-channel transistor.

■ Operation

1. Regulator block

1. 1 Basic operation

Figure 15 shows the block diagram of the regulator block to describe the basic operation.
The error amplifier compares the feedback voltage (V_{fb}) whose output voltage (V_{OUT}) is divided by the feedback resistors (R_s and R_f) with the reference voltage (V_{ref}). The error amplifier controls the output transistor, consequently, the regulator starts the operation that holds V_{OUT} constant without the influence of the input voltage (V_{IN}).



1. Parasitic diode

Figure 15

1. 2 Output transistor

In the S-1740/1741 Series, a low on-resistance P-channel MOS FET is used between the VIN pin and the VOUT pin as the output transistor. In order to keep V_{OUT} constant, the ON resistance of the output transistor varies appropriately according to the output current (I_{OUT}).

Caution Since a parasitic diode exists between the VIN pin and the VOUT pin due to the structure of the transistor, the IC may be damaged by a reverse current if V_{OUT} becomes higher than V_{IN}. Therefore, be sure that V_{OUT} does not exceed V_{IN} + 0.3 V.

1. 3 Overcurrent protection circuit

The S-1740/1741 Series has a built-in overcurrent protection circuit to limit the overcurrent of the output transistor. When the VOUT pin is shorted to the VSS pin, that is, at the time of the output short-circuit, the output current is limited to 60 mA typ. due to the overcurrent protection circuit operation. The S-1740/1741 Series restarts regulating when the output transistor is released from the overcurrent status.

Caution This overcurrent protection circuit does not work as for thermal protection. For example, when the output transistor keeps the overcurrent status long at the time of output short-circuit or due to other reasons, pay attention to the conditions of the input voltage and the load current so as not to exceed the power dissipation.

2. Supply voltage divider block

2. 1 Basic operation

2. 1. 1 S-1740/1741 Series A / C type

Figure 16 shows the block diagram of the S-1740/1741 Series A / C type to describe basic operation.
Reference voltage (V_{refpm}) is generated by dividing the input voltage (V_{IN}) to $V_{IN}/2$ or $V_{IN}/3$ using the dividing resistance (R_{pm1} and R_{pm2}). Since the buffer amplifier constitutes a voltage follower, it can perform the feedback control so that the output voltage (V_{PMOUT}) and V_{refpm} are the same. Low output impedance is realized by the buffer amplifier, while outputting V_{PMOUT} according to V_{IN}.
When "L" is input to the PMEN pin in the S-1740/1741 Series A type, or "H" is input to the PMEN pin in the C type, the current which flows to R_{pm1} and R_{pm2} and the current which flows to the buffer amplifier can be stopped. The buffer amplifier output is pulled down to V_{SS} by the built-in N-channel transistor, and V_{PMOUT} is set to the V_{SS} level.

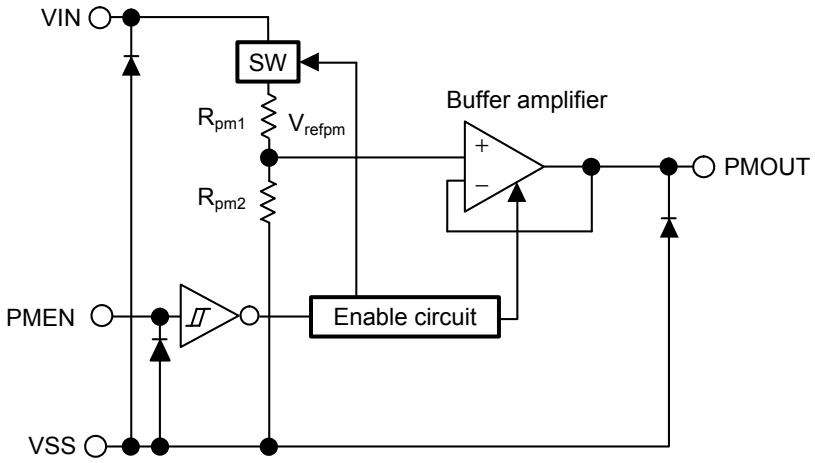


Figure 16

2. 1. 2 S-1740/1741 Series G type

Figure 17 shows the block diagram of the S-1740/1741 Series G type to describe basic operation.
V_{refpm} is made by dividing V_{IN} to $V_{IN}/2$ or $V_{IN}/3$ using R_{pm1} and R_{pm2}. Since the buffer amplifier constitutes a voltage follower, it can perform the feedback control so that V_{PMOUT} and V_{refpm} are the same. Low output impedance is realized by the buffer amplifier, while outputting V_{PMOUT} according to V_{IN}.

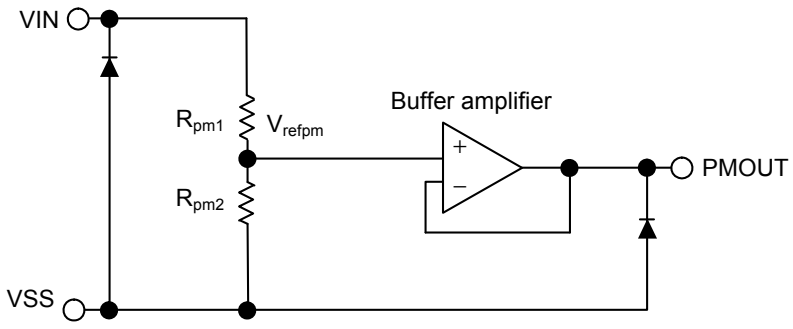


Figure 17

2. 2 PMEN pin

2. 2. 1 S-1740/1741 Series A / C type

The PMEN pin controls the enable circuit.
When "H" is input to the PMEN pin in the S-1740/1741 Series A type, or "L" is input to the PMEN pin in the C type, the enable circuit operates. This enables the supply voltage divided output and allows for monitoring of the power supply voltage. When "L" is input to the PMEN pin in the S-1740/1741 Series A type, or "H" is input to the PMEN pin in the C type, the enable circuit stops. This disables the supply voltage divided output, reducing the IC current consumption.
In addition, the PMEN pin has absolutely no effect on the operation of the regulator block.

Table 16

Product Type	PMEN Pin	Supply Voltage Divided Output	Output Voltage (V_{PMOUT})	Current Consumption	VOUT Pin Voltage
A	"H"	Enable	V_{PMOUT} *1	$I_{SS1} + I_{SS1P}$	V_{OUT}
A	"L"	Disable	V_{SS} level	I_{SS1}	V_{OUT}
C	"L"	Enable	V_{PMOUT} *1	$I_{SS1} + I_{SS1P}$	V_{OUT}
C	"H"	Disable	V_{SS} level	I_{SS1}	V_{OUT}

***1.** Refer to ***1** in **Table 15** in "■ **Electrical Characteristics**".

Figure 18 shows the internal equivalent circuit structure in relation to the PMEN pin. The PMEN pin is neither pulled up nor pulled down, so do not use it in the floating status. When not using the PMEN pin, connect it to the VIN pin. Note that the current consumption increases when a voltage of 0.25 V to V_{IN} – 0.3 V is applied to the PMEN pin.

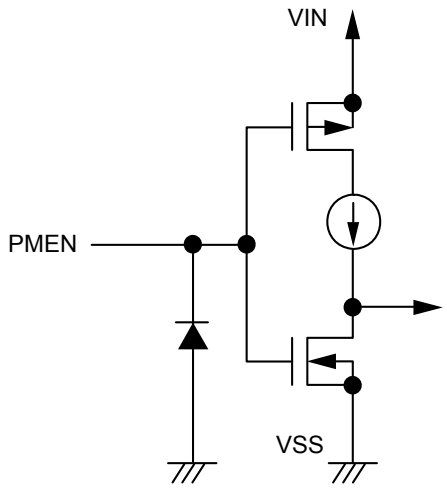


Figure 18

2. 3 PMEN pin voltage and output voltage (V_{PMOUT})

2. 3. 1 S-1740/1741 Series A / C type

Figure 19 shows the relation between the PMEN pin voltage and the supply voltage divided output.
When "H" is input to the PMEN pin in the S-1740/1741 Series A type, or "L" is input to the PMEN pin in the C type, the supply voltage divided output is enabled. Once set-up time (t_{PU}) = 10 ms max.*1 elapses, the output voltage (V_{PMOUT}) will settle and the power supply voltage can be monitored.
When "L" is input to the PMEN pin in the S-1740/1741 Series A type, or "H" is input to the PMEN pin in the C type, the supply voltage divided output is disabled. V_{PMOUT} is set to the V_{SS} level by the built-in N-channel transistor.
By inputting "H" and "L" alternately to the PMEN pin, allowing for minimization of current consumption during the period when the power supply voltage is not monitored.

***1.** When Ta = +25°C, V_{IN} = 3.6 V, C_{PM} = 220 nF, no load

Example of active "H"

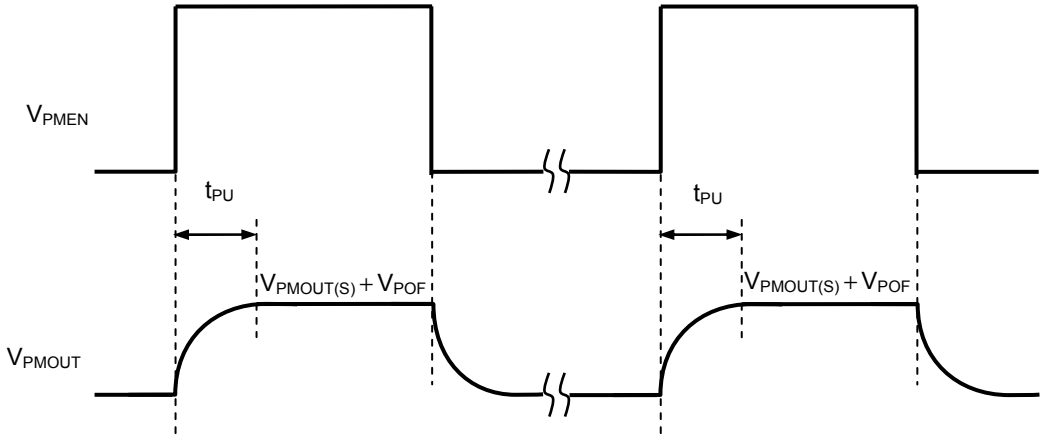


Figure 19

Remark $V_{PMEN} = V_{IN} \leftrightarrow V_{SS}$

■ Typical Application in S-1740/1741 Series A / C Type

Figure 20 shows the circuit diagram of the typical application in the S-1740/1741 Series A / C type, and **Figure 21** shows the timing chart.

As shown in **Figure 20**, connect the PMOUT pin to an analog input pin (AIN pin) of the A/D converter in the microcontroller. The microcontroller can monitor the battery voltage by inputting the output voltage (V_{PMOUT}) to the A/D converter.
The input voltage from the battery is converted to output voltage by the regulator operation, and the microcontroller starts driving with the voltage. The supply voltage divided output can be controlled by inputting "H" and "L" signals output from the microcontroller I/O pin to the PMEN pin. Control the supply voltage divided output according to the A/D converter operation timing.

When inputting "H" to the PMEN pin in the S-1740/1741 Series A type, or "L" to the PMEN pin in the C type, the microcontroller monitors the battery voltage. The IC current consumption can be minimized by inputting "L" to the PMEN pin in the S-1740/1741 Series A type, or "H" to the PMEN pin in the C type when battery voltage is not monitored.

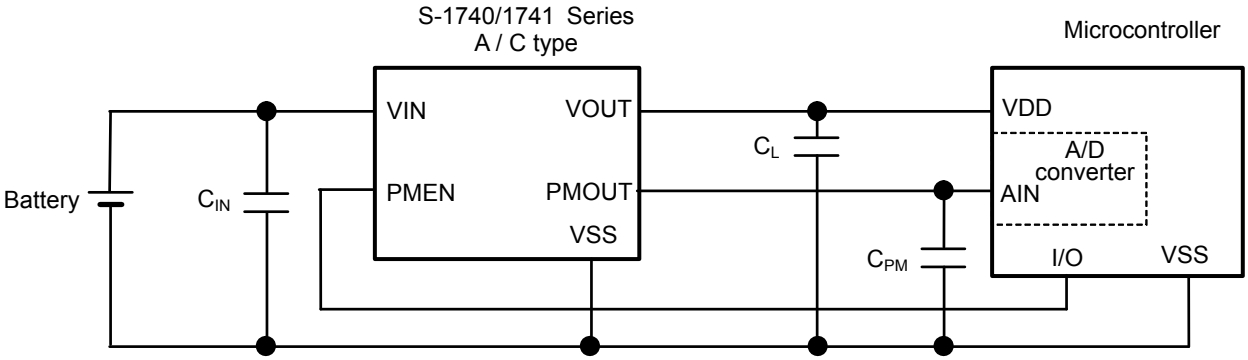


Figure 20

Example of active "H"

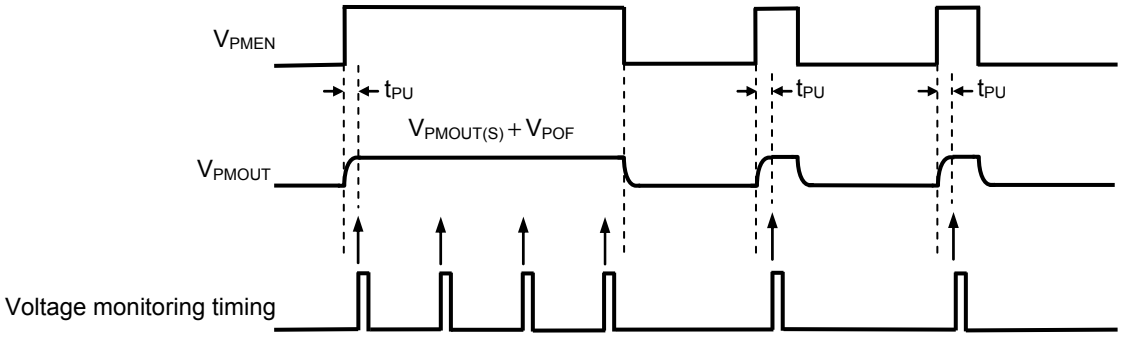


Figure 21

■ Precautions

- Generally, when a voltage regulator is used under the condition that the load current value is small (1.0 μA or less), the output voltage may increase due to the leakage current of an output transistor.
- Generally, when a voltage regulator is used under the condition that the temperature is high, the output voltage may increase due to the leakage current of an output transistor.
- Generally, when a voltage regulator is used under the condition that the impedance of the power supply is high, an oscillation may occur. Perform thorough evaluation including the temperature characteristics with an actual application to select C_{IN}.
- Generally, in a voltage regulator, an oscillation may occur depending on the selection of the external parts. The following use conditions are recommended in the S-1740/1741 Series, however, perform thorough evaluation including the temperature characteristics with an actual application to select C_{IN}, C_L and C_{PM}.

  Input capacitor (C_{IN}): A ceramic capacitor with capacitance of 1.0 μF or more is recommended.
  Output capacitor (C_L): A ceramic capacitor with capacitance of 1.0 μF to 100 μF is recommended.
  Output capacitor (C_{PM}): A ceramic capacitor with capacitance of 100 nF to 220 nF is recommended.

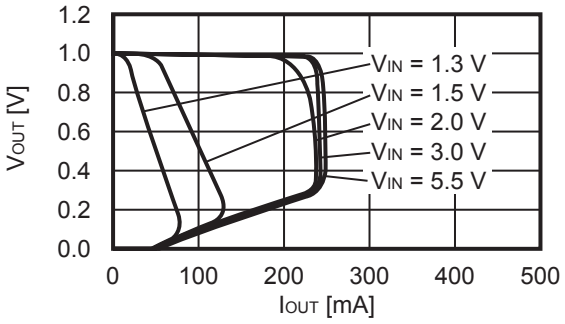
- Generally, in a voltage regulator, the values of an overshoot and an undershoot in the output voltage vary depending on the variation factors of input voltage start-up, input voltage fluctuation and load fluctuation etc., or the capacitance of C_{IN}, C_L or C_{PM} and the value of the equivalent series resistance (ESR), which may cause a problem to the stable operation. Perform thorough evaluation including the temperature characteristics with an actual application to select C_{IN}, C_L and C_{PM}.
- Generally, in a voltage regulator, if the VOUT pin is steeply shorted with GND, a negative voltage exceeding the absolute maximum ratings may occur in the VOUT pin due to resonance phenomenon of the inductance and the capacitance including C_L on the application. The resonance phenomenon is expected to be weakened by inserting a series resistor into the resonance path, and the negative voltage is expected to be limited by inserting a protection diode between the VOUT pin and the VSS pin.
- Make sure of the conditions for the input voltage, output voltage and the load current so that the internal loss does not exceed the power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- When considering the output current value that the IC is able to output, make sure of the output current value specified in **Table 14** in "■ **Electrical Characteristics**" and footnote ***5** of the table.
- Wiring patterns on the application related to the VIN pin, the VOUT pin and the VSS pin should be designed so that the impedance is low. When mounting C_{IN} between the VIN pin and the VSS pin and C_L between the VOUT pin and the VSS pin, connect the capacitors as close as possible to the respective destination pins of the IC.
- In the package equipped with heat sink of backside, mount the heat sink firmly. Since the heat radiation differs according to the condition of the application, perform thorough evaluation with an actual application to confirm no problems happen.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Typical Data)

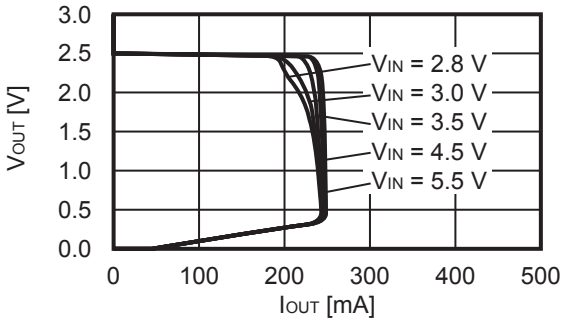
1. Regulator block

1. 1 Output voltage vs. Output current (When load current increases) (Ta = +25°C)

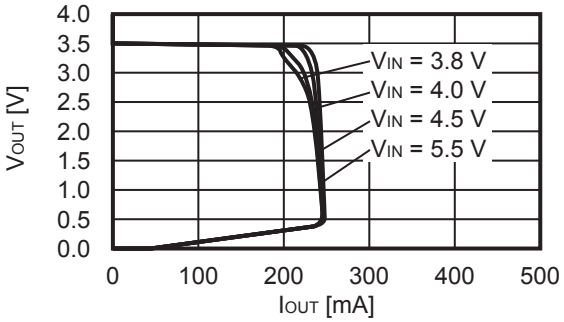
1. 1. 1 V_{OUT} = 1.0 V



1. 1. 2 V_{OUT} = 2.5 V



1. 1. 3 V_{OUT} = 3.5 V

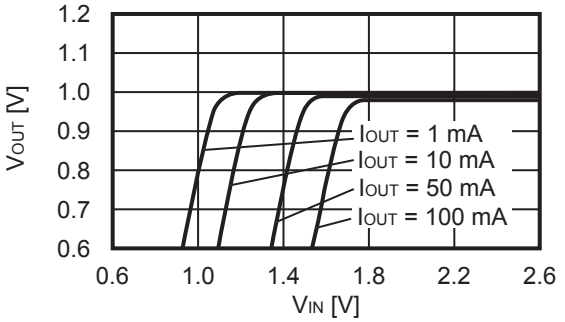


Remark In determining the output current, attention should be paid to the following.

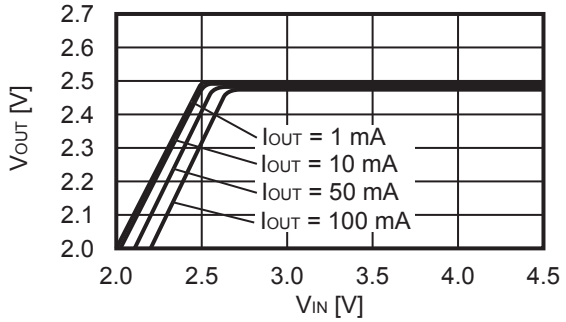
1. The minimum output current value and footnote ***5** of **Table 14** in "■ **Electrical Characteristics**"
2. Power dissipation

1. 2 Output voltage vs. Input voltage (Ta = +25°C)

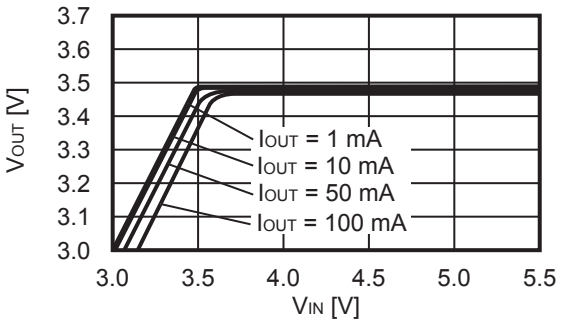
1. 2. 1 V_{OUT} = 1.0 V



1. 2. 2 V_{OUT} = 2.5 V

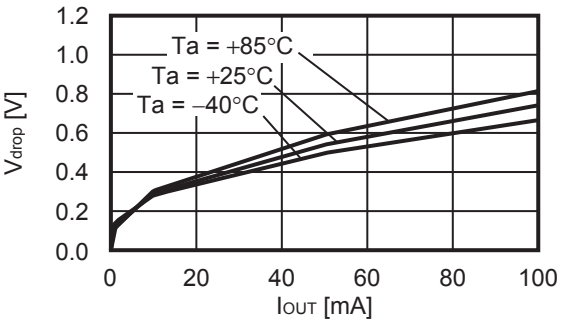


1. 2. 3 V_{OUT} = 3.5 V

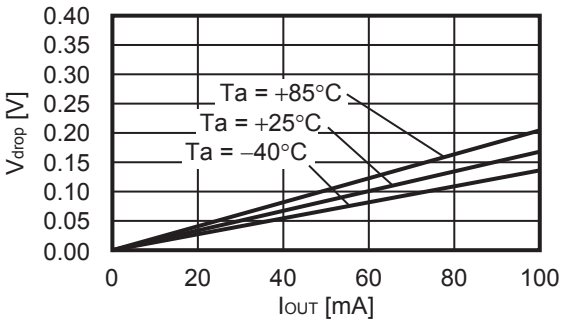


1. 3 Dropout voltage vs. Output current

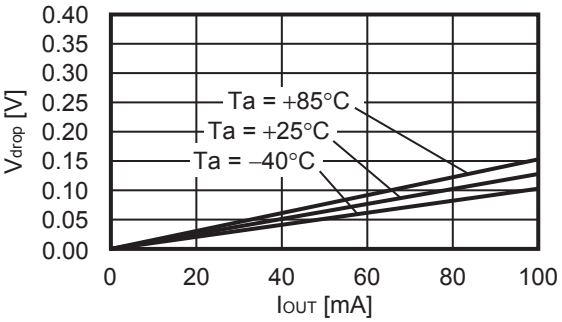
1. 3. 1 V_{OUT} = 1.0 V



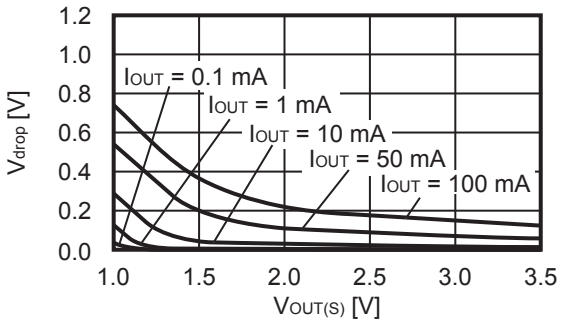
1. 3. 2 V_{OUT} = 2.5 V



1. 3. 3 V_{OUT} = 3.5 V

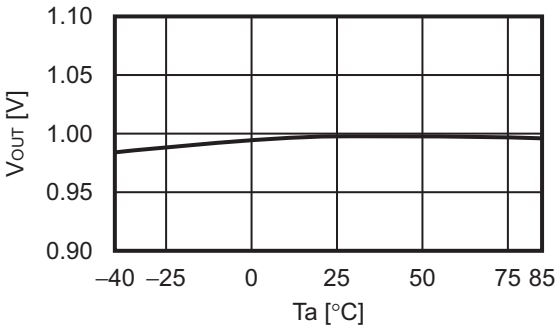


1. 4 Dropout voltage vs. Set output voltage

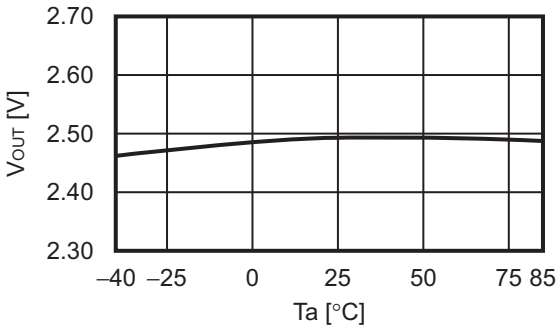


1. 5 Output voltage vs. Ambient temperature

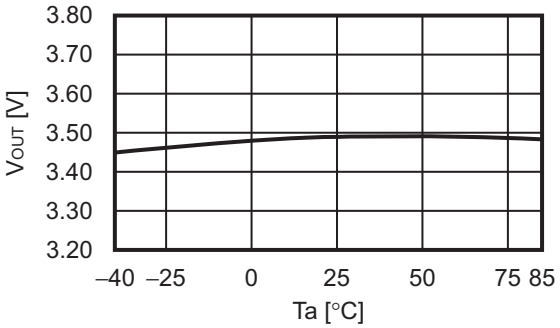
1. 5. 1 V_{OUT} = 1.0 V



1. 5. 2 V_{OUT} = 2.5 V

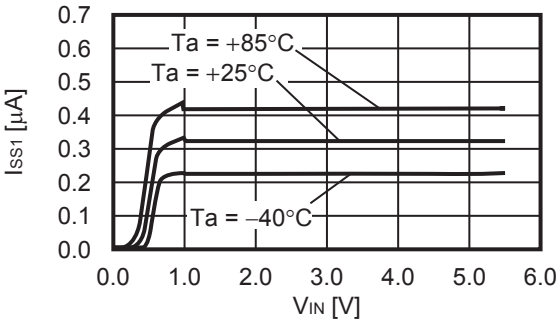


1. 5. 3 V_{OUT} = 3.5 V

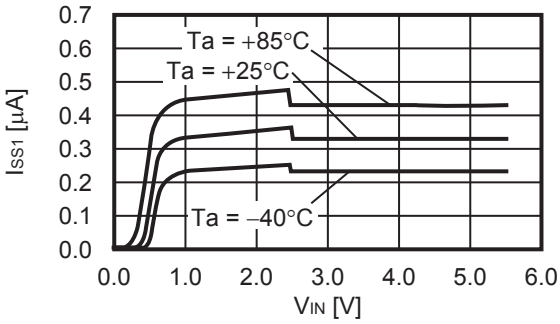


1. 6 Current consumption vs. Input voltage

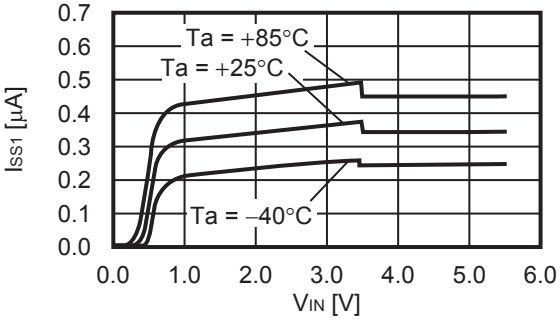
1. 6. 1 V_{OUT} = 1.0 V



1. 6. 2 V_{OUT} = 2.5 V

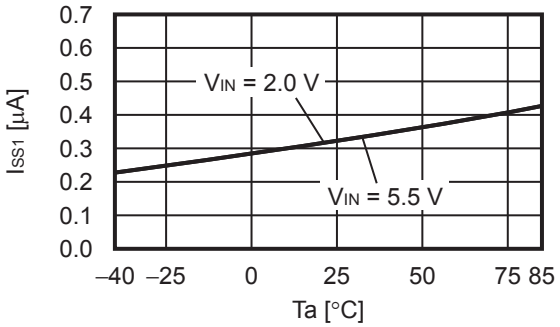


1. 6. 3 V_{OUT} = 3.5 V

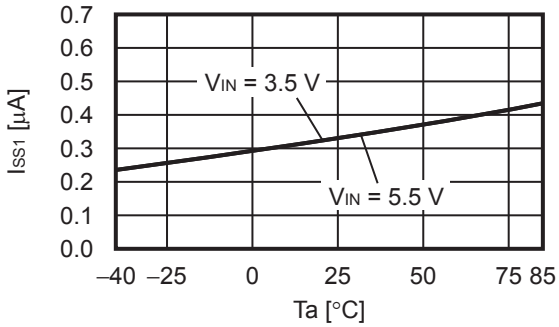


1. 7 Current consumption vs. Ambient temperature

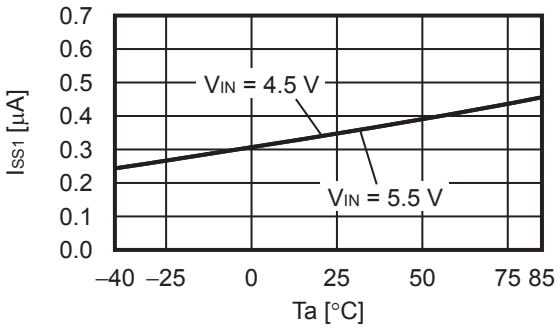
1. 7. 1 V_{OUT} = 1.0 V



1. 7. 2 V_{OUT} = 2.5 V

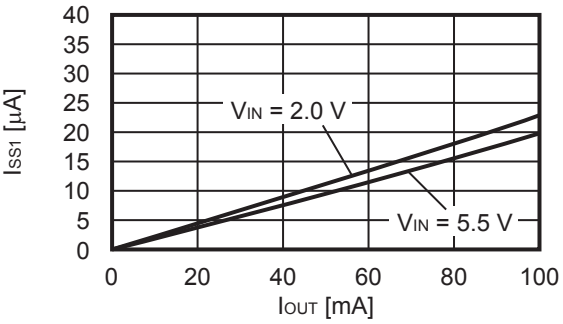


1. 7. 3 V_{OUT} = 3.5 V

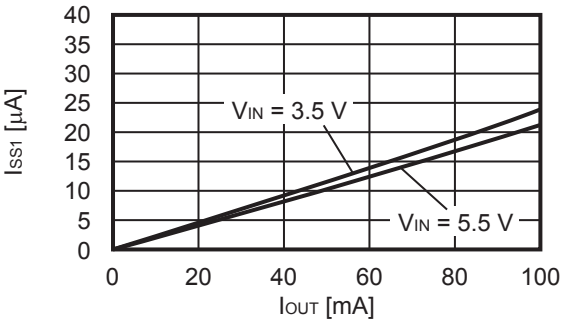


1. 8 Current consumption vs. Output current

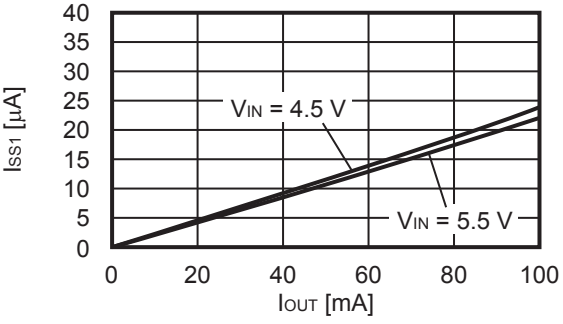
1. 8. 1 V_{OUT} = 1.0 V



1. 8. 2 V_{OUT} = 2.5 V

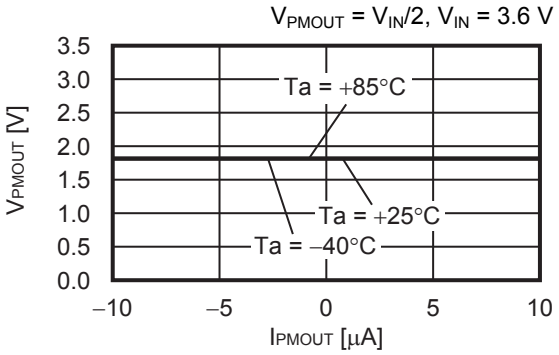


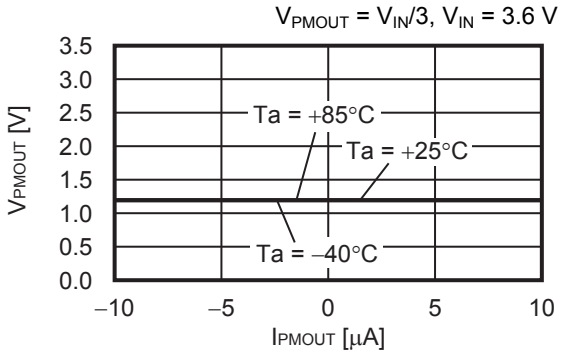
1. 8. 3 V_{OUT} = 3.5 V



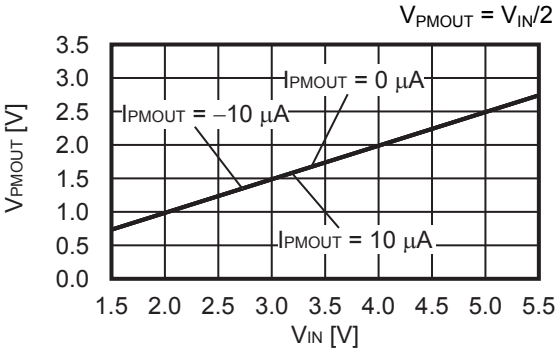
2. Supply voltage divider block

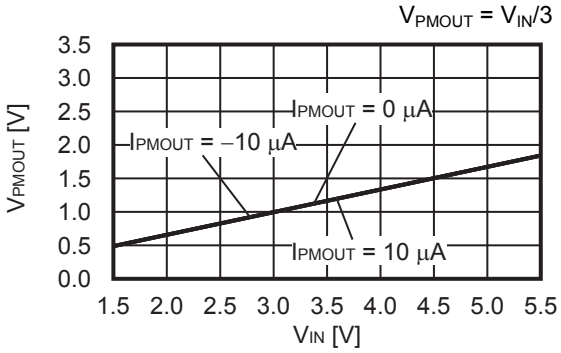
2. 1 Output voltage vs. Load current



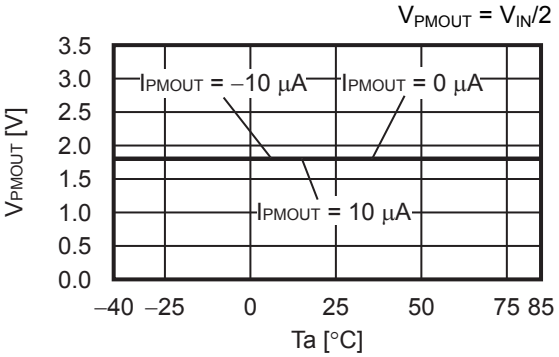


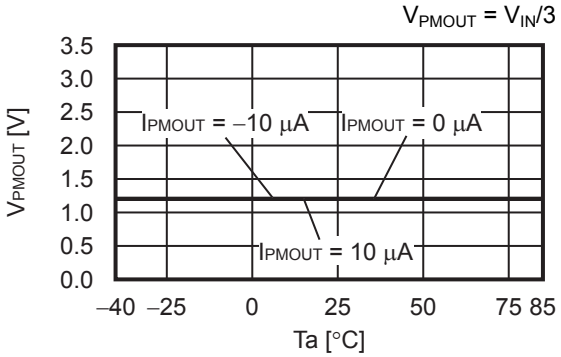
2. 2 Output voltage vs. Input voltage (Ta = +25°C)





2. 3 Output voltage vs. Ambient temperature



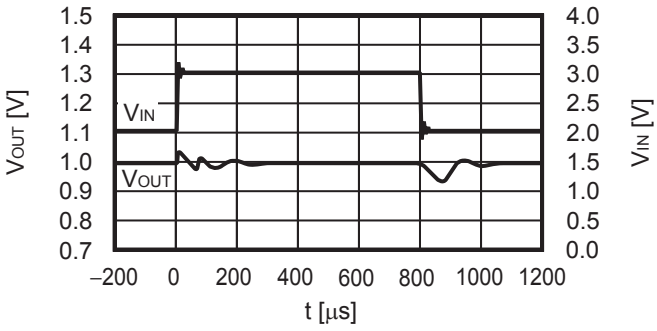


■ Reference Data

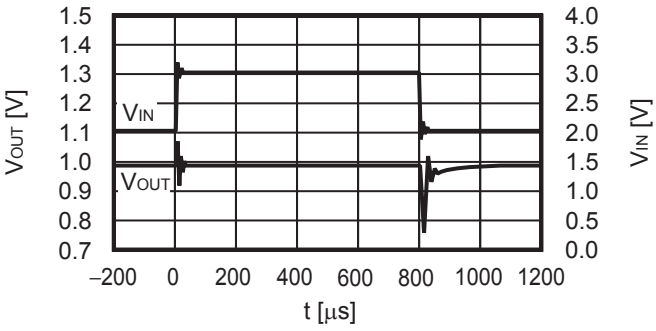
1. Characteristics of input transient response (Ta = +25°C)

1. 1 V_{OUT} = 1.0 V

I_{OUT} = 1 mA, C_{IN} = C_L = 1 µF, V_{IN} = 2.0 V ↔ 3.0 V, t_r = t_f = 5.0 µs

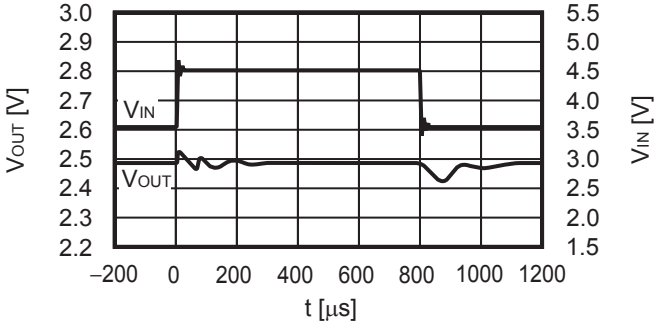


I_{OUT} = 50 mA, C_{IN} = C_L = 1 µF, V_{IN} = 2.0 V ↔ 3.0 V, t_r = t_f = 5.0 µs

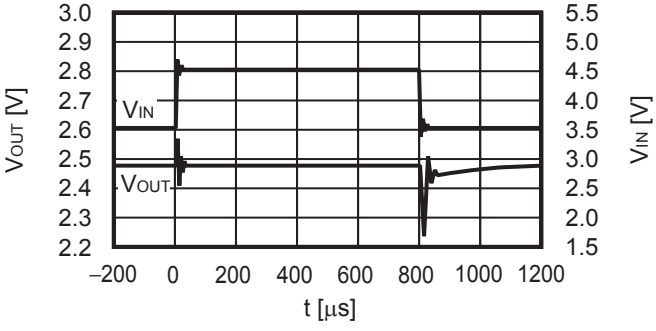


1. 2 V_{OUT} = 2.5 V

I_{OUT} = 1 mA, C_{IN} = C_L = 1 µF, V_{IN} = 3.5 V ↔ 4.5 V, t_r = t_f = 5.0 µs

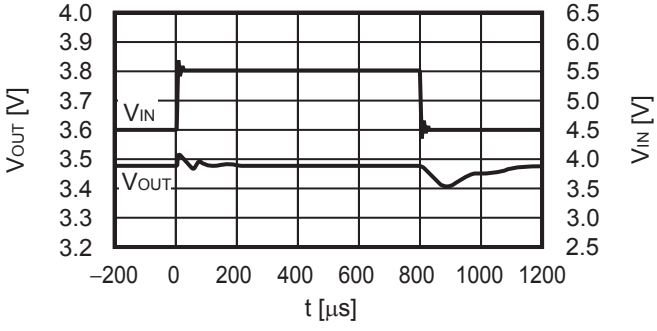


I_{OUT} = 50 mA, C_{IN} = C_L = 1 µF, V_{IN} = 3.5 V ↔ 4.5 V, t_r = t_f = 5.0 µs

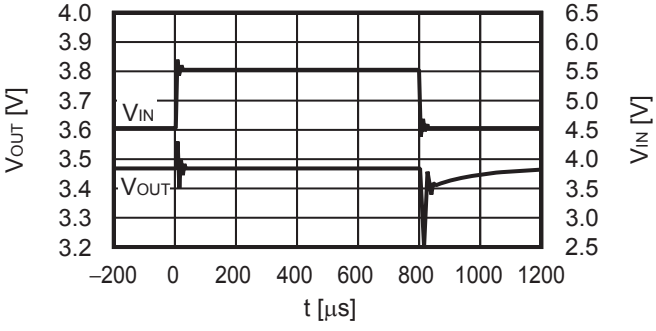


1. 3 V_{OUT} = 3.5 V

I_{OUT} = 1 mA, C_{IN} = C_L = 1 µF, V_{IN} = 4.5 V ↔ 5.5 V, t_r = t_f = 5.0 µs



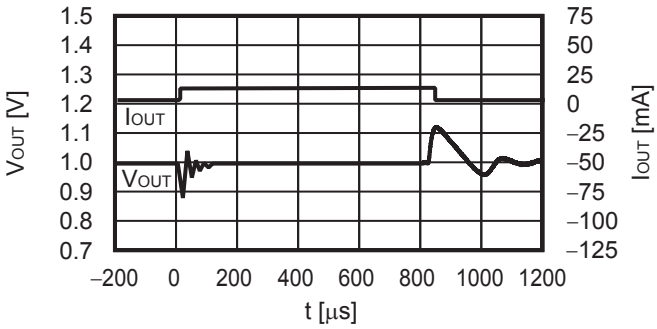
I_{OUT} = 50 mA, C_{IN} = C_L = 1 µF, V_{IN} = 4.5 V ↔ 5.5 V, t_r = t_f = 5.0 µs



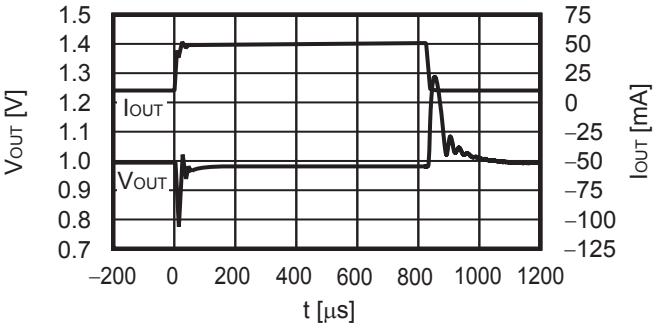
2. Characteristics of load transient response (Ta = +25°C)

2. 1 V_{OUT} = 1.0 V

V_{IN} = 2.0 V, C_{IN} = C_L = 1 µF, I_{OUT} = 1 mA ↔ 10 mA, t_r = t_f = 5.0 µs

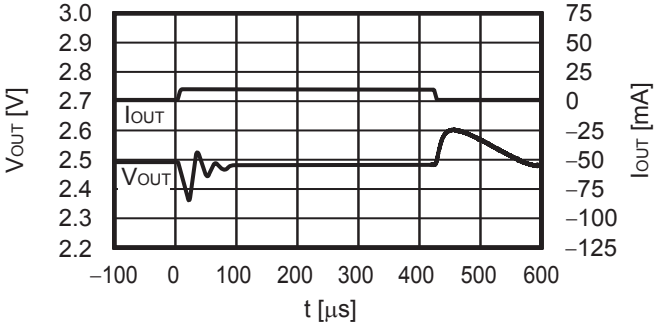


V_{IN} = 2.0 V, C_{IN} = C_L = 1 µF, I_{OUT} = 10 mA ↔ 50 mA, t_r = t_f = 5.0 µs

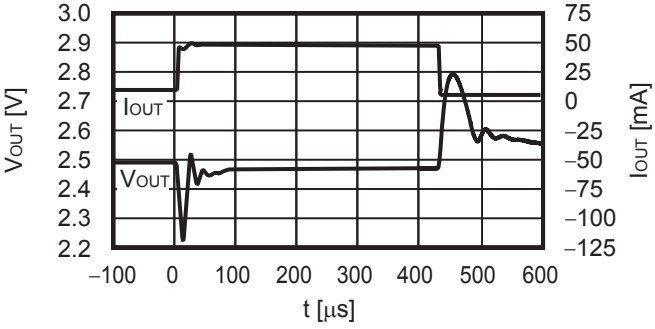


2. 2 V_{OUT} = 2.5 V

V_{IN} = 3.5 V, C_{IN} = C_L = 1 µF, I_{OUT} = 1 mA ↔ 10 mA, t_r = t_f = 5.0 µs

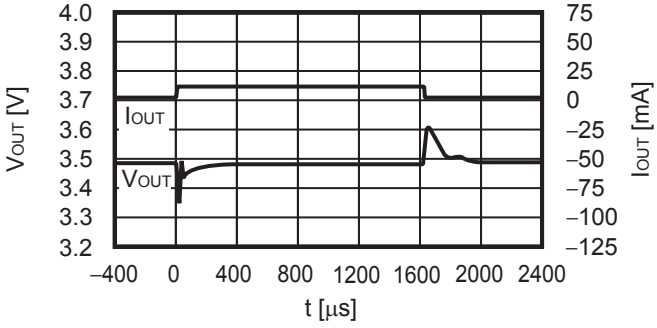


V_{IN} = 3.5 V, C_{IN} = C_L = 1 µF, I_{OUT} = 10 mA ↔ 50 mA, t_r = t_f = 5.0 µs

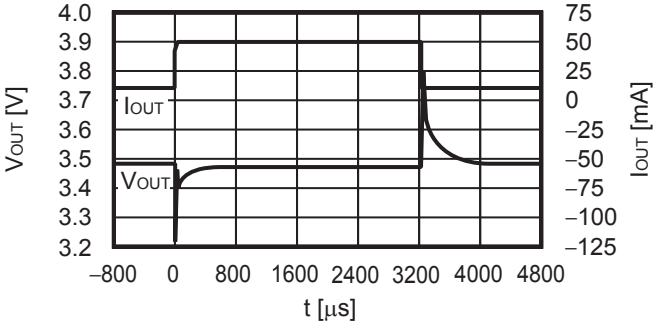


2. 3 V_{OUT} = 3.5 V

V_{IN} = 4.5 V, C_{IN} = C_L = 1 µF, I_{OUT} = 1 mA ↔ 10 mA, t_r = t_f = 5.0 µs



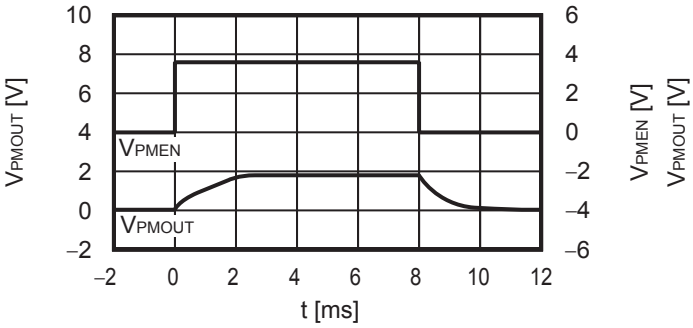
V_{IN} = 4.5 V, C_{IN} = C_L = 1 µF, I_{OUT} = 10 mA ↔ 50 mA, t_r = t_f = 5.0 µs



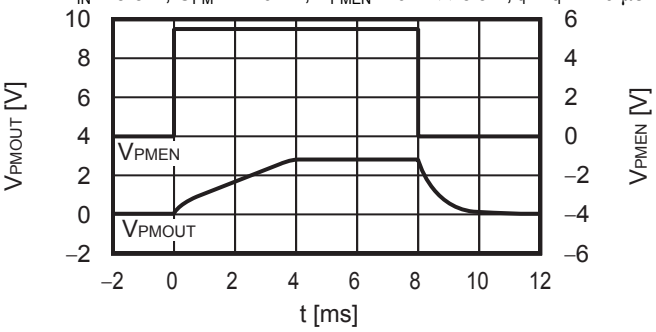
3. Transient response characteristics of PMEN pin (Ta = +25°C)

3. 1 $V_{PMOUT} = V_{IN}/2$

V_{IN} = 3.6 V, C_{PM} = 220 nF, V_{PMEN} = 0 V ↔ 3.6 V, $t_r = t_f$ = 1.0 µs

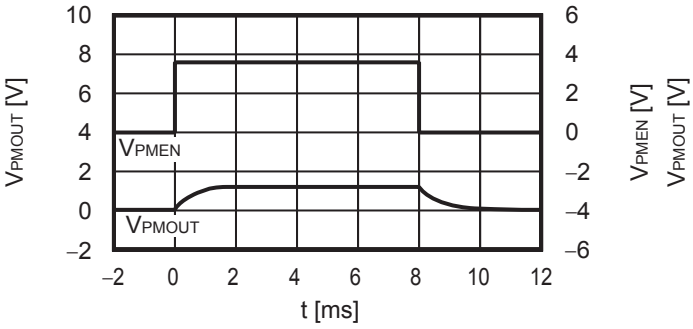


V_{IN} = 5.5 V, C_{PM} = 220 nF, V_{PMEN} = 0 V ↔ 5.5 V, $t_r = t_f$ = 1.0 µs

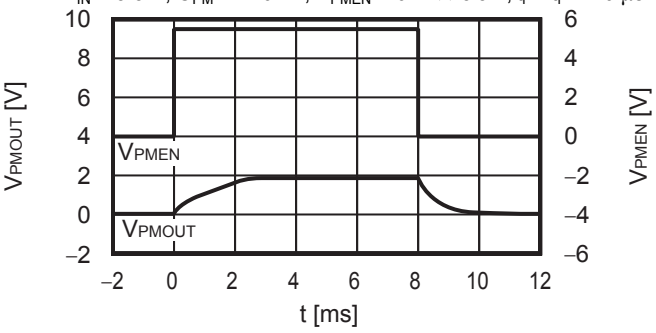


3. 2 $V_{PMOUT} = V_{IN}/3$

V_{IN} = 3.6 V, C_{PM} = 220 nF, V_{PMEN} = 0 V ↔ 3.6 V, $t_r = t_f$ = 1.0 µs



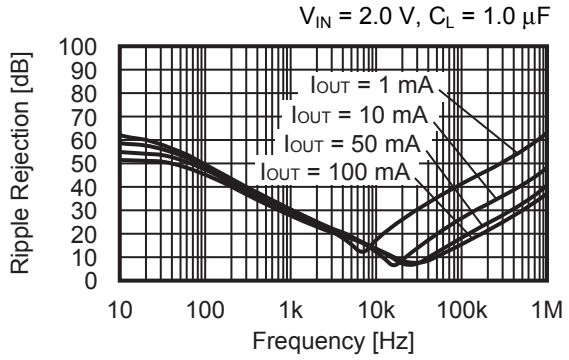
V_{IN} = 5.5 V, C_{PM} = 220 nF, V_{PMEN} = 0 V ↔ 5.5 V, $t_r = t_f$ = 1.0 µs



4. Ripple rejection (Ta = +25°C)

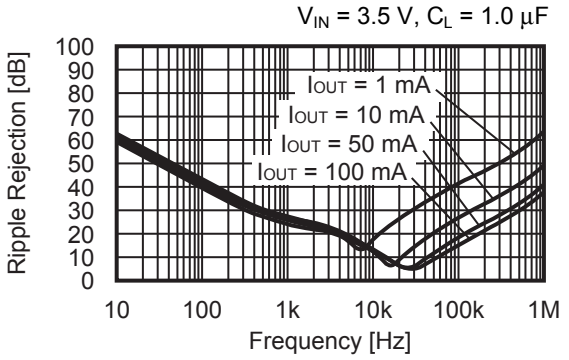
4. 1 V_{OUT} = 1.0 V

V_{IN} = 2.0 V, C_L = 1.0 µF



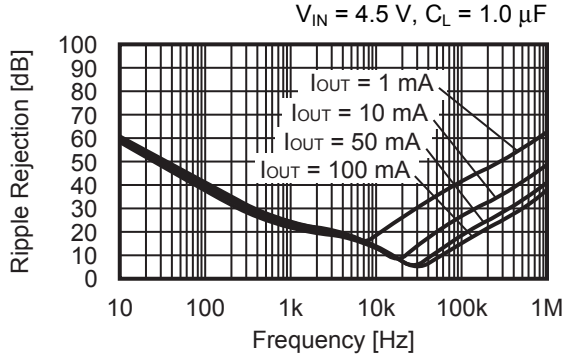
4. 2 V_{OUT} = 2.5 V

V_{IN} = 3.5 V, C_L = 1.0 µF



4. 3 V_{OUT} = 3.5 V

V_{IN} = 4.5 V, C_L = 1.0 µF



5. Example of equivalent series resistance vs. Output current characteristics (Ta = +25°C)

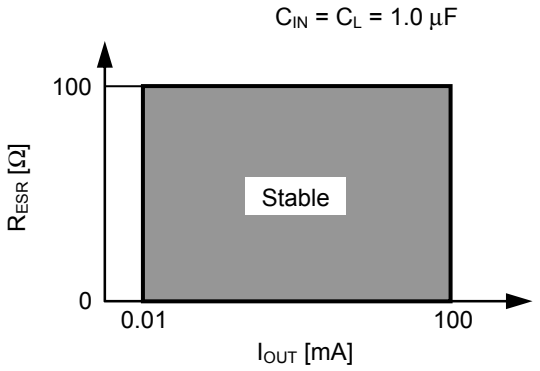


Figure 22

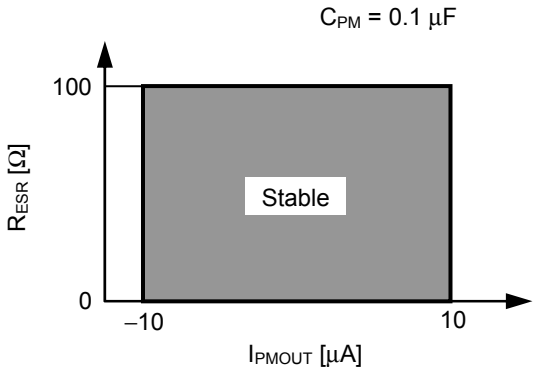
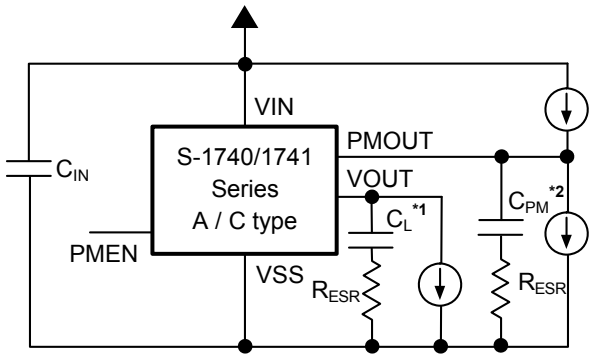
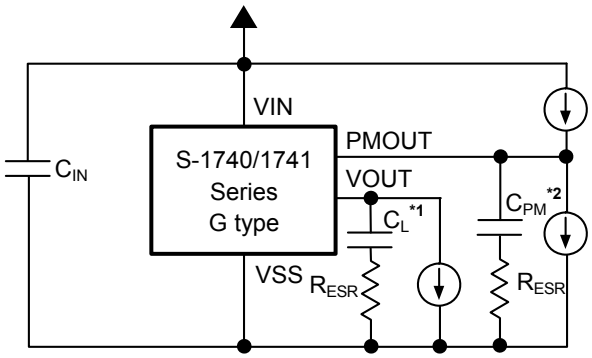


Figure 23



***1.** C_L: TDK Corporation C3216X7R1H105K160AB
***2.** C_{PM}: TDK Corporation C2012X7R1H104K

Figure 24

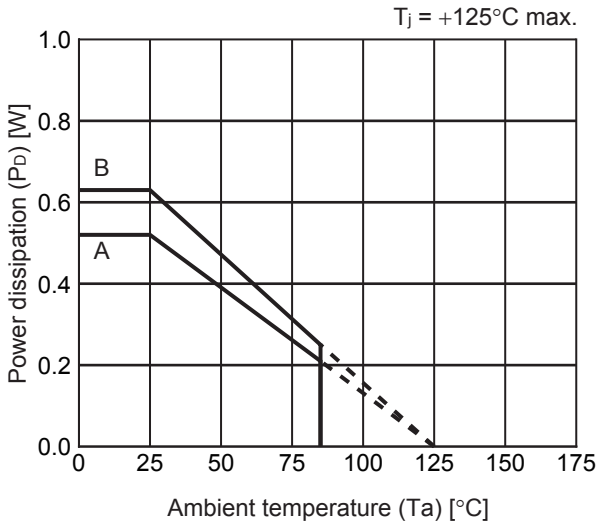


***1.** C_L: TDK Corporation C3216X7R1H105K160AB
***2.** C_{PM}: TDK Corporation C2012X7R1H104K

Figure 25

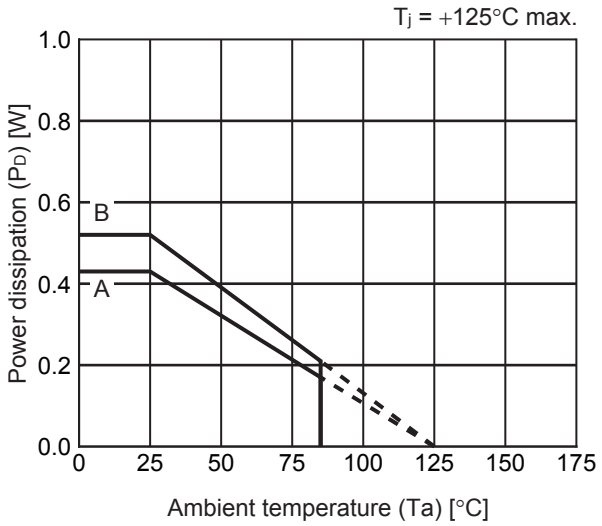
■ Power Dissipation

SOT-23-5



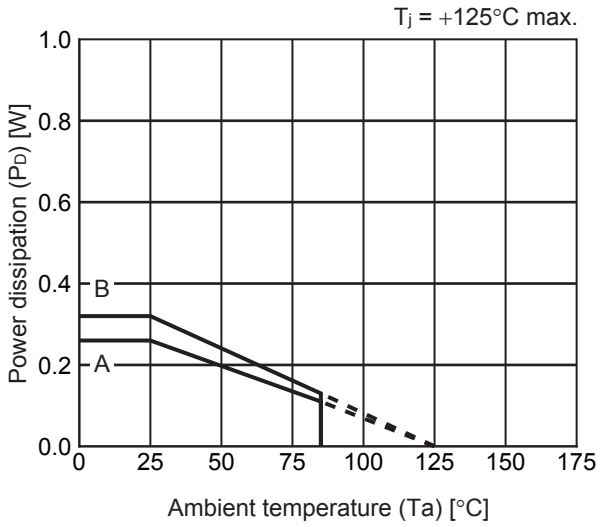
Board	Power Dissipation (P_D)
A	0.52 W
B	0.63 W
C	–
D	–
E	–

HSNT-6(1212)



Board	Power Dissipation (P_D)
A	0.43 W
B	0.52 W
C	–
D	–
E	–

HSNT-4(1010)

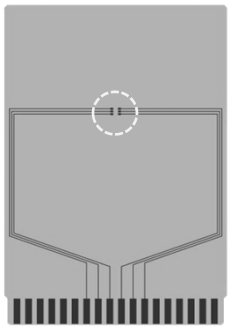


Board	Power Dissipation (P_D)
A	0.26 W
B	0.32 W
C	–
D	–
E	–

SOT-23-3/3S/5/6 Test Board

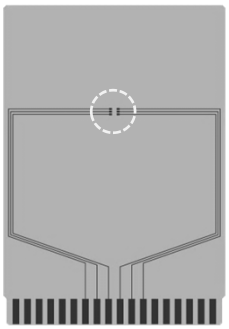
IC Mount Area

(1) Board A



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



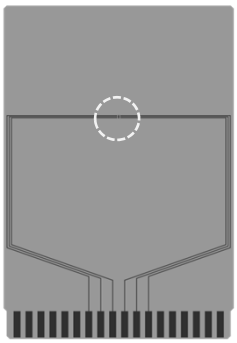
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. SOT23x-A-Board-SD-2.0

HSNT-6(1212) Test Board

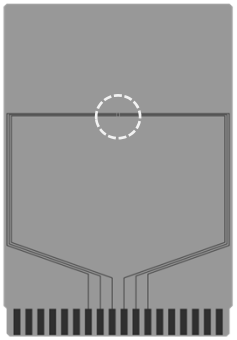
IC Mount Area

(1) Board A



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



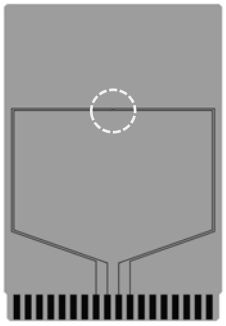
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. HSNT6-A-Board-SD-1.0

HSNT-4(1010) Test Board

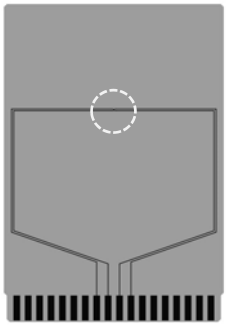
(1) Board A

IC Mount Area



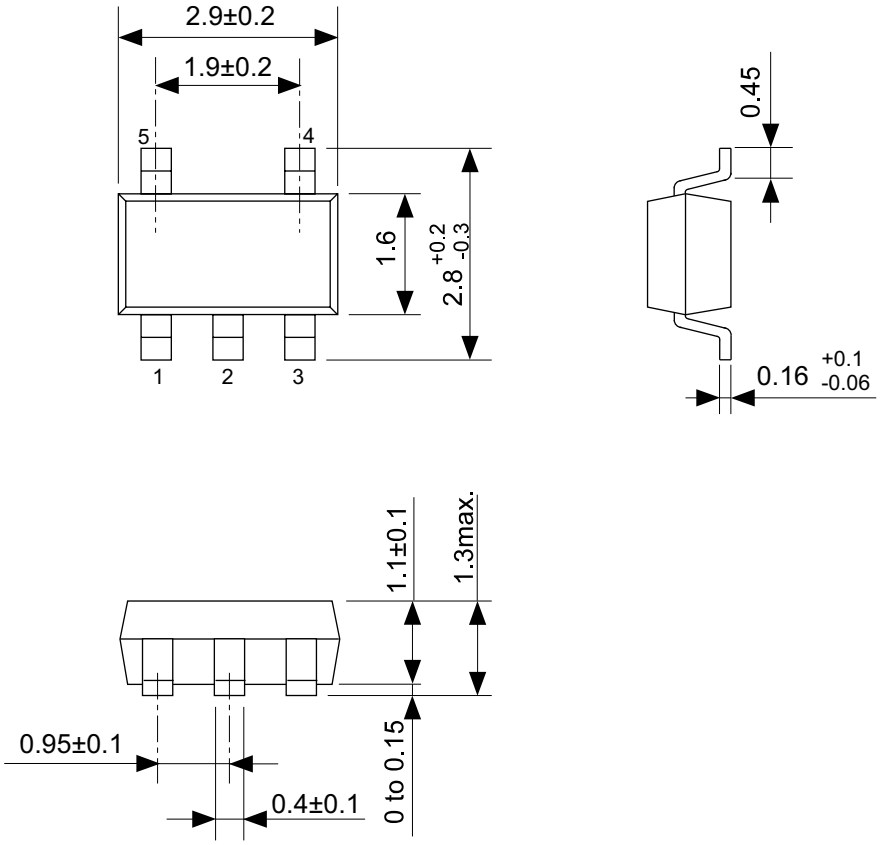
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

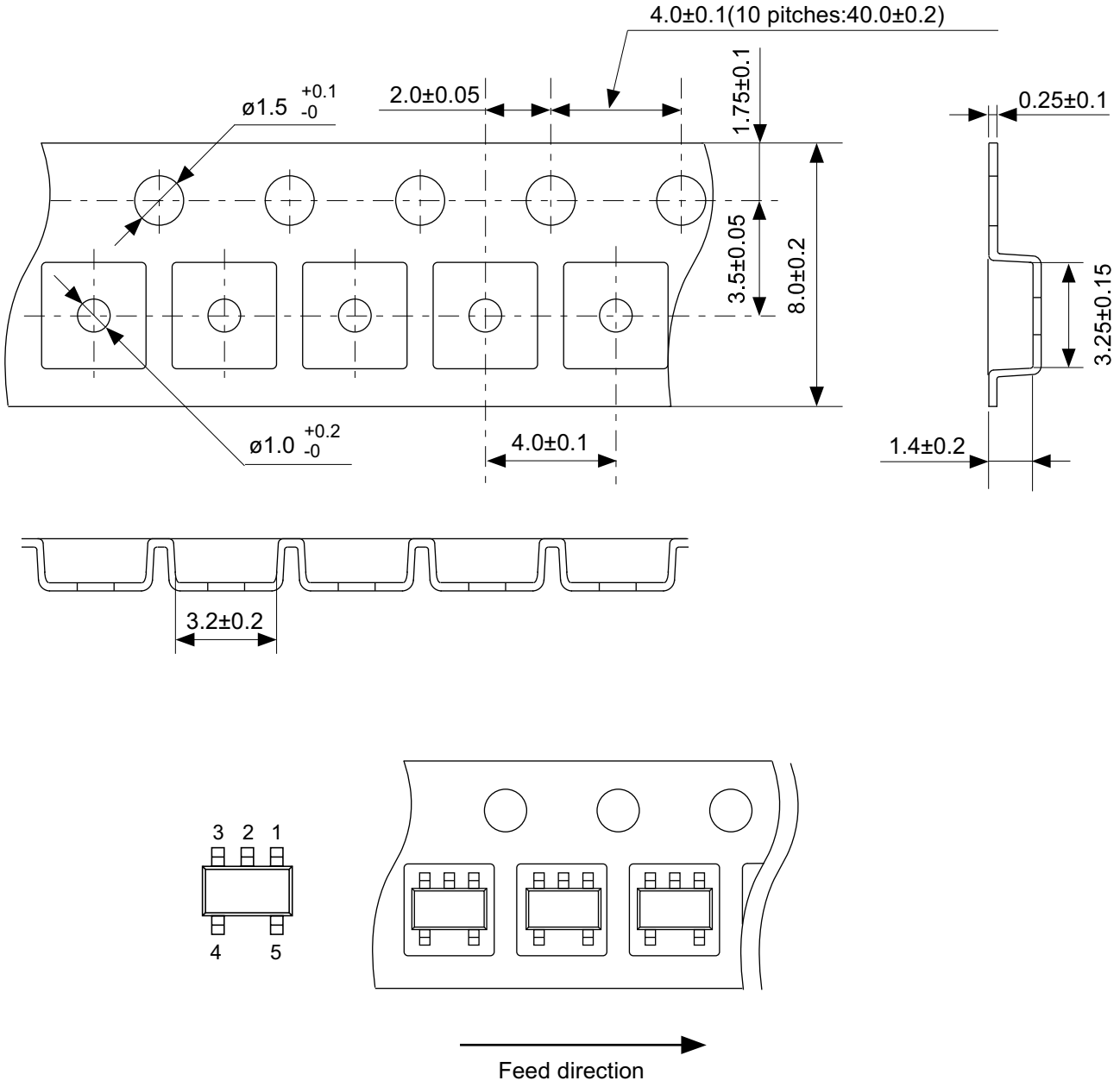
No. HSNT4-B-Board-SD-1.0



No. MP005-A-P-SD-1.3

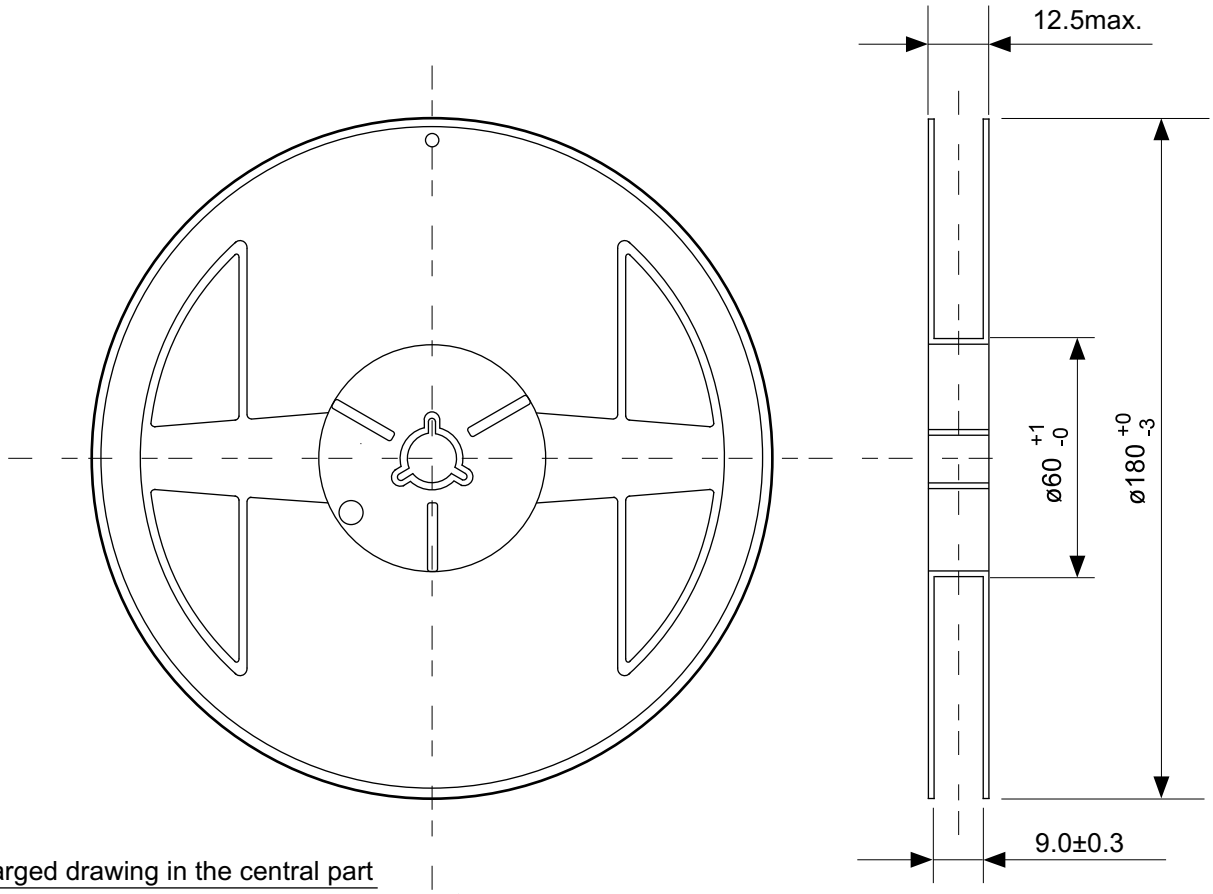
TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.3
ANGLE	
UNIT	mm

ABLIC Inc.

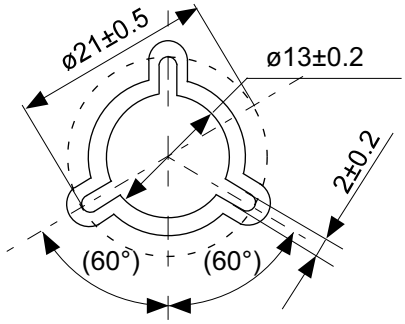


No. MP005-A-C-SD-2.1

TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

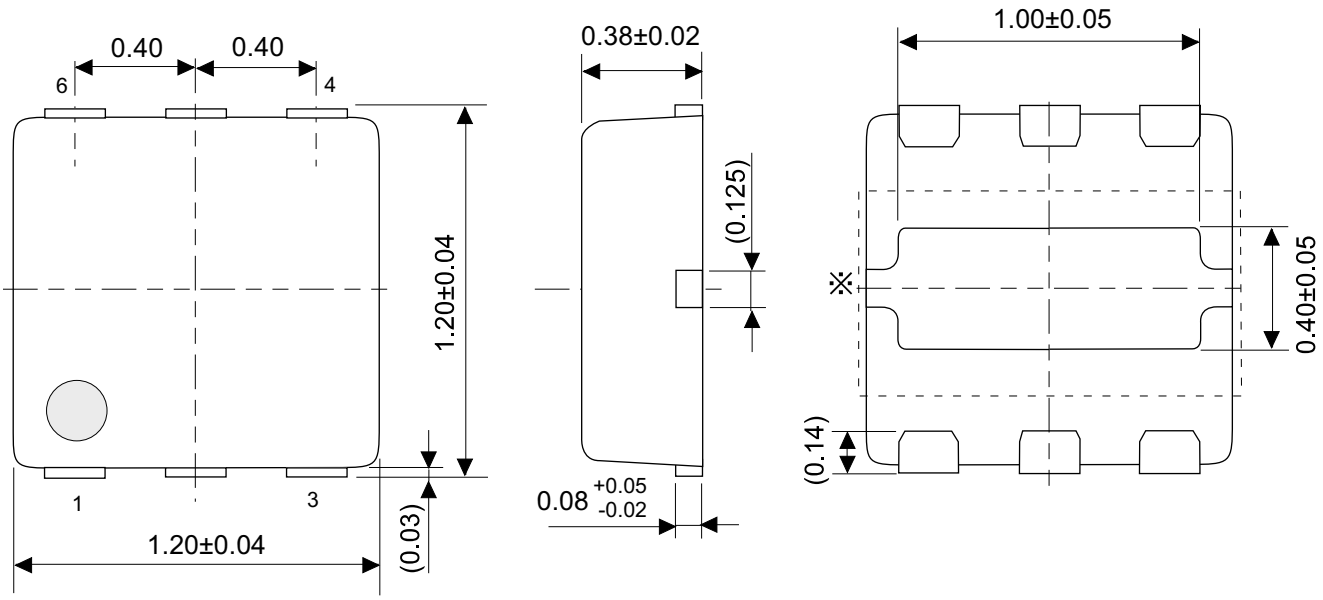


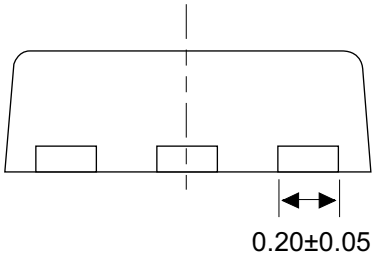
Enlarged drawing in the central part



No. MP005-A-R-SD-1.1

TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-1.1		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			



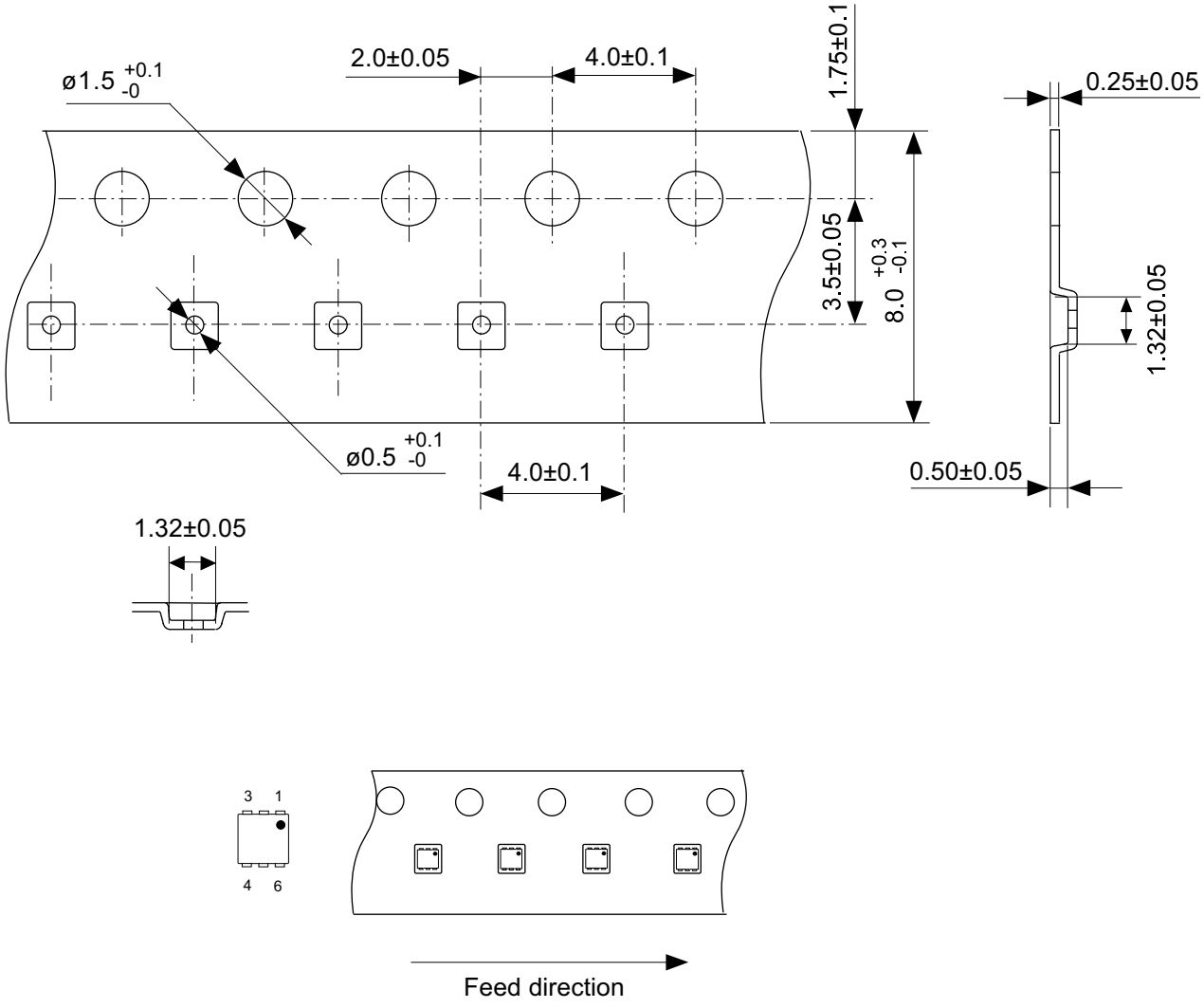


※ The heat sink of back side has different electric potential depending on the product.
Confirm specifications of each product.
Do not use it as the function of electrode.

No. PM006-A-P-SD-1.1

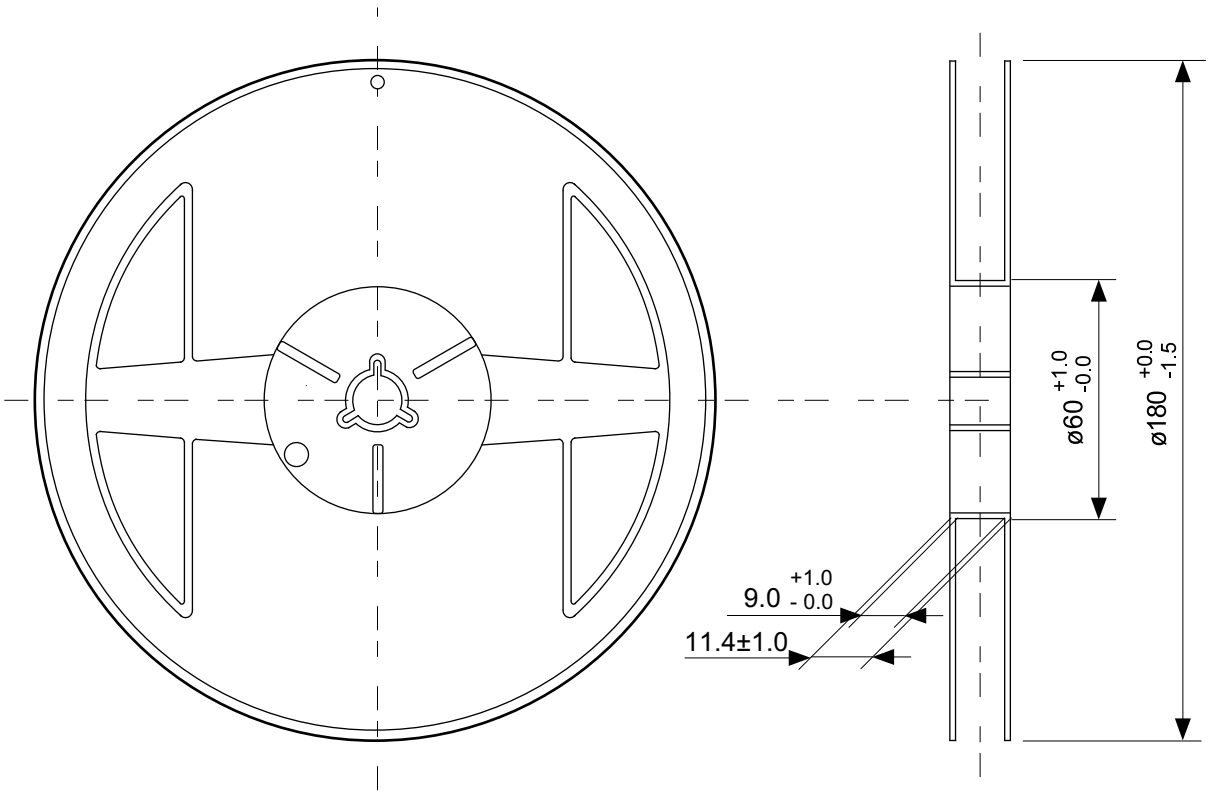
TITLE	HSNT-6-B-PKG Dimensions
No.	PM006-A-P-SD-1.1
ANGLE	
UNIT	mm

ABLIC Inc.

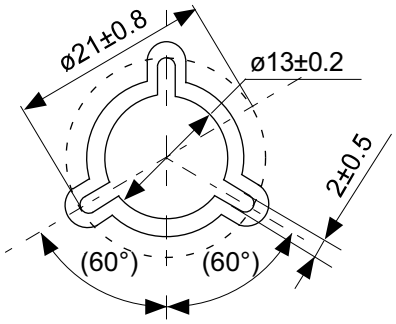


No. PM006-A-C-SD-2.0

TITLE	HSNT-6-B-Carrier Tape
No.	PM006-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



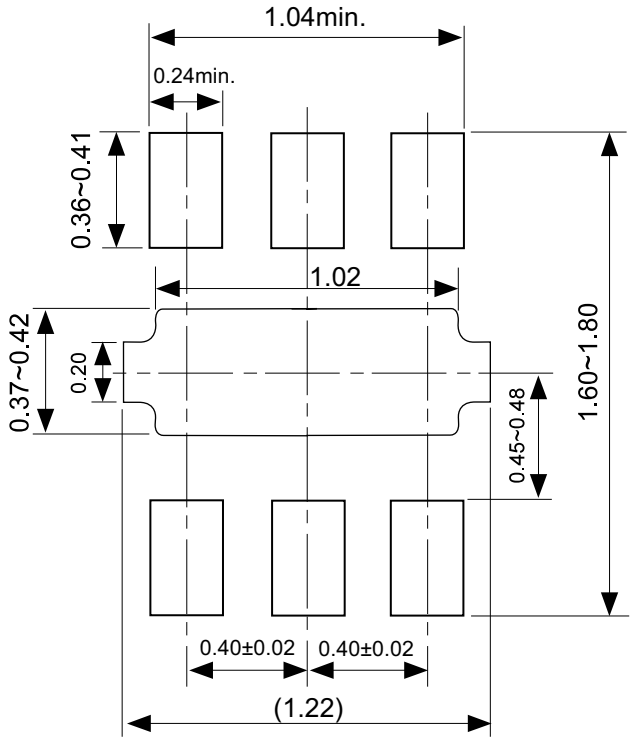
Enlarged drawing in the central part



No. PM006-A-R-SD-1.0

TITLE	HSNT-6-B-Reel		
No.	PM006-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			

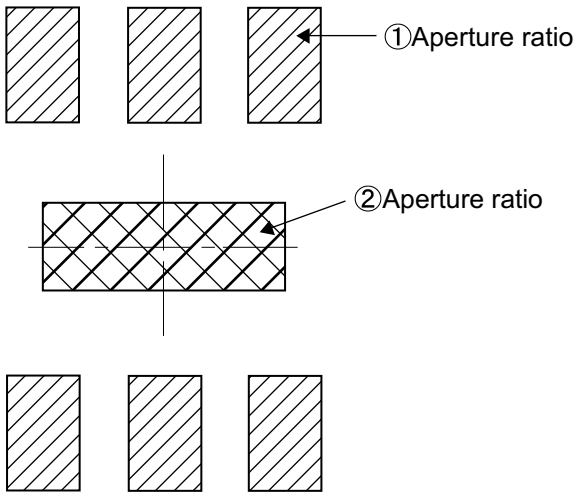
Land Pattern



Caution It is recommended to solder the heat sink to a board in order to ensure the heat radiation.

注意　放熱性を確保する為に、PKGの裏面放熱板（ヒートシンク）を基板に半田付けする事を推奨いたします。

Metal Mask Pattern

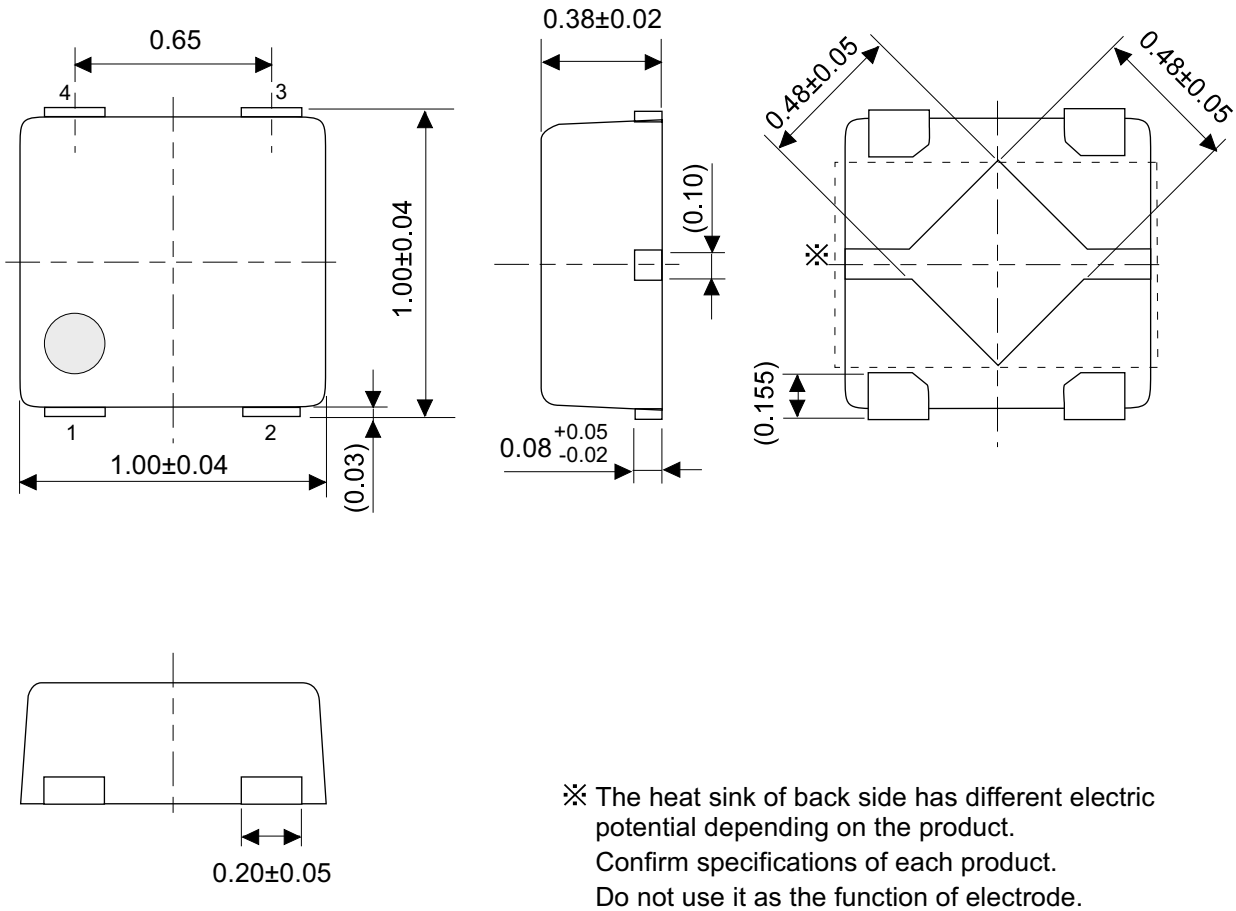


Caution ① Mask aperture ratio of the lead mounting part is 100%.
② Mask aperture ratio of the heat sink mounting part is 40%.
③ Mask thickness: t0.10mm to 0.12 mm

注意 ①リード実装部のマスク開口率は100%です。
②放熱板実装のマスク開口率は40%です。
③マスク厚み：t0.10mm ~ 0.12 mm

No. PM006-A-L-SD-2.0

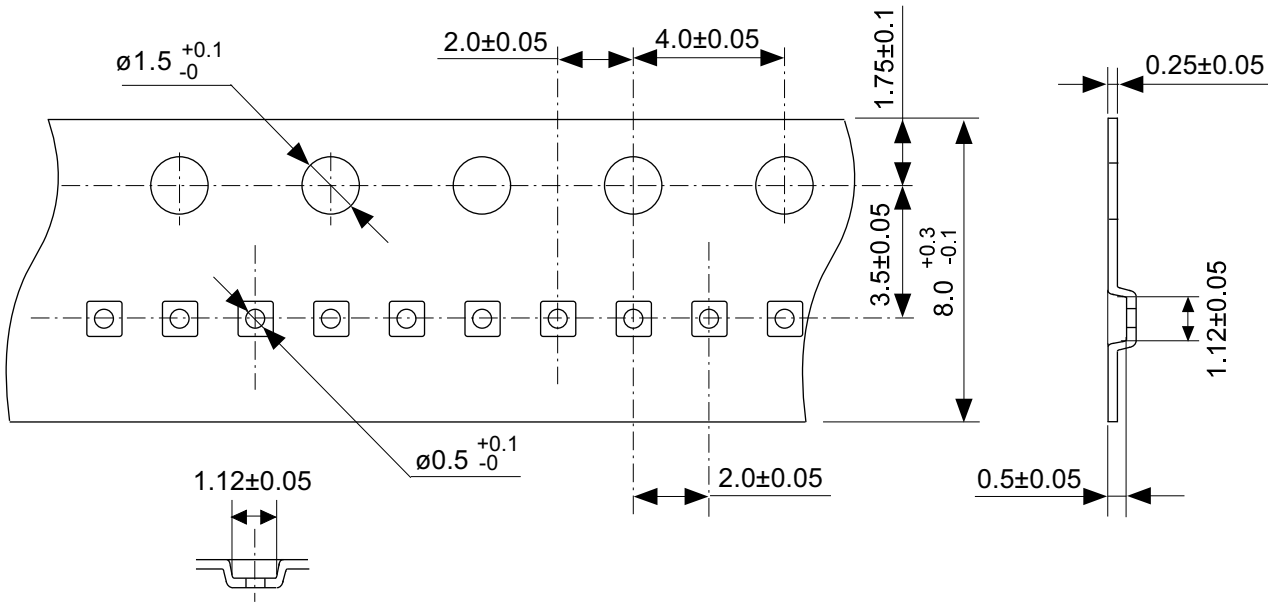
TITLE	HSNT-6-B -Land Recommendation
No.	PM006-A-L-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

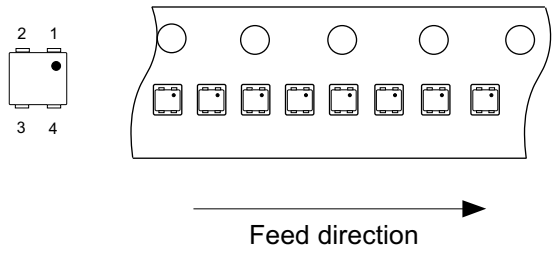


※ The heat sink of back side has different electric potential depending on the product.
Confirm specifications of each product.
Do not use it as the function of electrode.

No. PL004-A-P-SD-1.1

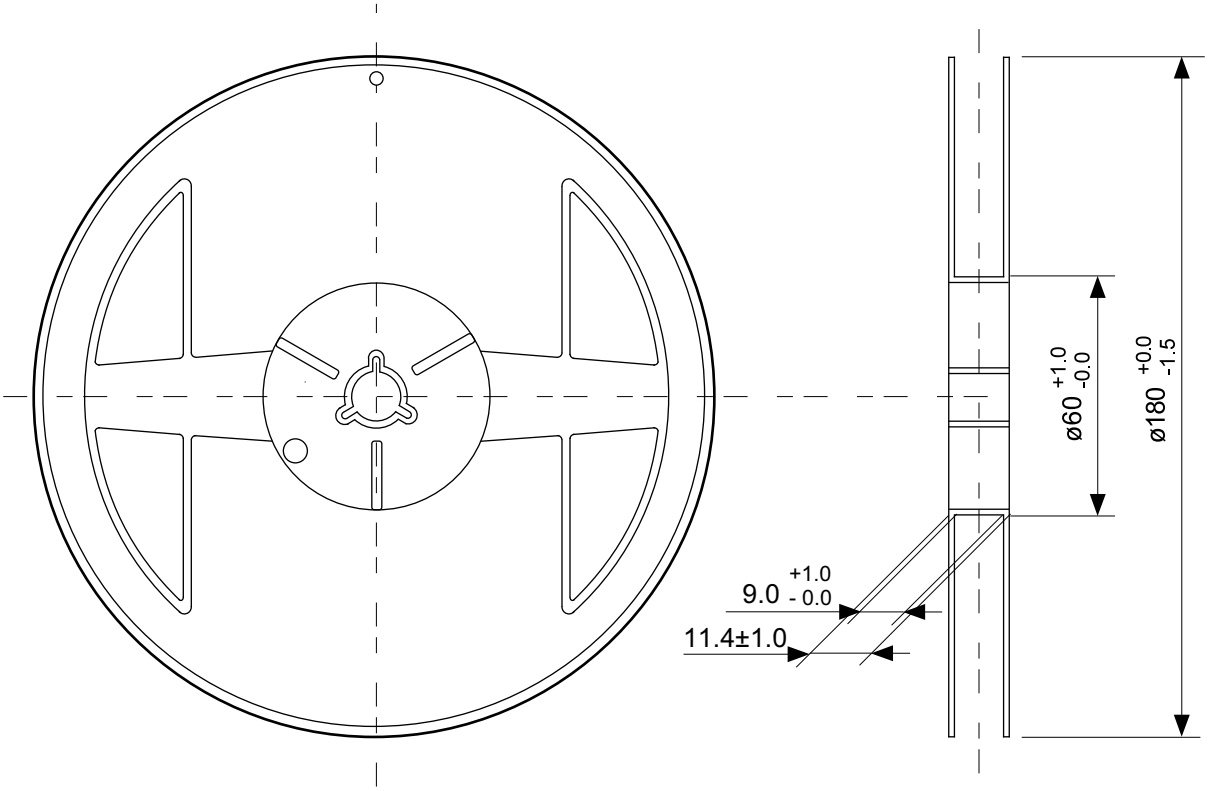
TITLE	HSNT-4-B-PKG Dimensions
No.	PL004-A-P-SD-1.1
ANGLE	
UNIT	mm
ABLIC Inc.	



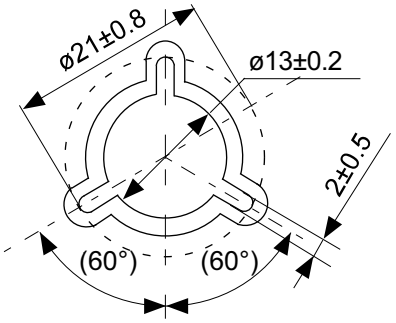


No. PL004-A-C-SD-2.0

TITLE	HSNT-4-B-Carrier Tape
No.	PL004-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



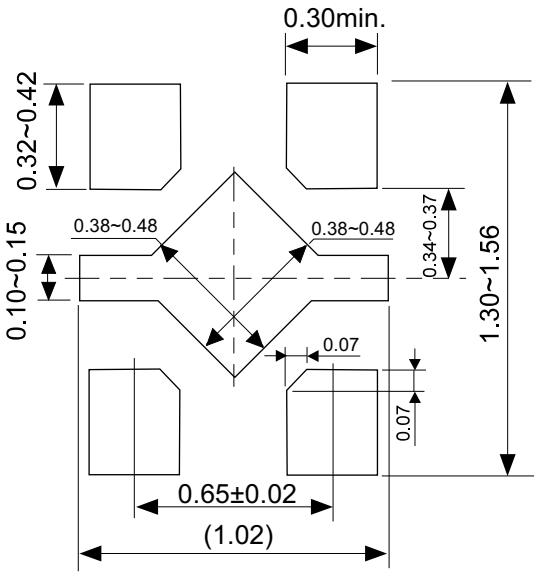
Enlarged drawing in the central part



No. PL004-A-R-SD-1.0

TITLE	HSNT-4-B-Reel		
No.	PL004-A-R-SD-1.0		
ANGLE		QTY.	10,000
UNIT	mm		
	ABLIC Inc.		

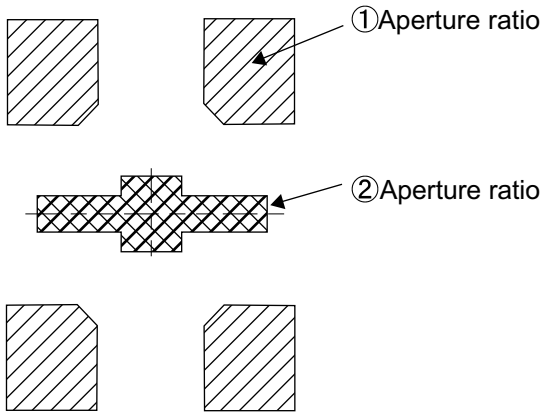
Land Pattern



Caution It is recommended to solder the heat sink to a board in order to ensure the heat radiation.

注意 放熱性を確保する為に、PKGの裏面放熱板（ヒートシンク）を基板に半田付けする事を推奨いたします。

Metal Mask Pattern



Caution ① Mask aperture ratio of the lead mounting part is 100%.
② Mask aperture ratio of the heat sink mounting part is 40%.
③ Mask thickness: t0.10mm to 0.12 mm

注意 ①リード実装部のマスク開口率は100%です。
②放熱板実装のマスク開口率は40%です。
③マスク厚み：t0.10mm ~ 0.12 mm

No. PL004-A-L-SD-2.0

TITLE	HSNT-4-B -Land Recommendation
No.	PL004-A-L-SD-2.0
ANGLE	
UNIT	mm
	ABLIC Inc.

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2.4-2019.07

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