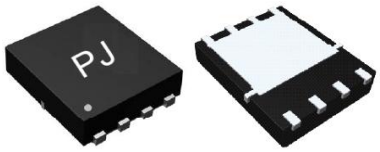
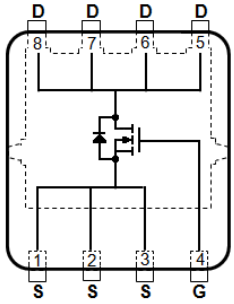
PJQ5450

40V N-Channel Enhancement Mode MOSFET

Voltage	40 V	Current	21A

DFN5060-8L





Features

- $R_{DS(ON)}$, V_{GS}@10V, I_D@12A<32mΩ
- $R_{DS(ON)}$, V_{GS}@4.5V, I_D@10A<40mΩ
- High switching speed
- Improved dv/dt capability
- Low reverse transfer capacitance.
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case: DFN5060-8L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0028 ounces, 0.08 grams

Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C=25°C	I_D	21	A
	T_C=100°C		13.2	
Pulsed Drain Current(Note 1)	T_C=25°C	I_{DM}	80	
Power Dissipation	T_C=25°C	P_D	25	W
	T_C=100°C		10	
Continuous Drain Current	T_A=25°C	I_D	5.9	A
	T_A=70°C		4.7	
Power Dissipation	T_A=25°C	P_D	2.0	W
Power Dissipation	T_A=70°C		1.3	
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55~150	°C
Typical Thermal Resistance(Note 4,5)	Junction to Case	$R_{\theta JC}$	5.0	°C/W
	Junction to Ambient	$R_{\theta JA}$	62.5	

- Limited only By Maximum Junction Temperature

PJQ5450

Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	40	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	1.2	1.8	2.5	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=12A	-	26	32	mΩ
		V_{GS}=4.5V, I_D=10A	-	32	40	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V, V_{GS}=0V	-	-	1.0	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Dynamic (Note 6)						
Total Gate Charge	Q_g	V_{DS}=20V, I_D=5A, V_{GS}=4.5V (Note 3)	-	4.4	-	nC
Gate-Source Charge	Q_{gs}		-	1.3	-	
Gate-Drain Charge	Q_{gd}		-	1.7	-	
Input Capacitance	Ciss	V_{DS}=25V, V_{GS}=0V, f=1.0MHZ	-	425	-	pF
Output Capacitance	Coss		-	48	-	
Reverse Transfer Capacitance	Crss		-	36	-	
Turn-On Delay Time	$td_{(on)}$	V_{DD}=20V, I_D=1A, V_{GS}=4.5V, R_G=25Ω (Note 3)	-	9.4	-	ns
Turn-On Rise Time	t_r		-	29	-	
Turn-Off Delay Time	$td_{(off)}$		-	21	-	
Turn-Off Fall Time	t_f		-	29	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	21	A
Diode Forward Voltage	V_{SD}	I_S=1A, V_{GS}=0V	-	0.74	1	V

NOTES :

1. Pulse width≤300us, Duty cycle≤2%.
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.
4. The maximum current rating is package limited.
5. $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 $inch^2$ with 2oz.square pad of copper.
6. Guaranteed by design, not subject to production testing.

PJQ5450

TYPICAL CHARACTERISTIC CURVES

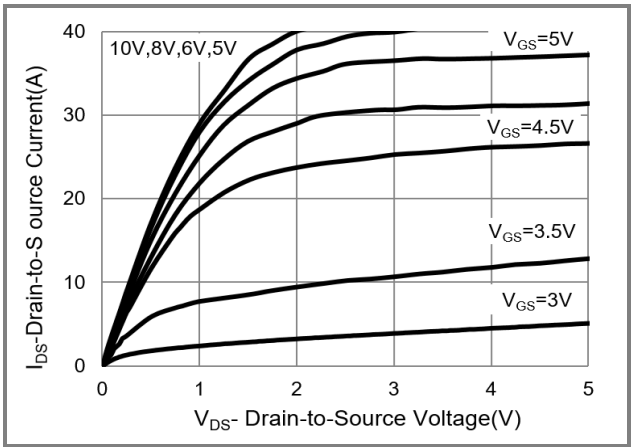


Fig.1 On-Region Characteristics

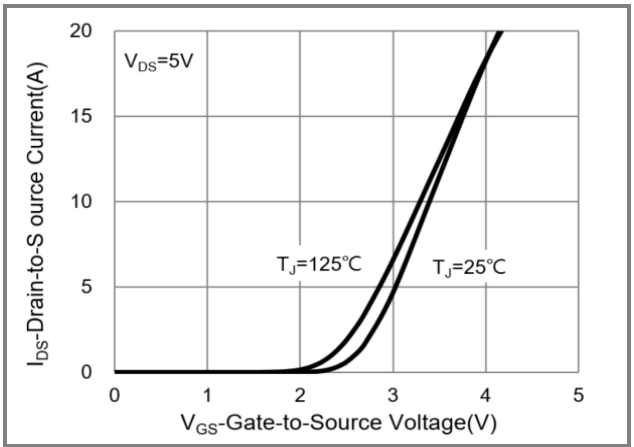


Fig.2 Transfer Characteristics

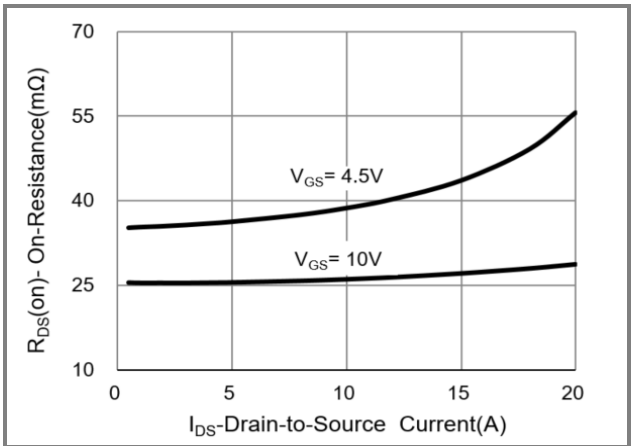


Fig.3 On-Resistance vs. Drain Current

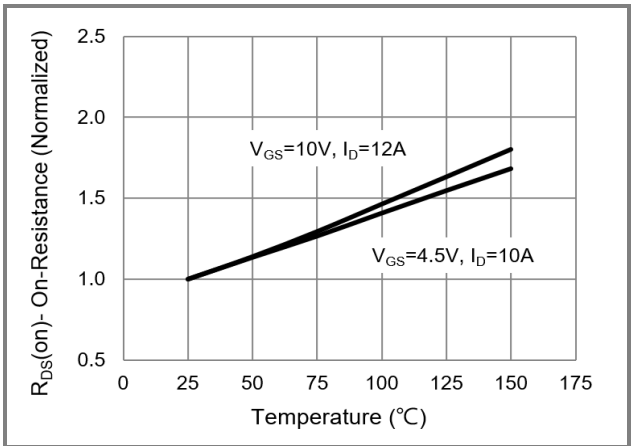


Fig.4 On-Resistance vs. Junction temperature

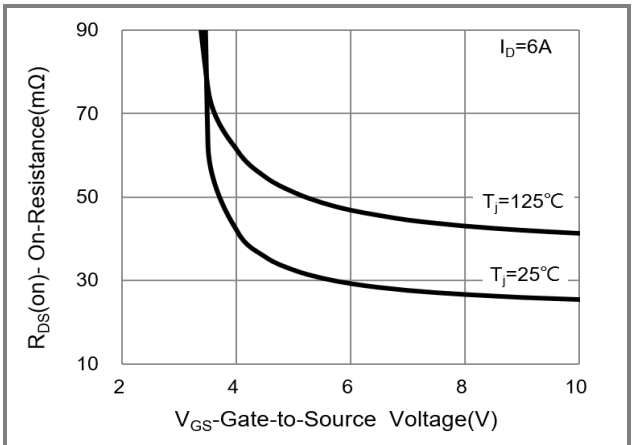


Fig.5 On-Resistance Variation with V_{GS}

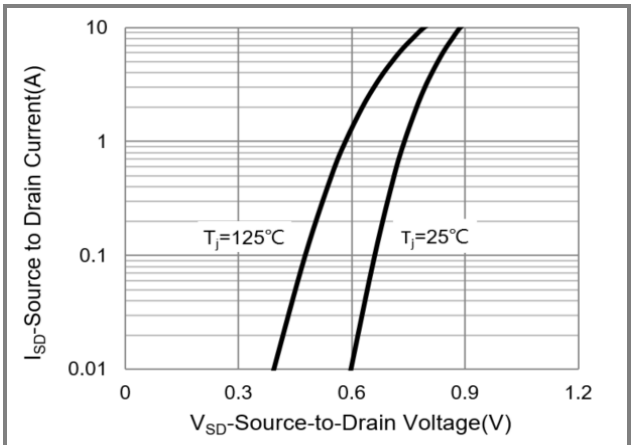


Fig.6 Body Diode Characteristics

PJQ5450

TYPICAL CHARACTERISTIC CURVES

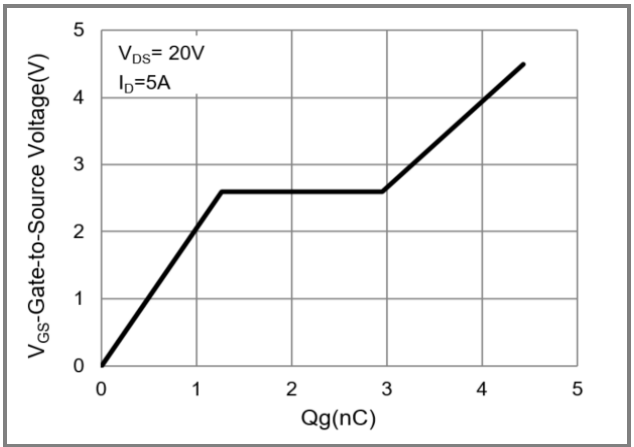


Fig.7 Gate-Charge Characteristics

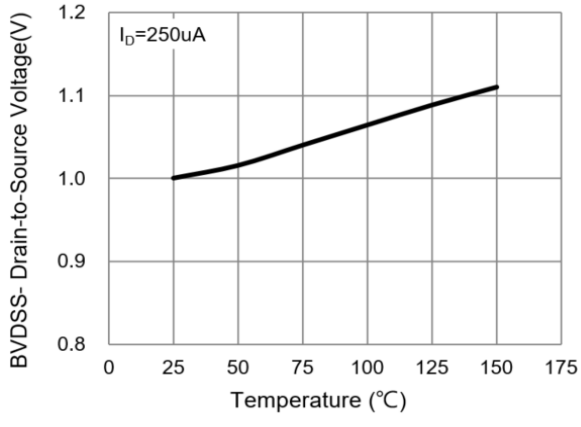


Fig.8 Breakdown Voltage Variation vs. Temperature

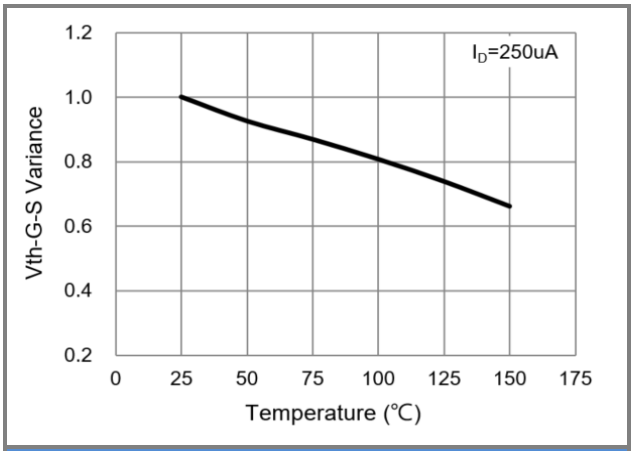


Fig.9 Threshold Voltage Variation with Temperature

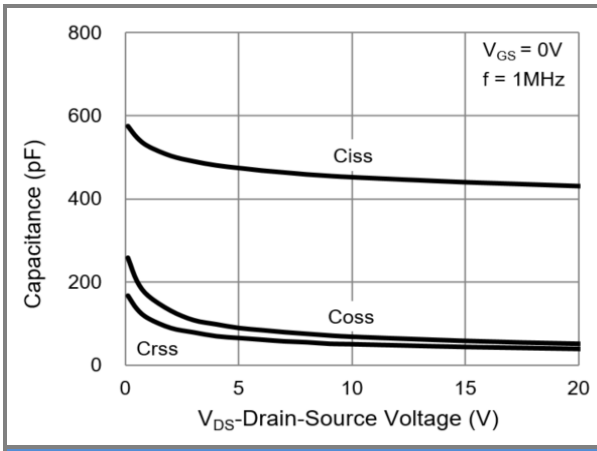


Fig.10 Capacitance vs. Drain-Source Voltage

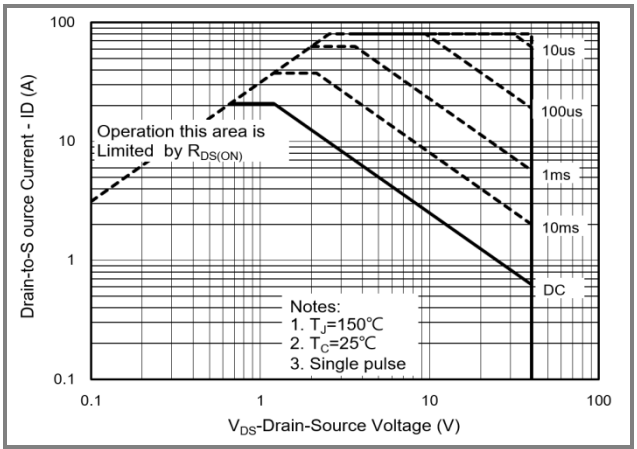


Fig.11 Maximum Safe Operating Area

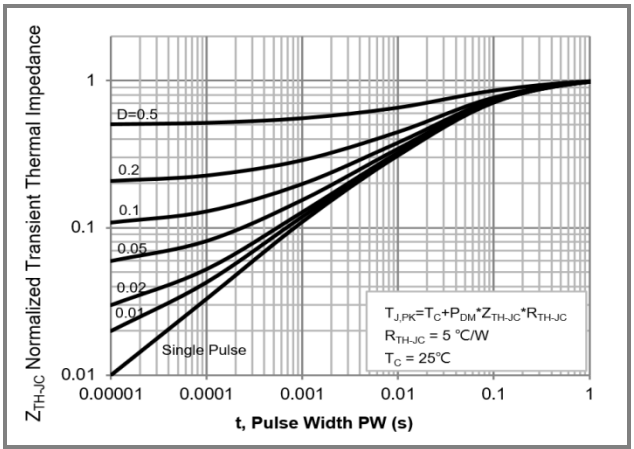


Fig.12 Normalized Transient Thermal Impedance

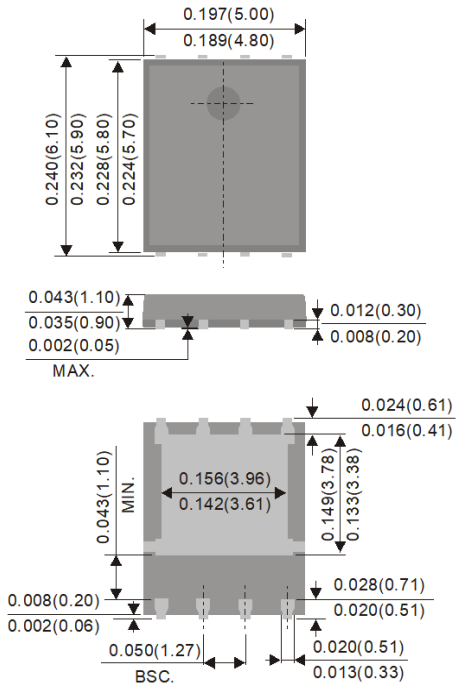
PJQ5450

Part No Packing Code Version

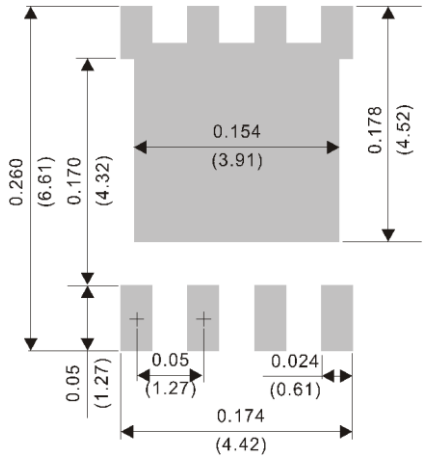
Part No Packing Code	Package Type	Packing Type	Marking	Version
PJQ5450_R2_00001	DFN5060-8L	3000pcs / 13” reel	Q5450	Halogen free

Packaging Information & Mounting Pad Layout

DFN5060-8L Dimension — Unit: inch(mm)



DFN5060-8L Pad Layout — Unit: inch(mm)



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