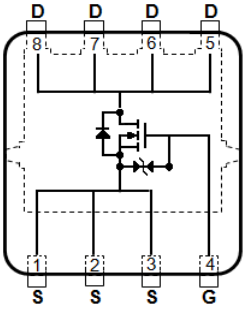
PJQ4548P-AU

40V N-Channel Enhancement Mode MOSFET

Voltage	40 V	Current	43 A

DFN3333-8L





Features

- $R_{DS(ON)}$, V_{GS}@10V, I_D@10A<9.1mΩ
- $R_{DS(ON)}$, V_{GS}@4.5V, I_D@6A<12.5mΩ
- Excellent FOM
- Logic Level Drive
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN3333-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.03 grams

Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current(Note 3)	T_C=25°C	I_D	43	A
	T_C=100°C		30	
Pulsed Drain Current(Note 1)	T_C=25°C	I_{DM}	172	
Power Dissipation	T_C=25°C	P_D	30	W
	T_C=100°C		15	
Continuous Drain Current(Note 4)	T_A=25°C	I_D	12.4	A
	T_A=70°C		10.3	
Power Dissipation	T_A=25°C	P_D	2.5	W
	T_A=70°C		1.8	
Single Pulse Avalanche Energy(Note 5)		E_{AS}	42	mJ
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55~175	°C
Thermal Resistance(Note 4)	Junction to Case	$R_{\theta JC}$	5	°C/W
	Junction to Ambient	$R_{\theta JA}$	60	

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Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	40	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=50uA	1.1	1.6	2.3	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=10A	-	7.3	9.1	mΩ
		V_{GS}=4.5V, I_D=6A	-	9.6	12.5	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V, V_{GS}=0V	-	-	1	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±10	uA
		V_{GS}=±10V, V_{DS}=0V	-	-	±1	
Dynamic(Note 6)						
Total Gate Charge	Q_g	V_{DS}=32V, I_D=10A, V_{GS}=10V	-	13	-	nC
Gate-Source Charge	Q_{gs}		-	3	-	
Gate-Drain Charge	Q_{gd}		-	2	-	
Input Capacitance	Ciss	V_{DS}=25V, V_{GS}=0V, f=1MHz	-	778	-	pF
Output Capacitance	Coss		-	180	-	
Reverse Transfer Capacitance	Crss		-	25	-	
Gate resistance	R_g	f=1MHz	-	1.6	-	Ω
Turn-On Delay Time	$td_{(on)}$	V_{DS}=32V, I_D=10A, V_{GS}=10V, R_G=3Ω (Note 2)	-	9	-	ns
Turn-On Rise Time	t_r		-	3	-	
Turn-Off Delay Time	$td_{(off)}$		-	21	-	
Turn-Off Fall Time	t_f		-	3	-	
Drain-Source Diode						
Diode Forward Current	I_S	T_C=25°C	-	-	43	A
Pulsed Diode Forward Current	I_{SM}		-	-	172	
Diode Forward Voltage	V_{SD}	I_S=20A, V_{GS}=0V	-	0.9	1.3	V
Reverse Recovery Time	Trr	V_{GS}=0V, I_S=20A dIs/dt=100A/us	-	21	-	ns
Reverse Recovery Charge	Qrr		-	10	-	nC

NOTES :

1. Pulse width≤100us, Duty cycle≤2%.
2. Essentially independent of operating temperature typical characteristics.
3. Chip capability with an $R_{\theta JC}$=5°C/W.
4. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch^2 with 2oz.square pad of copper.
5. The test condition is L=0.5mH, I_{AS}=13A, V_{DD}=30V, V_{GS}=10V, Starting T_J=25°C.
6. Guaranteed by design, not subject to production testing.

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TYPICAL CHARACTERISTIC CURVES

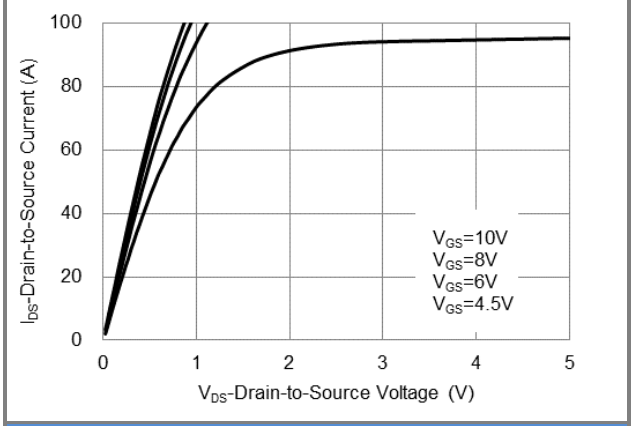

Fig.1 On-Region Characteristics

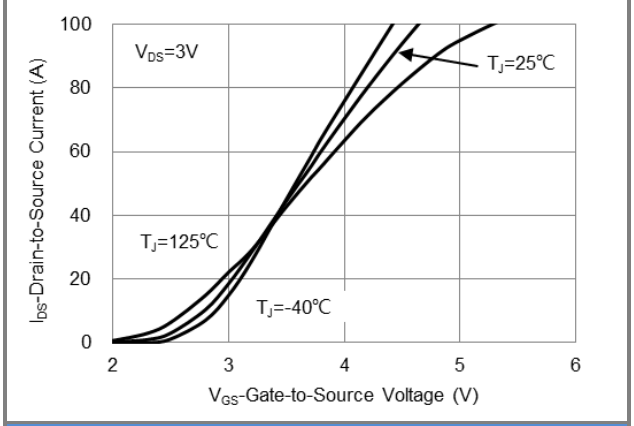

Fig.2 Transfer Characteristics

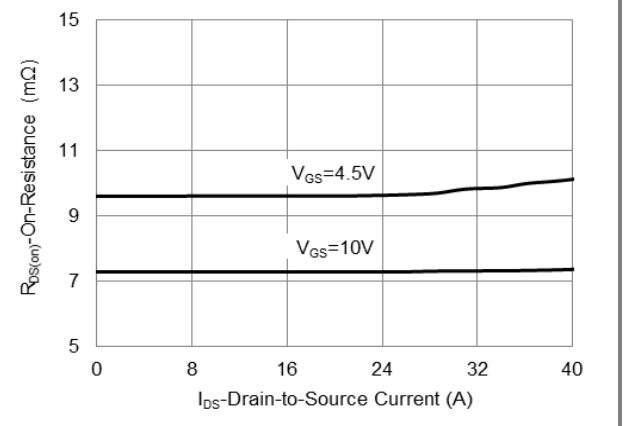

Fig.3 On-Resistance vs. Drain Current

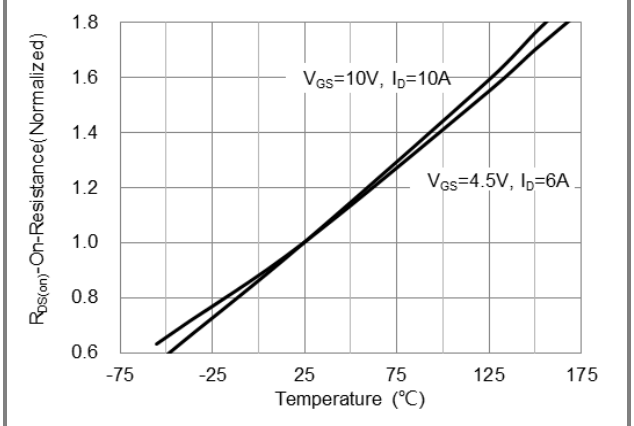

Fig.4 On-Resistance vs. Junction temperature

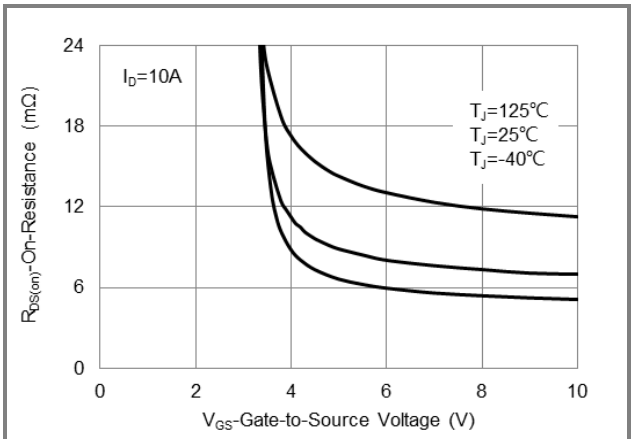

Fig.5 On-Resistance Variation with V_{GS}

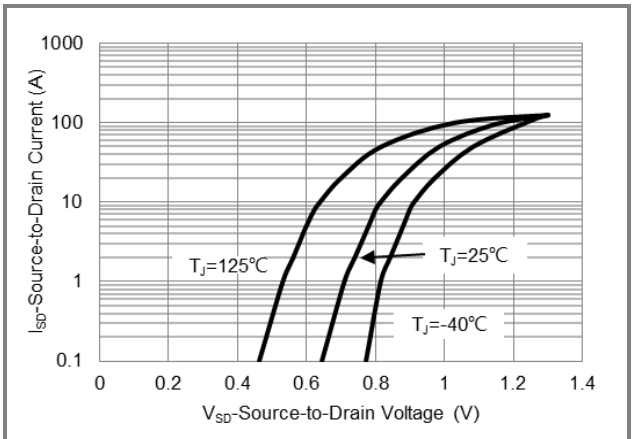

Fig.6 Source-Drain Diode Forward Voltage

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TYPICAL CHARACTERISTIC CURVES

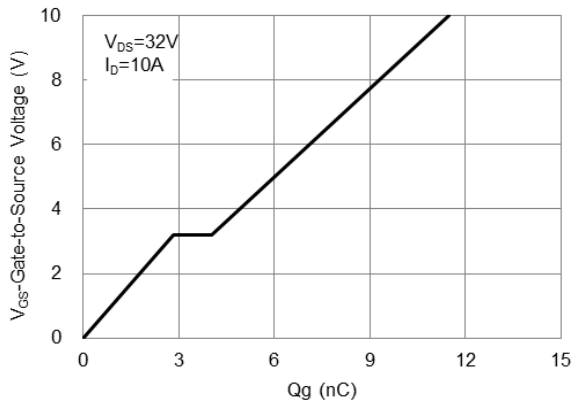


Fig.7 Gate-Charge Characteristics

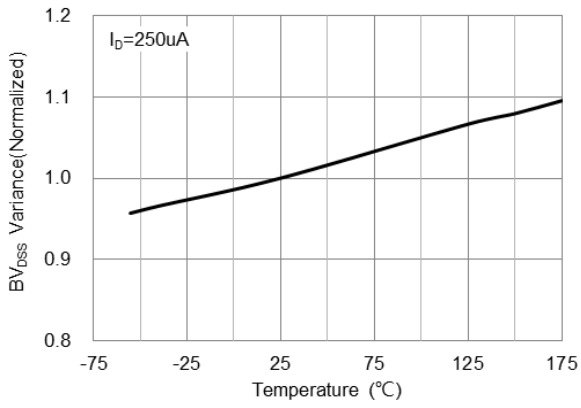


Fig.8 Breakdown Voltage Variation vs. Temperature

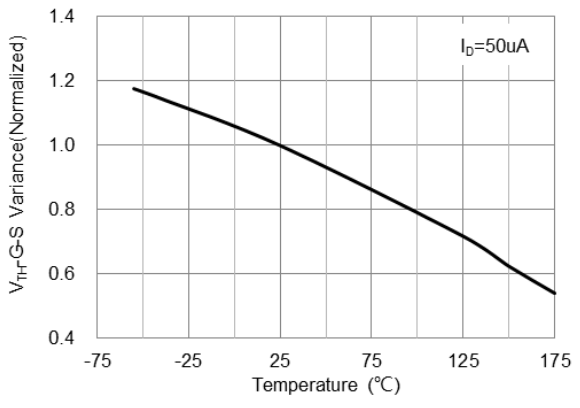


Fig.9 Threshold Voltage Variation with Temperature

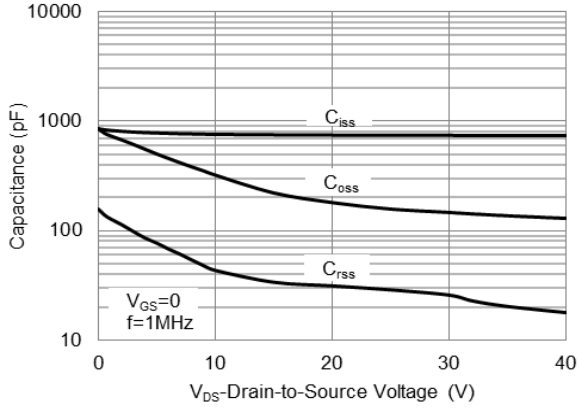


Fig.10 Capacitance vs. Drain-Source Voltage

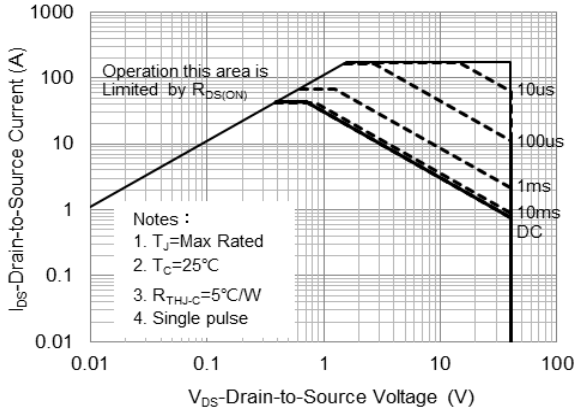


Fig.11 Maximum Safe Operating Area

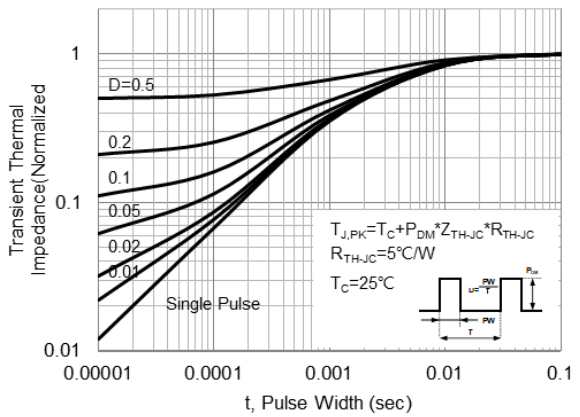


Fig.12 Normalized Transient Thermal Impedance

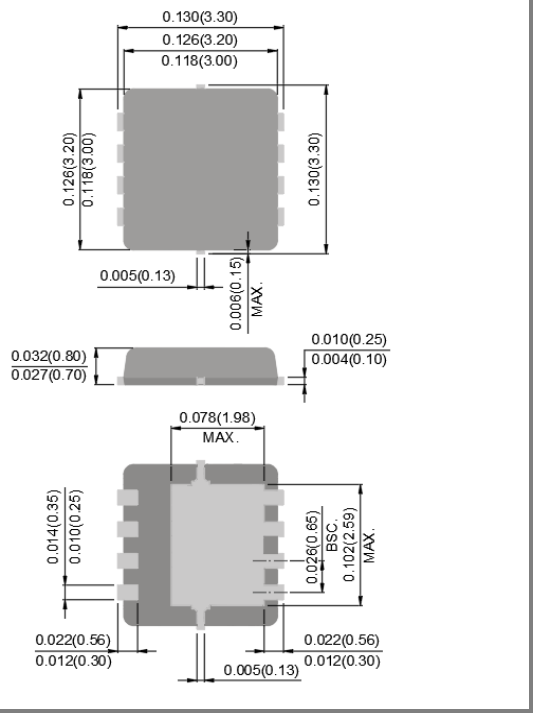
PJQ4548P-AU

Product and Packing Information

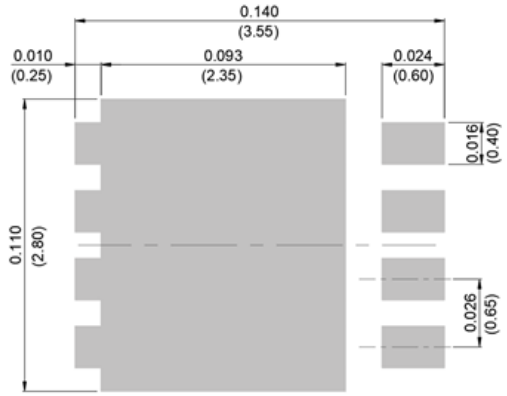
Part No.	Package Type	Packing Type	Marking
PJQ4548P-AU	DFN3333-8L	5K pcs / 13” reel	4548

Packaging Information & Mounting Pad Layout

DFN3333-8L Dimension — Unit: inch(mm)



DFN3333-8L Pad Layout — Unit: inch(mm)



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