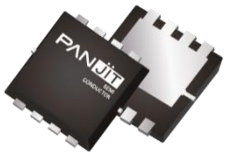
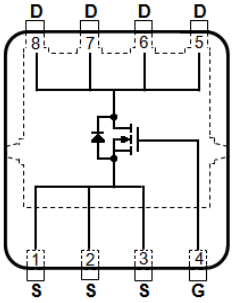
PJQ4442P-AU

40V N-Channel Enhancement Mode MOSFET

Voltage	40 V	Current	50 A

DFN3333-8L





Features

- $R_{DS(ON)}$, V_{GS}@10V, I_D@20A<7.5mΩ
- $R_{DS(ON)}$, V_{GS}@4.5V, I_D@10A<10.5mΩ
- Advanced Trench Process Technology
- High density cell design for ultralow on-resistance
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN3333-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.03 grams

Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C=25°C	I_D	50	A
	T_C=100°C		32	
Pulsed Drain Current(Note 1)	T_C=25°C	I_{DM}	200	
Power Dissipation	T_C=25°C	P_D	53.6	W
	T_C=100°C		26.8	
Continuous Drain Current	T_A=25°C	I_D	12.7	A
	T_A=70°C		10	
Power Dissipation	T_A=25°C	P_D	2.4	W
Power Dissipation	T_A=70°C		1.6	
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55~175	°C
Typical Thermal Resistance(Note 4,5)	Junction to Case	$R_{\theta JC}$	2.8	°C/W
	Junction to Ambient	$R_{\theta JA}$	62.5	

- Limited only By Maximum Junction Temperature

PJQ4442P-AU

Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	40	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	1	1.61	2.5	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=20A	-	6.3	7.5	mΩ
		V_{GS}=4.5V, I_D=10A	-	8	10.5	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V, V_{GS}=0V	-	-	1	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Dynamic(Note 6)						
Total Gate Charge	Q_g	V_{DS}=20V, I_D=10A, V_{GS}=4.5V(Note 1,2)	-	17	-	nC
Gate-Source Charge	Q_{gs}		-	4.9	-	
Gate-Drain Charge	Q_{gd}		-	6.4	-	
Input Capacitance	Ciss	V_{DS}=25V, V_{GS}=0V, f=1MHZ	-	1759	-	pF
Output Capacitance	Coss		-	176	-	
Reverse Transfer Capacitance	Crss		-	126	-	
Turn-On Delay Time	$td_{(on)}$	V_{DD}=15V, I_D=1A, V_{GS}=10V, R_G=6Ω (Note 1,2)	-	11	-	ns
Turn-On Rise Time	t_r		-	21	-	
Turn-Off Delay Time	$td_{(off)}$		-	40	-	
Turn-Off Fall Time	t_f		-	25	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	50	A
Diode Forward Voltage	V_{SD}	I_S=1A, V_{GS}=0V	-	0.7	1	V

NOTES :

1. Pulse width≤300us, Duty cycle≤2%.
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.
4. The maximum current rating is package limited.
5. $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 $inch^2$ with 2oz.square pad of copper.
6. Guaranteed by design, not subject to production testing.

PJQ4442P-AU

TYPICAL CHARACTERISTIC CURVES

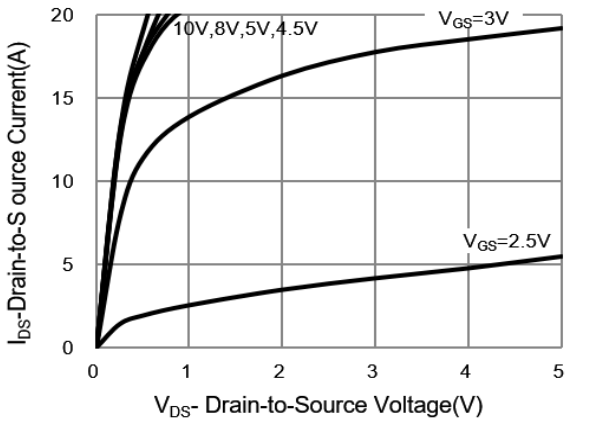


Fig.1 On-Region Characteristics

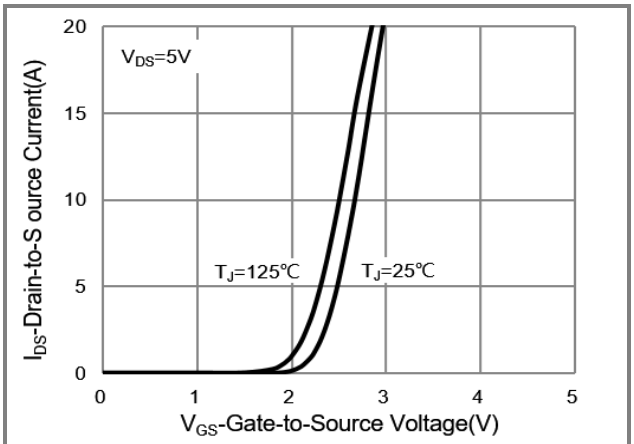


Fig.2 Transfer Characteristics

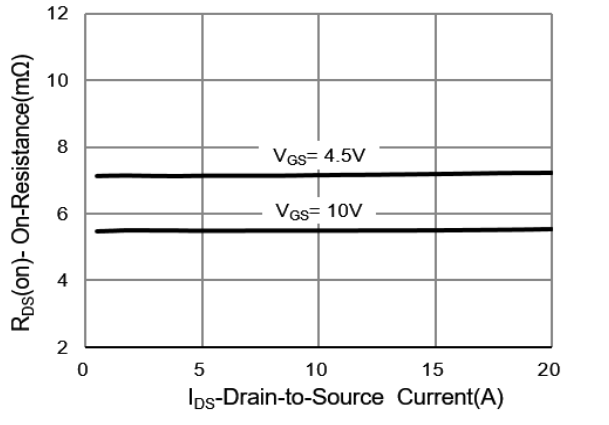


Fig.3 On-Resistance vs. Drain Current

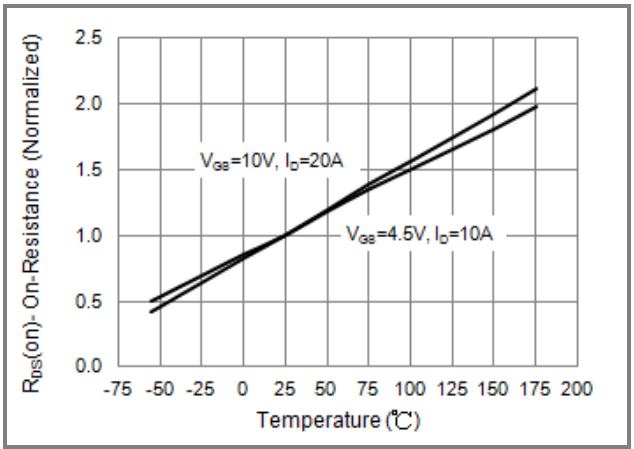


Fig.4 On-Resistance vs. Junction temperature

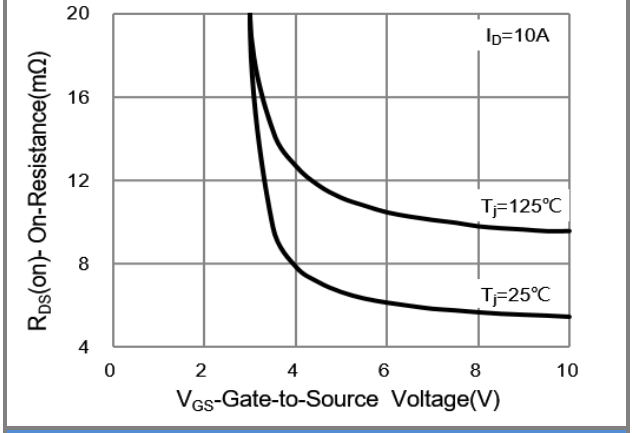


Fig.5 On-Resistance Variation with V_{GS}

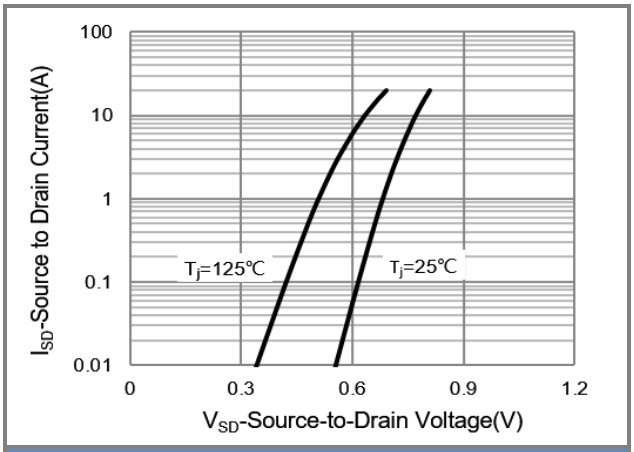


Fig.6 Source-Drain Diode Forward Voltage

PJQ4442P-AU

TYPICAL CHARACTERISTIC CURVES

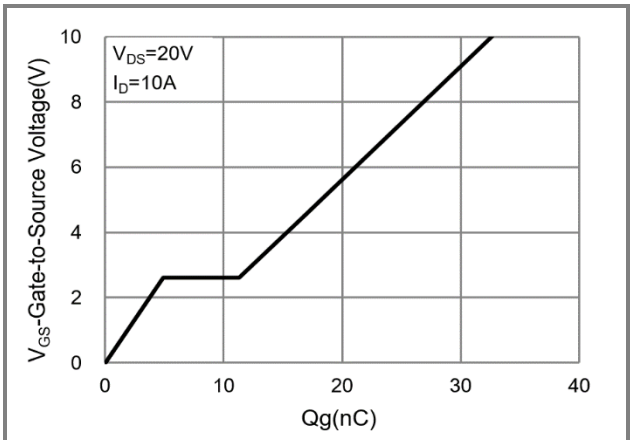


Fig.7 Gate-Charge Characteristics

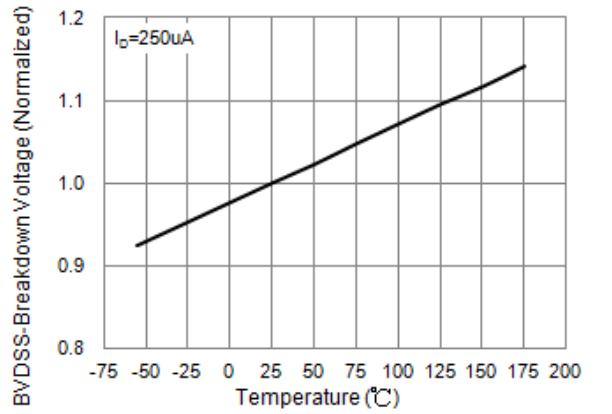


Fig.8 Breakdown Voltage Variation vs. Temperature

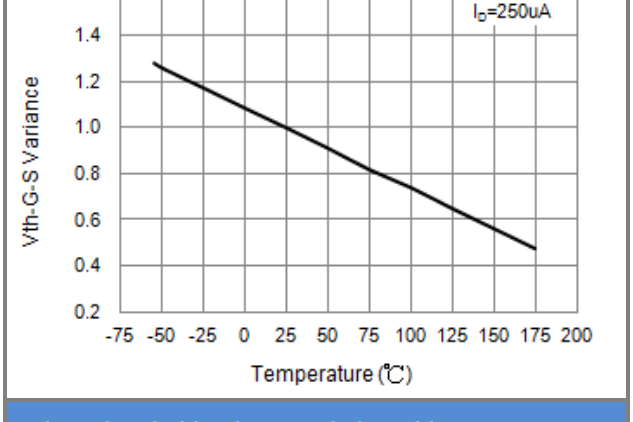


Fig.9 Threshold Voltage Variation with Temperature

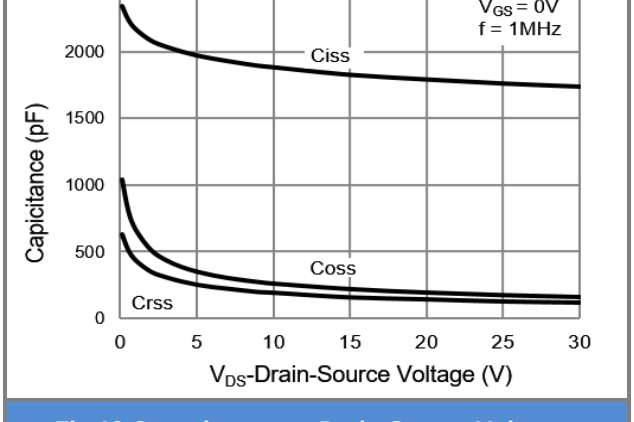


Fig.10 Capacitance vs. Drain-Source Voltage

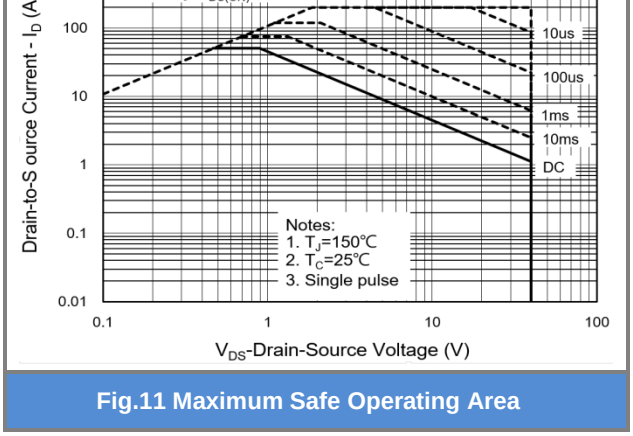


Fig.11 Maximum Safe Operating Area

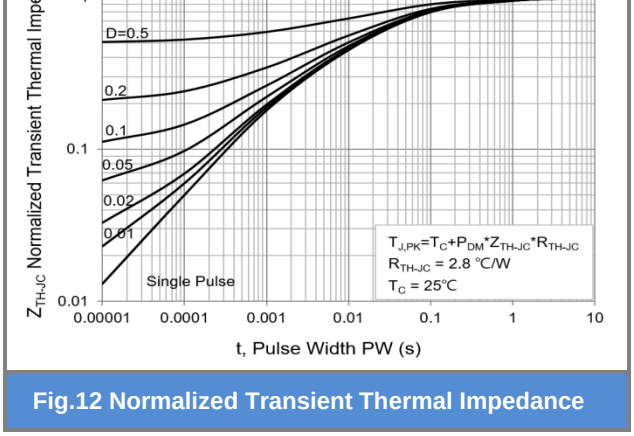


Fig.12 Normalized Transient Thermal Impedance

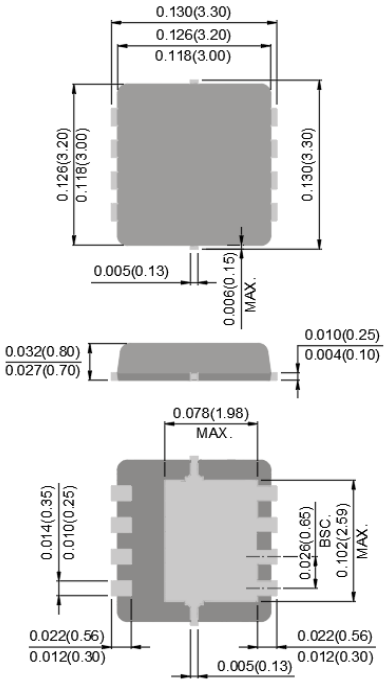
PJQ4442P-AU

Product and Packing Information

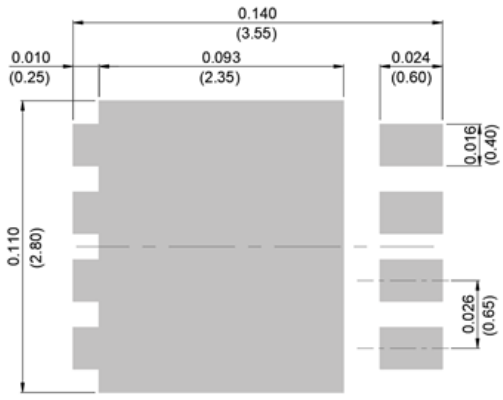
Part No.	Package Type	Packing Type	Marking
PJQ4442P-AU	DFN3333-8L	5K pcs / 13” reel	4442

Packaging Information & Mounting Pad Layout

DFN3333-8L Dimension — Unit: inch(mm)



DFN3333-8L Pad Layout — Unit: inch(mm)



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