# PAC194X

## Single/Multi-Channel Power Monitor with Accumulator, 9V Full-Scale Range

### Features

- High-Side/Low-Side Current Monitor with One, Two, Three or Four Channels:
  - 100 mV Full-Scale Range (FSR) for current sense voltage
  - 16-bit resolution for current measurement
  - Programmable FSR: -50 mv to +50 mv
  - External sense resistor sets the full-scale current range
  - Very low input current simplifies routing
- Voltage Monitor with Wide $V_{BUS}$ Range
  - 0V to 9V FSR
  - 4.5V programmable $V_{BUS}$ option
  - 16-bit resolution for voltage measurements
- $V_{SOURCE}$ Can Be Applied before $V_{DD}$ Is Applied
- Real-Time Auto-Calibration of Offset Error for Voltage and Current
- 1% Power Measurement Accuracy over a Wide Dynamic Range
- On-Chip Accumulation of 30-bit Power Results for Energy Measurement
  - User programmable sampling rates of 8, 64, 256 and 1024 SPS
  - 5120 SPS for a single channel in Burst mode
- 2.7V to 5.5V Supply Operation
  - 1.62-5.5V capable $I^2C$/SMBus and digital I/O
  - SMBus 3.1 and $I^2C$ Fast Mode Plus, 1 Mbps
  - High-Speed mode (3.4 Mbps)
- SMBus Address – 16 Options, Set with Resistor
- ALERT Features that Can Be Enabled:
  - ALERT on conversion complete
  - ALERT on Over/Undervoltage and Current or Overpower conditions
- Coulomb Counting: When Selected, the Accumulator Accumulates $V_{SENSE}$ Values.
- 8X Averaging Mode for Single-Shot Measurements to Reduce Noise and Offset
- Two Independent $\overline{ALERT}$/GPIO pins
- Available Packages
  - 3 x 3 mm 16-Lead VQFN with wettable flanks
  - 2.225 x 2.17 mm 16-Lead WLCSP

### Applications

- Embedded Computing
- Networking
- FPGA Systems
- Low-Voltage/High-Power – AI, GPU
- Industrial
- Linux® Applications
- Notebook and Tablet Computing
- Cloud, Linux and Server Computing
- Optical Networking Modules

### Computing Platform Support

- Windows® 10 Driver
- Linux Driver
- Python™ Script
- MCC Library

### Description

The PAC194X products are one, two, three and four-channel energy monitors, with bus voltage monitors and current sense amplifiers that feed high-resolution ADCs. There are two versions of the PAC194X: the PAC194X-1 devices are for high-side current sensing and the PAC194X-2 devices are for low-side current sensing or floating VBUS applications.

Digital circuitry performs power calculations and energy accumulation. This enables energy monitoring with integration periods up to one year or longer. Bus voltage, sense resistor voltage and accumulated proportional power are stored in registers for retrieval by the system host or embedded controller. The PAC194X devices have a set of digital comparators that allow the user to detect over/undervoltage, over/undercurrent and overpower against user programmed limits for each channel and generate an ALERT when the threshold is exceeded.

The sampling rate and energy integration period can be controlled over SMBus or $I^2C$. Active channel selection, single-shot measurements and other controls are also configurable by the SMBus or $I^2C$. The PAC194X device family uses real-time calibration to minimize the offset error. No input filters are required for this device.

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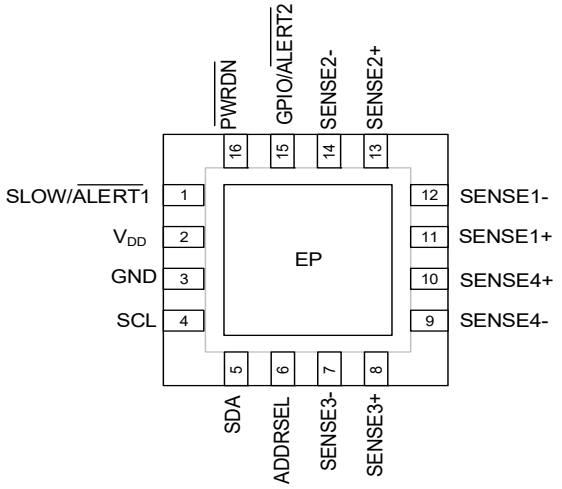
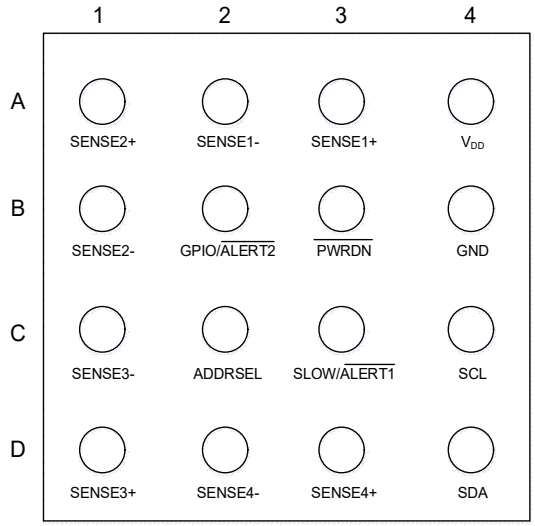
## Package Types

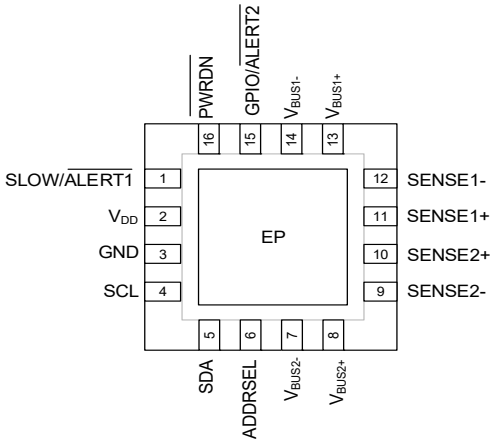
**PAC194X-1**
3 x 3 mm VQFN*



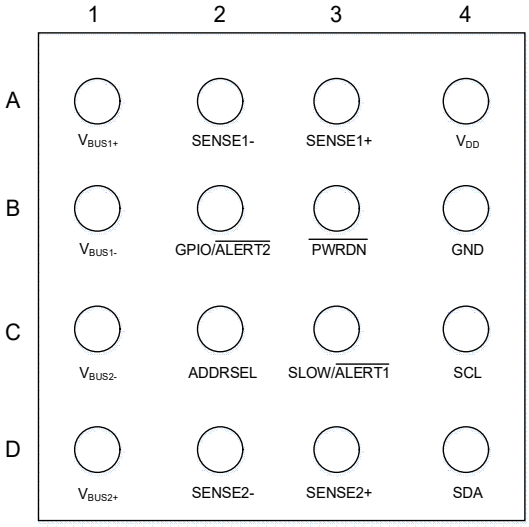

**PAC194X-1**
2.225 x 2.17 mm WLCSP




**PAC194X-2**
3 x 3 mm VQFN*




**PAC194X-2**
2.225 x 2.17 mm WLCSP




*Includes Exposed Thermal Pad; see Table 3-1 and Table 3-2.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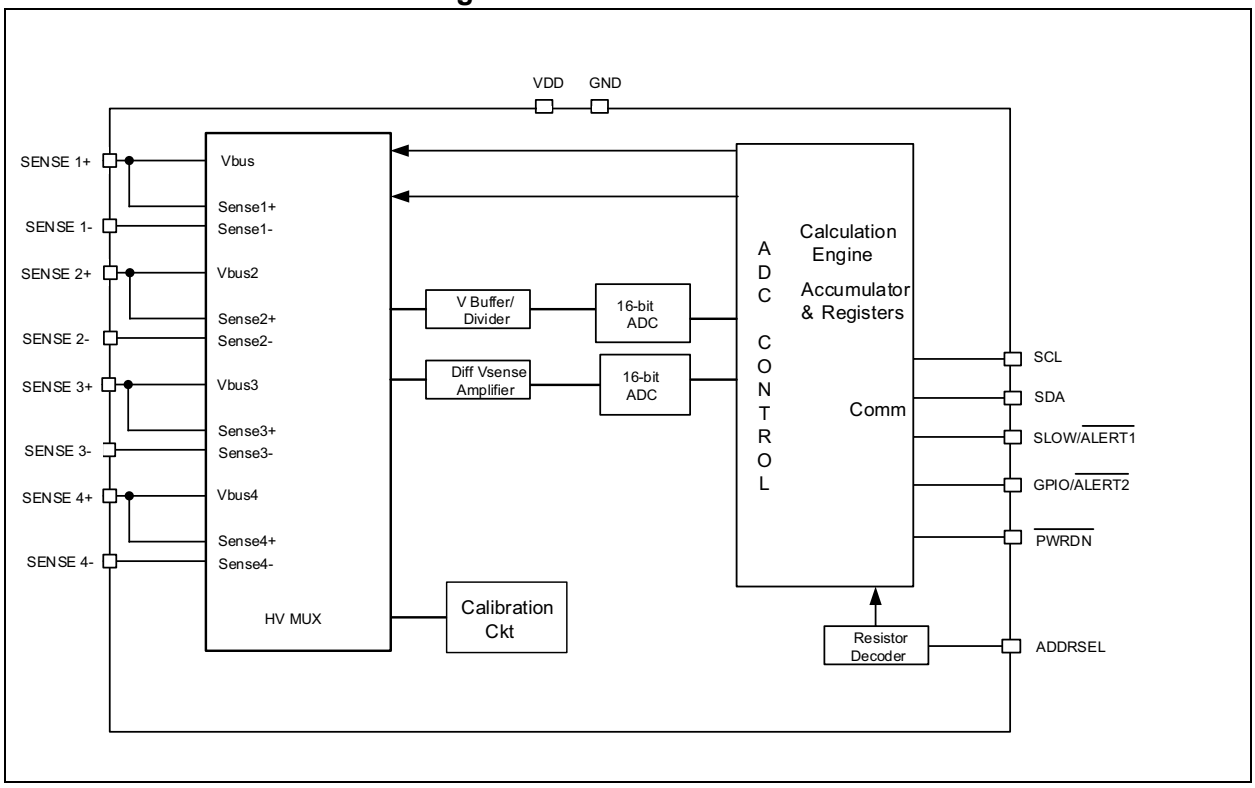
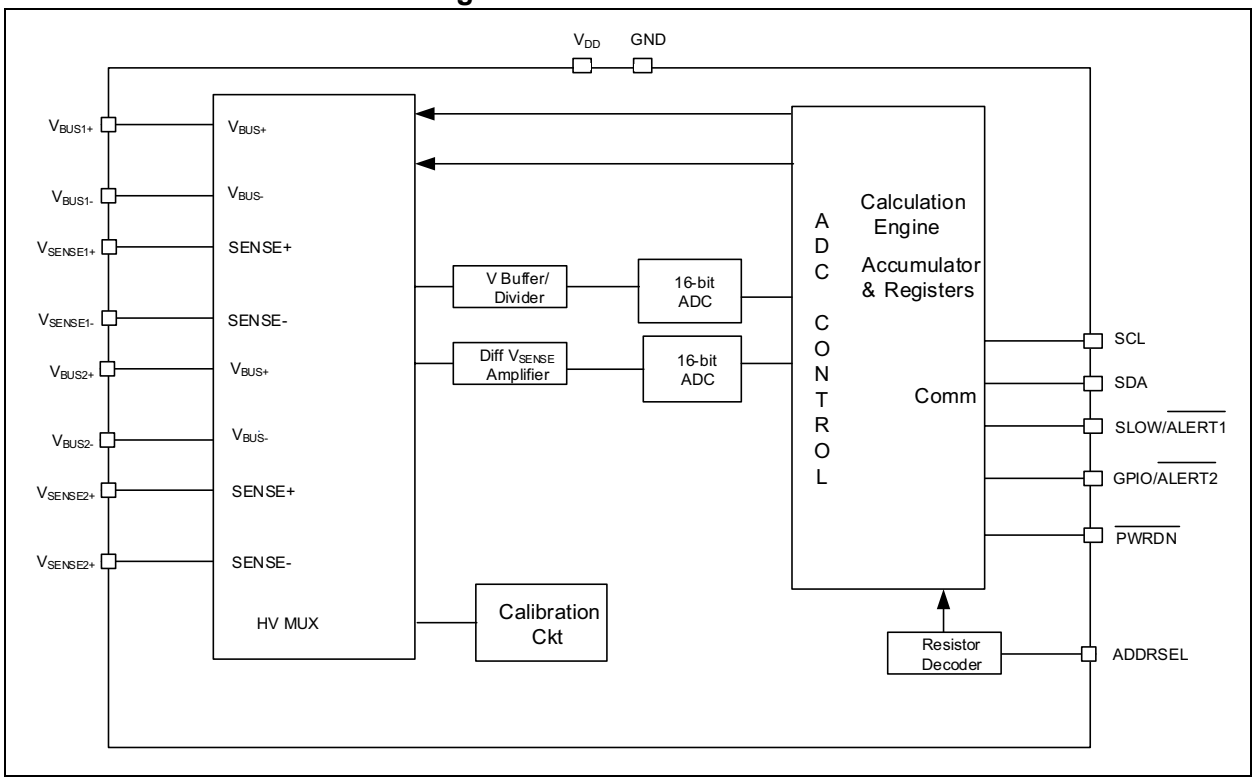
## PAC194X-1 Functional Block Diagram




## PAC194X-2 Functional Block Diagram



**NOTES:**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# 1.0 ELECTRICAL CHARACTERISTICS

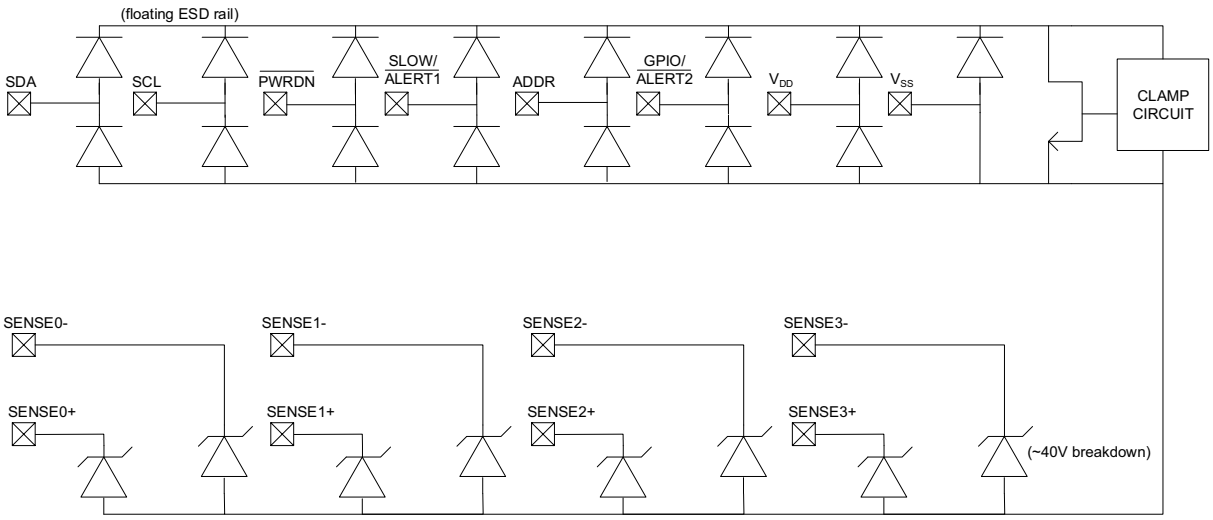
## 1.1 Electrical Specifications

### Absolute Maximum Ratings(†)

$V_{DD}$ Pin ..... -0.3 to 6.0V
Voltage on SENSE- and SENSE+ Pins ..... -0.3 to 40V
Voltage on Any Other Pin to GND ..... -0.3 to 6.0V
Voltage between Sense Pins (|(SENSE+ – SENSE-)|) ..... 500 mV
Input Current to Any Pin Except $V_{DD}$ ..... ±100 mA
Output Short-Circuit Current ..... Continuous
Operating Ambient Temperature Range ..... -40°C to +150°C
Storage Temperature Range ..... -55°C to +150°C
ESD Rating – All Pins – HBM ..... 7500V
ESD Rating – All Pins – CDM ..... 2000V

**† Notice**: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

### ESD Protection Diagram




**Note:** The SENSE+ and SENSE- pins may be at 9V (40V absolute maximum) when $V_{DD}$ is at zero.

## DC ELECTRICAL CHARACTERISTICS

**Electrical Characteristics**: Unless otherwise specified, $T_A$ = -40°C to +125°C, $V_{DD}$ = 2.7V to 5.5V, $V_{BUS}$ = 0V to 9V; $V_{SENSE}$ = (SENSE+ – SENSE-) = 0V; Typical values are at $T_A$ = +25°C, $V_{DD}$ = 3.3V

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| $V_{DD}$ Range | $V_{DD}$ | 2.7 | — | 5.5 | V | |
| $V_{DD}$ Active Current | $I_{DD}$ | — | 395 | 495 | µA | 1024 SPS, 4 channels enabled |
| | | — | 395 | 440 | | 1024 SPS, 4 channels enabled $T_A$ = 0°C to +85°C |
| | | — | 12 | 25 | | 8 SPS, 4 channels enabled $T_A$ = 0°C to +85°C |
| $V_{DD}$ Sleep Current | $I_{DD_SLEEP}$ | — | 5 | — | µA | |
| $V_{DD}$ Power-Down Current | $I_{DD_PWRDN}$ | 0 | — | 8 | µA | |
| Minimum $V_{DD}$ Rise Rate | $V_{DD_RISE_MIN}$ | — | 0.05 | — | V/ms | 0V to 5V in 100 ms |
| Maximum $V_{DD}$ Rise Rate | $V_{DD_RISE_MAX}$ | — | 1000 | — | V/ms | 0V to 5V in 5 µs |
| POR Level | $V_{POR}$ | — | 1.35 | — | V | |
| **Analog Input Characteristics** | | | | | | |
| Bus Voltage Range | $V_{BUS}$ | -0.2V | — | 9 | V | Common-mode voltage on SENSE pins, referenced to ground |
| $V_{SENSE}$ Differential Input Voltage Range | $V_{SENSE_DIF}$ | -100 | — | 100 | mV | |
| SENSE+, SENSE- Pin Input Current | $I_{SENSE+}$, $I_{SENSE-}$ | -6 | 0.6 | 6 | µA | $V_{SENSE+}$ = $V_{SENSE-}$ = Full scale All states include leakage current and average value of the capacitively coupled switching current. |
| | | -1 | 0.4 | 1 | | $V_{SENSE+}$ = 6V, $V_{SENSE-}$ = 5.9V All states include leakage current and average value of the capacitively coupled switching current. |
| $V_{BUS}$, $V_{SENSE}$ Input Trace Resistance (allowable trace resistance without measurement error) | $R_{TRACE}$ | — | 1 | — | kΩ | |
| **Measurement Accuracy** | | | | | | |
| $V_{SENSE}$ ADC Data Resolution | $V_{SENSE_RES}$ | — | — | 16 | Bits | |
| $V_{SENSE}$ LSB Step Size | $V_{SENSE_LSB}$ | — | 1.50 | — | µV | FSR = 100 mV |
| | | — | 3.05 | — | | FSR = ±100 mV |
| $V_{BUS}$ LSB Step Size | $V_{BUS_LSB}$ | — | 137 | — | µV | FSR = 9V, 16-bit resolution |
| | | — | 274 | — | | FSR = ±9V, 16-bit resolution |
| $V_{BUS}$ ADC Data Resolution | $V_{BUS_RES}$ | — | — | 16 | Bits | 14 bits are used for power calculations, 16 bits are reported when the $V_{BUS}$ measurement result is read |
| $V_{SENSE}$ Gain Accuracy | $V_{SENSE_GAIN_ERR}$ | — | ±0.1<br>±0.3 | ±0.5 | % | At +25°C<br>typical, -40°C to +125°C |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## DC ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical Characteristics**: Unless otherwise specified, $T_A$ = -40°C to +125°C, $V_{DD}$ = 2.7V to 5.5V, $V_{BUS}$ = 0V to 9V; $V_{SENSE}$ = (SENSE+ – SENSE-) = 0V; Typical values are at $T_A$ = +25°C, $V_{DD}$ = 3.3V

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{SENSE}$ Offset Accuracy, Referenced to Input | $V_{SENSE_OFFSET_ERR}$ | — | ±25 | ±100 | µV | 16-bit resolution |
| $V_{BUS}$ Gain Accuracy | $V_{BUS_GAIN_ERR}$ | — | ±0.02<br>±0.2 | ±0.25 | % | At +25°C<br>typical, -40°C to +125°C |
| **Power Accumulator Accuracy (1 Sigma Error Range with > 1000 Accumulations)** | | | | | | |
| Accumulator Error | ACC_Err | — | 0.1 | — | % | $V_{SENSE}$ = 97 mV |
| | | — | 0.1 | — | | $V_{SENSE}$ = 10 mV |
| | | — | 1 | — | | $V_{SENSE}$ = 1 mV |
| | | — | 2 | — | | $V_{SENSE}$ = 100 µV |
| | | — | 4 | — | | $V_{SENSE}$ = 50 µV |
| **Active Mode Timing** | | | | | | |
| Time to First Communications | $t_{INT_T}$ | — | — | 50 | ms | Time after $V_{DD}$ is applied before it is ready to begin communication and measurement. |
| Transition from Sleep State to Start of Conversion Cycle | $t_{SLEEP_TO_ACTIVE}$ | — | — | 5 | ms | Time from Sleep state exit commanded by register write to the beginning of the conversion cycle. |
| **Digital I/O Pins (SLOW/$\overline{\text{ALERT}}$, SM_CLK, SM_DATA Pins)** | | | | | | |
| Input High Voltage | $V_{IH}$ | 1.35 | — | — | V | |
| Input Low Voltage | $V_{IL}$ | — | — | 0.8 | V | |
| Output Low Voltage | $V_{OL}$ | — | — | 0.4 | V | Sinking 8 mA for the $\overline{\text{ALERT}}$ pins and 20 mA for the CLK pin in all modes. 4 mA for the SDA pin in 3.4 MHz mode. |
| Leakage Current | $I_{LEAK}$ | -0.5 | — | +0.5 | µA | Powered or unpowered |
| **Digital I/O Pin ($\overline{\text{PWRDN}}$)** | | | | | | |
| Input High Voltage | $V_{IH}$ | 1.3 | — | — | V | |
| Input Low Voltage | $V_{IL}$ | — | — | 0.6 | V | |

## AC ELECTRICAL CHARACTERISTICS – I²C/SMBUS TIMING

**Electrical Characteristics**: Unless otherwise specified, maximum values are at $T_A$ = -40°C to +125°C, $V_{DD}$ = 2.7V to 5.5V, $V_{I/O}$ = 1.62V to 5.5V, $V_{BUS}$ = 0V to 9V;
Typical values are at $T_A$ = +25°C, $V_{DD}$ = 3.3V, $V_{I/O}$ = 3.3V, $V_{BUS}$ = 9V, $V_{SENSE}$ = (SENSE+ – SENSE-) = 0V

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Clock Frequency | $f_{SMB}$ | 0.010 | — | 1 | MHz | Fast Mode Plus. No minimum if Time-out is not enabled. |
| | | 0.010 | — | 3.4 | | High-Speed mode. No minimum if Time-out is not enabled. |
| Spike Suppression | $t_{SP}$ | 0 | — | 50 | ns | Fast Mode Plus |
| | | 0 | — | 10 | | High-Speed mode |
| Bus Free Time Stop to Start | $t_{BUF}$ | 0.5 | — | — | µs | Per SMBus 3.1 |
| Hold Time after Repeated Start Condition | $t_{HD:STA}$ | 0.26 | — | — | µs | Per SMBus 3.1, Fast Mode Plus |
| | | 0.16 | — | — | | Per SMBus 3.1, High-Speed mode |
| Repeated Start Condition Setup Time | $t_{SU:STA}$ | 0.26 | — | — | µs | Per SMBus 3.1, Fast Mode Plus |
| | | 0.16 | — | — | | Per SMBus 3.1, High-Speed mode |
| Setup Time: Stop | $t_{SU:STO}$ | 0.26 | — | — | µs | Per SMBus 3.1, Fast Mode Plus |
| | | 0.16 | — | — | | Per SMBus 3.1, High-Speed mode |
| Setup Time: Start | $t_{SU:STA}$ | 0.26 | — | — | µs | Per SMBus 3.1, Fast Mode Plus |
| | | 0.16 | — | — | | Per SMBus 3.1, High-Speed mode |
| Data Hold Time | $t_{HD:DAT}$ | 0 | — | — | ns | Per SMBus 3.1, Fast Mode Plus |
| | | 0 | — | 70 | | Per SMBus 3.1, High-Speed mode |
| Data Setup Time | $t_{SU:DAT}$ | 50 | — | — | ns | Per SMBus 3.1, Fast Mode Plus |
| | | 10 | — | — | | Per SMBus 3.1, High-Speed mode |
| Clock Low Period | $t_{LOW}$ | 0.5 | — | — | µs | Per SMBus 3.1, Fast Mode Plus |
| | | 0.16 | — | — | | Per SMBus 3.1, High-Speed mode |
| Clock High Period | $t_{HIGH}$ | 0.26 | — | 50 | µs | Fast Mode Plus |
| | | 0.06 | — | 50 | | High-Speed mode |
| Clock/Data Fall Time | $t_{FALL}$ | 12 | — | 120 | ns | Fast Mode Plus |
| Clock/Data Rise Time | $t_{RISE}$ | — | — | 120 | ns | Fast Mode Plus |
| Clock Fall Time | $t_{fCL}$ | 10 | — | 40 | ns | High-Speed mode |
| Clock Rise Time | $t_{rCL}$ | 10 | — | 40 | ns | High-Speed mode |
| Data Fall Time | $t_{fDA}$ | 10 | — | 80 | ns | High-Speed mode |
| Data Rise Time | $t_{rDA}$ | 10 | — | 80 | ns | High-Speed mode |


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## AC ELECTRICAL CHARACTERISTICS – I²C/SMBUS TIMING (CONTINUED)

**Electrical Characteristics**: Unless otherwise specified, maximum values are at $T_A$ = -40°C to +125°C, $V_{DD}$ = 2.7V to 5.5V, $V_{I/O}$ = 1.62V to 5.5V, $V_{BUS}$ = 0V to 9V;
Typical values are at $T_A$ = +25°C, $V_{DD}$ = 3.3V, $V_{I/O}$ = 3.3V, $V_{BUS}$ = 9V, $V_{SENSE}$ = (SENSE+ – SENSE-) = 0V

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Capacitive Load | $C_{LOAD}$ | — | — | 550 | pF | Per bus line, Fast Mode Plus |
| | | — | — | 100 | | Per bus line, High-Speed mode |
| SLOW Pin Pulse Width | SLOWpw | 150 | — | — | µs | Pulses narrower than 150 µS may not be detected |

## TEMPERATURE SPECIFICATIONS

**Electrical Specifications:** Unless otherwise specified, all parameters apply for $T_A$ = -40°C to +125°C, $V_{DD}$ = 2.7V to 5.5V, $V_{BUS}$ = 0V to 9V, $V_{SENSE+} – V_{SENSE-}$ = 0

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Temperature Ranges** | | | | | | |
| Specified Temperature Range | $T_A$ | -40 | — | +125 | °C | |
| Operating Temperature Range | $T_A$ | -40 | — | +125 | °C | |
| Storage Temperature Range | $T_{STG}$ | -55 | — | +150 | °C | |
| **Thermal Package Resistance** | | | | | | |
| Thermal Resistance, 16-Lead VQFN | $\theta_{JA}$ | — | 39.9 | — | °C/W | |
| | $\theta_{JC}$ | — | 23.1 | — | °C/W | |
| Thermal Resistance, 16-Ball WLCSP | $\theta_{JA}$ | — | 51.16 | — | °C/W | |
| | $\theta_{JC}$ | — | 4.85 | — | °C/W | |

**NOTES:**


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## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

**Note:** Unless otherwise indicated, maximum values are at $T_A$ = -40°C to +125°C, $V_{DD}$ = 2.7V to 5.5V, $V_{BUS}$ = 0V to 9V. Typical values are at $T_A$ = +25°C, $V_{DD}$ = 3.3V, $V_{BUS}$ = 3.3V, $V_{SENSE}$ = (SENSE+ – SENSE-) = 0V.

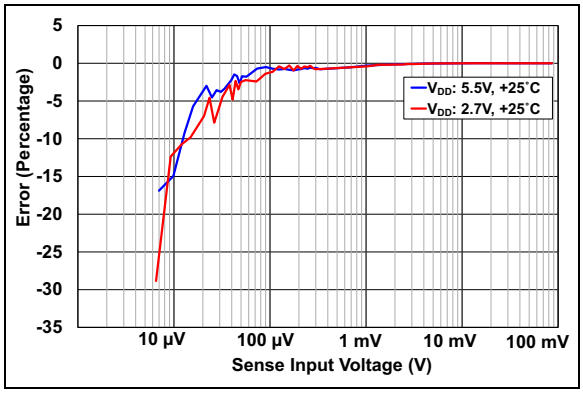


***FIGURE 2-1:*** *$V_{SENSE}$ Error vs. $V_{SENSE}$ Input Voltage.*

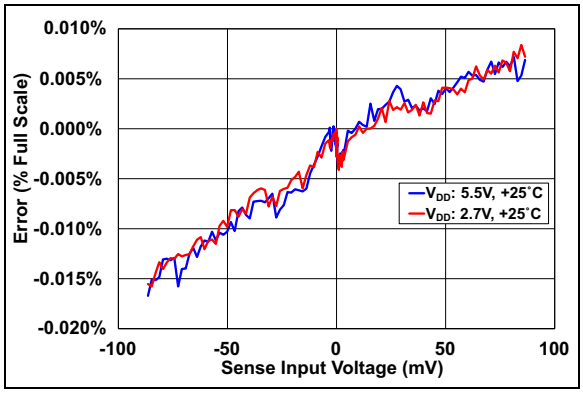


***FIGURE 2-4:*** *$V_{SENSE}$ Error vs. $V_{SENSE}$ Input Voltage, Bidirectional Mode.*

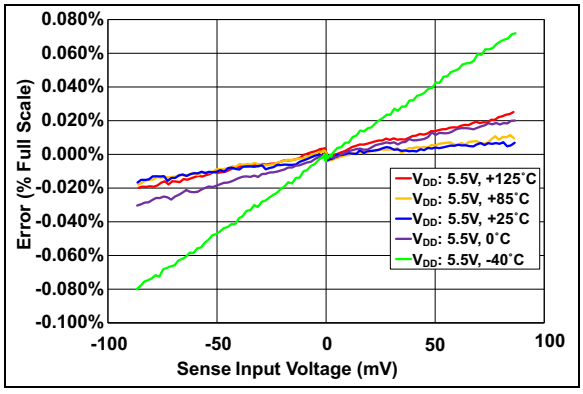


***FIGURE 2-2:*** *$V_{SENSE}$ Error vs. $V_{SENSE}$ Input Voltage, Bidirectional Mode.*

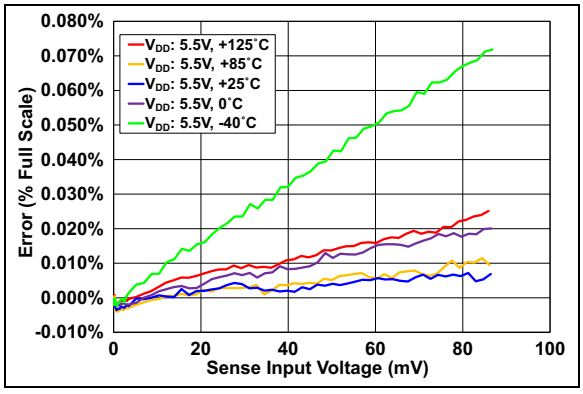


***FIGURE 2-5:*** *$V_{SENSE}$ Error vs. $V_{SENSE}$ Input Voltage at Multiple Temperatures.*

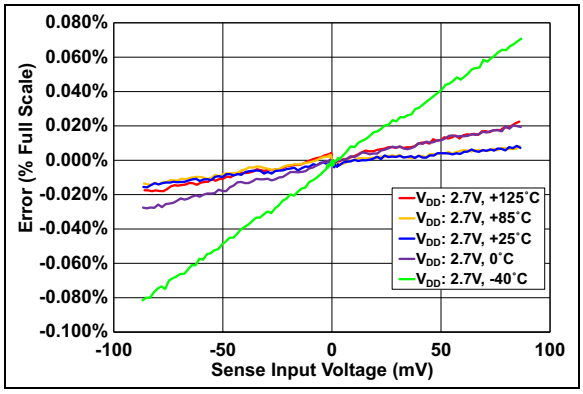


***FIGURE 2-3:*** *$V_{SENSE}$ Error vs. $V_{SENSE}$ Input Voltage, Bidirectional Mode.*

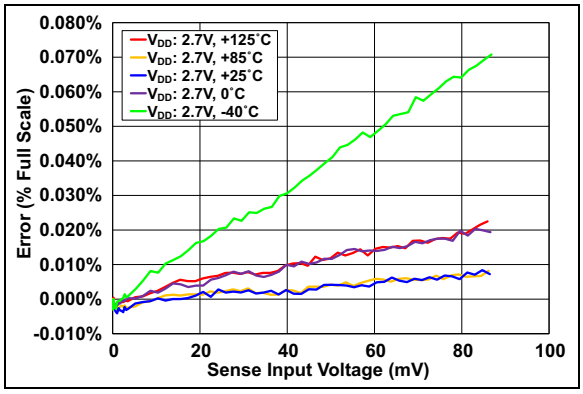


***FIGURE 2-6:*** *$V_{SENSE}$ Error vs. $V_{SENSE}$ Input Voltage at Multiple Temperatures.*

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**Note:** Unless otherwise indicated, maximum values are at $T_A$ = -40°C to +125°C, $V_{DD}$ = 2.7V to 5.5V, $V_{BUS}$ = 0V to 9V. Typical values are at $T_A$ = +25°C, $V_{DD}$ = 3.3V, $V_{BUS}$ = 3.3V, $V_{SENSE}$ = (SENSE+ – SENSE-) = 0V.

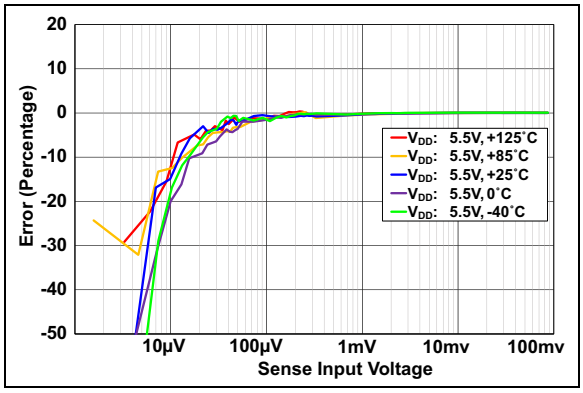


***FIGURE 2-7:*** *$V_{SENSE}$ Error vs. $V_{SENSE}$ Input Voltage at Multiple Temperatures.*

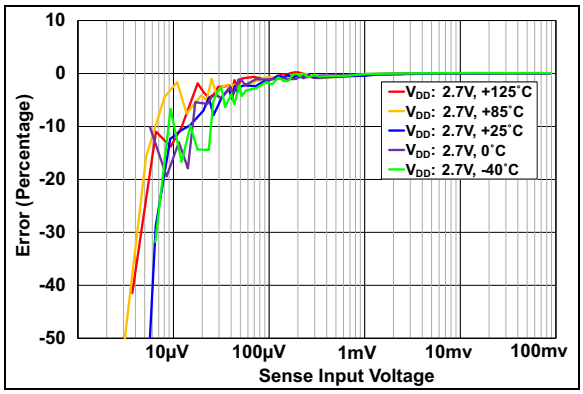


***FIGURE 2-8:*** *$V_{SENSE}$ Error vs. $V_{SENSE}$ Input Voltage at Multiple Temperatures.*

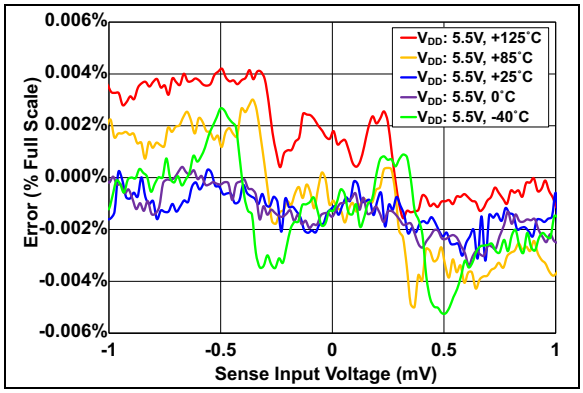


***FIGURE 2-9:*** *$V_{SENSE}$ Error vs. $V_{SENSE}$ Input Voltage, Bidirectional Mode (Zoom View).*

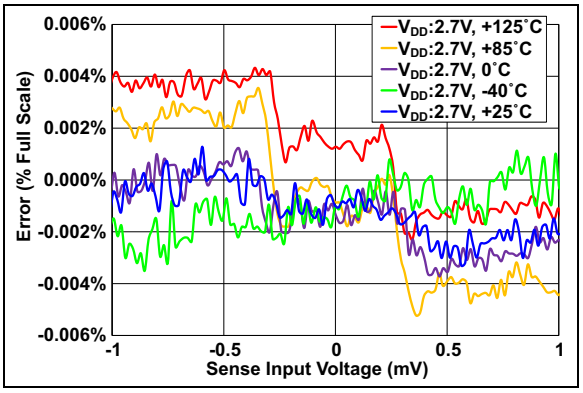


***FIGURE 2-10:*** *$V_{SENSE}$ Error vs. $V_{SENSE}$ Input Voltage, Bidirectional Mode (Zoom View).*

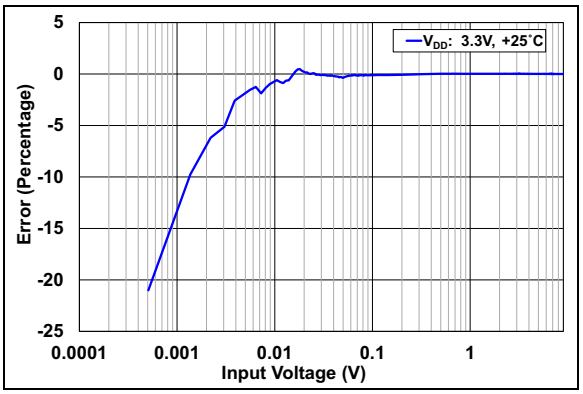


***FIGURE 2-11:*** *$V_{BUS}$ Error vs. $V_{BUS}$ Input Voltage.*

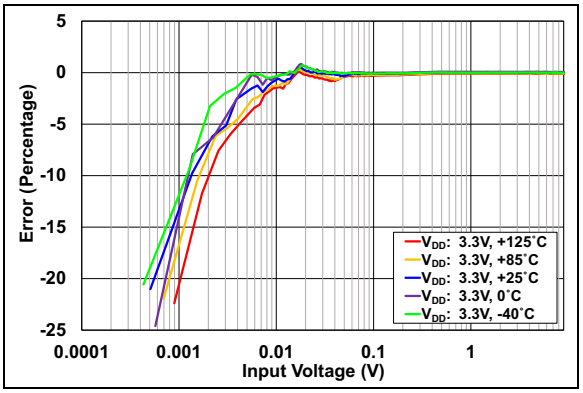


***FIGURE 2-12:*** *$V_{BUS}$ Error vs. $V_{BUS}$ Input Voltage at Multiple Temperatures.*


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**Note:** Unless otherwise indicated, maximum values are at $T_A$ = -40°C to +125°C, $V_{DD}$ = 2.7V to 5.5V, $V_{BUS}$ = 0V to 9V. Typical values are at $T_A$ = +25°C, $V_{DD}$ = 3.3V, $V_{BUS}$ = 3.3V, $V_{SENSE}$ = (SENSE+ – SENSE-) = 0V.

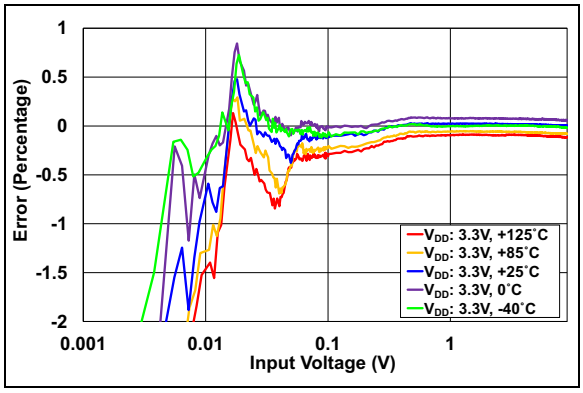


***FIGURE 2-13:*** *$V_{BUS}$ Error vs. $V_{BUS}$ Input Voltage at Multiple Temperatures (Zoom View).*

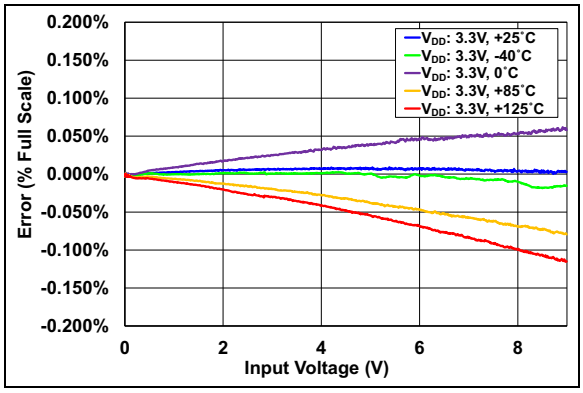


***FIGURE 2-16:*** *$V_{BUS}$ Error vs. $V_{BUS}$ Input Voltage at Multiple Temperatures.*

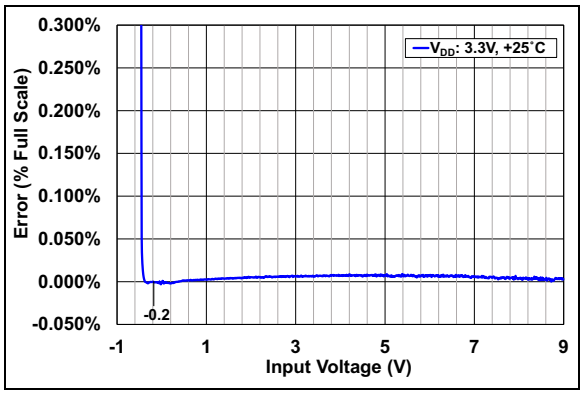


***FIGURE 2-14:*** *$V_{BUS}$ Error vs. $V_{BUS}$ Input Voltage.*

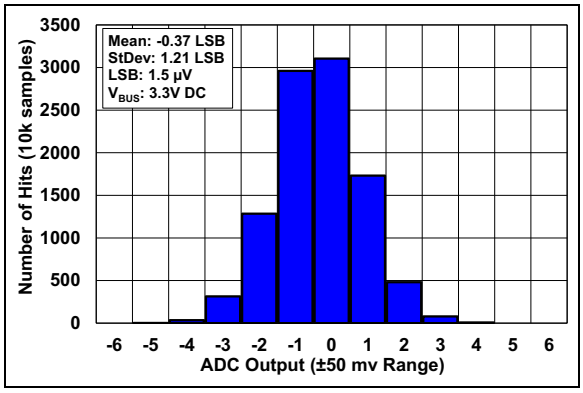


***FIGURE 2-17:*** *Zero Input Histogram for $V_{SENSE}$ (LSBs, 8X Average Results, Total Measurements 10,000).*

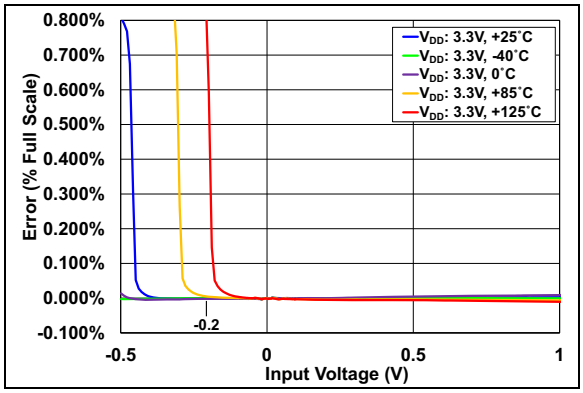


***FIGURE 2-15:*** *$V_{BUS}$ Error vs. $V_{BUS}$ Input Voltage at Multiple Temperatures (Bipolar Mode).*

**Note:** Unless otherwise indicated, maximum values are at $T_A$ = -40°C to +125°C, $V_{DD}$ = 2.7V to 5.5V, $V_{BUS}$ = 0V to 9V. Typical values are at $T_A$ = +25°C, $V_{DD}$ = 3.3V, $V_{BUS}$ = 3.3V, $V_{SENSE}$ = (SENSE+ – SENSE-) = 0V.

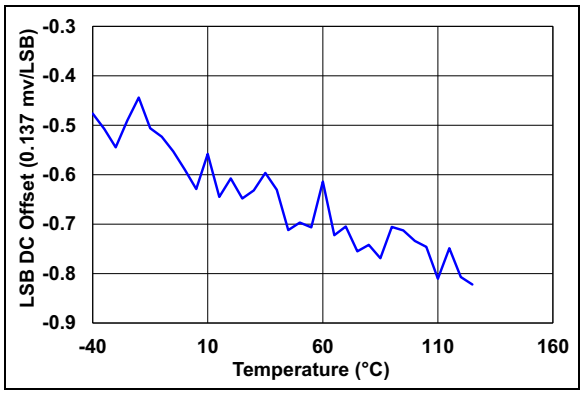


***FIGURE 2-18:*** *Input Offset for $V_{BUS}$ Measurements vs. Temperature.*

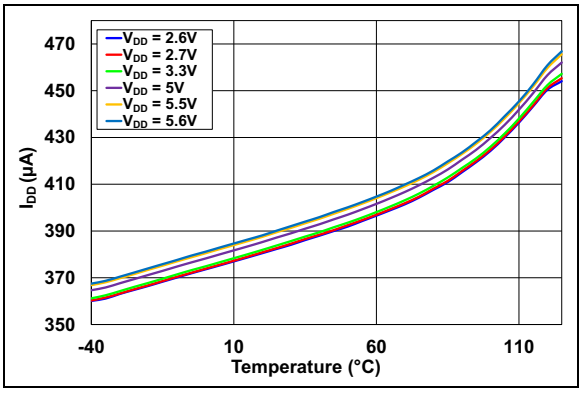


***FIGURE 2-21:*** *$I_{DD}$ vs. Temperature and Supply at 1024 SPS.*

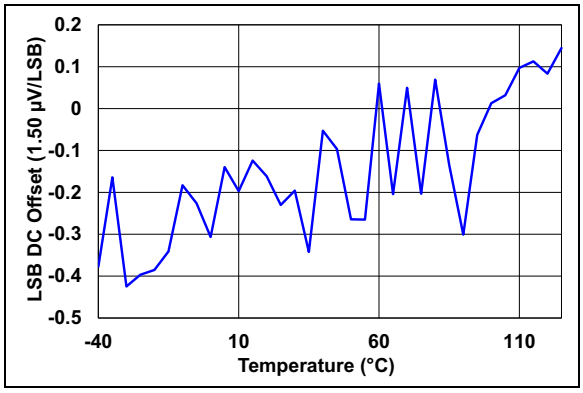


***FIGURE 2-19:*** *Input Offset for $V_{SENSE}$ Measurements vs. Temperature.*

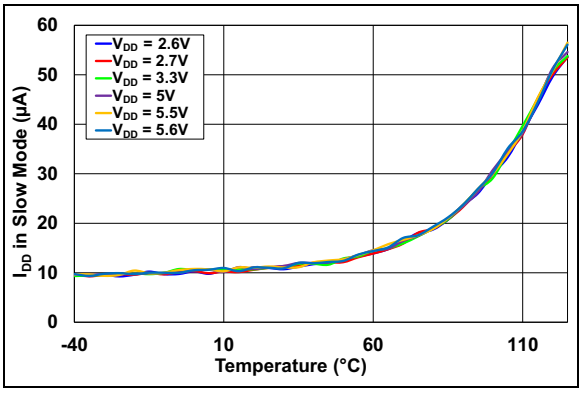


***FIGURE 2-22:*** *$I_{DD}$ in Slow Mode vs. Temperature and Supply.*

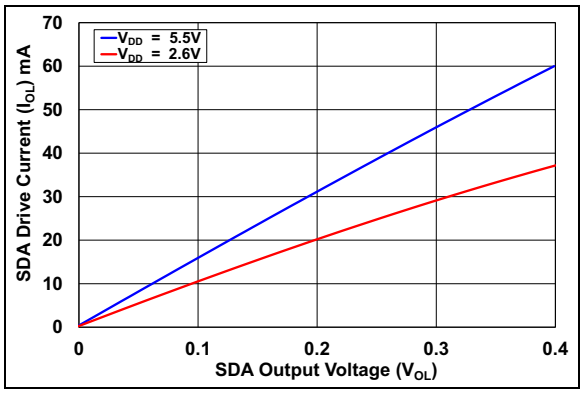


***FIGURE 2-20:*** *SDA Drive Current vs. $V_{OL}$ at +25°C.*

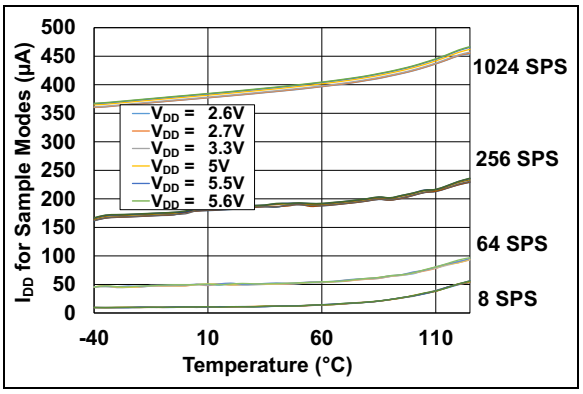


***FIGURE 2-23:*** *$I_{DD}$ vs.Temperature, Supply and Sample Rate.*


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**Note:** Unless otherwise indicated, maximum values are at $T_A$ = -40°C to +125°C, $V_{DD}$ = 2.7V to 5.5V, $V_{BUS}$ = 0V to 9V. Typical values are at $T_A$ = +25°C, $V_{DD}$ = 3.3V, $V_{BUS}$ = 3.3V, $V_{SENSE}$ = (SENSE+ – SENSE-) = 0V.

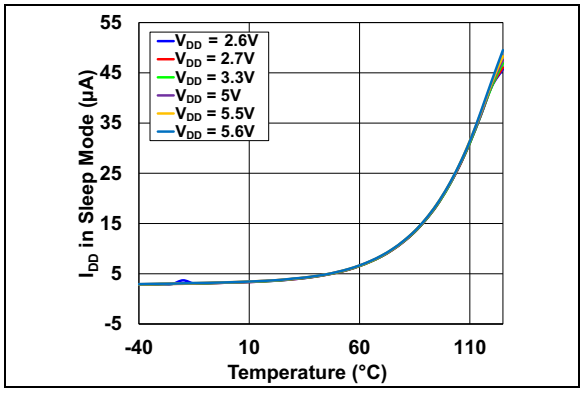


***FIGURE 2-24:*** *Sleep Mode Current vs. Temperature and Supply.*

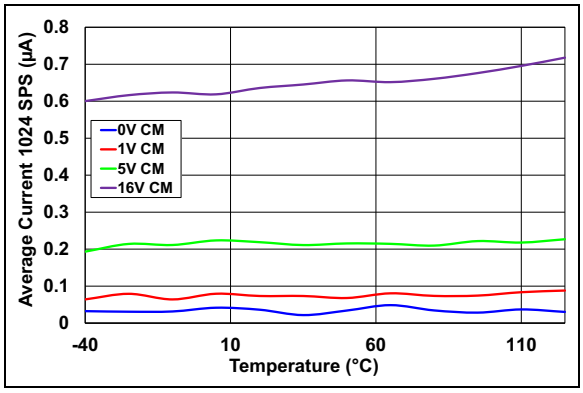


***FIGURE 2-27:*** *Average $V_{SENSE}$ Input Current – Active Mode, 1024 SPS vs. Temperature and Common-Mode.*

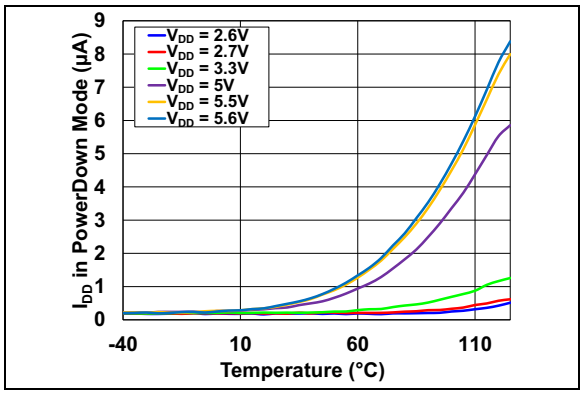


***FIGURE 2-25:*** *Power-Down Mode Current vs. Temperature and Supply.*

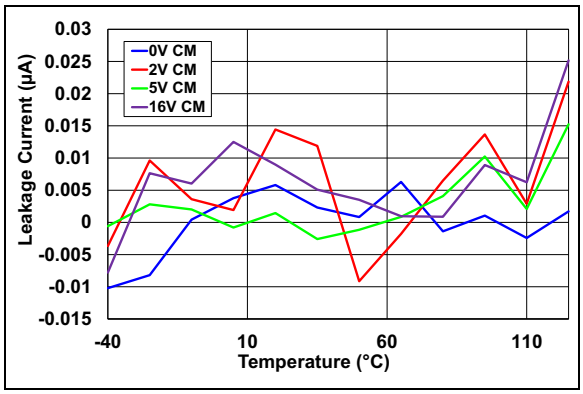


***FIGURE 2-28:*** *$V_{BUS}$ Input Leakage Current vs. Temperature and Common-Mode.*

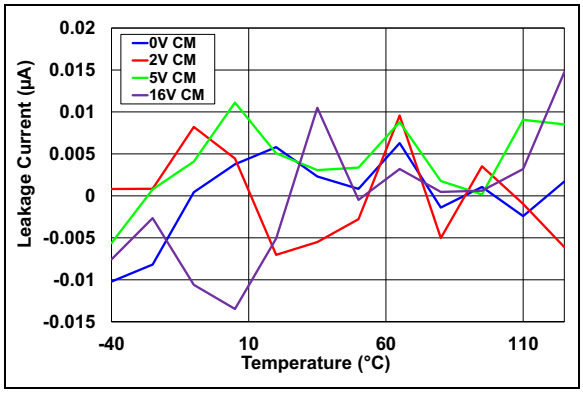


***FIGURE 2-26:*** *$V_{SENSE}$ Input Leakage Current vs. Temperature and Common-Mode.*

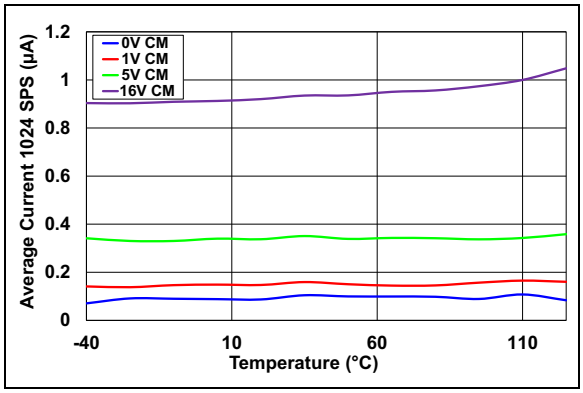


***FIGURE 2-29:*** *$V_{BUS}$ Input Current – Active Mode, 1024 SPS vs. Temperature and Common-Mode.*

**Note:** Unless otherwise indicated, maximum values are at $T_A$ = -40°C to +125°C, $V_{DD}$ = 2.7V to 5.5V, $V_{BUS}$ = 0V to 9V. Typical values are at $T_A$ = +25°C, $V_{DD}$ = 3.3V, $V_{BUS}$ = 3.3V, $V_{SENSE}$ = (SENSE+ – SENSE-) = 0V.

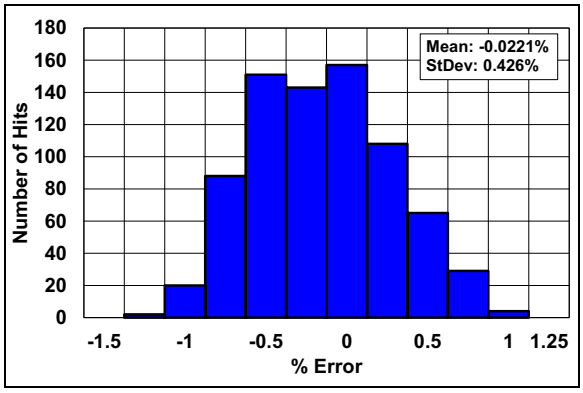


***FIGURE 2-30:*** *Clock Frequency Error -40°C to +125°C. Total Population 768 Devices.*

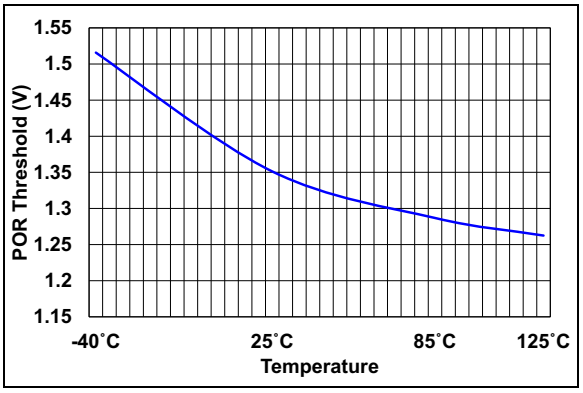


***FIGURE 2-32:*** *POR vs. Temperature.*

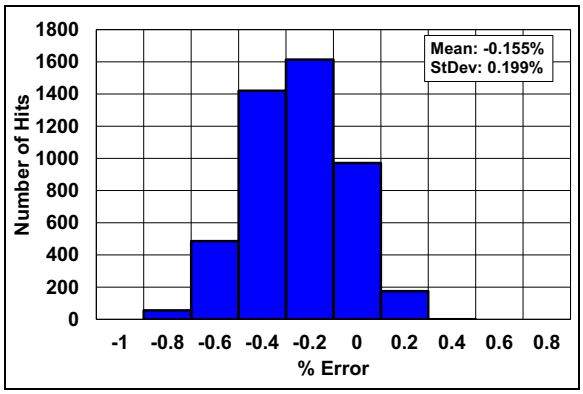


***FIGURE 2-31:*** *Clock Frequency Error at +30°C. Total Population 4,723 Devices.*


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## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1 and Table 3-2.

**TABLE 3-1: PAC194X-1 PIN FUNCTION TABLE**

| VQFN | WLCSP | Symbol | Pin Type | Description |
|---|---|---|---|---|
| 1 | C3 | SLOW/$\overline{\text{ALERT1}}$ | Digital I/O Pin | Default: SLOW Input pin. When high, all channels sample at 8 SPS. The pin may be programmed to function as the $\overline{\text{ALERT1}}$ pin or GPIO (open-drain). |
| 2 | A4 | $V_{DD}$ | Power for IC | Positive power supply voltage. |
| 3 | B4 | GND | Ground Pin | Ground for the IC. |
| 4 | C4 | SCL | SMBus Clock Input | Clock Input pin. |
| 5 | D4 | SDA | SMBus Data I/O | Open-drain requires a pull-up resistor to Host $V_{DD}$. |
| 6 | C2 | ADDRSEL | Analog I/O Pin | Address selection for the SMBus client address. |
| 7 | C1(2) | SENSE3-(1) | Analog Input Pin | 0-FSR, connect to the load side of the sense resistor. |
| 8 | D1(2) | SENSE3+(1) | Analog Input Pin | 0-FSR, connect to the supply side of the sense resistor. |
| 9 | D2(2) | SENSE4-(1) | Analog Input Pin | 0-FSR, connect to the load side of the sense resistor. |
| 10 | D3(2) | SENSE4+(1) | Analog Input Pin | 0-FSR, connect to the supply side of the sense resistor. |
| 11 | A3 | SENSE1+ | Analog Input Pin | 0-FSR, connect to the supply side of the sense resistor. |
| 12 | A2 | SENSE1- | Analog Input Pin | 0-FSR, connect to the load side of the sense resistor. |
| 13 | A1(2) | SENSE2+(1) | Analog Input Pin | 0-FSR, connect to the supply side of the sense resistor. |
| 14 | B1(2) | SENSE2-(1) | Analog Input Pin | 0-FSR, connect to the load side of the sense resistor. |
| 15 | B2 | GPIO/$\overline{\text{ALERT2}}$ | Digital I/O Pin | Default: GPIO, Input mode. May be programmed to be the $\overline{\text{ALERT2}}$ pin indicator (open-drain) or GPIO (open-drain). |
| 16 | B3 | $\overline{\text{PWRDN}}$ | Digital Input Pin | Active-low puts the device in a Power-Down state (all circuitry is powered down, including SMBus). |
| 17 | — | EP | N/C | The Exposed Pad is not electrically connected. |

**Note 1:** VQFN Package: for PAC1941-1, pins 7, 8, 9, 10, 13 and 14 are not connected inside and must be grounded. For PAC1942-1, pins 7, 8, 9 and 10 are not connected inside and must be grounded. For PAC1943-1, pins 9 and 10 are not connected inside and must be grounded.

**2:** WLCSP Package: for PAC1941-1, pins A1, B1, C1, D1, D2 and D3 are inactive and must be grounded. For PAC1942-1, pins C1,D1, D2, D3 are inactive and must be grounded. For PAC1943-1, pins D2 and D3 are inactive and must be grounded.

**3:** Analog Input pins: for any unused channels, connect the SENSE+ and SENSE- pins to ground. Voltage may be applied to the analog input pins before or after $V_{DD}$ is applied to the device.

**4:** For the analog input pins, the safe operating voltage range is up to 9V.

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**TABLE 3-2: PAC194X-2 PIN FUNCTION TABLE**

| VQFN | WLCSP | Symbol | Pin Type | Description |
|---|---|---|---|---|
| 1 | C3 | SLOW/$\overline{\text{ALERT1}}$ | Digital I/O Pin | Default: SLOW input pin. When high, all channels sample at 8 SPS. The pin may be programmed to function as the $\overline{\text{ALERT1}}$ pin or GPIO (open-drain). |
| 2 | A4 | $V_{DD}$ | Power for IC | Positive power supply voltage. |
| 3 | B4 | GND | Ground Pin | Ground for the IC. |
| 4 | C4 | SCL | SMBus Clock Input | Clock Input pin requires a pull-up resistor $V_{DD}$ voltage for the digital controller. |
| 5 | D4 | SDA | SMBus Data I/O | Open-drain requires a pull-up resistor $V_{DD}$ voltage for the digital controller. |
| 6 | C2 | ADDRSEL | Analog I/O Pin | Address selection for the SMBus client address. |
| 7 | C1(2) | $V_{BUS2-}$(1) | Analog Input Pin | 0-FSR, connect to the ground sense point for $V_{BUS2}$. |
| 8 | D1(2) | $V_{BUS2+}$(1) | Analog Input Pin | 0-FSR, connect to $V_{BUS2+}$. |
| 9 | D2(2) | SENSE2-(1) | Analog Input Pin | 0-FSR, connect to the low side of the sense resistor. |
| 10 | D3(2) | SENSE2+(1) | Analog Input Pin | 0-FSR, connect to the low side of the sense resistor. |
| 11 | A3 | SENSE1+ | Analog Input Pin | 0-FSR, connect to the low side of the sense resistor. |
| 12 | A2 | SENSE1- | Analog Input Pin | 0-FSR, connect to the low side of the sense resistor. |
| 13 | A1 | $V_{BUS1+}$ | Analog Input Pin | 0-FSR, connect to $V_{BUS1+}$. |
| 14 | B1 | $V_{BUS1-}$ | Analog Input Pin | 0-FSR, connect to the ground sense point for $V_{BUS1}$. |
| 15 | B2 | GPIO/$\overline{\text{ALERT2}}$ | Digital I/O Pin | Default: GPIO, Input mode. May be programmed to be the $\overline{\text{ALERT2}}$ pin indicator (open-drain) or the GPIO function (open-drain). |
| 16 | B3 | $\overline{\text{PWRDN}}$ | Digital Input Pin | Active-low puts the device in a Power-Down state (all circuitry is powered down, including SMBus). |
| 17 | — | EP | N/C | The Exposed Pad is not electrically connected. |

**Note 1:** VQFN Package: for PAC1941-2, pins 7, 8, 9 and 10 are not connected inside and must be grounded.

**2:** WLCSP: for PAC1942-2, pins C1, D1, D2 and D3 are inactive and must be grounded

**3:** Analog Input pins: for any unused channels, connect the SENSE+ and SENSE- pins to ground. Voltage may be applied to the analog input pins before or after $V_{DD}$ is applied to the device. For the PAC194X-2 devices, the SENSE+ and SENSE- pins have a Common-mode range from 0V to 9V.

**4:** For the analog input pins, the safe operating voltage range is up to 9V.

## 3.1 SENSE[N]+/- (N = 1, 2, 3, 4)

These two pins form the differential input for measuring voltage across a sense resistor in the application. The positive input (SENSE[N]+) also acts as the input pin for bus voltage.

## 3.2 Ground (GND)

System ground.

## 3.3 SMBus Data (SM_DATA)

This is the bidirectional SMBus data pin. This pin is open-drain and requires a pull-up resistor to $V_{DD}$.

## 3.4 SMBus Clock (SM_CLK)

This is the SMBus clock input pin and requires an external pull-up resistor, except if used in High-Speed mode, which requires a CMOS driver from the host.

## 3.5 Positive Power Supply Voltage ($V_{DD}$)

Power supply input pin for the device. 2.7V-5.5V range, bypass with 100 nF ceramic capacitor to ground near the IC.

## 3.6 Address Selection (ADDRSEL)

Connect a resistor from this pin to ground to select the SMBus address.


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### 3.7 Enable Pin ($\overline{\text{PWRDN}}$)

Power-down input pin for the device, active-low.

### 3.8 SLOW/$\overline{\text{ALERT1}}$

In default mode, if this pin is forced high, the sampling rate is forced to 8 SPS. When it is forced low, the sampling rate is 1024 SPS, unless a different sample rate has been programmed. This pin may be programmed to act as the $\overline{\text{ALERT1}}$ pin. In ALERT mode, the pin needs a pull-up resistor to $V_{DD}$. In GPIO mode, the default is an input but it can be configured as an output (open-drain).

### 3.9 GPIO/$\overline{\text{ALERT2}}$

In default mode, this pin is a GPIO input pin. It can be configured to be an output pin, as well as the ALERT2 function. This pin is an open-drain configuration and needs a pull-up resistor to $V_{DD}$.

### 3.10 Exposed Thermal Pad Pin (EP)

The Exposed Pad is not electrically connected. It is recommended that you connect it to ground.

**NOTES:**


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## 4.0 GENERAL DESCRIPTION

The PAC194X is an up to four-channel, bidirectional, high-side/low-side current-sensing device with precision voltage measurement capabilities, DSP for power calculation and a power accumulator. PAC1941, PAC1942 and PAC1943 are one, two and three-channel versions of the PAC1944. These devices measure the voltage developed across an external sense resistor ($V_{SENSE}$) to represent the current of a battery or voltage regulator.

The PAC194X also measures the SENSE+ pin voltages ($V_{BUS}$). Both $V_{BUS}$ and $V_{SENSE}$ are converted to digital results by a 16-bit ADC and the digital results are multiplied to give $V_{POWER}$. The $V_{POWER}$ results are accumulated on-chip, which enables energy measurement over the accumulation period.

The PAC194X has an $I^2C$/SMBus interface for digital control and reading results. A system diagram is shown in Figure 4-1.

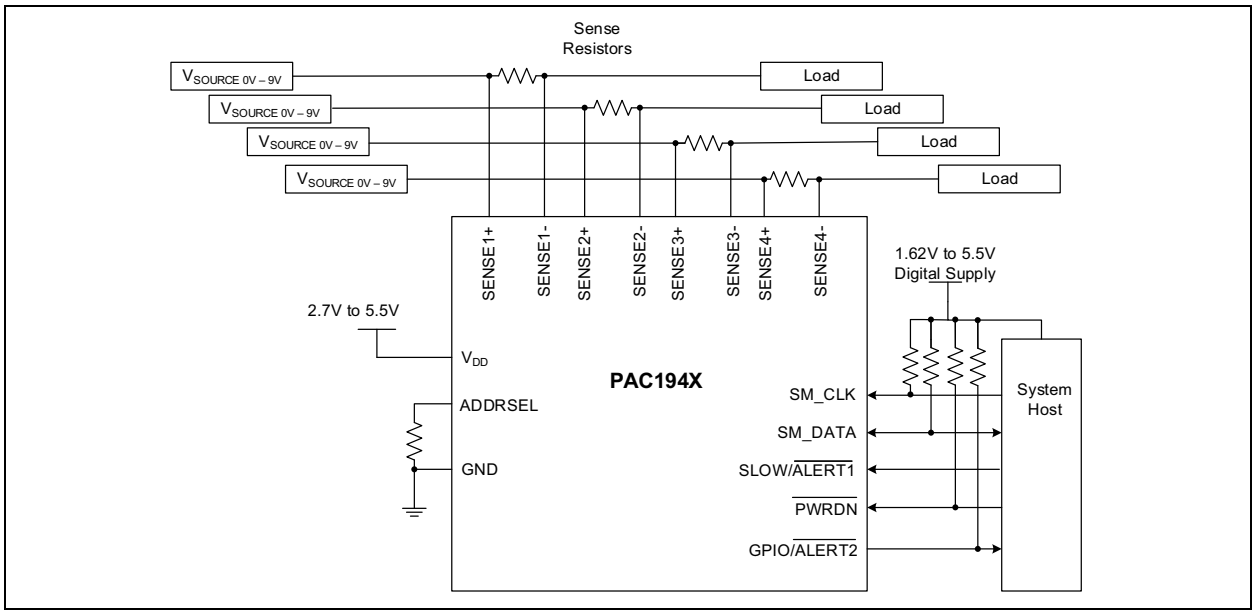
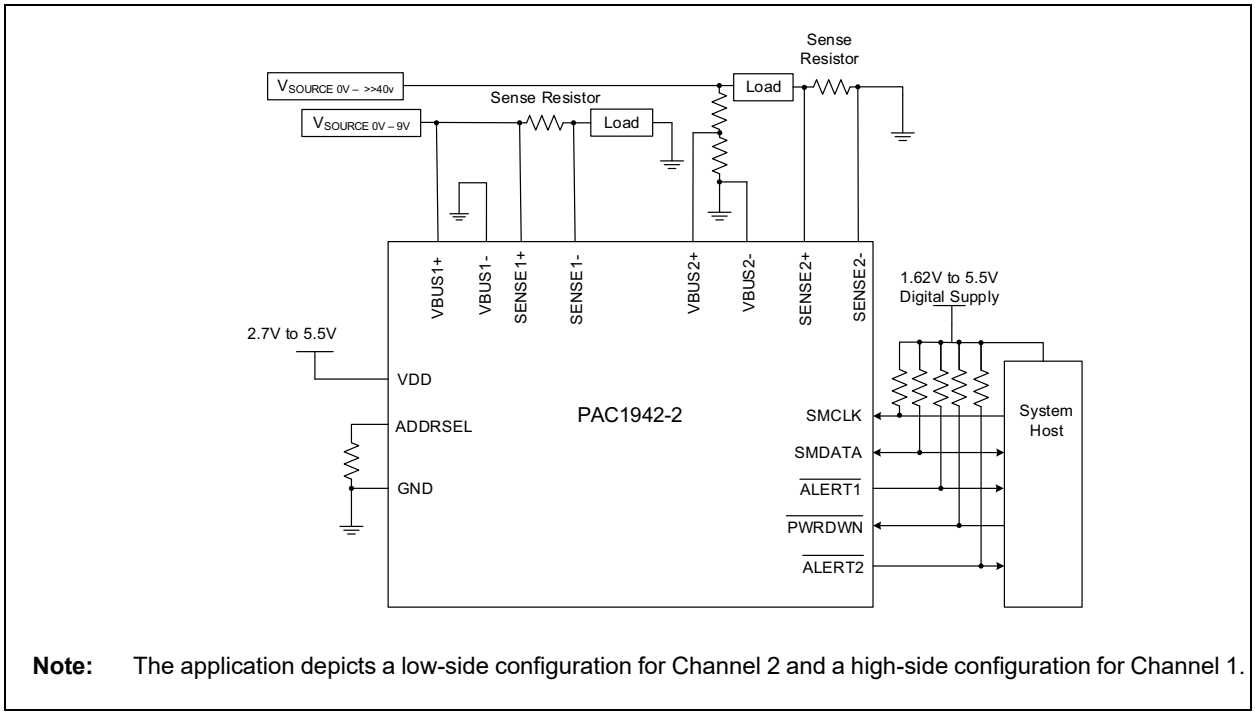



***FIGURE 4-1:*** *PAC194X-1 Typical Application Diagram.*




**Note:** The application depicts a low-side configuration for Channel 2 and a high-side configuration for Channel 1.

***FIGURE 4-2:*** *PAC194X-2 Low-Side Typical Application Diagram.*

## 4.1 Layout Considerations

It is important to optimize the layout of the $R_{SENSE}$ to ensure the most accurate measurements. When $R_{SENSE}$ values are very low, resistor connections and solder joint variation can play a large role in the accuracy of the system. Figure 4-3 shows the recommended PCB pattern for a sense resistor (highlighted in red) with wide metal trace for the high-current path. The drawing shows metal, solder paste openings and the resistor outline. $V_{SOURCE}$ connects to the +terminal of the high-current path and the load connects to the -terminal of the high-current path. SENSE+ and SENSE- have a Kelvin connection to the current sense resistor to ensure that no metal with high current is included in the $V_{SENSE}$ measurement path. SENSE+ and SENSE- must be routed as a differential pair to the SENSE inputs at the chip. The input pins allow for a typical $V_{SENSE}$ trace resistance of 1 kΩ, which allows the routing flexibility far from the chip itself on the board.

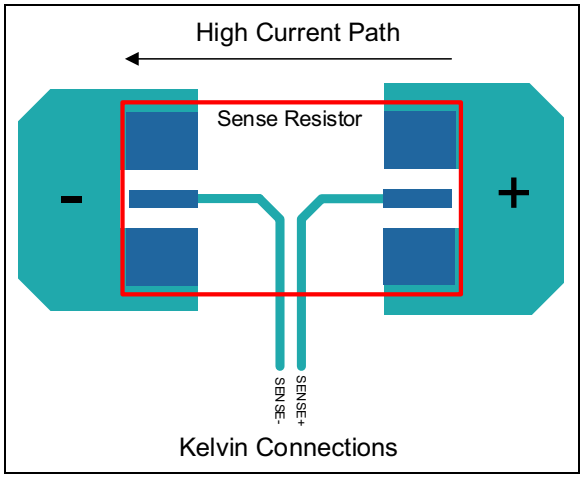



***FIGURE 4-3:*** *PCB Pattern for Sense Resistor.*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## 5.0 DEVICE OVERVIEW

A high-voltage multiplexer connects the input pins to the $V_{BUS}$ and $V_{SENSE}$ amplifiers. The amplifier outputs are sampled simultaneously for each channel, converted by 16-bit ADCs and processed for gain and offset error correction. After each conversion, $V_{BUS}$ and $V_{SENSE}$ are multiplied together to give $V_{POWER}$.

An internal oscillator and digital control signals control the two ADCs and the MUX. The MUX sequentially connects each channel's amplifiers to the ADC inputs.

The PAC1941-1, PAC1942-1, PAC1943-1 and PAC1944-1 devices share a pin for the $V_{BUS}$ measurement and the source-side voltage $V_{SENSE+}$ across an external current sense resistor, $R_{SENSE}$. This enables four input channels with eight pins. For PAC1941-2 and PAC1942-2, the chip allows $V_{BUS+}$ and $V_{BUS-}$ to go to separate pins for two channels, unconnected from the $V_{SENSE+}$ and $V_{SENSE-}$ pins. This enables the low-side current measurement.

### 5.1 Initial Operation

After Power-on Reset and a start-up sequence, the device is in the Active state and begins sampling the inputs sequentially. Voltage and current are sampled for all active channels and power is calculated and accumulated. All active channels are sampled at 1024 SPS by default. Sample rates of 256, 64 or 8 SPS may be programmed over the $I^2C$ or SMBus. If the SLOW pin is asserted, the sample rate is 8 SPS. For sampling rates lower than 1024 SPS, the device is in Sleep mode for a portion of the conversion cycle, which results in lower power dissipation. If fewer than four channels are active, power is also reduced.

To read accumulator data and reset the accumulators, the REFRESH command is used. To read the voltage, current, power and accumulator data without resetting the accumulators, the REFRESH_V command is used. Changes to the Control register (01h) are activated by sending any REFRESH command. When a new value is written to the Control register (01h), the new values take effect after the current round robin cycle (actively sampling) or before the next round robin sampling cycle following any REFRESH command.

### 5.2 REFRESH Command

The host sends the REFRESH command after changing the Control register and/or before reading accumulator data from the device. The host controls the accumulation period in this manner.

The readable registers for the $V_{BUS}$, $V_{SENSE}$, Power, accumulator outputs and accumulator count are updated by the REFRESH command and the values are static until the next REFRESH command.

These readable registers will be stable within 1 ms from sending the REFRESH command and may be read by the host at any time up until the next REFRESH command is sent.

| | |
|---|---|
| **Note:** | In Burst/Fast modes with one or more channels disabled, the 1 ms REFRESH delay will be 200 µs per channel, with an additional 200 µs delay in Fast mode for the calibration channel. The internal accumulator values and accumulator count are reset by the REFRESH command, but the sampling of the inputs, data conversion and power integration are not interrupted and continue as determined by the settings in the Control register. |

Changes written to the Control and Configuration registers take effect within 1 ms after a REFRESH command is sent. Any new commands written within this 1 ms window will be ignored and NACKed to indicate that they are ignored.

The values for $V_{BUS}$ and $V_{SENSE}$ measurement results and Power calculation results respond to the REFRESH command in the same fashion as the accumulators and accumulator count. The readable registers will be stable within 1 ms from sending the REFRESH command and may be read by the host at any time. The internal values continue to be updated according to the sampling plan determined by the settings in the Control register. The results that are sent to the readable registers for $V_{BUS}$, $V_{SENSE}$ and Power are the values from the most recent complete conversion cycle. See Register 7-1.

### 5.3 REFRESH_G Command

The REFRESH_G command is identical in every respect to the REFRESH command, but it is used with the $I^2C$ General Call address (0000 000). This allows the system to issue a REFRESH command to all of the PAC194X devices in the system with a single command. After the REFRESH_G command, the data may be read device by device to capture a snapshot of the system power and energy for all devices (see Register 7-12). Note that the REFRESH_G command can also be used with a valid client address, but in this case, only the device with this client address will receive the command. In other words, it has the same properties as the REFRESH command with the possibility of being compatible with the $I^2C$ General Call address.

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## 5.4 REFRESH_V Command

If the user wants to read $V_{SENSE}$ and $V_{BUS}$ results, the most recent Power calculation and/or the accumulator values and count without resetting the accumulators, the REFRESH_V command may be sent. Sending the REFRESH_V command and waiting 1 ms ensure that the $V_{SENSE}$, $V_{BUS}$, Power, accumulator and accumulator count values will be stable when read by the host.

**Note:** In Burst/Fast modes with one or more channels disabled, the 1 ms REFRESH delay will be 200 µs per channel, with an additional 200 µs delay in Fast mode for the calibration channel. The internal accumulator values and accumulator count are reset by the REFRESH command, but the sampling of the inputs, data conversion and power integration are not interrupted and continue as determined by the settings in the Control register.

The sampling of the inputs, data conversion and power integration are not interrupted and will continue as determined by the settings in the Control register. The data in these readable registers will remain stable until the next REFRESH or REFRESH_V/G command. The internal accumulator values and accumulator count are unaffected by the REFRESH_V command.

Note that the REFRESH_V/G command may also be used to activate changes to the Control register, just like the REFRESH command, except with the REFRESH_V command, changes to the Control register will be enacted without resetting the accumulators or accumulator count (see Register 7-13).

## 5.5 Sleep State

The Sleep state is a lower power state than the Active state. While in this state, the device will draw a supply current of $I_{SLEEP}$ from the $V_{DD}$ pin. The device automatically goes to this state between conversion cycles when sampling rates lower than 1,024 SPS are selected or if fewer than four channels are active. All digital states and data are retained in Sleep state. The device can be put in Sleep state by writing to Register 7-2, followed by a REFRESH or REFRESH_V command, and sampling will resume when a sampling mode is selected in this register, followed by a REFRESH of REFRESH_V command. The device does not go into Sleep state based on any other condition such as static conditions on the SMBus pins. If the SMBus time-out is enabled, it is supported in Sleep mode or Active mode.

## 5.6 Power-Down State

The Power-Down state is entered only by pulling the $\overline{\text{PWRDN}}$ pin low. In this state, all circuits on the chip including the SMBus pins are inactive and the device is in a state of minimum power dissipation.

In the Power-Down state, no data are retained in the chip (neither register configuration nor measurement data). When the $\overline{\text{PWRDN}}$ pin is pulled high, integration, measurement and accumulation will resume using the default register settings. The first measurement data may be requested by a REFRESH or REFRESH_V command 50 ms after the $\overline{\text{PWRDN}}$ pin is pulled high.

There is a bit called POR in Register 7-10 that is set to '1' on POR. This bit may be used to detect that a POR has occurred as follows:

1. After the initial POR, clear this bit.
2. Poll the register to see if the bit is still cleared.
3. If the bit is set when polled, a POR has occurred and the device needs to be reprogrammed (unless operating it with the default programming for all registers).

## 5.7 Slow Sampling State and $\overline{\text{ALERT1}}$

If the SLOW/$\overline{\text{ALERT1}}$ pin is pulled high, the device will sample at 8 SPS. No matter the programmed sample rate, this new SLOW sample rate takes effect on the next conversion cycle (if a round robin conversion cycle is in process when the SLOW pin goes high, that conversion cycle will complete before the SLOW sample rate takes effect).

The SLOW pin can function as the $\overline{\text{ALERT1}}$ pin instead of the conversion rate control described above. See **Section 5.16, "ALERT Functionality"** for a complete discussion on the ALERT functionality, including the $\overline{\text{ALERT2}}$ pin. If this ALERT1 functionality for the SLOW pin is enabled, the pin can no longer be used to control the conversion rate. If a pull-up resistor is attached to the SLOW/$\overline{\text{ALERT1}}$ pin for the ALERT1 functionality, the device will power-up in Slow mode because of being pulled up at power-up. Once the ALERT1 functionality is assigned to the pin (see Register 7-2), conversion will proceed at the default or programmed rate.

The SLOW pin functionality and the ALERT1 functionality cannot be used at the same time on this pin.

If the SLOW pin is configured to serve as an $\overline{\text{ALERT}}$ pin, the slower sampling rate of 8 SPS is available by programming Register 7-2.

If the device is programmed for Single-Shot mode and the SLOW pin is asserted, the first sampling will begin approximately 1 ms after the SLOW pin is asserted to allow for the analog circuitry to power up. If the device is in the Sleep state, asserting the SLOW pin will not cause sampling to start.


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Whenever the SLOW pin changes the state, a limited REFRESH or REFRESH_V command may be executed by the chip hardware (default is REFRESH). Like any other REFRESH command, this resets the accumulators and accumulator count for a REFRESH command and updates the readable registers for either REFRESH or REFRESH_V. These are limited REFRESH commands because no programmed changes to the Control or Status registers take effect (Control and Status registers are registers 01h, 1Ch, 1Dh and 20h-26h). The readable registers are stable with the new values within 1 ms of the SLOW pin transition.

The Slow register allows a selection of REFRESH or REFRESH_V commands on the SLOW pin transitions, allows this function to be disabled for either edge and also tracks both the state of the SLOW pin and the transitions on the SLOW pin (see Register 7-14).

## 5.8 Voltage Measurement

The $V_{BUS}$ voltage for each channel is measured by the SENSE+ pin for each channel. A high-voltage multiplexer is connected to each SENSE+ pin and the multiplexer sequentially connects each SENSE+ pin to an ADC input for conversion. The result is stored in a 16-bit $V_{BUS}$ results register and the 14 MSBs are multiplied by the $V_{SENSE}$ number for the $V_{POWER}$ results value. The $V_{POWER}$ results are accumulated in the accumulator.

For the PAC194X, the default FSR is 9V. The device may be programmed for bipolar $V_{BUS}$ measurements. In this Bipolar mode, the mathematical range for $V_{BUS}$ numbers is ±9V, the actual range is limited to about -200 mV due to the impact of the ESD structures. This bipolar capability for $V_{BUS}$ enables accurate offset measurement and correction. For bipolar operation, the 16-bit $V_{BUS}$ result is a two's complement (signed) number.

The measured voltage at SENSE+ can be calculated using Equation 5-1. The FSR value stays the same but the maximum range is divided in half.

**EQUATION 5-1: BUS VOLTAGE**

$$V_{SOURCE} = 9V \times \frac{V_{BUS}}{Denominator}$$

Where:

| | | |
|---|---|---|
| $V_{SOURCE}$ | = | The measured voltage on the SENSE+ pin |
| $V_{BUS}$ | = | The value read from the $V_{BUS}$ results registers |
| *Denominator* | = | $2^{16}$ for unipolar measurements |
| | = | $2^{16}$ for FSR/2 measurements |
| | = | $2^{15}$ for bipolar measurements |

## 5.9 Current Measurement

The PAC194X device family includes high-side current sensing circuits. These circuits measure the voltage ($V_{SENSE}$) induced across a fixed external current sense resistor ($R_{SENSE}$) and store the voltage as a 16-bit number in the $V_{SENSE}$ results registers.

The PAC194X current sensing operates with a FSR of 100 mV in Unidirectional mode (default).

When sensing unidirectional currents (the default mode), the ADC results are presented in unsigned binary format. For bidirectional current sensing, the ADC results are in two's complement (signed) format. For bipolar current measurements, the range is ±100 mV, but use FSR = 100 mV in the equations that follow. For best accuracy on current values near zero, it is recommended to use the bidirectional current mode and 8X average current results.

## 5.10 Selecting $R_{SENSE}$ Values

$R_{SENSE}$ can easily be calculated if the maximum current sensed is known, as shown in Equation 5-2. Consider the need to select a value for $I_{Max}$ that includes current peaks well beyond your nominal current.

**EQUATION 5-2: CALCULATING $R_{SENSE}$**

$$R_{SENSE} = \frac{FSR}{I_{Max}}$$

Where:

| | | |
|---|---|---|
| $FSR$ | = | Full-scale $V_{SENSE}$ voltage input |
| $R_{SENSE}$ | = | External $R_{SENSE}$ resistor value |
| $I_{Max}$ | = | Maximum current to measure |

Full-Scale Current (FSC) can be calculated with Equation 5-3.

**EQUATION 5-3: FULL-SCALE CURRENT**

$$FSC = \frac{100\ mV}{R_{SENSE}}$$

Where:

| | | |
|---|---|---|
| $FSC$ | = | Full-Scale Current |
| $R_{SENSE}$ | = | External sense resistor value |

The actual current through $R_{SENSE}$ can then be calculated using Equation 5-4.

**EQUATION 5-4: SENSE CURRENT**

$$I_{SENSE} = FSC \times \frac{V_{SENSE}}{Denominator}$$

Where:

| | | |
|---|---|---|
| $I_{SENSE}$ | = | Actual bus current |
| *FSC* | = | Full-Scale Current value (from Equation 5-3) |
| $V_{SENSE}$ | = | The value read from the $V_{SENSE}$ results registers |
| *Denominator* | = | $2^{16}$ for unipolar measurements |
| | = | $2^{16}$ for FSR/2 measurements |
| | = | $2^{15}$ for bipolar measurements |

## 5.11 FSR/2 RANGES

The PAC194X has a mode called FSR/2. In this mode, the FSR may be reduced by a factor of two for $V_{SENSE}$ and/or $V_{BUS}$. This mode is programmable on a channel by channel basis, for $V_{SENSE}$ and/or $V_{BUS}$ for each channel. Because of the way the ADC's 17-bit bipolar results are manipulated, in Bipolar/Bidirectional modes, the 16-bit resolution is maintained in FSR/2 and the graphs provided are valid for this mode.

The modes can be enabled for $V_{SENSE}$ and/or $V_{BUS}$ by setting bits in Register 7-19.

**TABLE 5-1: FSR/2 RANGES – $V_{BUS}$**

| $V_{BUS}$ Range | PAC194X, FSR = 9V, FSR/2 = 4.5V | Denominator for Equation 5-1 |
|---|---|---|
| Unipolar 0-FSR | 0.137 mV/LSB | $2^{16}$ |
| Bipolar +/-FSR | 0.2745 mV/LSB | $2^{15}$ |
| Bipolar +/- FSR/2 | 0.137 mV/LSB | $2^{16}$ |

**TABLE 5-2: FSR/2 RANGES – $V_{SENSE}$**

| $V_{SENSE}$ Range | PAC194X, FSR = 100 mV, FSR/2 = 50 mV | Denominator for Equation 5-4 |
|---|---|---|
| Unipolar 0-FSR | 1.5 µV/LSB | $2^{16}$ |
| Bipolar +/-FSR | 3.05 µV/LSB | $2^{15}$ |
| Bipolar +/- FSR/2 | 1.5 µV/LSB | $2^{16}$ |


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## 5.12 ADC Measurements, Offset and 8X Averaging

The PAC194X devices are primarily designed for energy measurements where many power readings are accumulated. This is inherently an averaging process. Individual voltage and current measurements can also benefit from averaging to reduce noise and offset. Averaged values are internally calculated for $V_{BUS}$ and $V_{SENSE}$, with a rolling average of the most recent eight values present in Register 7-7 and Register 7-8. The average is updated internally after every conversion cycle. The readable registers are updated with REFRESH, REFRESH_V or REFRESH_G commands like all the other readable results registers. These averaged results may be used for the most accurate, lowest noise and lowest offset measurements.

The ADC channels use a special offset canceling technique. If users observe the unaveraged results for near-zero values of $V_{BUS}$ and $V_{SENSE}$, they may observe a cyclical pattern of offset variation. The user may think this is noise, but in fact it is due to internal circuitry switching through different permutations of offset cancellation circuitry. This small variation in unaveraged offset is canceled in the 8X averaged result and minimized in single-sample results via the offset calibration channel. It is also canceled in the Power Accumulator results. The overall effect is offset that is consistently very close to zero LSB over supply and temperature variations.

The offset canceling technique is illustrated in Figure 5-1. It is very difficult to accurately observe, as it is a challenge to read the data from every conversion cycle. The effect of capturing data points at a rate that does not correspond exactly to the internal sampling rate of the PAC194X can make these permutations appear less periodic and deterministic than they are inside the chip. The data conversion uses one of the permute positions 1-4 for each input on each conversion, cycling through all four permutations in four conversions. When averaged, the permute enabled result shown below is realized, evenly distributed around zero.

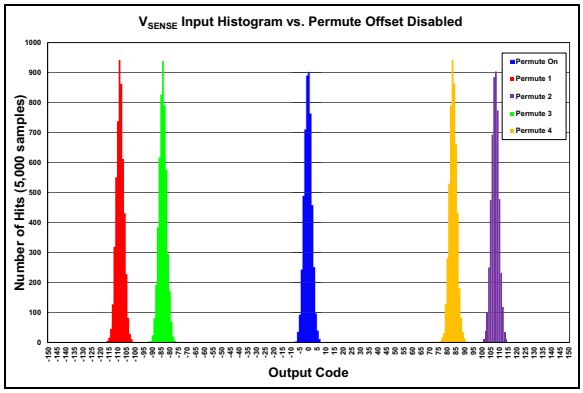


***FIGURE 5-1:*** *Illustration of the four permute combinations that the ADC cycles through and the resulting low average offset. Each bin represents one code.*

Results from both the $V_{BUS}$ and the $V_{SENSE}$ ADCs are 17-bit two's complement (signed) internally. There is an additional bit of resolution that is not accessible from the results register. Register 7-11 determines whether the conversion results are reported in the readable registers as unipolar or bipolar numbers. Using bipolar numbers can give more accurate results for very small numbers that may actually be negative for some readings, in addition to measuring bidirectional currents (charging/discharging) and voltages that can dip below ground.

Averaged values are also calculated for $V_{BUS}$ and $V_{SENSE}$. A rolling average of the most recent eight values is present in Register 7-7 and Register 7-8. These registers require eight conversion cycles after POR before they represent an accurate value, they are updated after every conversion cycle. The readable registers are updated with REFRESH, REFRESH_V or REFRESH_G commands like all the other readable results registers.

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## 5.13 Power and Energy

The PAC194X has a 56-bit accumulator and a 32-bit accumulator counter:

- 56 bits for accumulator
- 32 bits for accumulator count
- 30 bits for the power realized by multiplication of the 17-bit current number and a 14-bit voltage number

The FSR for power depends on the external sense resistor used, as shown in Equation 5-5.

**EQUATION 5-5: POWER FSR CALCULATION**

$$PowerFSR = (100\ mV / R_{SENSE}\Omega) \times 9V$$

$$PowerFSR = (0.9V^2) / R_{SENSE}\Omega$$

Where:

$R_{SENSE}\Omega$ = External $R_{SENSE}$ resistor value
$100\ mV$ = Full-scale $V_{SENSE}$ voltage input
$9V$ = Full-scale $V_{BUS}$ voltage input

The device implements power measurements by multiplying $V_{BUS}$ and $V_{SENSE}$ to give a $V_{POWER}$ result. $V_{POWER}$ values are used to calculate the proportional power, as shown in Equation 5-6. The proportional power is the fractional portion of the FSR power measured in one sample.

**EQUATION 5-6: PROPORTIONAL POWER CALCULATION**

$$P_{PROP} = \frac{V_{POWER}}{Denominator}$$

Where:

*Denominator* = $2^{30}$ (Unipolar mode)
= $2^{30}$ (FSR/2 mode)
= $2^{29}$ (Bipolar mode)

To calculate the actual power from the proportional power, multiply by the FSR power, as shown in Equation 5-7. This actual power number is the power measured in one sample.

**EQUATION 5-7: POWER CALCULATION**

$$P_{ACTUAL} = PowerFSR \times P_{PROP}$$

These $V_{POWER}$ results are digitally accumulated on chip and stored in the $V_{ACCN}$ registers.

The energy calculation in Equation 5-8 and 5-9 uses a different denominator term depending on the Unipolar or Bipolar mode. Bipolar mode for energy applies when the Bipolar/Bidirectional mode is used for $V_{BUS}$ and/or $V_{SENSE}$. Equation 5-8 shows how to realize this using the accumulator results, accumulator count and the accumulation period, T. In this equation, T must be known from a system clock time stamp or other accurate indicator of the total accumulation period.

**EQUATION 5-8: ENERGY CALCULATION**

$$Energy = \frac{V_{ACCN}}{Denominator} \times (PwrFSR) \times \frac{T}{AccCount}$$

Where:

*Denominator* = $2^{30}$ (Unipolar mode)
= $2^{30}$ (FSR/2 mode)
= $2^{29}$ (Bipolar mode)

**EQUATION 5-9: ENERGY CALCULATION**

$$Energy = \frac{V_{ACCN}}{Denominator} \times \frac{(PwrFSR)}{f_S}$$

Where:

*Denominator* = $2^{30}$ (Unipolar mode)
= $2^{30}$ (FSR/2 mode)
= $2^{29}$ (Bipolar mode)

Equation 5-9 shows how to calculate energy using the accumulated power and the sampling rate, $f_S$.

### 5.13.1 ADAPTIVE ACCUMULATOR

The PAC194X has a feature called Adaptive Accumulator mode. In this mode, sampling is programmed at one of the valid sample rates and samples are accumulated. If the SLOW pin is asserted and the device begins sampling at 8 SPS, these samples are shifted by 7 bits to the left and accumulated so as to simulate sampling at the maximum sampling rate, 1024 SPS, and the accumulator count is also incremented by 128 for each sample in Slow mode (when using the Adaptive Accumulator mode) to simulate samples being accumulated at the maximum sampling rate.

This offers a big reduction in host overhead and bus traffic for systems that need to use the SLOW pin for lower power operation during certain times and want to have continuous accurate energy monitoring for both the maximum sampling rate and the SLOW sampling rate.


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As shown in Equation 5-8 and Equation 5-9, it is necessary to know the sampling frequency and sampling period for each interval that we want to accumulate energy over. If the SLOW pin is used and the period changes, the accumulator value and count must be fetched and calculated each time the sampling rate changes. With the adaptive accumulator, the data only need to be fetched before the accumulator and/or accumulator count overflow and an accurate energy calculation can be made, independent of how many times the SLOW pin was asserted and deasserted during the period. The sample rate for these calculations is the programmed sample rate.

Because the Adaptive Accumulator mode is the default mode, the feature of an internal REFRESH being generated on assertion/deassertion of the SLOW pin is defaulted to inactive. The user must manually program a REFRESH on SLOW pin transition, if desired, using Register 7-14.

By programming one of the adaptive accumulator sampling rates in Register 7-2 other than 1024 SPS, the accumulator and accumulator count will shift the data and count to mimic accumulation at 1024 SPS.

### 5.13.2 ADDITIONAL ACCUMULATOR INFORMATION

The math for the power calculation and accumulation inside the chip is always done in two's complement math, no matter what the user sets the output registers to show. $V_{BUS}$ and $V_{SENSE}$ are 17-bit two's complement (signed) numbers internally. $V_{POWER}$ is the product of $V_{SENSE}$ multiplied by the 14 MSBs of $V_{BUS}$ and this is a 30-bit two's complement result (signed) internally. In some cases, this results in a power result that is not identical to the product of the $V_{BUS}$ results register multiplied by the $V_{SENSE}$ register. However, the power result from the $V_{POWER}$ results register is more accurate than the product of the $V_{BUS}$ register multiplied by the $V_{SENSE}$ register in these cases, as explained below.

If $V_{SENSE}$ and $V_{BUS}$ are both programmed to be unsigned (unipolar) in register Register 7-11, 16 bits without sign are exported to the $V_{BUS}$ and $V_{SENSE}$ results registers.

If $V_{BUS}$ is programmed to be signed (bipolar) in Register 7-11, the corresponding data are truncated to 16-bit two's complement (signed) for the readable results register.

If $V_{SENSE}$ is programmed to be signed (bidirectional) in register Register 7-11, the corresponding $V_{SENSE}$ register value is truncated to 16-bit two's complement, but the power calculation uses 17-bit two's complement. Therefore, a mismatch is possible between an externally calculated power value ($V_{BUS}$ times $V_{SENSE}$) and the actual power value calculated internally to the chip.

The internally calculated (and accumulated) value is more accurate than the externally calculated value in every case.

This is also true for FSR/2 modes, in that the FSR/2 mode uses bit shifting to change the FSR so no accuracy is lost in the power calculation (similar to Unipolar mode).

The continuous power integration periods (also called energy accumulation periods) can range from ~1 ms to many hours, depending on the number of samples per second selected via SMBus. The number of samples is limited by the size of the Accumulator Count register to 4,294,967,296 ($2^{32}$). This count corresponds to about 1165 hours at 1024 SPS or about 17 years at 8 SPS. This accumulator count can overflow and it will not reset when it overflows.

When the accumulation registers reach their maximum value, this is called accumulator overflow. The accumulator outputs remain at their maximum value; they do not rollover. The user can calculate the worst-case time to saturation and read them at or before that time or use the accumulator fullness limits to detect when the accumulators and/or accumulator count are 15/16, 7/8, 3/4 or completely full and read and/or reset them at that time (see Register 7-23).

Worst-case accumulator overflow time can be calculated assuming that every measurement that is accumulated is a full-scale number. Since the power numbers are 30 bits and the accumulator is 56 bits, $2^{26}$ samples can be accumulated before overflow, if they are all full-scale values. For most applications, they will not all be full-scale numbers; this is especially true if $V_{BUS}$ is nominally less than the maximum $V_{BUS}$ for the device. If the maximum $V_{BUS}$ for the system is always lower than FSR for $V_{BUS}$, the maximum number of full-scale samples that can be accumulated is scaled by FSR/$V_{BUS}$ maximum for the system. If both $V_{BUS}$ and $V_{SENSE}$ values are always near full scale, this can limit the accumulation period before overflow to 1092 minutes at 1024 SPS or 2330 hours at 8 SPS. If sample values are well below full scale, the user can calculate how many samples can be accumulated before the accumulator will overflow. As described above, the accumulator count will likely not limit the number of samples that can be accumulated and counted.

#### 5.13.3 ALTERNATIVE USES FOR THE ACCUMULATOR

For the PAC194X, the accumulator may be used to accumulate $V_{SENSE}$ or $V_{BUS}$ values instead of $V_{POWER}$ values for any channel. This functionality is invoked by setting bits in Register 7-19.

Setting the accumulator for a channel to accumulate $V_{SENSE}$ values gives a measure of accumulated current, which is equivalent to charge. This allows the accumulator to be used as a coulomb counter.

For either $V_{SENSE}$ or $V_{BUS}$, many samples may be accumulated on chip and the result collected by the host and divided by the accumulator counter count value to yield an average value with a very long integration time to reduce noise. This feature is also very useful for system calibration, allowing many averages to be accumulated for fast averaging/noise reduction. Calibration time can be further reduced by combining this with the Fast mode.

## 5.14 Conversion Cycles

A conversion cycle for the device consists of the analog-to-digital conversion being complete for all channels (including the real-time calibration that is part of each conversion cycle). Immediately following the data conversion, the power results are calculated for that channel and the power value is added to the accumulator. Averaged values for $V_{SENSE}$ and $V_{BUS}$ are also updated internally as part of each conversion cycle.

Data conversion and processing are performed for each active channel in sequential fashion until all active channels are converted, completing the conversion cycle for the device. The sequential sampling of each channel, along with the calculation time and any sleep time needed to set the overall sampling rate, is referred to as a round robin sampling period.

## 5.15 Conversion Cycle Controls

#### 5.15.1 REDUCING THE NUMBER OF CHANNELS TO BE SAMPLED

Register 7-2 allows the user to reduce the number of channels that are active. The sample rate is unaffected, but power dissipation is reduced if some channels are disabled. Any or all channels may be disabled; if all channels are disabled, the device goes into Sleep mode.

#### 5.15.2 BURST MODE

For the PAC194X, Burst mode is added for faster sampling. In this mode, the round robin sequencer enables each active channel sequentially and restarts the round robin sequence again without sleeping in between as it normally does. The fifth channel that is used for offset canceling is not sampled in this mode, the previous value for offset canceling is repeatedly used, so sampling will not be as accurate if this mode is used for long periods of time, especially if temperature changes, although the 8X average accuracy will not be significantly affected.

The effective sampling mode changes with the number of active channels, as shown in Table 5-3. The Burst mode is enabled by setting a bit in Register 7-2.

**TABLE 5-3: BURST MODE ENABLED**

| Active Channels | Sampling Frequency |
|---|---|
| 1 | 1024*5/1 = 5120 SPS |
| 2 | 1024*5/2 = 2560 SPS |
| 3 | 1024*5/3 = 1706 SPS |
| 4 | 1024*5/4 = 1280 SPS |

#### 5.15.3 FAST MODE

Fast mode is also a mode for faster sampling. It is similar to Burst mode, only in Fast Mode, the fifth channel is converted and used for continuous offset correction.

The effective sampling mode changes with the number of active channels, as shown in Table 5-4. The Burst mode is enabled by setting a bit in Register 7-2.

**TABLE 5-4: FAST MODE ENABLED**

| Active Channels | Sampling Frequency |
|---|---|
| 1 | 1024*5/2 = 2560 SPS |
| 2 | 1024*5/3 = 1706.6 SPS |
| 3 | 1024*5/4 = 1280 SPS |
| 4 | 1024*5/5 = 1024 SPS |


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### 5.15.4 SINGLE-SHOT MODE

The Control register also allows the device to operate in Single-Shot mode. In this mode, all active channels will sample and convert, followed by results being calculated. The accumulator and accumulator count operate the same as for Continuous Conversion mode, accumulating each single-shot power calculation and incrementing the accumulator count. The conversion cycle will start when the REFRESH command (or REFRESH_V/REFRESH_G) is sent.

After the single-shot measurements and calculations are complete, the device goes into Sleep mode. A REFRESH, REFRESH_G or REFRESH_V command may be sent to read the data. The user needs to wait about 2 ms after the REFRESH command before commanding another single-shot conversion, by means of sending one of the REFRESH commands. This is because a 1 ms delay is required between REFRESH commands and coming out of Sleep requires 1 ms (band gap start-up delay). In general, single-shot commands are not this close together in time; instead, one of the lower sampling rates is used.

There is an option to use a single REFRESH command to collect eight samples and average them in Single-Shot 8X mode. This reduces noise and offset in the result (see Register 7-2). In this mode, all eight samples are added to the accumulator and the accumulator count is incremented by eight each time a REFRESH is sent to trigger an additional Single-Shot 8X acquisition and conversion.

In Single-Shot 8X mode, the 8X averaged result is read from the 8X averaged registers (Register 7-7 and Register 7-8) and the unaveraged result registers (Register 7-5 and Register 7-6) hold the last of the 8 samples.

## 5.16 ALERT Functionality

The ALERT functionality has multiple purposes: to notify the system that a conversion cycle for all active channels is complete, to notify the system that the accumulator or accumulator count has overflowed or that an electrical parameter is outside the programmed limit.

Alerts will cause the $\overline{\text{ALERT}}$ pin to be asserted low and latched low. The only exception to this is for the ALERT after COMPLETE_CONVERSION, this will cause a 5 µs pulse of the $\overline{\text{ALERT}}$ pin. Alerts are set at the end of the round robin cycle.

### 5.16.1 ALERT AFTER COMPLETE CONVERSION

Register 7-21 and Register 7-22 have bits ALERT_CC1 and ALERT_CC2 that can be used to enable the ALERT_CC function. If this bit is set, the assigned $\overline{\text{ALERT}}$ pin goes low for 5 µs after each round robin conversion cycle is complete. This function may be used when you want to read data continuously as soon as each round robin conversion cycle is complete.

| **Note:** | When using the device in single-channel Burst mode, the Conversion Complete ALERT will not assert. |
|---|---|

This Conversion Complete ALERT does not set a bit in Register 7-20.

### 5.16.2 $\overline{\text{ALERT}}$ PIN ASSIGNMENTS

The ALERT function may be assigned to either the SLOW/$\overline{\text{ALERT1}}$ pin or the GPIO/$\overline{\text{ALERT2}}$ pin. Use Register 7-21 and/or Register 7-22 to assign any of the ALERT functions to these pins.

To configure the SLOW/$\overline{\text{ALERT}}$ pin to function as $\overline{\text{ALERT}}$, use Register 7-2. Note that the SLOW function of this pin cannot be used once the ALERT function is programmed for this pin.

There is a general ALERT signal on bit 5 of the SMBus Settings (1Ch). This register bit can be monitored over the $I^2C$/SMBus or monitored on the $\overline{\text{ALERT}}$/SLOW, as mentioned above. This register does not require a Refresh signal to update the values, so it is easy to poll if the user desires.

### 5.16.3 USING THE $\overline{\text{ALERT}}$ PINS AS I/O PINS

The $\overline{\text{ALERT}}$ pins may also be used as I/O pins. This functionality is enabled in Register 7-2. When used as an I/O pin, there are bits for holding input and output data (read or to be written) in Register 7-10. This register does not need a Refresh to update it, so the input data may be read or the output data changed without affecting anything else.

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### 5.16.4 ALERT FUNCTIONALITY – VOLTAGE, CURRENT AND POWER

The ALERT functionality enables the user to capture voltage and current events that exceed programmable limits, for one or more samples. The ALERT function may be monitored on a digital output pin by configuring one of the $\overline{\text{ALERT}}$ pins to correspond to a specific ALERT or to multiple ALERT signals using Register 7-21 or Register 7-22. The ALERT status may also be monitored over the $I^2C$/SMBus by reading Register 7-20.

$\overline{\text{ALERT}}$ can be triggered by a variety of triggers; $V_{BUS}$ overvoltage or undervoltage (OV or UV), $V_{SENSE}$ overcurrent or undercurrent (OC or UC), overpower (OP), conversion cycle complete or accumulator/accumulator count hitting a limit for fullness or overflowing.

The OV, UV, OC, UC and/or OP limits must be enabled for any of the channels that will be using them, by setting a bit in Register 7-34. These limits are specified with two's complement values independent of whether Unipolar/Bipolar Or Unidirectional/Bidirectional modes are set for $V_{BUS}$ and $V_{SENSE}$ measurements. Only ALERT conditions that are enabled here are capable of triggering any ALERT. A REFRESH (or REFRESH_V/G) command is required after writing to Register 7-34 for the ALERTs to be enabled.

### 5.16.5 ALERT THRESHOLD LIMITS

Each channel has programmable 16-bit limits for overcurrent, undercurrent, overvoltage and undervoltage. The overpower limit is a 24-bit number.

The thresholds for these ALERTs are set in Register 7-24, Register 7-25, Register 7-26, Register 7-27 and Register 7-28.

### 5.16.6 SAMPLES OVER LIMIT TO TRIGGER ALERT

The user can also program how many samples must exceed the threshold to trigger the $\overline{\text{ALERT}}$ pin (over limit samples). The default value for over limit samples is 1 (up to a maximum 16 samples), which means the ALERT will be triggered on the first sample that exceeds the threshold. For OC, OP and OV, exceeding the threshold means a sample that is of larger value than the programmed limit. For UC and UV, exceeding the threshold means a sample that is of smaller value than the programmed limit. The OP limit differs slightly from the other limits in that it is always magnitude based. Thus a more positive value or more negative value will trigger an OP alert.

The user can program how many samples over the threshold are required to trigger the ALERT for each of these parameters in Register 7-28, Register 7-29, Register 7-31, Register 7-32 and Register 7-33.

### 5.16.7 ACCUMULATOR-BASED ALERTS

The ALERT function can also be programmed to trigger when the accumulator or accumulator count for any channel is filled to a specified amount. This amount can be programmed from 15/16 full through 7/8, 3/4 or completely full. This enables the user to maximize the accumulation time instead of simply planning for the worst case. The limits for each channel are specified in Register 7-23.

When the ALERT is tripped, the user can interrogate Register 7-20 to determine which conditional limit, which channel(s) or if the accumulator/accumulator count condition triggered the ALERT. The ALERT condition is cleared when these ALERT cause registers are read, specifically when the register that caused for the specific ALERT cause is read.

Register 7-20 is updated immediately on an ALERT condition, it does not require a REFRESH command.

When the ALERT function is tripped by accumulator overflow, it remains asserted until a REFRESH command is received. REFRESH_G will also clear the ALERT bit and the ALERT function, but REFRESH_V will not.

### 5.16.8 ALERT CLEARING AND PERSISTENT FAULT CONDITIONS

If the over/undervoltage, over/undercurrent or overpower conditions that tripped the ALERT or accumulator full conditions are still present after the ALERT cause register is read (which clears all the bits in that register and resets the ALERT function), the ALERT function will reassert, if the next converted sample that detects the limit is exceeded.

Register 7-20 is cleared when it is read. If the ALERT condition is still present after the next conversion cycle is complete, the ALERT is reasserted.


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## 6.0 SMBUS AND I²C COMMUNICATIONS PROTOCOL

The PAC194X devices communicate over a two-wire bus with a controller, using a SMBus or I²C serial communication protocol. A detailed timing diagram is shown in Figure 6-1.

Stretching of the SMCLK signal is supported. However, the PAC194X will not stretch the clock signal itself.

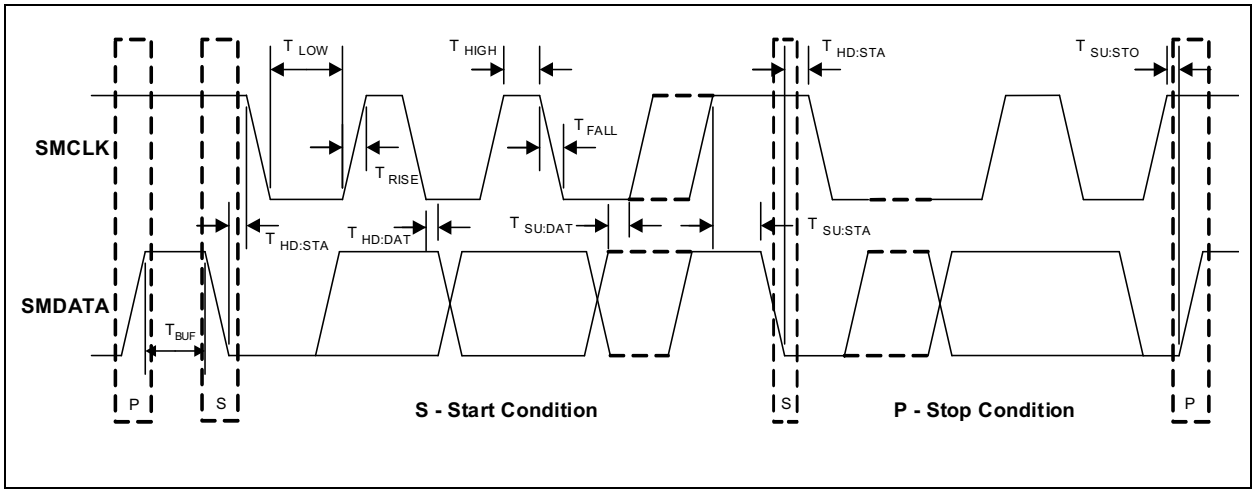


***FIGURE 6-1:*** *SMBus Timing Diagram.*

## 6.1 I²C/SMBus Addressing and Control Bits

### 6.1.1 SMBUS ADDRESS AND RD/$\overline{WR}$ BIT

The SMBus Address byte consists of the 7-bit client address followed by a 1-bit RD/$\overline{WR}$ indicator. If this RD/$\overline{WR}$ bit is a logic '0', the SMBus host writes data to the client device. If this RD/$\overline{WR}$ bit is a logic '1', the SMBus host reads data from the client device.

The PAC194X I²C/SMBus address is determined by a single pull-down resistor connected between ground and the ADDRSEL pin, as shown in Table 6-1. The chip translates the resistor value into an address on power-up and the value is latched until another power-up event takes place. The address cannot be changed on the fly.

### 6.1.2 SMBUS START BIT

The SMBus Start bit is defined as a transition of the SMBus data line from a logic '1' state to a logic '0' state, while the SMBus clock line is in a logic '1' state.

### 6.1.3 SMBUS ACK AND NACK BITS

The SMBus client will ACK (acknowledge) all data bytes that it receives. This is done by the client device pulling the SMBus data line low after the eighth bit of each byte that is transmitted.

### 6.1.4 SMBUS STOP BIT

The SMBus Stop bit is defined as a transition of the SMBus data line from a logic '0' state to a logic '1' state, while the SMBus clock line is in a logic '1' state. When the PAC194X detects an SMBus Stop bit and it has been communicating with the SMBus protocol, it resets its client interface and prepares to receive further communications.

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### 6.1.5 SMBUS DATA BYTES

All SMBus data bytes are sent MSb first and composed of 8 bits of information.

**TABLE 6-1: ADDRESS SELECT RESISTOR**

| Resistor (1%) | SMBus Address |
|---|---|
| 0 (GND) | 0010 000 (R/W) |
| 499 | 0010 001 (R/W) |
| 806 | 0010 010 (R/W) |
| 1,270 | 0010 011 (R/W) |
| 2,050 | 0010 100 (R/W) |
| 3,240 | 0010 101 (R/W) |
| 5,230 | 0010 110 (R/W) |
| 8,450 | 0010 111 (R/W) |
| 13,300 | 0011 000 (R/W) |
| 21,500 | 0011 001 (R/W) |
| 34,000 | 0011 010 (R/W) |
| 54,900 | 0011 011 (R/W) |
| 88,700 | 0011 100 (R/W) |
| 140,000 | 0011 101 (R/W) |
| 226,000 | 0011 110 (R/W) |
| Tie to $V_{DD}$ | 0011 111 (R/W) |

## 6.2 SMBus Time-out

The PAC194X devices can support the SMBus time-out functionality. This functionality is disabled by default and can be enabled by writing to the TIMEOUT bit (see Register 7-10).

If time-out is enabled and the clock is held at logic '0' for 25 ms-35 ms, the device will time-out and reset the SMBus interface. Communication is restored with a Start condition.

## 6.3 SMBus and I²C Compatibility

The PAC194X devices are compatible with the SMBus 3.1 1 MHz class and the I²C Fast mode Plus. The major differences between SMBus and I²C devices are highlighted below (for more information, refer to the SMBus 3.1 and I²C specifications):

1. The minimum frequency for SMBus communications is 10 kHz, if the time-out function is enabled. If the time-out function is disabled (default condition), there is no minimum frequency for SMBus communications.
2. I²C does not have a time-out, this is the default condition. The SMBus client protocol will reset if the clock is held at a logic '0' for $t_{TIMEOUT}$, if SMBus time-out is enabled in Register 7-10.
3. I²C devices do not support the Alert Response Address functionality (which is optional for SMBus). The PAC194X does not support the Alert Response Address functionality. Instead, the $\overline{ALERT}$ pin, when configured for ALERT, is an open-drain output pin that may be monitored by the host or embedded controller.
4. I²C devices support Block Read and Block Write differently. The I²C protocol allows for an unlimited number of bytes to be sent in either direction. The SMBus protocol for Block Read and Block Write requires that an additional data byte indicating the number of bytes to read/write is transmitted. The PAC194X devices support the I²C protocol for Block Read by default (no byte count information is sent). If the Byte Count bit is set (see Register 7-10), the Byte Count will be sent as the first data byte in response to the Block Read command, per SMBus protocol.
5. SMBus uses fixed logic thresholds for logical high and low signals. I²C uses levels that are proportional to $V_{DD}$. PAC194X uses fixed logic levels of 0.8V and 1.35V, as specified by SMBus.


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## 6.4 I²C/SMBus Protocols

The PAC194X supports Write Byte, Block Write, Read Byte, Block Read, Send Byte and Receive Byte as valid protocols.

It does not respond to the Alert Response Address protocol. It responds to the I²C General Call Address.

All the protocol charts listed below use the convention in Table 6-2.

**TABLE 6-2: PROTOCOL FORMAT**

| Data Sent to Device | Data Sent to the Host |
|---|---|
| # of bits sent | # of bits sent |

## 6.5 Auto-Incrementing Pointer

The PAC194X has an auto-incrementing address pointer. The pointer has two loops for auto-incrementing, a read loop and a write loop.

The read loop includes all the readable registers, all the configuration and control registers, the results registers, Product ID, Manufacturer ID and Revision ID registers.

The write loop includes only the writable control and configuration registers.

Neither loop includes the REFRESH commands.

The read loop skips the inactive channels, if some channels are disabled. This automatic channel skipping feature can be disabled by setting the NO SKIP bit in Register 7-10.

There are two cases to consider when a channel is disabled and a read is performed on it:

- the SKIP function is OFF, the register address will be ACKed and the data returned are FFh, followed by a NACK.
- the SKIP function is ON, the register address will be NACKed and the data returned are FFh, followed by a NACK.

In the first case, the channel address is still part of the register map and is still a valid address, thus the I²C/SMBus ACK the address. In the second case, the channel address is removed from the register map and becomes an invalid address, thus the I²C/SMBus NACK the address. In both cases, the value returned is FFh, because the channel is disabled (invalid) and the I²C/SMBus NACK the data. See Figure 6-2 for a graphic representation.

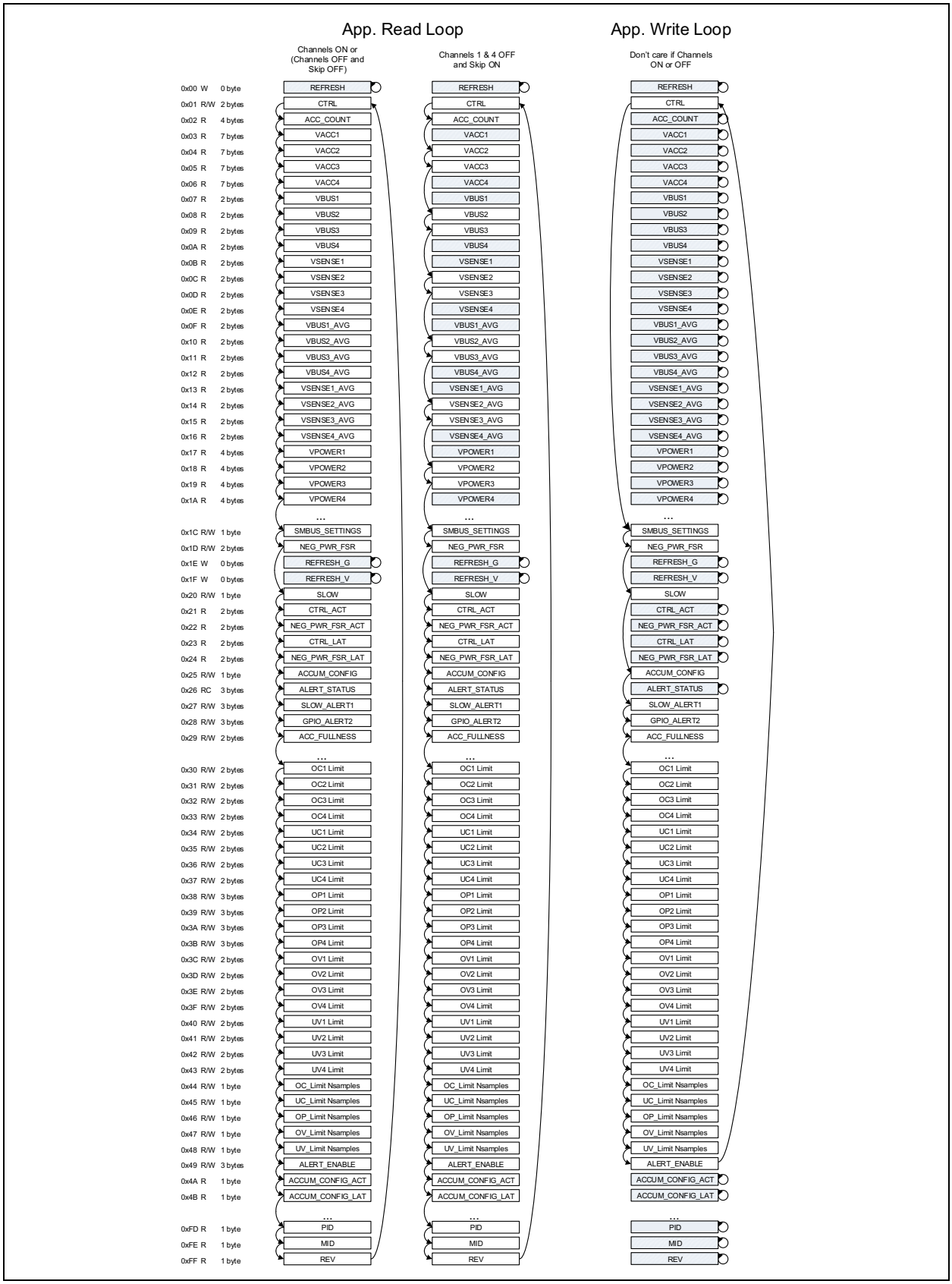


***FIGURE 6-2:*** *Read and Write Auto-Incrementing Loops.*


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Figure 6-2 shows how the auto-incrementing read loop works with the SKIP option on and off. It also shows how the write loop works with the REFRESH, REFRESH_V and REFRESH_G commands.

## 6.6 I²C/SMBus Commands

### 6.6.1 REFRESH AND REFRESH_V

REFRESH and REFRESH_V commands are sent using the Send Byte command, the client address and the desired command (00h for REFRESH or 1Fh for REFRESH_V). See Table 6-3.

**TABLE 6-3: REFRESH AND REFRESH_V COMMANDS**

| START | Client Address | WR | ACK | REFRESH or REFRESH_V Command | ACK | STOP |
|---|---|---|---|---|---|---|
| 1 → 0 | YYYY_YYY | 0 | 0 | 00h or 1Fh | 0 | 0 → 1 |

### 6.6.2 GENERAL CALL ADDRESS RESPONSE

When the host sends the General Call address, the PAC194X is able to execute the REFRESH command by means of a second version of the REFRESH command called REFRESH_G (see Register 7-12).

Just as the REFRESH command is sent using a Send Byte command with the client address and the REFRESH command (00h), the REFRESH_G command is sent using Send Byte with the General Call address (0000 000) and the REFRESH_G command (1Eh).

Table 6-4 shows the response to the General Call command for REFRESH_G.

**TABLE 6-4: GENERAL CALL RESPONSE**

| START | General Call Address | WR | ACK | REFRESH_G Command | ACK | STOP |
|---|---|---|---|---|---|---|
| 1 → 0 | 0000_000 | 0 | 0 | 1Eh | 0 | 0 → 1 |

### 6.6.3 WRITE BYTE

The Write Byte is used to write one byte of data to the registers, as shown in Table 6-5.

**TABLE 6-5: WRITE BYTE PROTOCOL**

| START | Client Address | WR | ACK | Register Address | ACK | Register Data | ACK | STOP |
|---|---|---|---|---|---|---|---|---|
| 1 → 0 | YYYY_YYY | 0 | 0 | XXh | 0 | XXh | 0 | 0 → 1 |

### 6.6.4 READ BYTE

The Read Byte protocol is used to read one byte of data from the registers, as shown in Table 6-6.

If an invalid register address is specified, the client will ACK its address but NACK the register address.

The host will NACK (not acknowledge) the data received from the client by holding the SMBus data line high after the eighth data bit is sent.

**TABLE 6-6: READ BYTE PROTOCOL**

| START | Client Address | WR | ACK | Register Address | ACK | START | Client Address | RD | ACK | Register Data | NACK | STOP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 → 0 | YYYY_YYY | 0 | 0 | XXh | 0 | 1 → 0 | YYYY_YYY | 1 | 0 | XXh | 1 | 0 → 1 |

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### 6.6.5 SEND BYTE

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data are transferred during the Send Byte protocol, as shown in Table 6-7.

**TABLE 6-7: SEND BYTE PROTOCOL**

| START | Client Address | WR | ACK | Register Address | ACK | STOP |
|---|---|---|---|---|---|---|
| 1 → 0 | YYYY_YYY | 0 | 0 | XXh | 0 | 0 → 1 |

### 6.6.6 RECEIVE BYTE

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g., set via Send Byte). This is shown in Table 6-8.

When an ACK is received after the register data, the address pointer automatically increments.

When a NACK is received after the register data, the address pointer stays at the same position.

If the host wishes to continue clocking and reading the next register, the host will ACK after the register data, instead of sending NACK followed by STOP.

If some channels are deactivated, their data registers will be skipped by the auto-incrementing pointer. Alternatively, you may set bit 0 in Register 7-10 and the pointer will not skip the addresses associated with the inactive channels. The measurement data for these inactive channels will read FFh.

**TABLE 6-8: RECEIVE BYTE PROTOCOL**

| START | Client Address | RD | ACK | Register Data | NACK | STOP |
|---|---|---|---|---|---|---|
| 1 → 0 | YYYY_YYY | 1 | 0 | XXh | 1 | 0 → 1 |

### 6.6.7 BLOCK WRITE – $I^2C$ VERSION

Block Write is used to write multiple data bytes from a register that contains more than one byte of data or from a group of contiguous registers, as shown in Table 6-9. The PAC194X supports $I^2C$ Block Write by default, the SMBus format is not supported.

If an invalid register address is specified, the client will ACK its address but NACK the register address.

The host will NACK the data received from the client by holding the SMBus data line high after the eighth data bit is sent.

**TABLE 6-9: BLOCK WRITE PROTOCOL – $I^2C$ VERSION (DEFAULT)**

| START | Client Address | WR | ACK | Register Address | ACK | Register Data | ACK |
|---|---|---|---|---|---|---|---|
| 1 → 0 | YYYY_YYY | 0 | 0 | XXh | 0 | XXh | 0 |
| **Register Data** | **ACK** | **Register Data** | **ACK** | | **Register Data** | **ACK** | **STOP** |
| XXh | 0 | XXh | 0 | | XXh | 0 | 0 → 1 |

### 6.6.8 BLOCK READ – $I^2C$ VERSION

Block Read is used to read multiple data bytes from a register that contains more than one byte of data or from a group of contiguous registers, as shown in Table 6-10. The PAC194X supports $I^2C$ Block Read by default, but the SMBus format can also be supported (see Table 6-11).

If an invalid register address is specified, the client will ACK its address but NACK the register address.

The host will NACK the data received from the client by holding the SMBus data line high after the eighth data bit is sent.


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**TABLE 6-10: BLOCK READ PROTOCOL – I²C VERSION (DEFAULT)**

| START | Client Address | WR | ACK | Register Address | ACK | STAR T | Client Address | RD | ACK | Register Data |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 → 0 | YYYY_YYY | 0 | 0 | XXh | 0 | 1 → 0 | YYYY_YYY | 1 | 0 | XXh |
| **ACK** | **Register Data** | **ACK** | **Register Data** | **ACK** | **Register Data** | **ACK** | | **Register Data** | **NACK** | **STOP** |
| 0 | XXh | 0 | XXh | 0 | XXh | 0 | | XXh | 1 | 0 → 1 |

### 6.6.9 BLOCK READ – SMBUS VERSION

The PAC194X can also support the SMBus version of Block Read. If the Byte Count bit is set, Block Read will result in the device sending the Byte Count data before the first data byte. This protocol is shown in Table 6-11.

**TABLE 6-11: BLOCK READ PROTOCOL – SMBUS VERSION (MUST SET BYTE COUNT BIT)**

| START | Client Address | WR | ACK | Register Address | ACK | STAR T | Client Address | RD | ACK | Byte Count |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 → 0 | YYYY_YYY | 0 | 0 | XXh | 0 | 1 → 0 | YYYY_YYY | 1 | 0 | XXh = N |
| **ACK** | **Register Data** | **ACK** | **Register Data** | **ACK** | **Register Data** | **ACK** | | **Register Data** | **NACK** | **STOP** |
| 0 | XXh | 0 | XXh | 0 | XXh | 0 | | XXh | 1 | 0 → 1 |

**NOTES:**


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## 7.0 REGISTERS DESCRIPTION

**TABLE 7-1: REGISTER SET IN HEXADECIMAL ORDER**

| Register Name | Description | Type | Bytes | POR Value |
|---|---|---|---|---|
| REFRESH (Address 00h) Register | Send Byte for REFRESH command | SEND | 0 | N/A |
| CTRL (ADDRESS 01H) Register | Configures sampling modes and $\overline{\text{ALERT}}$ pins | R/W | 2 | 0700h (**Note 2**) |
| ACC_COUNT (02H) Register | Accumulator count for all channels | Block Read | 4 | **Note 1** |
| VACCN (03H-06H) Register | Accumulator output for Channel 1 | Block Read | 7 | **Note 1** |
| | Accumulator output for Channel 2 | Block Read | 7 | **Note 1** |
| | Accumulator output for Channel 3 | Block Read | 7 | **Note 1** |
| | Accumulator output for Channel 4 | Block Read | 7 | **Note 1** |
| VBUSN (07H-0AH) Register | $V_{BUS}$ measurement for Channel 1 | Block Read | 2 | **Note 1** |
| | $V_{BUS}$ measurement for Channel 2 | Block Read | 2 | **Note 1** |
| | $V_{BUS}$ measurement for Channel 3 | Block Read | 2 | **Note 1** |
| | $V_{BUS}$ measurement for Channel 4 | Block Read | 2 | **Note 1** |
| VSENSEN (0BH-0EH) Register | $V_{SENSE}$ measurement for Channel 1 | Block Read | 2 | **Note 1** |
| | $V_{SENSE}$ measurement for Channel 2 | Block Read | 2 | **Note 1** |
| | $V_{SENSE}$ measurement for Channel 3 | Block Read | 2 | **Note 1** |
| | $V_{SENSE}$ measurement for Channel 4 | Block Read | 2 | **Note 1** |
| VBUSN_AVG (0FH-12H) Register | Rolling average of the eight most recent $V_{BUS1}$ measurements | Block Read | 2 | **Note 1** |
| | Rolling average of the eight most recent $V_{BUS2}$ measurements | Block Read | 2 | **Note 1** |
| | Rolling average of the eight most recent $V_{BUS3}$ measurements | Block Read | 2 | **Note 1** |
| | Rolling average of the eight most recent $V_{BUS4}$ measurements | Block Read | 2 | **Note 1** |

**Note 1:** All the results registers, 03H-1Ah, have a POR value that is all zeros: 2 bytes → 0000h; 3 bytes → 000000h; 4 bytes → 00000000h; 7 bytes → 00000000000000h.

**2:** Register 01h has different default values for different devices, see Register 7-2.

**3:** Register FDh has different values depending on which member of the product family is selected. See Register 7-37.

**TABLE 7-1: REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)**

| Register Name | Description | Type | Bytes | POR Value |
|---|---|---|---|---|
| VSENSEN_AVG (13H-16H) Register | Rolling average of the eight most recent $V_{SENSE1}$ measurements | Block Read | 2 | **Note 1** |
| | Rolling average of the eight most recent $V_{SENSE2}$ measurements | Block Read | 2 | **Note 1** |
| | Rolling average of the eight most recent $V_{SENSE3}$ measurements | Block Read | 2 | **Note 1** |
| | Rolling average of the eight most recent $V_{SENSE4}$ measurements | Block Read | 2 | **Note 1** |
| VPOWERN (17H-1AH) Register | $V_{SENSE}$ x $V_{BUS}$ for Channel 1 | Block Read | 4 | **Note 1** |
| | $V_{SENSE}$ x $V_{BUS}$ for Channel 2 | Block Read | 4 | **Note 1** |
| | $V_{SENSE}$ x $V_{BUS}$ for Channel 3 | Block Read | 4 | **Note 1** |
| | $V_{SENSE}$ x $V_{BUS}$ for Channel 4 | Block Read | 4 | **Note 1** |
| SMBUS SETTINGS (1CH) Register | Activate SMBus functionality, I/O data for R/W on I/O pins | R/W | 1 | 10h |
| NEG_PWR_FSR (1DH) Register | Configuration control for bidirectional current | R/W | 2 | 0000h |
| REFRESH_G (1EH) Register | REFRESH response to General Call Address | SEND | 0 | N/A |
| REFRESH_V (1FH) Register | Refreshes $V_{BUS\ and}$ $V_{SENSE}$ data only, no accumulator reset | SEND | 0 | N/A |
| SLOW (20H) Register | Status and control for SLOW pin functions | R/W | 1 | 00h |
| CTRL_ACT (21H) Register | Currently active value of 01h | R | 2 | 0700h |
| NEG_PWR_FSR_ACT (22H) Register | Currently active value of NEG_PWR | R | 2 | 0000h |
| CTRL_LAT (23H) Register | Latched active value of 01h | R | 2 | 0700h |
| NEG_PWR_FSR _LAT (24H) Register | Latched active value of NEG_PWR | R | 2 | 0000h |
| ACCUM CONFIG (25H) Register | Enable $V_{SENSE}$ and $V_{BUS}$ accumulation | R/W | 1 | 00h |
| ALERT STATUS (26H) Register | Reads to see what triggered the ALERT | RC | 3 | 000000h |
| SLOW_ALERT1 (27H) Register | Assigns specific ALERT to ALERTn/SLOW | RW | 3 | 000000h |
| GPIO_ALERT2 (28H) Register | Assigns specific ALERT to $\overline{\text{ALERT}}$n/I/O | R/W | 3 | 000000h |
| ACC FULLNESS LIMITS (29H) Register | ACC and ACC Count Fullness limits | R/W | 2 | 5540h |
| OC LIMITN (30H-33H) Register | OC limit for Channel 1 | R/W | 2 | 0000h |
| | OC limit for Channel 2 | R/W | 2 | 0000h |
| | OC limit for Channel 3 | R/W | 2 | 0000h |
| | OC limit for Channel 4 | R/W | 2 | 0000h |

**Note 1:** All the results registers, 03H-1Ah, have a POR value that is all zeros: 2 bytes → 0000h; 3 bytes → 000000h; 4 bytes → 00000000h; 7 bytes → 00000000000000h.

**2:** Register 01h has different default values for different devices, see Register 7-2.

**3:** Register FDh has different values depending on which member of the product family is selected. See Register 7-37.


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**TABLE 7-1: REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)**

| Register Name | Description | Type | Bytes | POR Value |
|---|---|---|---|---|
| UC LIMITN (34H-37H) Register | UC limit for Channel 1 | R/W | 2 | 0000h |
| | UC limit for Channel 2 | R/W | 2 | 0000h |
| | UC limit for Channel 3 | R/W | 2 | 0000h |
| | UC limit for Channel 4 | R/W | 2 | 0000h |
| OP LIMITN (38H-3BH) Register | OP limit for Channel 1 | R/W | 3 | 000000h |
| | OP limit for Channel 2 | R/W | 3 | 000000h |
| | OP limit for Channel 3 | R/W | 3 | 000000h |
| | OP limit for Channel 4 | R/W | 3 | 000000h |
| OV LIMITN (3CH-3FH) Register | OV limit for Channel 1 | R/W | 2 | 0000h |
| | OV limit for Channel 2 | R/W | 2 | 0000h |
| | OV limit for Channel 3 | R/W | 2 | 0000h |
| | OV limit for Channel 4 | R/W | 2 | 0000h |
| UV LIMITN (40H-43H) Register | UV limit for Channel 1 | R/W | 2 | 0000h |
| | UV limit for Channel 2 | R/W | 2 | 0000h |
| | UV limit for Channel 3 | R/W | 2 | 0000h |
| | UV limit for Channel 4 | R/W | 2 | 0000h |
| OC LIMIT NSAMPLES (44H) Register | Consecutive OC samples over threshold for ALERT | R/W | 1 | 00h |
| UC LIMIT NSAMPLES (45H) Register | Consecutive UC samples over threshold for ALERT | R/W | 1 | 00h |
| OP LIMIT NSAMPLES (46H) Register | Consecutive OP samples over threshold for ALERT | R/W | 1 | 00h |
| OV LIMIT NSAMPLES (47H) Register | Consecutive OV samples over threshold for ALERT | R/W | 1 | 00h |
| UV LIMIT NSAMPLES (48H) Register | Consecutive UV samples over threshold for ALERT | R/W | 1 | 00h |
| ALERT ENABLE (49H) Register | ALERT Enable | R/W | 3 | 000000h |
| ACCUM CONFIG ACT (4AH) Register | Currently active value of 25h | R | 1 | 00h |
| ACCUM CONFIG LAT (4BH) Register | Latched active value of 25h | R | 1 | 00h |
| PRODUCT ID (FDH) Register | Stores the Product ID | R | 1 | **Note 3** |
| MANUFACTURER ID (FEH) Register | Stores the Manufacturer ID | R | 1 | 54h |
| REVISION ID (FFH) Register | Stores the revision | R | 1 | 02h |

**Note 1:** All the results registers, 03H-1Ah, have a POR value that is all zeros: 2 bytes → 0000h; 3 bytes → 000000h; 4 bytes → 00000000h; 7 bytes → 00000000000000h.

**2:** Register 01h has different default values for different devices, see Register 7-2.

**3:** Register FDh has different values depending on which member of the product family is selected. See Register 7-37.

## 7.1 Reading Data Bytes

Data represented by the data registers are ensured to be synchronized and stable for 1 ms after any of the REFRESH commands are sent. Immediately after the REFRESH commands are sent, the data bytes change dynamically until 1 ms elapses.

When new data are written to a control register and the host reads it back, the new data are read back even if no REFRESH command is sent to cause the new data to take effect.

| **Note:** | The letter N or n is used to represent 1, 2, 3, 4 in the register and bit names below, in sections that describe registers that are grouped for all four channels. |
|---|---|

**REGISTER 7-1: REFRESH (ADDRESS 00H) REGISTER**

| SEND | |
|---|---|
| No Data in this command, Send Byte only | |
| bit 7 | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-0 This command is a Send byte, it does not contain any data. When it is sent to the device, the REFRESH command is executed. The accumulator data, accumulator count, $V_{BUS}$ and $V_{SENSE}$ measurements are all refreshed and the accumulators are reset. The host can read the accumulator data and accumulator count 1 ms after the REFRESH command is sent and anytime after, up until the next REFRESH command is sent. The host can read $V_{BUS}$ and $V_{SENSE}$ data in the same time period. The accumulator results, accumulator count, $V_{BUS}$ and $V_{SENSE}$ data can be refreshed with the REFRESH_V command without resetting the accumulators. See **Section 5.2, "REFRESH Command"**.


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**REGISTER 7-2: CTRL (ADDRESS 01H) REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| SAMPLE_MODE[3:0] | | | | GPIO_ALERT2[1:0] | | SLOW_ALERT1[1:0] | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| CHANNEL_N_OFF[3:0] | | | | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **SAMPLE_MODE[3:0]**: These bits select one of the sampling modes listed below. These modes are exclusive – that is, only one mode can be set at any given time. One of the sampling modes is Sleep, when no sampling occurs.

0b0000 = 1024 SPS adaptive accumulation (default), see **Section 5.13.1, "Adaptive Accumulator"**
0b0001 = 256 SPS adaptive accumulation
0b0010 = 64 SPS adaptive accumulation
0b0011 = 8 SPS adaptive accumulation
0b0100 = 1024 SPS, see **Section 5.15, "Conversion Cycle Controls"**
0b0101 = 256 SPS
0b0110 = 64 SPS
0b0111 = 8 SPS
0b1000 = Single-Shot mode, see **Section 5.15.4, "Single-Shot Mode"**
0b1001 = Single-Shot 8X
0b1010 = Fast mode, see **Section 5.15.3, "Fast Mode"**
0b1011 = Burst mode, see **Section 5.15.2, "Burst Mode"**
0b1100 = Reserved
0b1101 = Reserved
0b1110 = Reserved
0b1111 = Sleep, see **Section 5.5, "Sleep State"**

bit 11-10 **GPIO_ALERT2[1:0]**: Select the signals for the GPIO/$\overline{\text{ALERT2}}$ pin. If the pin is configured as a GPIO pin, the R/W data for the pin are stored in Register 7-10.

00 = ALERT functions as an $\overline{\text{ALERT}}$ pin
01 = GPIO digital input. Read the digital value input to this pin from Register 7-10. Default for this pin.
10 = GPIO digital output. Write the digital value to be output from this pin to Register 7-10.
11 = The pin functions as the SLOW pin, taking the pin high overrides the programmed sample rate and yields a sampling rate of 8 SPS. Only one pin can be selected to set the SLOW functionality. If both GPIO/$\overline{\text{ALERT2}}$ and SLOW/$\overline{\text{ALERT1}}$ pins are set to SLOW, the SLOW/$\overline{\text{ALERT1}}$ pin will control the SLOW functionality.

bit 9-8 **SLOW_ALERT1[1:0]**: Select the signals for SLOW/$\overline{\text{ALERT1}}$ pin. If the pin is configured as a GPIO pin, the R/W data for the pin are stored in Register 7-10.

00 = ALERT functions as an $\overline{\text{ALERT1}}$ pin
01 = GPIO digital input. Read the digital value input to this pin from Register 7-10.
10 = GPIO digital output. Write the digital value to be output from this pin to Register 7-10.
11 = SLOW functions as the SLOW pin, taking the pin high overrides the programmed sample rate and yields a sampling rate of 8 SPS (default for this pin).

**REGISTER 7-2: CTRL (ADDRESS 01H) REGISTER (CONTINUED)**

bit 7-4 **CHANNEL_N_OFF[3:0]**:

Allow one or more channels to be disabled (bit value = 1) during the conversion cycle. A bit value = 0 means the channel is active. These settings apply for normal continuous round robin conversion cycles or Single-Shot mode, if Single-Shot mode is selected. If a channel is set to inactive, the auto-incrementing address pointer will skip addresses associated with that channel unless the No Skip bit 1 in Register 7-10 is set.

Channel 1: bit 3

Channel 2: bit 2

Channel 3: bit 1

Channel 4: bit 0

Example: Channel 2 disabled, Channel 1, 3 and 4 enabled. CHANNEL_N_OFF = 0b0100.

In PAC194X devices, deactivating channels allows faster sampling. Burst or Fast modes are selected using bits [15:12] in this register.

PAC1944-1 default = 0b0000 (register default 0700h) (shown above)

PAC1943-1 default = 0b0001 (register value 0710h)

PAC1942-1 default = 0b0011 (register value 0730h)

PAC1942-2 default = 0b0011 (register value 0730h)

PAC1941-1 default = 0b0111 (register value 0770h)

PAC1941-2 default = 0b0111 (register value 0770h)

bit 3-0 Unimplemented, read as '0'.

**REGISTER 7-3: ACC_COUNT (02H) REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ACC_COUNT[31:24] | | | | | | | |
| bit 31 | | | | | | | bit 24 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ACC_COUNT[23:16] | | | | | | | |
| bit 23 | | | | | | | bit 16 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ACC_COUNT[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ACC_COUNT[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **ACC_COUNT[31:0]**: This register contains the count for each time a power result is summed in the accumulator.


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**REGISTER 7-4: VACCN (03H-06H) REGISTER**

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| VACCn[55:48] | | | | | | | |
| bit 55 | | | | | | | bit 48 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| VACCn[47:40] | | | | | | | |
| bit 47 | | | | | | | bit 40 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| VACCn[39:32] | | | | | | | |
| bit 39 | | | | | | | bit 32 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| VACCn[31:24] | | | | | | | |
| bit 31 | | | | | | | bit 24 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| VACCn[23:16] | | | | | | | |
| bit 23 | | | | | | | bit 16 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| VACCn[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| VACCn[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 55-0 **VACCn[55:0]**: This register contains the accumulated sum of $V_{POWER}$ samples, where n = 1 to 4, depending on the device by default. It can also hold the accumulated values of $V_{SENSE}$ and $V_{BUS}$ if bits are set in Register 7-19. These are 56-bit unsigned numbers, unless either $V_{BUS}$ or $V_{SENSE}$ is configured to have a bipolar range. In that case, they will be 55 bits + sign (two’s complement) numbers. Power is always calculated using signed numbers for $V_{BUS}$ and $V_{SENSE}$, but if both $V_{BUS}$ and $V_{SENSE}$ are in the default Unipolar mode, power is reported as an unsigned number. This can lead to very small discrepancies between a manual comparison of the product of $V_{BUS}$ and $V_{SENSE}$ and the results that the chip calculates and accumulates for $V_{POWER}$. The digital math in the chip uses more bits than the reported results for $V_{BUS}$ and $V_{SENSE}$, so the results registers for $V_{POWER}$ and the accumulated power will in some cases have a more accurate number than calculations using the results registers for $V_{SENSE}$ and $V_{POWER}$ will provide.

**REGISTER 7-5: VBUSN (07H-0AH) REGISTER**

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| VBUSn[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| VBUSn[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **VBUSn[15:0]**: This register contains the most recent digitized value of a $V_{BUS}$ sample, where n = 1 to 4, depending on the device. These are 16-bit unsigned numbers, unless $V_{BUS}$ is configured to have a bipolar range. In that case, they will be 15 bits + sign (two's complement) numbers.

**REGISTER 7-6: VSENSEN (0BH-0EH) REGISTER**

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| VSENSEn[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| VSENSEn[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **VSENSEn[15:0]**: This register contains the most recent digitized value of $V_{SENSE}$ samples, where n = 1 to 4, depending on the device. These are 16-bit unsigned numbers, unless $V_{SENSE}$ is configured to have a bipolar range. In that case, they will be 15 bits + sign (two's complement) numbers.


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**REGISTER 7-7: VBUSN_AVG (0FH-12H) REGISTER**

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| VBUSn_AVG[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| VBUSn_AVG[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **VBUSn_AVG[15:0]**: This register contain a rolling average of the eight most recent $V_{BUS}$ measurements. It has the same format as the values in the $V_{BUS}$ registers.

**REGISTER 7-8: VSENSEN_AVG (13H-16H) REGISTER**

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| VSENSEn_AVG[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| VSENSEn_AVG[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **VSENSEn_AVG[15:0]**: This register contains a rolling average of the eight most recent $V_{SENSE}$ results. It has the same format as the values in the $V_{SENSE}$ registers.

**REGISTER 7-9: VPOWERN (17H-1AH) REGISTER**

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| VPOWERn[29:22] | | | | | | | |
| bit 31 | | | | | | | bit 24 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| VPOWERn[21:14] | | | | | | | |
| bit 23 | | | | | | | bit 16 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| VPOWERn[13:6] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| VPOWERn[5:0] | | | | | | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-2 **VPOWERn[29-0]**: This register contains the product of $V_{BUS}$ (14 MSBs) and $V_{SENSE}$, which represents the proportional power for each channel. These are 30-bit unsigned numbers unless either $V_{BUS}$ or $V_{SENSE}$ is configured to have a bipolar range. In that case, they will be 29 bits + sign (two's complement) numbers. These are the numbers that are accumulated in the accumulators. Power is always calculated using signed numbers for $V_{BUS}$ and $V_{SENSE}$, but if both $V_{BUS}$ and $V_{SENSE}$ are in the default Unipolar mode, power is reported as an unsigned number. This can lead to very small discrepancies between a manual comparison of the product of $V_{BUS}$ and $V_{SENSE}$ and the results that the chip calculates for $V_{POWER}$. The digital math in the chip uses more bits than the reported results for $V_{BUS}$ and $V_{SENSE}$, so the results registers for $V_{POWER}$ and the accumulated power will in some cases have a more accurate number than calculations using the results registers for $V_{SENSE}$ and $V_{POWER}$ will provide.

bit 1-0 Unimplemented, read as '0'.


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**REGISTER 7-10: SMBUS SETTINGS (1CH) REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| GPIO_ DATA2 | GPIO_ DATA1 | ANY_ALERT | POR | TIMEOUT | BYTE COUNT | NO SKIP | I2C_ HISPEED |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

Bits in this register may be written or read at any time and are active immediately. Refresh is not required to activate them or update them.

bit 7 **GPIO_DATA2**: R/W data for the pin GPIO/$\overline{\text{ALERT2}}$ if the pin is configured as a GPIO pin. See Register 7-2 to configure GPIO/$\overline{\text{ALERT2}}$ as a GPIO pin.

0 = Pull the GPIO pin low when configured to be an output (default)

1 = GPIO pin pulled to external $V_{IO}$ via an external resistor when configured to be an output

bit 6 **GPIO_DATA1**: R/W data for the pin SLOW/$\overline{\text{ALERT1}}$ if the pin is configured as a GPIO pin. See Register 7-2 to configure SLOW/$\overline{\text{ALERT1}}$ as a GPIO pin.

0 = Pull the GPIO pin low when configured to be an output (default)

1 = GPIO pin pulled to external $V_{IO}$ via an external resistor when configured to be an output

bit 5 **ANY_ALERT**: This bit is set by any of the active ALERT functions being triggered, except ALERT_CC. This bit is cleared when the ALERT function that set the bit is cleared. See **Section 5.16.2, "ALERT Pin Assignments"**.

0 = No ALERT condition has occurred (default)

1 = An ALERT condition has occurred, read Register 7-20 for cause

bit 4 **POR**: The POR bit is for the purpose of enabling the system designer to learn if the chip is reset after it is programed. The user can clear this bit after POR and then monitor it to detect if the device was powered cycled or somehow reset since the POR. If the reset is detected in this manner, any non-default programming can be reprogrammed. This bit is only reset by the internal POR, which can occur from power cycling or the $\overline{\text{PWRDN}}$ pin going low.

0 = This bit has been cleared over $I^2C$ since the last POR occurred

1 = Default. This bit has the POR default value of '1' and has not been cleared since the last reset occurred

bit 3 **TIMEOUT** enable bit. The SMBus time-out is disabled by default and is enabled by setting this bit.

0 = No SMBus time-out feature (default)

1 = SMBus time-out feature is available

bit 2 **BYTE COUNT**: This bit causes Byte Count data to be included in the response to the SMBus Block Read command for each register read. This functionality is disabled by default and Block Read corresponds to the $I^2C$ protocol.

0 = No Byte Count in response to a Block Read command (default)

1 = Data in response to a Block Read command include the Byte Count data

bit 1 **NO SKIP**: This bit controls the auto-incrementing of the address pointer for channels that are inactive.

0 = The auto-incrementing pointer will skip over addresses used by/for channels that are inactive (default)

1 = The auto-incrementing pointer will not skip over addresses used by/for channels that are inactive. When these channels are disabled, if a read is performed, it will read FF.

bit 0 **I2C_HISPEED:** Setting this bit enables the 3.4 MHz $I^2C$ operation by changing the pulse-width parameters of the Pulse Gobbler. Default = 0.

**REGISTER 7-11: NEG_PWR_FSR (1DH) REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CFG_VS1[1:0] | | CFG_VS2[1:0] | | CFG_VS3[1:0] | | CFG_VS4[1:0] | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CFG_VB1[1:0] | | CFG_VB2[1:0] | | CFG_VB3[1:0] | | CFG_VB4[1:0] | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **CFG_VS1[1:0]**: Configure Channel 1 FSR for $V_{SENSE}$ measurements
00 = Channel 1 $V_{SENSE}$ has unipolar +100 mV to 0V FSR (default)
01 = Channel 1 $V_{SENSE}$ has bipolar +100 mV to -100 mV FSR
10 = Channel 1 $V_{SENSE}$ has bipolar +50 mV to -50 mV FSR
11 = Reserved

bit 13-12 **CFG_VS2[1:0]**: Configure Channel 2 FSR for $V_{SENSE}$ measurements
00 = Channel 2 $V_{SENSE}$ has unipolar +100 mV to 0V FSR (default)
01 = Channel 2 $V_{SENSE}$ has bipolar +100 mV to -100 mV FSR
10 = Channel 2 $V_{SENSE}$ has bipolar +50 mV to -50 mV FSR
11 = Reserved

bit 11-10 **CFG_VS3[1:0]**: Configure Channel 3 FSR for $V_{SENSE}$ measurements
00 = Channel 3 $V_{SENSE}$ has unipolar +100 mV to 0V FSR (default)
01 = Channel 3 $V_{SENSE}$ has bipolar +100 mV to -100 mV FSR
10 = Channel 3 $V_{SENSE}$ has bipolar +50 mV to -50 mV FSR
11 = Reserved

bit 9-8 **CFG_VS4[1:0]**: Configure Channel 4 FSR for $V_{SENSE}$ measurements
00 = Channel 4 $V_{SENSE}$ has unipolar +100 mV to 0V FSR (default)
01 = Channel 4 $V_{SENSE}$ has bipolar +100 mV to -100 mV FSR
10 = Channel 4 $V_{SENSE}$ has bipolar +50 mV to -50 mV FSR
11 = Reserved

bit 7-6 **CFG_VB1[1:0]**: Configure Channel 1 FSR for $V_{BUS}$ measurements
00 = Channel 1 $V_{BUS}$ has unipolar +9V to 0V FSR (default)
01 = Channel 1 $V_{BUS}$ has bipolar +9V to -9V FSR
10 = Channel 1 $V_{BUS}$ has bipolar +4.5V to -4.5V FSR
11 = Reserved

bit 5-4 **CFG_VB2[1:0]**: Configure Channel 2 FSR for $V_{BUS}$ measurements
00 = Channel 2 $V_{BUS}$ has unipolar +9V to 0V FSR (default)
01 = Channel 2 $V_{BUS}$ has bipolar +9V to -9V FSR
10 = Channel 2 $V_{BUS}$ has bipolar +4.5V to -4.5V FSR
11 = Reserved

bit 3-2 **CFG_VB3[1:0]**: Configure Channel 3 FSR for $V_{BUS}$ measurements
00 = Channel 3 $V_{BUS}$ has unipolar +9V to 0V FSR (default)
01 = Channel 3 $V_{BUS}$ has bipolar +9V to -9V FSR
10 = Channel 3 $V_{BUS}$ has bipolar +4.5V to -4.5V FSR
11 = Reserved

bit 1-0 **CFG_VB4[1:0]**: Configure Channel 4 FSR for $V_{BUS}$ measurements
00 = Channel 4 $V_{BUS}$ has unipolar +9V to 0V FSR (default)
01 = Channel 4 $V_{BUS}$ has bipolar +9V to -9V FSR
10 = Channel 4 $V_{BUS}$ has bipolar +4.5V to -4.5V FSR
11 = Reserved


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**REGISTER 7-12: REFRESH_G (1EH) REGISTER**

| SEND | |
|---|---|
| No Data in this command, Send Byte only | |
| bit 7 | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-0 This command is a Send Byte, it does not contain any data. It is exactly like the REFRESH command, but it is intended for use with the General Call command. When it is sent to the device, the REFRESH_G command is executed and the readable accumulator data, readable accumulator count, $V_{BUS}$ and $V_{SENSE}$ measurements are all refreshed and the internal accumulator values or accumulator count are reset, exactly like the REFRESH command. The host can read the updated data 1 ms after the REFRESH_G command is sent and anytime after, up until the next REFRESH, REFRESH_G or REFRESH_V command is sent.

**REGISTER 7-13: REFRESH_V (1FH) REGISTER**

| SEND | |
|---|---|
| No Data in this command, Send Byte only | |
| bit 7 | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-0 This command is a Send Byte, it does not contain any data. When it is sent to the device, the REFRESH_V command is executed. It is similar to the REFRESH command except the accumulators and accumulator count are not reset. The readable accumulator data, readable accumulator count, $V_{BUS}$ and $V_{SENSE}$ measurements are all refreshed without affecting the internal accumulators values or accumulator count. The host can read the updated data 1 ms after the REFRESH_V command is sent and anytime after, up until the next REFRESH, REFRESH_G or REFRESH_V command is sent.

**REGISTER 7-14: SLOW (20H) REGISTER**

| R-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| SLOW | SLOW_LH | SLOW_HL | R_RISE | R_V_RISE | R_FALL | R_V_FALL | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

This register tracks the state of the SLOW pin, tracks transitions on the SLOW pin and controls the type of limited REFRESH command (if any) that will occur on a SLOW pin transition. This allows software to monitor the state of the SLOW pin and its transitions over the $I^2C$ even though the SLOW pin is asynchronous to the $I^2C$ pins and may have a different controller. As such, no REFRESH or REFRESH_V command is required to activate new written values or to update readable values. On a transition of the SLOW pin, a limited REFRESH function may be executed if bits 1-4 are set. These limited REFRESH and REFRESH_V functions update all of the readable results registers. The limited REFRESH does not update the CTRL_LAT, NEG_PWR_FSR_LAT or the ACCUM_CONFIG_LAT registers. For the limited REFRESH function only, it also resets the accumulators and accumulator count. These are called limited REFRESH and limited REFRESH_V functions because there is no activation of any pending changes to the control registers. If limited REFRESH and limited REFRESH_V are both enabled for a certain SLOW pin transition, REFRESH will be executed (REFRESH wins over REFRESH_V).

bit 7 **SLOW**:
0 = SLOW pin, the current status is not active
1 = SLOW pin, the current status is active

bit 6 **SLOW_LH**:
0 = The SLOW pin has not transitioned low to high since the last REFRESH command
1 = The SLOW pin has transitioned low to high since the last REFRESH command
The bit is reset to '0' by a REFRESH or REFRESH_G command.

bit 5 **SLOW_HL**:
0 = The SLOW pin has not transitioned high to low since the last REFRESH command
1 = The SLOW pin has transitioned high to low since the last REFRESH command
The bit is reset to '0' by a REFRESH or REFRESH_G command.

bit 4 **R_RISE**:
0 = Disables limited REFRESH function to take place on the rising edge of the SLOW pin
1 = Enables limited REFRESH function to take place on the rising edge of the SLOW pin
The bit is not reset automatically, it must be written to be changed.

bit 3 **R_V_RISE**:
0 = Disables limited REFRESH_V function to take place on the rising edge of the SLOW pin
1 = Enables limited REFRESH_V function to take place on the rising edge of the SLOW pin
The bit is not reset automatically, it must be written to be changed.

bit 2 **R_FALL**:
0 = Disables limited REFRESH function to take place on the falling edge of the SLOW pin
1 = Enables limited REFRESH function to take place on the falling edge of the SLOW pin
The bit is not reset automatically, it must be written to be changed.

bit 1 **R_V_FALL**:
0 = Disables limited REFRESH_V function to take place on the falling edge of the SLOW pin
1 = Enables limited REFRESH_V function to take place on the falling edge of the SLOW pin
The bit is not reset automatically, it must be written to be changed.

bit 0 Unimplemented, read as '0'.


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**REGISTER 7-15: CTRL_ACT (21H) REGISTER**

| R-0 | R-0 | R-0 | R-0 | R-0 | R-1 | R-1 | R-1 |
|---|---|---|---|---|---|---|---|
| SAMPLE_MODE[3:0] | | | | GPIO_ALERT2[1:0] | | SLOW_ALERT1[1:0] | |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| CHANNEL_N_OFF[3:0] | | | | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

This register contains an image of Register 7-2 and reflects the current active value of these settings, whereas the values in register 01h may be programmed but not activated by one of the REFRESH commands. This register allows software to determine the actual active settings. This register is valid when the results registers are valid, 1 ms after a REFRESH/_V/_G command, in most cases. However, if you program a conversion rate change followed by REFRESH, the new conversion rate will not become effective until the current conversion cycle is complete. This can cause a delay in some cases before the conversion cycle (and the CTRL_ACT register) is updated. This delay can be variable, depending on where you are in the conversion cycle when the REFRESH command is sent.

bit 15-12 **SAMPLE_MODE[3:0]**: These bits select one of the sampling modes listed below. These modes are exclusive – that is, only one mode can be set at any given time. One of the sampling modes is Sleep, when no sampling occurs.

0b0000 = 1024 SPS adaptive accumulation (default), see **Section 5.13.1, "Adaptive Accumulator"**
0b0001 = 256 SPS adaptive accumulation
0b0010 = 64 SPS adaptive accumulation
0b0011 = 8 SPS adaptive accumulation
0b0100 = 1024 SPS, see **Section 5.15, "Conversion Cycle Controls"**
0b0101 = 256 SPS
0b0110 = 64 SPS
0b0111 = 8 SPS
0b1000 = Single-Shot mode, see **Section 5.15.4, "Single-Shot Mode"**
0b1001 = Single-Shot 8X
0b1010 = Fast mode, see **Section 5.15.3, "Fast Mode"**
0b1011 = Burst mode, see **Section 5.15.2, "Burst Mode"**
0b1100 = Reserved
0b1101 = Reserved
0b1110 = Reserved
0b1111 = Sleep, see **Section 5.5, "Sleep State"**

bit 11-10 **GPIO_ALERT2[1:0]**: Select the signals for the GPIO/$\overline{\text{ALERT2}}$ pin. If the pin is configured as a GPIO pin, the R/W data for the pin are stored in Register 7-10.

00 = ALERT functions as an $\overline{\text{ALERT}}$ pin
01 = GPIO digital input. Read the digital value input to this pin from Register 7-10. Default for this pin.
10 = GPIO digital output. Write the digital value to be output from this pin to Register 7-10.
11 = The pin functions as the SLOW pin, taking the pin high overrides the programmed sample rate and yields a sampling rate of 8 SPS.

### REGISTER 7-15: CTRL_ACT (21H) REGISTER (CONTINUED)

bit 9-8 **SLOW_ALERT1[1:0]**: Select the signals for SLOW/$\overline{\text{ALERT1}}$ pin. If the pin is configured as a GPIO pin, the R/W data for the pin are stored in Register 7-10.
00 = ALERT functions as an $\overline{\text{ALERT1}}$ pin
01 = GPIO digital input. Read the digital value input to this pin from Register 7-10.
10 = GPIO digital output. Write the digital value to be output from this pin to Register 7-10.
11 = SLOW functions as the SLOW pin, taking the pin high overrides the programmed sample rate and yields a sampling rate of 8 SPS (default for this pin).

bit 7-4 **CHANNEL_N_OFF[3:0]**:
Allow one or more channels to be inactive during the conversion cycle. These settings apply for normal continuous round robin conversion cycles or Single-Shot mode, if Single-Shot mode is selected. If a channel is set to inactive, the auto-incrementing address pointer will skip addresses associated with that channel unless the pointer skipping bit 1 in this register is set.
In PAC194X devices, deactivating channels allows faster sampling. Burst or Fast modes are selected using bits [15:12] in this register.
PAC1944-1 default = 0b0000 (register default 0700h) (shown above)
PAC1943-1 default = 0b0001 (register value 0710h)
PAC1942-1 default = 0b0011 (register value 0730h)
PAC1942-2 default = 0b0011 (register value 0730h)
PAC1941-1 default = 0b0111 (register value 0770h)
PAC1941-2 default = 0b0111 (register value 0770h)

bit 3-0 Unimplemented, read as '0'.

### REGISTER 7-16: NEG_PWR_FSR_ACT (22H) REGISTER

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CFG_VS1[1:0] | | CFG_VS2[1:0] | | CFG_VS3[1:0] | | CFG_VS4[1:0] | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CFG_VB1[1:0] | | CFG_VB2[1:0] | | CFG_VB3[1:0] | | CFG_VB4[1:0] | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

This register contains an image of Register 7-11. The bits in this register reflect the current active value of these settings, whereas the values in register 1Dh may be programmed but not activated by one of the REFRESH commands. This register allows software to determine the actual active setting. This register is valid when the results registers are valid, 1 ms after a REFRESH/_V/_G command.

bit 15-14 **CFG_VS1[1:0]**: Configure Channel 1 FSR for $V_{SENSE}$ measurements
00 = Channel 1 $V_{SENSE}$ has unipolar +100 mV to 0V FSR (default)
01 = Channel 1 $V_{SENSE}$ has bipolar +100 mV to -100 mV FSR
10 = Channel 1 $V_{SENSE}$ has bipolar +50 mV to -50 mV FSR
11 = Reserved


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**REGISTER 7-16: NEG_PWR_FSR_ACT (22H) REGISTER (CONTINUED)**

bit 13-12 **CFG_VS2[1:0]**: Configure Channel 2 FSR for $V_{SENSE}$ measurements
00 = Channel 2 $V_{SENSE}$ has unipolar +100 mV to 0V FSR (default)
01 = Channel 2 $V_{SENSE}$ has bipolar +100 mV to -100 mV FSR
10 = Channel 2 $V_{SENSE}$ has bipolar +50 mV to -50 mV FSR
11 = Reserved

bit 11-10 **CFG_VS3[1:0]**: Configure Channel 3 FSR for $V_{SENSE}$ measurements
00 = Channel 3 $V_{SENSE}$ has unipolar +100 mV to 0V FSR (default)
01 = Channel 3 $V_{SENSE}$ has bipolar +100 mV to -100 mV FSR
10 = Channel 3 $V_{SENSE}$ has bipolar +50 mV to -50 mV FSR
11 = Reserved

bit 9-8 **CFG_VS4[1:0]**: Configure Channel 4 FSR for $V_{SENSE}$ measurements
00 = Channel 4 $V_{SENSE}$ has unipolar +100 mV to 0V FSR (default)
01 = Channel 4 $V_{SENSE}$ has bipolar +100 mV to -100 mV FSR
10 = Channel 4 $V_{SENSE}$ has bipolar +50 mV to -50 mV FSR
11 = Reserved

bit 7-6 **CFG_VB1[1:0]**: Configure Channel 1 FSR for $V_{BUS}$ measurements
00 = Channel 1 $V_{BUS}$ has unipolar +9V to 0V FSR (default)
01 = Channel 1 $V_{BUS}$ has bipolar +9V to -9V FSR
10 = Channel 1 $V_{BUS}$ has bipolar +4.5V to -4.5V FSR
11 = Reserved

bit 5-4 **CFG_VB2[1:0]**: Configure Channel 2 FSR for $V_{BUS}$ measurements
00 = Channel 2 $V_{BUS}$ has unipolar +9V to 0V FSR (default)
01 = Channel 2 $V_{BUS}$ has bipolar +9V to -9V FSR
10 = Channel 2 $V_{BUS}$ has bipolar +4.5V to -4.5V FSR
11 = Reserved

bit 3-2 **CFG_VB3[1:0]**: Configure Channel 3 FSR for $V_{BUS}$ measurements
00 = Channel 3 $V_{BUS}$ has unipolar +9V to 0V FSR (default)
01 = Channel 3 $V_{BUS}$ has bipolar +9V to -9V FSR
10 = Channel 3 $V_{BUS}$ has bipolar +4.5V to -4.5V FSR
11 = Reserved

bit 1-0 **CFG_VB4[1:0]**: Configure Channel 4 FSR for $V_{BUS}$ measurements
00 = Channel 4 $V_{BUS}$ has unipolar +9V to 0V FSR (default)
01 = Channel 4 $V_{BUS}$ has bipolar +9V to -9V FSR
10 = Channel 4 $V_{BUS}$ has bipolar +4.5V to -4.5V FSR
11 = Reserved

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**REGISTER 7-17: CTRL_LAT (23H) REGISTER**

| R-0 | R-0 | R-0 | R-0 | R-0 | R-1 | R-1 | R-1 |
|---|---|---|---|---|---|---|---|
| SAMPLE_MODE[3:0] | | | | GPIO_ALERT2[1:0] | | SLOW_ALERT1[1:0] | |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| CHANNEL_N_OFF[3:0] | | | | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

This register contains an image of Register 7-2. The bits in this register reflect the value of these settings, that was active before the most recent REFRESH command (including REFRESH_V and/or REFRESH_G). The values in register 01h may be programmed but not activated by one of the REFRESH commands and the values in 21h are currently active. This register allows software to determine the actual active setting that was active prior to the most recent REFRESH command and therefore corresponds to the dataset that is held in the readable registers. This register is valid when the results registers are valid, 1 ms after a REFRESH/_V/_G command. The CTRL_LAT register is not valid until the first REFRESH is sent after a POR event.

bit 15-12 **SAMPLE_MODE[3:0]**: These bits select one of the sampling modes listed below. These modes are exclusive – that is, only one mode can be set at any given time. One of the sampling modes is Sleep, when no sampling occurs.

0b0000 = 1024 SPS adaptive accumulation (default), see **Section 5.13.1, "Adaptive Accumulator"**
0b0001 = 256 SPS adaptive accumulation
0b0010 = 64 SPS adaptive accumulation
0b0011 = 8 SPS adaptive accumulation
0b0100 = 1024 SPS, see **Section 5.15, "Conversion Cycle Controls"**
0b0101 = 256 SPS
0b0110 = 64 SPS
0b0111 = 8 SPS
0b1000 = Single-Shot mode, see **Section 5.15.4, "Single-Shot Mode"**
0b1001 = Single-Shot 8X
0b1010 = Fast mode, see **Section 5.15.3, "Fast Mode"**
0b1011 = Burst mode, see **Section 5.15.2, "Burst Mode"**
0b1100 = Reserved
0b1101 = Reserved
0b1110 = Reserved
0b1111 = Sleep, see **Section 5.5, "Sleep State"**

bit 11-10 **GPIO_ALERT2[1:0]**: Select the signals for the GPIO/$\overline{\text{ALERT2}}$ pin. If the pin is configured as a GPIO pin, the R/W data for the pin are stored in Register 7-10.

00 = ALERT functions as an $\overline{\text{ALERT}}$ pin
01 = GPIO digital input. Read the digital value input to this pin from Register 7-10. Default for this pin.
10 = GPIO digital output. Write the digital value to be output from this pin to Register 7-10.
11 = The pin functions as the SLOW pin, taking the pin high overrides the programmed sample rate and yields a sampling rate of 8 SPS.

bit 9-8 **SLOW_ALERT1[1:0]**: Select the signals for SLOW/$\overline{\text{ALERT1}}$ pin. If the pin is configured as a GPIO pin, the R/W data for the pin are stored in Register 7-10.

00 = ALERT functions as an $\overline{\text{ALERT1}}$ pin
01 = GPIO digital input. Read the digital value input to this pin from Register 7-10.
10 = GPIO digital output. Write the digital value to be output from this pin to Register 7-10.
11 = SLOW functions as the SLOW pin, taking the pin high overrides the programmed sample rate and yields a sampling rate of 8 SPS (default for this pin).


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**REGISTER 7-17: CTRL_LAT (23H) REGISTER (CONTINUED)**

bit 7-4 **CHANNEL_N_OFF[3:0]**:

Allow one or more channels to be inactive during the conversion cycle. These settings apply for normal continuous round robin conversion cycles or Single-Shot mode, if Single-Shot mode is selected. If a channel is set to inactive, the auto-incrementing address pointer will skip addresses associated with that channel unless the pointer skipping bit 1 in this register is set.

In PAC194X devices, deactivating channels allows faster sampling. Burst or Fast modes are selected using bits [15:12] in this register.

PAC1944-1 default = 0b0000 (register default 0700h) (shown above)

PAC1943-1 default = 0b0001 (register value 0710h)

PAC1942-1 default = 0b0011 (register value 0730h)

PAC1942-2 default = 0b0011 (register value 0730h)

PAC1941-1 default = 0b0111 (register value 0770h)

PAC1941-2 default = 0b0111 (register value 0770h)

bit 3-0 Unimplemented, read as '0'.

**REGISTER 7-18: NEG_PWR_FSR _LAT (24H) REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CFG_VS1[1:0] | | CFG_VS2[1:0] | | CFG_VS3[1:0] | | CFG_VS4[1:0] | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CFG_VB1[1:0] | | CFG_VB2[1:0] | | CFG_VB3[1:0] | | CFG_VB4[1:0] | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

This register holds an image of Register 7-11. The bits in this register reflect the settings that were active before the most recent REFRESH command (including REFRESH_V and/or REFRESH_G). The values in register 1Dh may be programmed but not activated by one of the REFRESH commands. This register shows the settings that were active prior to the most recent REFRESH command and therefore correspond to the dataset that is held in the readable registers. This register is valid when the results registers are valid, 1 ms after a REFRESH/_V/_G command.

bit 15-14 **CFG_VS1[1:0]**: Configure Channel 1 FSR for $V_{SENSE}$ measurements
00 = Channel 1 $V_{SENSE}$ has unipolar +100 mV to 0V FSR (default)
01 = Channel 1 $V_{SENSE}$ has bipolar +100 mV to -100 mV FSR
10 = Channel 1 $V_{SENSE}$ has bipolar +50 mV to -50 mV FSR
11 = Reserved

bit 13-12 **CFG_VS2[1:0]**: Configure Channel 2 FSR for $V_{SENSE}$ measurements
00 = Channel 2 $V_{SENSE}$ has unipolar +100 mV to 0V FSR (default)
01 = Channel 2 $V_{SENSE}$ has bipolar +100 mV to -100 mV FSR
10 = Channel 2 $V_{SENSE}$ has bipolar +50 mV to -50 mV FSR
11 = Reserved

bit 11-10 **CFG_VS3[1:0]**: Configure Channel 3 FSR for $V_{SENSE}$ measurements
00 = Channel 3 $V_{SENSE}$ has unipolar +100 mV to 0V FSR (default)
01 = Channel 3 $V_{SENSE}$ has bipolar +100 mV to -100 mV FSR
10 = Channel 3 $V_{SENSE}$ has bipolar +50 mV to -50 mV FSR
11 = Reserved

**REGISTER 7-18: NEG_PWR_FSR _LAT (24H) REGISTER (CONTINUED)**

bit 9-8 **CFG_VS4[1:0]**: Configure Channel 4 FSR for $V_{SENSE}$ measurements
00 = Channel 4 $V_{SENSE}$ has unipolar +100 mV to 0V FSR (default)
01 = Channel 4 $V_{SENSE}$ has bipolar +100 mV to -100 mV FSR
10 = Channel 4 $V_{SENSE}$ has bipolar +50 mV to -50 mV FSR
11 = Reserved

bit 7-6 **CFG_VB1[1:0]**: Configure Channel 1 FSR for $V_{BUS}$ measurements
00 = Channel 1 $V_{BUS}$ has unipolar +9V to 0V FSR (default)
01 = Channel 1 $V_{BUS}$ has bipolar +9V to -9V FSR
10 = Channel 1 $V_{BUS}$ has bipolar +4.5V to -4.5V FSR
11 = Reserved

bit 5-4 **CFG_VB2[1:0]**: Configure Channel 2 FSR for $V_{BUS}$ measurements
00 = Channel 2 $V_{BUS}$ has unipolar +9V to 0V FSR (default)
01 = Channel 2 $V_{BUS}$ has bipolar +9V to -9V FSR
10 = Channel 2 $V_{BUS}$ has bipolar +4.5V to -4.5V FSR
11 = Reserved

bit 3-2 **CFG_VB3[1:0]**: Configure Channel 3 FSR for $V_{BUS}$ measurements
00 = Channel 3 $V_{BUS}$ has unipolar +9V to 0V FSR (default)
01 = Channel 3 $V_{BUS}$ has bipolar +9V to -9V FSR
10 = Channel 3 $V_{BUS}$ has bipolar +4.5V to -4.5V FSR
11 = Reserved

bit 1-0 **CFG_VB4[1:0]**: Configure Channel 4 FSR for $V_{BUS}$ measurements
00 = Channel 4 $V_{BUS}$ has unipolar +9V to 0V FSR (default)
01 = Channel 4 $V_{BUS}$ has bipolar +9V to -9V FSR
10 = Channel 4 $V_{BUS}$ has bipolar +4.5V to -4.5V FSR
11 = Reserved


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**REGISTER 7-19: ACCUM CONFIG (25H) REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ACC1_CONFIG[1:0] | | ACC2_CONFIG[1:0] | | ACC3_CONFIG[1:0] | | ACC4_CONFIG[1:0] | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

This register is used to configure the Accumulator for one of the alternate modes: $V_{SENSE}$ Accumulation (Coulomb Counting) or $V_{BUS}$ Accumulation ($V_{BUS}$ integration). All bits default to zero, which is the $V_{POWER}$ Accumulation mode for the Accumulator, useful for energy measurements.

bit 7-6 **ACC1_CONFIG[1:0]**: Configure the accumulator for Channel 1 to accumulate $V_{POWER}$ (default), $V_{SENSE}$ or $V_{BUS}$.
00 = Channel 1 Accumulator accumulates $V_{POWER}$
01 = Channel 1 Accumulator accumulates $V_{SENSE}$
10 = Channel 1 Accumulator accumulates $V_{BUS}$
11 = Reserved, read as '0'.

bit 5-4 **ACC2_CONFIG[1:0]**: Configure the accumulator for Channel 2 to accumulate $V_{POWER}$ (default), $V_{SENSE}$ or $V_{BUS}$.
00 = Channel 2 Accumulator accumulates $V_{POWER}$
01 = Channel 2 Accumulator accumulates $V_{SENSE}$
10 = Channel 2 Accumulator accumulates $V_{BUS}$
11 = Reserved, read as '0'.

bit 3-2 **ACC3_CONFIG[1:0]**: Configure the accumulator for Channel 3 to accumulate $V_{POWER}$ (default), $V_{SENSE}$ or $V_{BUS}$.
00 = Channel 3 Accumulator accumulates $V_{POWER}$
01 = Channel 3 Accumulator accumulates $V_{SENSE}$
10 = Channel 3 Accumulator accumulates $V_{BUS}$
11 = Reserved, read as '0'.

bit 1-0 **ACC4_CONFIG[1:0]**: Configure the accumulator for Channel 4 to accumulate $V_{POWER}$ (default), $V_{SENSE}$ or $V_{BUS}$.
00 = Channel 4 Accumulator accumulates $V_{POWER}$
01 = Channel 4 Accumulator accumulates $V_{SENSE}$
10 = Channel 4 Accumulator accumulates $V_{BUS}$
11 = Reserved, read as '0'.

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**REGISTER 7-20: ALERT STATUS (26H) REGISTER**

| RC-0 | RC-0 | RC-0 | RC-0 | RC-0 | RC-0 | RC-0 | RC-0 |
|---|---|---|---|---|---|---|---|
| CH1OC | CH2OC | CH3OC | CH4OC | CH1UC | CH2UC | CH3UC | CH4UC |
| bit 23 | | | | | | | bit 16 |

| RC-0 | RC-0 | RC-0 | RC-0 | RC-0 | RC-0 | RC-0 | RC-0 |
|---|---|---|---|---|---|---|---|
| CH1OV | CH2OV | CH3OV | CH4OV | CH1UV | CH2UV | CH3UV | CH4UV |
| bit 15 | | | | | | | bit 8 |

| RC-0 | RC-0 | RC-0 | RC-0 | RC-0 | RC-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| CH1OP | CH2OP | CH3OP | CH4OP | ACC_OVF | ACC_COUNT | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

Read this register to determine the cause of ALERT being tripped. See **Section 5.16.4, "ALERT Functionality – Voltage, Current and Power"**. This register is cleared when read and another conversion cycle completes. If the condition that set the ALERT is still present when the conversion cycle completes, the bit remains set. The register does not require a REFRESH to update the readable register value. The OC, UC, OP, OV and UV ALERTs are disabled by default. To enable the ones you want, set the appropriate bits in Register 7-34.

bit 23 **CH1OC**:
0 = ALERT for overcurrent on Channel 1 is not tripped
1 = ALERT for overcurrent on Channel 1 is tripped

bit 22 **CH2OC**:
0 = ALERT for overcurrent on Channel 2 is not tripped
1 = ALERT for overcurrent on Channel 2 is tripped

bit 21 **CH3OC**:
0 = ALERT for overcurrent on Channel 3 is not tripped
1 = ALERT for overcurrent on Channel 3 is tripped

bit 20 **CH4OC**:
0 = ALERT for overcurrent on Channel 4 is not tripped
1 = ALERT for overcurrent on Channel 4 is tripped

bit 19 **CH1UC**:
0 = ALERT for undercurrent on Channel 1 is not tripped
1 = ALERT for undercurrent on Channel 1 is tripped

bit 18 **CH2UC**:
0 = ALERT for undercurrent on Channel 2 is not tripped
1 = ALERT for undercurrent on Channel 2 is tripped

bit 17 **CH3UC**:
0 = ALERT for undercurrent on Channel 3 is not tripped
1 = ALERT for undercurrent on Channel 3 is tripped

bit 16 **CH4UC**:
0 = ALERT for undercurrent on Channel 4 is not tripped
1 = ALERT for undercurrent on Channel 4 is tripped

bit 15 **CH1OV**:
0 = ALERT for overvoltage on Channel 1 is not tripped
1 = ALERT for overvoltage on Channel 1 is tripped


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**REGISTER 7-20: ALERT STATUS (26H) REGISTER (CONTINUED)**

bit 14 **CH2OV**:
0 = ALERT for overvoltage on Channel 2 is not tripped
1 = ALERT for overvoltage on Channel 2 is tripped

bit 13 **CH3OV**:
0 = ALERT for overvoltage on Channel 3 is not tripped
1 = ALERT for overvoltage on Channel 3 is tripped

bit 12 **CH4OV**:
0 = ALERT for overvoltage on Channel 4 is not tripped
1 = ALERT for overvoltage on Channel 4 is tripped

bit 11 **CH1UV**:
0 = ALERT for undervoltage on Channel 1 is not tripped
1 = ALERT for undervoltage on Channel 1 is tripped

bit 10 **CH2UV**:
0 = ALERT for undervoltage on Channel 2 is not tripped
1 = ALERT for undervoltage on Channel 2 is tripped

bit 9 **CH3UV**:
0 = ALERT for undervoltage on Channel 3 is not tripped
1 = ALERT for undervoltage on Channel 3 is tripped

bit 8 **CH4UV**:
0 = ALERT for undervoltage on Channel 4 is not tripped
1 = ALERT for undervoltage on Channel 4 is tripped

bit 7 **CH1OP**:
0 = ALERT for overpower on Channel 1 is not tripped
1 = ALERT for overpower on Channel 1 is tripped

bit 6 **CH2OP**:
0 = ALERT for overpower on Channel 2 is not tripped
1 = ALERT for overpower on Channel 2 is tripped

bit 5 **CH3OP**:
0 = ALERT for overpower on Channel 3 is not tripped
1 = ALERT for overpower on Channel 3 is tripped

bit 4 **CH4OP**:
0 = ALERT for overpower on Channel 4 has is not tripped
1 = ALERT for overpower on Channel 4 is tripped

bit 3 **ACC_OVF**: This bit signals when the Accumulator for any channel overflows or exceeds its fullness limit specified in Register 7-23.
0 = No Accumulator full related ALERT for this channel
1 = ALERT triggered by Accumulator fullness limit exceeded

bit 2 **ACC_COUNT**: This bit signals when the Accumulator Count overflows or exceeds its fullness limit specified in Register 7-23.
0 = No Accumulator full related ALERT for this channel
1 = ALERT triggered by Accumulator Count fullness limit exceeded

bit 1-0 Unimplemented, read as '0'.

**REGISTER 7-21: SLOW_ALERT1 (27H) REGISTER**

| RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 |
|---|---|---|---|---|---|---|---|
| CH1OC | CH2OC | CH3OC | CH4OC | CH1UC | CH2UC | CH3UC | CH4UC |
| bit 23 | | | | | | | bit 16 |

| RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 |
|---|---|---|---|---|---|---|---|
| CH1OV | CH2OV | CH3OV | CH4OV | CH1UV | CH2UV | CH3UV | CH4UV |
| bit 15 | | | | | | | bit 8 |

| RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | U-0 |
|---|---|---|---|---|---|---|---|
| CH1OP | CH2OP | CH3OP | CH4OP | ACC_OVF | ACC_COUNT | ALERT_CC1 | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

Write to this register to assign a specific ALERT signal to the SLOW/$\overline{\text{ALERT1}}$ pin. The SLOW/$\overline{\text{ALERT1}}$ pin must be configured for the ALERT function in Register 7-2 for this register to control the pin. See **Section 5.16.2, "ALERT Pin Assignments"**. ALERTs must be enabled in Register 7-34 before you can route them to a pin. Disable ALERTs in Register 7-34 before changing any limit to avoid false triggers.

bit 23 **CH1OC**:
0 = ALERT for overcurrent on Channel 1 is not enabled
1 = ALERT for overcurrent on Channel 1 is enabled

bit 22 **CH2OC**:
0 = ALERT for overcurrent on Channel 2 is not enabled
1 = ALERT for overcurrent on Channel 2 is enabled

bit 21 **CH3OC**:
0 = ALERT for overcurrent on Channel 3 is not enabled
1 = ALERT for overcurrent on Channel 3 is enabled

bit 20 **CH4OC**:
0 = ALERT for overcurrent on Channel 4 is not enabled
1 = ALERT for overcurrent on Channel 4 is enabled

bit 19 **CH1UC**:
0 = ALERT for undercurrent on Channel 1 is not enabled
1 = ALERT for undercurrent on Channel 1 is enabled

bit 18 **CH2UC**:
0 = ALERT for undercurrent on Channel 2 is not enabled
1 = ALERT for undercurrent on Channel 2 is enabled

bit 17 **CH3UC**:
0 = ALERT for undercurrent on Channel 3 is not enabled
1 = ALERT for undercurrent on Channel 3 is enabled

bit 16 **CH4UC**:
0 = ALERT for undercurrent on Channel 4 is not enabled
1 = ALERT for undercurrent on Channel 4 is enabled

bit 15 **CH1OV**:
0 = ALERT for overvoltage on Channel 1 is not enabled
1 = ALERT for overvoltage on Channel 1 is enabled


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**REGISTER 7-21: SLOW_ALERT1 (27H) REGISTER (CONTINUED)**

bit 14 **CH2OV**:
0 = ALERT for overvoltage on Channel 2 is not enabled
1 = ALERT for overvoltage on Channel 2 is enabled

bit 13 **CH3OV**:
0 = ALERT for overvoltage on Channel 3 is not enabled
1 = ALERT for overvoltage on Channel 3 is enabled

bit 12 **CH4OV**:
0 = ALERT for overvoltage on Channel 4 is not enabled
1 = ALERT for overvoltage on Channel 4 is enabled

bit 11 **CH1UV**:
0 = ALERT for undervoltage on Channel 1 is not enabled
1 = ALERT for undervoltage on Channel 1 is enabled

bit 10 **CH2UV**:
0 = ALERT for undervoltage on Channel 2 is not enabled
1 = ALERT for undervoltage on Channel 2 is enabled

bit 9 **CH3UV**:
0 = ALERT for undervoltage on Channel 3 is not enabled
1 = ALERT for undervoltage on Channel 3 is enabled

bit 8 **CH4UV**:
0 = ALERT for undervoltage on Channel 4 is not enabled
1 = ALERT for undervoltage on Channel 4 is enabled

bit 7 **CH1OP**:
0 = ALERT for overpower on Channel 1 is not enabled
1 = ALERT for overpower on Channel 1 is enabled

bit 6 **CH2OP**:
0 = ALERT for overpower on Channel 2 is not enabled
1 = ALERT for overpower on Channel 2 is enabled

bit 5 **CH3OP**:
0 = ALERT for overpower on Channel 3 is not enabled
1 = ALERT for overpower on Channel 3 is enabled

bit 4 **CH4OP**:
0 = ALERT for overpower on Channel 4 is not enabled
1 = ALERT for overpower on Channel 4 is enabled

bit 3 **ACC_OVF**: This bit signals when the Accumulator for any channel overflows or exceeds its fullness limit specified in Register 7-23.
0 = No Accumulator full related ALERT for this channel
1 = ALERT triggered by Accumulator fullness limit exceeded

bit 2 **ACC_COUNT**: This bit signals when the Accumulator Count overflows or exceeds its fullness limit specified in Register 7-23.
0 = No Accumulator full related ALERT for this channel
1 = ALERT triggered by Accumulator Count fullness limit exceeded

bit 1 **ALERT_CC1**: Setting this bit to '1' causes the SLOW/$\overline{\text{ALERT1}}$ pin to be asserted for 5 µs at the end of each conversion cycle. This pin must be configured as an $\overline{\text{ALERT}}$ pin for this function to trigger the SLOW/$\overline{\text{ALERT1}}$ pin. The SLOW function is not available on this pin when the pin is used as an $\overline{\text{ALERT}}$ pin. See **Section 5.16.1, "ALERT after Complete Conversion"**.
0 = No ALERT on SLOW/$\overline{\text{ALERT1}}$ pin at each conversion cycle complete event
1 = ALERT function on SLOW/$\overline{\text{ALERT1}}$ pin asserted for 5 µs on each completion of the conversion cycle

bit 0 Unimplemented, read as '0'.

**REGISTER 7-22: GPIO_ALERT2 (28H) REGISTER**

| RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 |
|---|---|---|---|---|---|---|---|
| CH1OC | CH2OC | CH3OC | CH4OC | CH1UC | CH2UC | CH3UC | CH4UC |
| bit 23 | | | | | | | bit 16 |

| RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 |
|---|---|---|---|---|---|---|---|
| CH1OV | CH2OV | CH3OV | CH4OV | CH1UV | CH2UV | CH3UV | CH4UV |
| bit 15 | | | | | | | bit 8 |

| RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | U-0 |
|---|---|---|---|---|---|---|---|
| CH1OP | CH2OP | CH3OP | CH4OP | ACC_OVF | ACC_COUNT | ALERT_CC2 | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

Write to this register to assign a specific ALERT signal to the GPIO/$\overline{\text{ALERT2}}$ pin. The GPIO/$\overline{\text{ALERT2}}$ pin must be configured for ALERT function in Register 7-2 for this register to control the pin. See **Section 5.16.2, "ALERT Pin Assignments"**. ALERTs must be enabled in Register 7-34 before you can route them to a pin. Disable ALERTs in Register 7-34 before changing any limit to avoid false triggers.

bit 23 **CH1OC**:
0 = ALERT for overcurrent on Channel 1 is not enabled
1 = ALERT for overcurrent on Channel 1 is enabled

bit 22 **CH2OC**:
0 = ALERT for overcurrent on Channel 2 is not enabled
1 = ALERT for overcurrent on Channel 2 is enabled

bit 21 **CH3OC**:
0 = ALERT for overcurrent on Channel 3 is not enabled
1 = ALERT for overcurrent on Channel 3 is enabled

bit 20 **CH4OC**:
0 = ALERT for overcurrent on Channel 4 is not enabled
1 = ALERT for overcurrent on Channel 4 is enabled

bit 19 **CH1UC**:
0 = ALERT for undercurrent on Channel 1 is not enabled
1 = ALERT for undercurrent on Channel 1 is enabled

bit 18 **CH2UC**:
0 = ALERT for undercurrent on Channel 2 is not enabled
1 = ALERT for undercurrent on Channel 2 is enabled

bit 17 **CH3UC**:
0 = ALERT for undercurrent on Channel 3 is not enabled
1 = ALERT for undercurrent on Channel 3 is enabled

bit 16 **CH4UC**:
0 = ALERT for undercurrent on Channel 4 is not enabled
1 = ALERT for undercurrent on Channel 4 is enabled

bit 15 **CH1OV**:
0 = ALERT for overvoltage on Channel 1 is not enabled
1 = ALERT for overvoltage on Channel 1 is enabled


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**REGISTER 7-22: GPIO_ALERT2 (28H) REGISTER (CONTINUED)**

bit 14 **CH2OV**:
0 = ALERT for overvoltage on Channel 2 is not enabled
1 = ALERT for overvoltage on Channel 2 is enabled

bit 13 **CH3OV**:
0 = ALERT for overvoltage on Channel 3 is not enabled
1 = ALERT for overvoltage on Channel 3 is enabled

bit 12 **CH4OV**:
0 = ALERT for overvoltage on Channel 4 is not enabled
1 = ALERT for overvoltage on Channel 4 is enabled

bit 11 **CH1UV**:
0 = ALERT for undervoltage on Channel 1 is not enabled
1 = ALERT for undervoltage on Channel 1 is enabled

bit 10 **CH2UV**:
0 = ALERT for undervoltage on Channel 2 is not enabled
1 = ALERT for undervoltage on Channel 2 is enabled

bit 9 **CH3UV**:
0 = ALERT for undervoltage on Channel 3 is not enabled
1 = ALERT for undervoltage on Channel 3 is enabled

bit 8 **CH4UV**:
0 = ALERT for undervoltage on Channel 4 is not enabled
1 = ALERT for undervoltage on Channel 4 is enabled

bit 7 **CH1OP**:
0 = ALERT for overpower on Channel 1 is not enabled
1 = ALERT for overpower on Channel 1 is enabled

bit 6 **CH2OP**:
0 = ALERT for overpower on Channel 2 is not enabled
1 = ALERT for overpower on Channel 2 is enabled

bit 5 **CH3OP**:
0 = ALERT for overpower on Channel 3 is not enabled
1 = ALERT for overpower on Channel 3 is enabled

bit 4 **CH4OP**:
0 = ALERT for overpower on Channel 4 is not enabled
1 = ALERT for overpower on Channel 4 is enabled

bit 3 **ACC_OVF**: This bit signals when the Accumulator for any channel overflows or exceeds its fullness limit specified in Register 7-23.
0 = No Accumulator full related ALERT for any channel
1 = ALERT triggered by Accumulator fullness limit exceeded for one or more channels

bit 2 **ACC_COUNT**: This bit signals when the Accumulator Count for any channel overflows or exceeds its fullness limit specified in Register 7-23.
0 = No Accumulator full related ALERT
1 = ALERT triggered by Accumulator Count fullness limit exceeded

bit 1 **ALERT_CC2**: Setting this bit to '1' causes the GPIO/$\overline{\text{ALERT2}}$ pin to be asserted for 5 µs at the end of each conversion cycle. This pin must be configured as an $\overline{\text{ALERT}}$ pin for this function to trigger the GPIO/$\overline{\text{ALERT2}}$ pin. The SLOW function is not available on this pin when the pin is used as an $\overline{\text{ALERT}}$ pin. See **Section 5.16.1, "ALERT after Complete Conversion"**.
0 = No ALERT on GPIO/$\overline{\text{ALERT2}}$ pin at each conversion cycle complete event
1 = ALERT function on GPIO/$\overline{\text{ALERT2}}$ pin asserted for 5 µs on each completion of the conversion cycle

bit 0 Unimplemented, read as '0'.

**REGISTER 7-23: ACC FULLNESS LIMITS (29H) REGISTER**

| R/W-0 | R/W-1 | R/W-0 | R/W-1 | R/W-0 | R/W-1 | R/W-0 | R/W-1 |
|---|---|---|---|---|---|---|---|
| CH1 ACC FULL[1:0] | | CH2 ACC FULL[1:0] | | CH3 ACC FULL[1:0] | | CH4 ACC FULL[1:0] | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-1 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| ACC COUNT FULL[1:0] | | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

These limits are used to set a limit for how full the Accumulators and Accumulator Count registers can be before the Accumulator Full and Accumulator Count full limits are tripped. This allows an ALERT to be registered when the Accumulator and Accumulator Count are approaching 100% full. Disable ALERTs in Register 7-34 before changing the value to avoid false triggers.

bit 15-14 **CH1 ACC FULL[1:0]**: Fullness limit for the Channel 1 Accumulator:
00 = Full
01 = 15/16 full (default)
10 = 7/8 full
11 = 3/4 full

bit 13-12 **CH2 ACC FULL[1:0]**: Fullness limit for the Channel 2 Accumulator:
00 = Full
01 = 15/16 full (default)
10 = 7/8 full
11 = 3/4 full

bit 11-10 **CH3 ACC FULL[1:0]**: Fullness limit for the Channel 3 Accumulator:
00 = Full
01 = 15/16 full (default)
10 = 7/8 full
11 = 3/4 full

bit 9-8 **CH4 ACC FULL[1:0]**: Fullness limit for the Channel 4 Accumulator:
00 = Full
01 = 15/16 full (default)
10 = 7/8 full
11 = 3/4 full

bit 7-6 **ACC COUNT FULL[1:0]**: Fullness limit for the Accumulator Count register:
00 = Full
01 = 15/16 full (default)
10 = 7/8 full
11 = 3/4 full

bit 5-0 Unimplemented, read as '0'.


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**REGISTER 7-24: OC LIMITN (30H-33H) REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OC LIMIT[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OC LIMIT[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **OC LIMIT[15:0]**: Overcurrent (OC) limit for each channel. This limit is a two's complement number for all modes. Disable ALERTs in Register 7-34 before changing the value to avoid false triggers. Each channel has its own limit and addressable register. Address 30h determines the limit for Channel 1, 33h for Channel 4.

**REGISTER 7-25: UC LIMITN (34H-37H) REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| UC LIMIT[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| UC LIMIT[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **UC LIMIT[15:0]**: Undercurrent (UC) limit for each channel. This limit is a two's complement number for all modes. Disable ALERTs in Register 7-34 before changing the value to avoid false triggers. Each channel has its own limit and addressable register. Address 34h determines the limit for Channel 1, 37h for Channel 4.

**REGISTER 7-26: OP LIMITN (38H-3BH) REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OP LIMIT[23:16] | | | | | | | |
| bit 23 | | | | | | | bit 16 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OP LIMIT[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OP LIMIT[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 23-0 **OP LIMIT[23:0]**: Overpower (OP) limit for each channel. This limit is a two's complement number for all modes. These 24 bits correspond to the upper 24 MSBs in the $V_{POWER}$ number. The OP limit (only) is magnitude based, an OP trigger occurs when the result is more positive or more negative than the limit. Disable ALERTs in Register 7-34 before changing the value to avoid false triggers. Each channel has its own limit and addressable register. Address 38h determines the limit for Channel 1, 3Bh for Channel 4.

**REGISTER 7-27: OV LIMITN (3CH-3FH) REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OV LIMIT[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OV LIMIT[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **OV LIMIT[15:0]**: Overvoltage (OV) limit for each channel. This limit is a two's complement number for all modes. Disable ALERTs in Register 7-34 before changing the value to avoid false triggers. Each channel has its own limit and addressable register. Address 3Ch determines the limit for Channel 1, 3Fh for Channel 4.


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**REGISTER 7-28: UV LIMITN (40H-43H) REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| UV LIMIT[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| UV LIMIT[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **UV LIMIT[15:0]**: Undervoltage (UV) limit for each channel. This limit is a two's complement number for all modes. Disable ALERTs in Register 7-34 before changing the value to avoid false triggers. Each channel has its own limit and addressable register. Address 40h determines the limit for Channel 1, 43h for Channel 4.

**REGISTER 7-29: OC LIMIT NSAMPLES (44H) REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| NSAMPLES OC CH1[1:0] | | NSAMPLES OC CH2[1:0] | | NSAMPLES OC CH3[1:0] | | NSAMPLES OC CH4[1:0] | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

Number of consecutive samples exceeding the overcurrent limit that are required to trigger the ALERT function for each channel. The default is 1 sample (00). The sample counter is not reset until a conversion is completed to confirm that the ALERT condition is no longer present. A single conversion immediately after the ALERT is cleared will reset the ALERT. Disable ALERTs in Register 7-34 before changing the value to avoid false triggers.

bit 7-6 **NSAMPLES OC CH1[1:0]**: Consecutive sample count to trigger the OC ALERT for Channel 1
00 = 1 (default)
01 = 4 samples
10 = 8 samples
11 = 16

bit 5-4 **NSAMPLES OC CH2[1:0]**: Consecutive sample count to trigger the OC ALERT for Channel 2
00 = 1 (default)
01 = 4 samples
10 = 8 samples
11 = 16

bit 3-2 **NSAMPLES OC CH3[1:0]**: Consecutive sample count to trigger the OC ALERT for Channel 3
00 = 1 (default)
01 = 4 samples
10 = 8 samples
11 = 16

bit 1-0 **NSAMPLES OC CH4[1:0]**: Consecutive sample count to trigger the OC ALERT for Channel 4
00 = 1 (default)
01 = 4 samples
10 = 8 samples
11 = 16


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**REGISTER 7-30: UC LIMIT NSAMPLES (45H) REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| NSAMPLES UC CH1[1:0] | | NSAMPLES UC CH2[1:0] | | NSAMPLES UC CH3[1:0] | | NSAMPLES UC CH4[1:0] | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

Number of consecutive samples exceeding the undercurrent limit that are required to trigger the ALERT function for each channel. The default is 1. Disable ALERTs in Register 7-34 before changing the value to avoid false triggers.

bit 7-6 **NSAMPLES UC CH1[1:0]**: Consecutive sample count to trigger the UC ALERT for Channel 1
00 = 1 (default)
01 = 4 samples
10 = 8 samples
11 = 16

bit 5-4 **NSAMPLES UC CH2[1:0]**: Consecutive sample count to trigger the UC ALERT for Channel 2
00 = 1 (default)
01 = 4 samples
10 = 8 samples
11 = 16

bit 3-2 **NSAMPLES UC CH3[1:0]**: Consecutive sample count to trigger the UC ALERT for Channel 3
00 = 1 (default)
01 = 4 samples
10 = 8 samples
11 = 16

bit 1-0 **NSAMPLES UC CH4[1:0]**: Consecutive sample count to trigger the UC ALERT for Channel 4
00 = 1 (default)
01 = 4 samples
10 = 8 samples
11 = 16

**REGISTER 7-31: OP LIMIT NSAMPLES (46H) REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| NSAMPLES OP CH1[1:0] | | NSAMPLES OP CH2[1:0] | | NSAMPLES OP CH3[1:0] | | NSAMPLES OP CH4[1:0] | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

Number of consecutive samples exceeding the overpower limit that are required to trigger the ALERT function for each channel. The default is 1. Disable ALERTs in Register 7-34 before changing the value to avoid false triggers.

bit 7-6 **NSAMPLES OP CH1[1:0]**: Consecutive sample count to trigger the OP ALERT for Channel 1
00 = 1 (default)
01 = 4 samples
10 = 8 samples
11 = 16

bit 5-4 **NSAMPLES OP CH2[1:0]**: Consecutive sample count to trigger the OP ALERT for Channel 2
00 = 1 (default)
01 = 4 samples
10 = 8 samples
11 = 16

bit 3-2 **NSAMPLES OP CH3[1:0]**: Consecutive sample count to trigger the OP ALERT for Channel 3
00 = 1 (default)
01 = 4 samples
10 = 8 samples
11 = 16

bit 1-0 **NSAMPLES OP CH4[1:0]**: Consecutive sample count to trigger the OP ALERT for Channel 4
00 = 1 (default)
01 = 4 samples
10 = 8 samples
11 = 16


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**REGISTER 7-32: OV LIMIT NSAMPLES (47H) REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| NSAMPLES OV CH1[1:0] | | NSAMPLES OV CH2[1:0] | | NSAMPLES OV CH3[1:0] | | NSAMPLES OV CH4[1:0] | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

Number of consecutive samples exceeding the overvoltage limit that are required to trigger the ALERT function for each channel. The default is 1. Disable ALERTs in Register 7-34 before changing the value to avoid false triggers.

bit 7-6 **NSAMPLES OV CH1[1:0]**: Consecutive sample count to trigger the OV ALERT for Channel 1
00 = 1 (default)
01 = 4 samples
10 = 8 samples
11 = 16

bit 5-4 **NSAMPLES OV CH2[1:0]**: Consecutive sample count to trigger the OV ALERT for Channel 2
00 = 1 (default)
01 = 4 samples
10 = 8 samples
11 = 16

bit 3-2 **NSAMPLES OV CH3[1:0]**: Consecutive sample count to trigger the OV ALERT for Channel 3
00 = 1 (default)
01 = 4 samples
10 = 8 samples
11 = 16

bit 1-0 **NSAMPLES OV CH4[1:0]**: Consecutive sample count to trigger the OV ALERT for Channel 4
00 = 1 (default)
01 = 4 samples
10 = 8 samples
11 = 16

**REGISTER 7-33: UV LIMIT NSAMPLES (48H) REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| NSAMPLES UV CH1[1:0] | | NSAMPLES UV CH2[1:0] | | NSAMPLES UV CH3[1:0] | | NSAMPLES UV CH4[1:0] | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

Number of consecutive samples exceeding the undervoltage limit that are required to trigger the ALERT function for each channel. The default is 1. Disable ALERTs in Register 7-34 before changing the value to avoid false triggers.

bit 7-6 **NSAMPLES UV CH1[1:0]**: Consecutive sample count to trigger the UV ALERT for Channel 1
00 = 1 (default)
01 = 4 samples
10 = 8 samples
11 = 16

bit 5-4 **NSAMPLES UV CH2[1:0]**: Consecutive sample count to trigger the UV ALERT for Channel 2
00 = 1 (default)
01 = 4 samples
10 = 8 samples
11 = 16

bit 3-2 **NSAMPLES UV CH3[1:0]**: Consecutive sample count to trigger the UV ALERT for Channel 3
00 = 1 (default)
01 = 4 samples
10 = 8 samples
11 = 16

bit 1-0 **NSAMPLES UV CH4[1:0]**: Consecutive sample count to trigger the UV ALERT for Channel 4
00 = 1 (default)
01 = 4 samples
10 = 8 samples
11 = 16


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**REGISTER 7-34: ALERT ENABLE (49H) REGISTER**

| RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 |
|---|---|---|---|---|---|---|---|
| CH1OC | CH2OC | CH3OC | CH4OC | CH1UC | CH2UC | CH3UC | CH4UC |
| bit 23 | | | | | | | bit 16 |

| RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 |
|---|---|---|---|---|---|---|---|
| CH1OV | CH2OV | CH3OV | CH4OV | CH1UV | CH2UV | CH3UV | CH4UV |
| bit 15 | | | | | | | bit 8 |

| RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | RW-0 | U-0 |
|---|---|---|---|---|---|---|---|
| CH1OP | CH2OP | CH3OP | CH4OP | ACC_OVF | ACC_COUNT | ALERT_CC | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

Write to these bits to enable ALERT functions. See **Section 5.16.4, "ALERT Functionality – Voltage, Current and Power"**. To enable OC, UC, OP, OV, UV ALERTs, write '1' to the appropriate bit. ALERTs must be enabled in this register before they can be routed to an $\overline{\text{ALERT}}$ pin. Disable ALERTs in this register before modifying any of the various limits in Register 7-24, Register 7-25, Register 7-26, Register 7-27, Register 7-28 to avoid false triggers. A REFRESH (or REFRESH_V/G) is required to activate the enabled ALERTs.

bit 23 **CH1OC**:
0 = ALERT for overcurrent on Channel 1 is disabled
1 = ALERT for overcurrent on Channel 1 is enabled

bit 22 **CH2OC**:
0 = ALERT for overcurrent on Channel 2 is disabled
1 = ALERT for overcurrent on Channel 2 is enabled

bit 21 **CH3OC**:
0 = ALERT for overcurrent on Channel 3 is disabled
1 = ALERT for overcurrent on Channel 3 is enabled

bit 20 **CH4OC**:
0 = ALERT for overcurrent on Channel 4 is disabled
1 = ALERT for overcurrent on Channel 4 is enabled

bit 19 **CH1UC**:
0 = ALERT for undercurrent on Channel 1 is disabled
1 = ALERT for undercurrent on Channel 1 is enabled

bit 18 **CH2UC**:
0 = ALERT for undercurrent on Channel 2 is disabled
1 = ALERT for undercurrent on Channel 2 is enabled

bit 17 **CH3UC**:
0 = ALERT for undercurrent on Channel 3 is disabled
1 = ALERT for undercurrent on Channel 3 is enabled

bit 16 **CH4UC**:
0 = ALERT for undercurrent on Channel 4 is disabled
1 = ALERT for undercurrent on Channel 4 is enabled

**REGISTER 7-34: ALERT ENABLE (49H) REGISTER (CONTINUED)**

bit 15 **CH1OV**:
0 = ALERT for overvoltage on Channel 1 is disabled
1 = ALERT for overvoltage on Channel 1 is enabled

bit 14 **CH2OV**:
0 = ALERT for overvoltage on Channel 2 is disabled
1 = ALERT for overvoltage on Channel 2 is enabled

bit 13 **CH3OV**:
0 = ALERT for overvoltage on Channel 3 is disabled
1 = ALERT for overvoltage on Channel 3 is enabled

bit 12 **CH4OV**:
0 = ALERT for overvoltage on Channel 4 is disabled
1 = ALERT for overvoltage on Channel 4 is enabled

bit 11 **CH1UV**:
0 = ALERT for undervoltage on Channel 1 is disabled
1 = ALERT for undervoltage on Channel 1 is enabled

bit 10 **CH2UV**:
0 = ALERT for undervoltage on Channel 2 is disabled
1 = ALERT for undervoltage on Channel 2 is enabled

bit 9 **CH3UV**:
0 = ALERT for undervoltage on Channel 3 is disabled
1 = ALERT for undervoltage on Channel 3 is enabled

bit 8 **CH4UV**:
0 = ALERT for undervoltage on Channel 4 is disabled
1 = ALERT for undervoltage on Channel 4 is enabled

bit 7 **CH1OP**:
0 = ALERT for overpower on Channel 1 is disabled
1 = ALERT for overpower on Channel 1 is enabled

bit 6 **CH2OP**:
0 = ALERT for overpower on Channel 2 is disabled
1 = ALERT for overpower on Channel 2 is enabled

bit 5 **CH3OP**:
0 = ALERT for overpower on Channel 3 is disabled
1 = ALERT for overpower on Channel 3 is enabled

bit 4 **CH4OP**:
0 = ALERT for overpower on Channel 4 is disabled
1 = ALERT for overpower on Channel 4 is enabled

bit 3 **ACC_OVF**:
0 = ALERT for Accumulator fullness limit exceeded is disabled
1 = ALERT for Accumulator fullness limit exceeded for one or more channels is enabled

bit 2 **ACC_COUNT**:
0 = ALERT for Accumulator Count fullness is disabled
1 = ALERT for Accumulator Count fullness limit exceeded is enabled

bit 1 **ALERT_CC**:
0 = ALERT for Conversion Cycle Complete is disabled
1 = ALERT for Conversion Cycle Complete is enabled

bit 0 Unimplemented, read as '0'.


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**REGISTER 7-35: ACCUM CONFIG ACT (4AH) REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ACC1_CONFIG[1:0] | | ACC2_CONFIG[1:0] | | ACC3_CONFIG[1:0] | | ACC4_CONFIG[1:0] | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

This register contains an image of Register 7-19 and reflects the current active values of these settings, whereas the values in register 25h may be programmed but not activated by one of the REFRESH commands. This register allows software to determine the actual active settings.

bit 7-6 **ACC1_CONFIG[1:0]**: Configure the accumulator for Channel 1 to accumulate $V_{POWER}$ (default), $V_{SENSE}$ or $V_{BUS}$.
00 = Channel 1 Accumulator accumulates $V_{POWER}$
01 = Channel 1 Accumulator accumulates $V_{SENSE}$
10 = Channel 1 Accumulator accumulates $V_{BUS}$
11 = Reserved, read as '0'.

bit 5-4 **ACC2_CONFIG[1:0]**: Configure the accumulator for Channel 2 to accumulate $V_{POWER}$ (default), $V_{SENSE}$ or $V_{BUS}$.
00 = Channel 2 Accumulator accumulates $V_{POWER}$
01 = Channel 2 Accumulator accumulates $V_{SENSE}$
10 = Channel 2 Accumulator accumulates $V_{BUS}$
11 = Reserved, read as '0'.

bit 3-2 **ACC3_CONFIG[1:0]**: Configure the accumulator for Channel 3 to accumulate $V_{POWER}$ (default), $V_{SENSE}$ or $V_{BUS}$.
00 = Channel 3 Accumulator accumulates $V_{POWER}$
01 = Channel 3 Accumulator accumulates $V_{SENSE}$
10 = Channel 3 Accumulator accumulates $V_{BUS}$
11 = Reserved, read as '0'.

bit 1-0 **ACC4_CONFIG[1:0]**: Configure the accumulator for Channel 4 to accumulate $V_{POWER}$ (default), $V_{SENSE}$ or $V_{BUS}$.
00 = Channel 4 Accumulator accumulates $V_{POWER}$
01 = Channel 4 Accumulator accumulates $V_{SENSE}$
10 = Channel 4 Accumulator accumulates $V_{BUS}$
11 = Reserved, read as '0'.

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### REGISTER 7-36: ACCUM CONFIG LAT (4BH) REGISTER

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ACC1_CONFIG[1:0] | | ACC2_CONFIG[1:0] | | ACC3_CONFIG[1:0] | | ACC4_CONFIG[1:0] | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

This register contains an image of Register 7-19. The bits in this register reflect the value of these settings that were active before the most recent REFRESH command (including REFRESH_V and/of REFRESH_G). The values in register 25h may be programmed but not activated by one of the REFRESH commands and the values in register 4Ah are currently active. This register allows software to determine the actual setting that was active prior to the most recent REFRESH command and, therefore, corresponds to the dataset that is held in the readable registers. This register is valid when the results registers are valid, 1 ms after a REFRESH/_V/_G command.

bit 7-6 **ACC1_CONFIG[1:0]**: Configure the accumulator for Channel 1 to accumulate $V_{POWER}$ (default), $V_{SENSE}$ or $V_{BUS}$.
00 = Channel 1 Accumulator accumulates $V_{POWER}$
01 = Channel 1 Accumulator accumulates $V_{SENSE}$
10 = Channel 1 Accumulator accumulates $V_{BUS}$
11 = Reserved, read as '0'.

bit 5-4 **ACC2_CONFIG[1:0]**: Configure the accumulator for Channel 2 to accumulate $V_{POWER}$ (default), $V_{SENSE}$ or $V_{BUS}$.
00 = Channel 2 Accumulator accumulates $V_{POWER}$
01 = Channel 2 Accumulator accumulates $V_{SENSE}$
10 = Channel 2 Accumulator accumulates $V_{BUS}$
11 = Reserved, read as '0'.

bit 3-2 **ACC3_CONFIG[1:0]**: Configure the accumulator for Channel 3 to accumulate $V_{POWER}$ (default), $V_{SENSE}$ or $V_{BUS}$.
00 = Channel 3 Accumulator accumulates $V_{POWER}$
01 = Channel 3 Accumulator accumulates $V_{SENSE}$
10 = Channel 3 Accumulator accumulates $V_{BUS}$
11 = Reserved, read as '0'.

bit 1-0 **ACC4_CONFIG[1:0]**: Configure the accumulator for Channel 4 to accumulate $V_{POWER}$ (default), $V_{SENSE}$ or $V_{BUS}$.
00 = Channel 4 Accumulator accumulates $V_{POWER}$
01 = Channel 4 Accumulator accumulates $V_{SENSE}$
10 = Channel 4 Accumulator accumulates $V_{BUS}$
11 = Reserved, read as '0'.


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**REGISTER 7-37: PRODUCT ID (FDH) REGISTER**

| R-0 | R-1 | R-1 | R-1 | R-0 | R-1 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| PID[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-0 **PID[7:0]**: This register contains the Product ID for the PAC194X. These values depend on the part version:

0110_1000 for PAC1941-1
0110_1001 for PAC1942-1
0110_1010 for PAC1943-1
0110_1011 for PAC1944-1
0110_1100 for PAC1941-2
0110_1101 for PAC1942-2

**REGISTER 7-38: MANUFACTURER ID (FEH) REGISTER**

| R-0 | R-1 | R-0 | R-1 | R-0 | R-1 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| MID[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-0 **MID[7:0]**: The Manufacturer ID register identifies Microchip as the manufacturer of the PAC194X. This value is 54h.

**REGISTER 7-39: REVISION ID (FFH) REGISTER**

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-1 | R-0 |
|---|---|---|---|---|---|---|---|
| RID[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-0 **RID[7:0]**: The Revision register identifies the die revision.
`0000 0010b` for the initial release.

**NOTES:**


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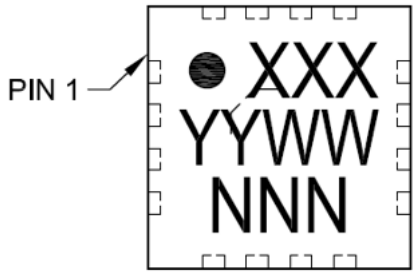
## 8.0 PACKAGING INFORMATION

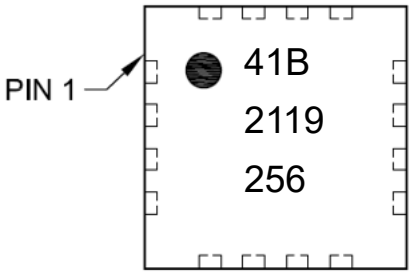
### 8.1 Package Marking Information

16-Lead VQFN, (3 x 3 mm)

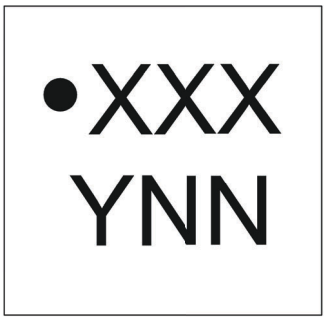



| Part Number | Code |
|---|---|
| PAC1941T-1E/4MX | 941 |
| PAC1941T-2E/4MX | 41B |
| PAC1942T-1E/4MX | 942 |
| PAC1942T-2E/4MX | 42B |
| PAC1943T-E/4MX | 943 |
| PAC1944T-E/4MX | 944 |

Example:

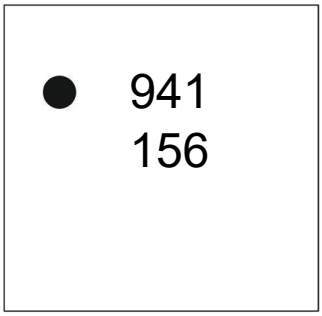



16-Lead WLCSP (2.225 x 2.17 mm)




| Part Number | Code |
|---|---|
| PAC1941T-1E/J6CX | 941 |
| PAC1941T-2E/J6CX | 41B |
| PAC1942T-1E/J6CX | 942 |
| PAC1942T-2E/J6CX | 42B |
| PAC1943T-E/J6CX | 943 |
| PAC1944T-E/J6CX | 944 |

Example:

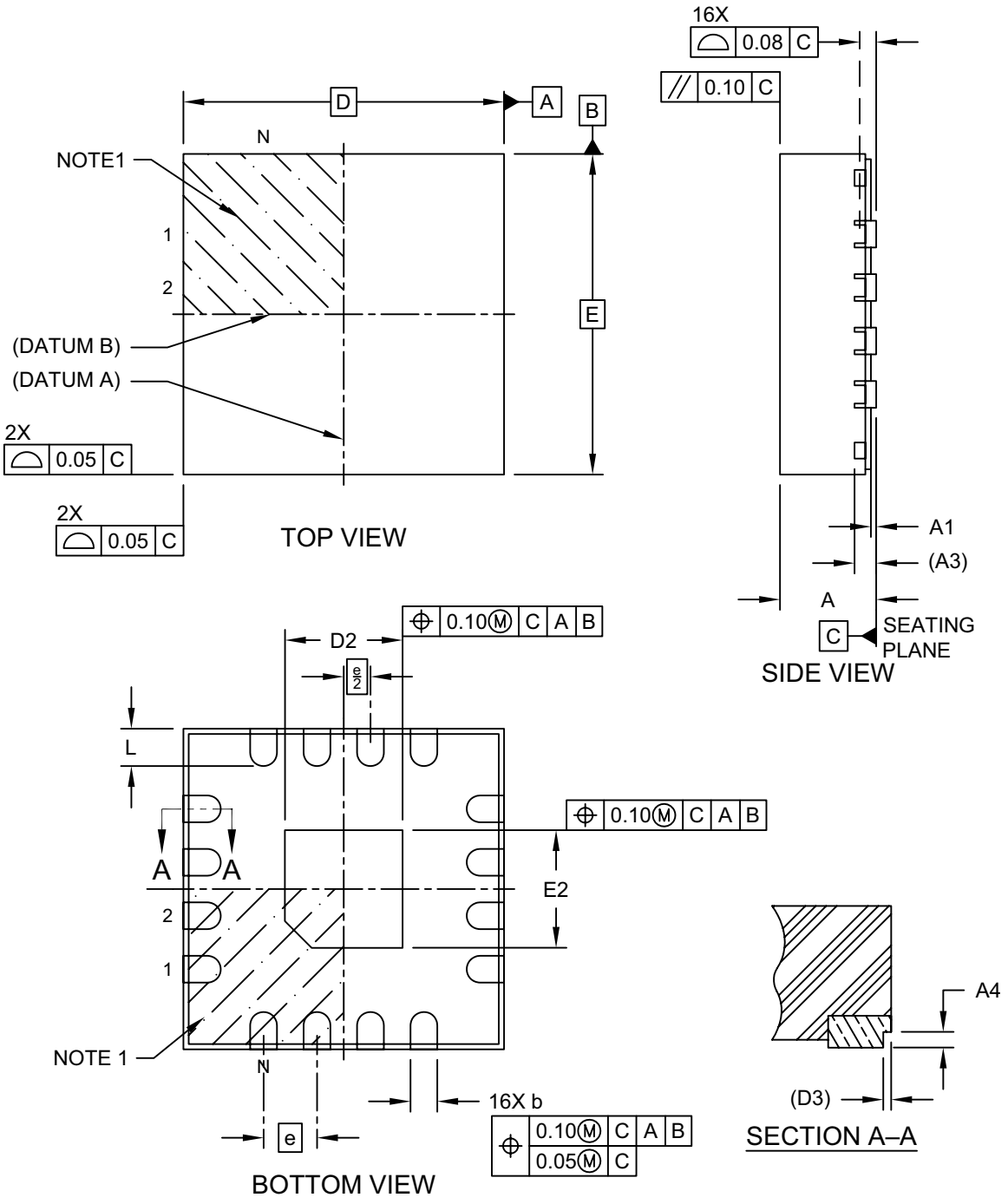



| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

**16-Lead Very Thin Quad Flat, No Lead Package (4MX) - 3x3x0.9 mm Body [VQFN]**
**With 1.10 mm Exposed Pad and Stepped Wettable Flanks**

| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|




Microchip Technology Drawing C04-508 Rev A Sheet 1 of 2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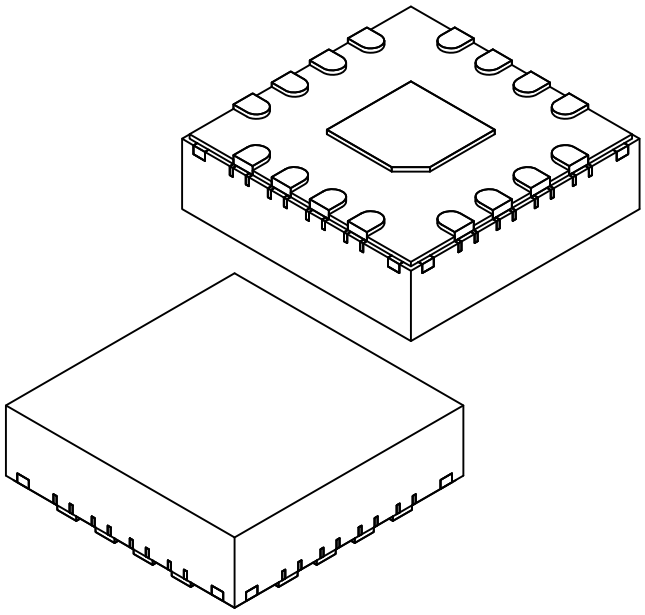
## 16-Lead Very Thin Quad Flat, No Lead Package (4MX) - 3x3x0.9 mm Body [VQFN] With 1.10 mm Exposed Pad and Stepped Wettable Flanks

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 16 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.85 | 0.90 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.203 REF | |
| Overall Length | D | | 3.00 BSC | |
| Exposed Pad Length | D2 | 1.00 | 1.10 | 1.20 |
| Overall Width | E | | 3.00 BSC | |
| Exposed Pad Width | E2 | 1.00 | 1.10 | 1.20 |
| Terminal Width | b | 0.20 | 0.25 | 0.30 |
| Terminal Length | L | 0.25 | 0.35 | 0.45 |
| Wettable Flank Step Length | D3 | | 0.05 REF | |
| Wettable Flank Step Height | A4 | 0.10 | - | 0.19 |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-508 Rev A Sheet 2 of 2

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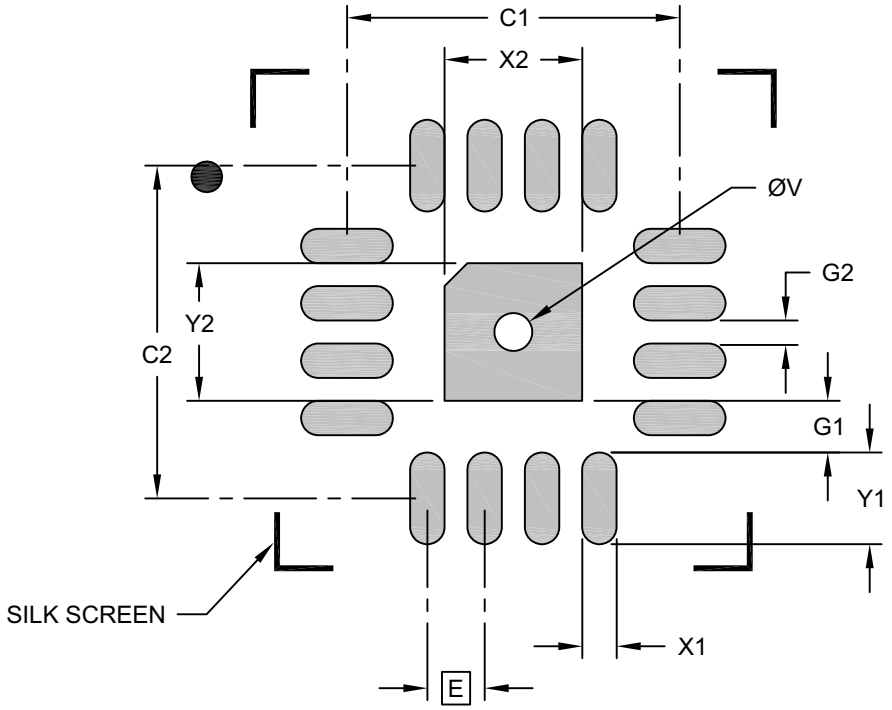
### 16-Lead Very Thin Quad Flat, No Lead Package (4MX) - 3x3x0.9 mm Body [VQFN] With 1.10 mm Exposed Pad and Stepped Wettable Flanks

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | X2 | | | 1.20 |
| Optional Center Pad Length | Y2 | | | 1.20 |
| Contact Pad Spacing | C1 | | 2.90 | |
| Contact Pad Spacing | C2 | | 2.90 | |
| Contact Pad Width (X16) | X1 | | | 0.30 |
| Contact Pad Length (X16) | Y1 | | | 0.80 |
| Contact Pad to Center Pad (X16) | G1 | 0.45 | | |
| Contact Pad to Contact Pad (X12) | G2 | 0.20 | | |
| Thermal Via Diameter | V | | 0.33 | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2508 Rev A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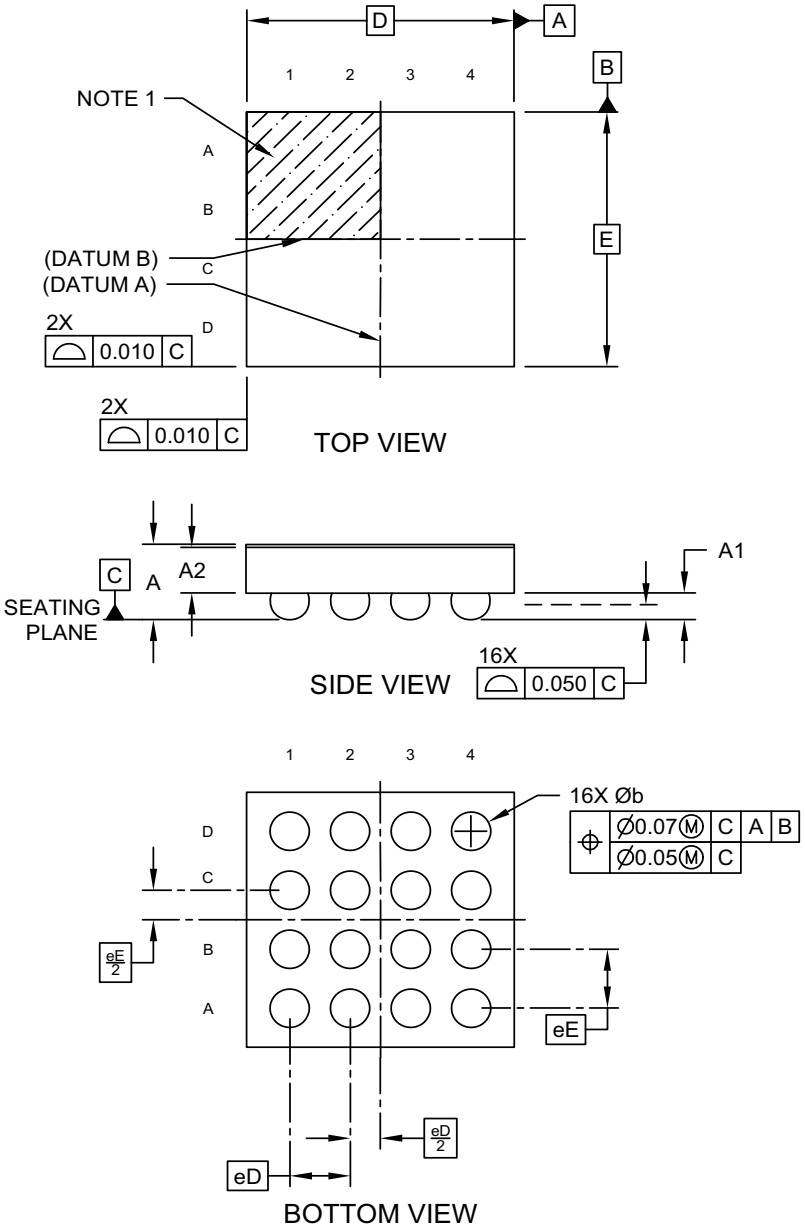
### 16-Ball Wafer Level Chip Scale Package (CS) - 2.225x2.17 mm Body [WLCSP]

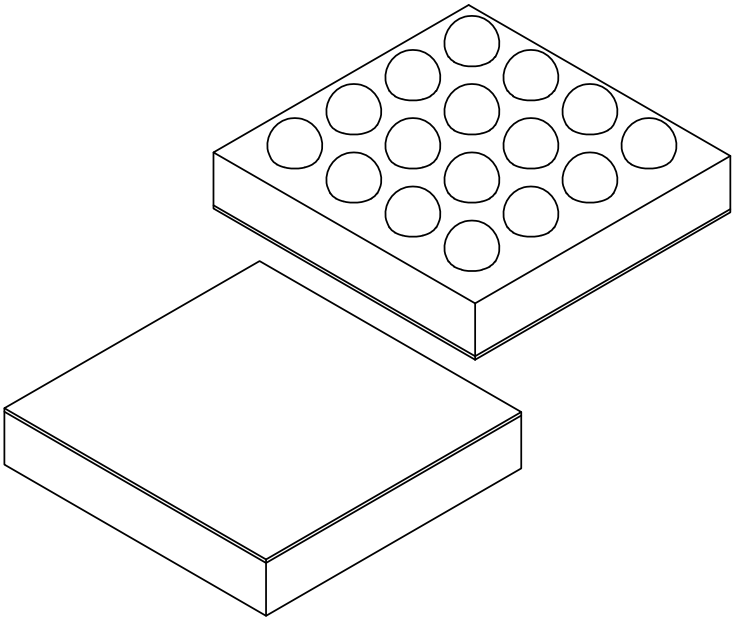
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-6036-01 Rev. C Sheet 1 of 2

### 16-Ball Wafer Level Chip Scale Package (CS) - 2.225x2.17 mm Body [WLCSP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Bump Pitch | eD | | 0.50 BSC | |
| Bump Pitch | eE | | 0.50 BSC | |
| Length | D | | 2.225 BSC | |
| Width | E | | 2.170 BSC | |
| Overall Height | A | 0.601 | 0.641 | 0.679 |
| Bump Height | A1 | 0.197 | - | 0.257 |
| Die Thickness | A2 | 0.363 | 0.388 | 0.413 |
| Bump Diameter | b | 0.297 | 0.327 | 0.357 |

Notes:

1. Topside A1 indicator is an engraved figure.
2. Under-fill is recommended for best solder joint reliability.
3. Solder diameter at interface to package body is 300µm (nominal).
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-6036-01 Rev. C Sheet 2 of 2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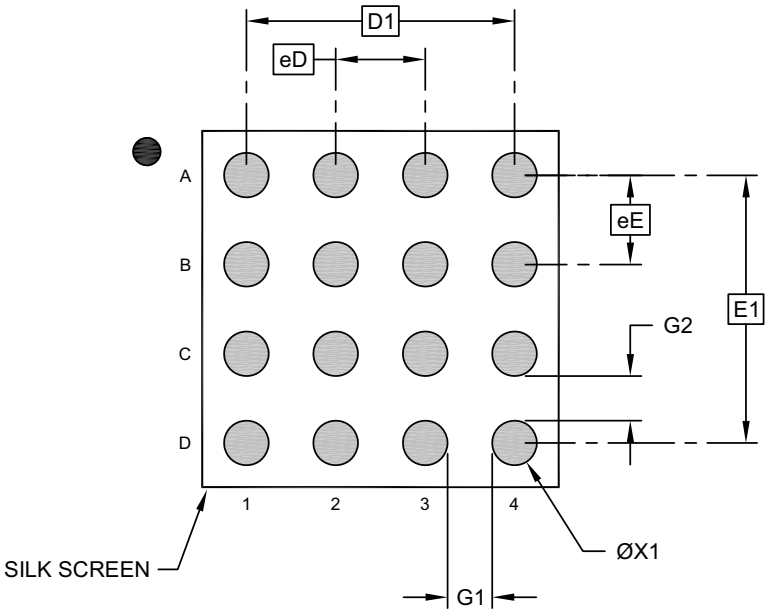
### 16-Ball Wafer Level Chip Scale Package (CS) - 2.225x2.17 mm Body [WLCSP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | eD | | 0.50 BSC | |
| Contact Pitch | eE | | 0.50 BSC | |
| Overall Pitch | D1 | | 1.50 BSC | |
| Overall Pitch | E1 | | 1.50 BSC | |
| Space Between Contacts | G1 | | 0.25 | |
| Space Between Contacts | G2 | | 0.25 | |
| Contact Diameter | ØX1 | | 0.25 | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-8036-01 Rev. C

**NOTES:**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# APPENDIX A: REVISION HISTORY

## Revision A (June 2021)

- Initial release of this document.

**Note:** The $I^2C$ standard uses the terminology “Master” and “Slave”. The equivalent Microchip terminology used in this document is “Host” and “Client”, respectively.

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X | -X | X | /XXX |
|---|---|---|---|---|
| Device | Tape and Reel | Device Option | Temperature Range | Package |

| | | |
|---|---|---|
| **Device:** | PAC194X: Single/Multi-Channel Power Monitor with Accumulator (9V) | |
| **Tape and Reel:** | T | = Tape and Reel |
| **Device Option** | 1(2) | = High-Side Power Monitor |
| | 2(2) | = Low-Side Power Monitor |
| **Temperature Range:** | E | = -40°C to +125°C (Extended) |
| **Package:** | 4MX | = 16-Lead Very Thin Quad Flat, No Lead Package, 3 mm x 3 mm (VQFN) |
| | J6CX | = 16-Ball Wafer Level Chip Scale Package, 2.225 mm x 2.17 mm (WLCSP) |

**Example:**

a) PAC1941T-1E/4MX: 16-lead 3 mm x 3 mm VQFN, Single-Channel, High-Side Power, Extended Temperature, Shipped in 120-piece, Tape and Reel

b) PAC1944T-E/4MX: 16-lead 3 mm x 3 mm VQFN, Four-Channel, High-Side Power, Extended Temperature, Shipped in 3300-piece, Tape and Reel

c) PAC1942T-2E/J6CX: 16-lead 2.225 mm x 2.17 mm WLCSP, Dual-Channel, Low-Side Power, Extended Temperature, Shipped in 5.000-piece, Tape and Reel

d) PAC1943T-E/J6CX: 16-lead 2.225 mm x 2.17 mm WLCSP, Three-Channel, High-Side Power, Extended Temperature, Shipped in 5.000-piece, Tape and Reel

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

**2:** Only appears on single and dual-channel devices. Other devices are high-side power only.

**NOTES:**


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ISBN: 978-1-5224-8341-0

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