PAC1921

High-Side Power/Current Monitor with Analog Output

Features

- Configurable Measurement Type Output: Power, Current or Bus Voltage
- Configurable Voltage Output (3V, 2V, 1.5V, 1V)
  - All output values also available over SMBus
- New Device Topology
  - Provides integrated average power measurement
  - Power measurements provided to microcontroller with ADC inputs
  - Unique lossless integrating architecture allows operation at low sense voltages
  - Output voltage proportional to selected measurement
- High-Side Current Sensor
  - 100 mV full-scale current sense voltage range
  - Second-order delta-sigma ADC with 11-bit or 14-bit resolution
  - Selectable current binary gain ranges: 1x through 128x
- 1% Power Measurement Accuracy
- Auto-Zero Offset
- Auto Sleep State
  - Automatically shifts to low-power state (3.5 µA)
- Power Supply
  - V_{DD} = 3.3V nominal (operational range 3.0V to 5.5V)
- Bus Range 0V to 32V
- No Input Filters Required
- Available in a 10-pin 3 mm x 3 mm VDFN RoHS Compliant Package

Applications

- Diagnostic Equipment
- Servers
- Power Supplies
- Industrial and Power Management Systems
- Notebook and Desktop Computers

Description

The PAC1921 is a dedicated power-monitoring device with a configurable analog output that can present power, current or voltage. The PAC1921 is designed for power measurement and diagnostic systems that cannot allow for latency when performing high-speed power management. Measurements are accumulated in large lossless registers, allowing for integration periods of 500 µs to 2.9 seconds. The measurement is averaged and presented on the analog output with a full scale range of 3V, 2V, 1.5V or 1.0V.

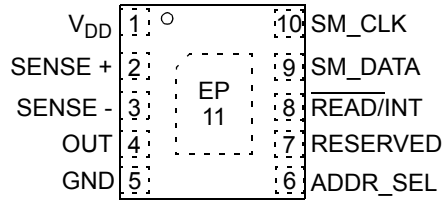
The PAC1921 has a $\overline{\text{READ}}$/INT pin for host control of the measurement integration period. This pin can be used to synchronize readings of multiple buses between several devices. Alternatively, PAC1921 is able to provide outputs in a free-running mode. Information is provided on the OUT pin and is available via SMBus if desired. Data sampling and output attributes, such as the internal ADC resolution (11-bit or 14-bit) and sample rate, are configurable. The SMBus interface has more selections for user-configurable options.

The PAC1921 is a 1% accurate power measurement device that measures and cancels the zero offset from the input pins. The PAC1921 was designed to monitor power rails from 0-32V with a full-scale capability of 100 mV across the sense resistor. No input filters are required for this device.

Package Types

PAC1921

3x3 VDFN*



*Includes Exposed Thermal Pad (EP), see Table 3-1

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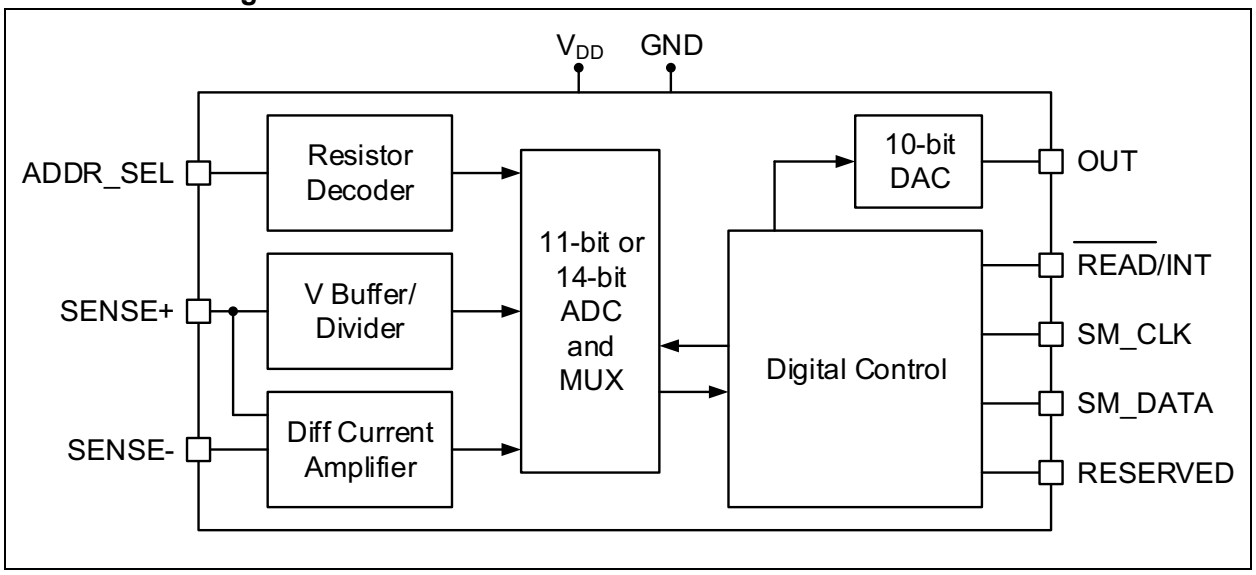
Device Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

1.1 Electrical Specifications

Absolute Maximum Ratings(†)

V_{DD} pin ..... -0.3 to 6.0V

Voltage on SENSE- and SENSE+ pins ..... -0.3 to 42V

Voltage on ADDR_SEL pin ..... -0.3 to 2.6V

Voltage on any other pin to GND ..... -0.3 to 6.0V

Voltage between Sense pins (|(SENSE+ – SENSE-)|) 40V

Input current to any pin except V_{DD} ..... ±10 mA

Output short circuit current ..... Continuous

Package Power Dissipation (Note) ..... 0.5W up to T_A = +85°C

Junction to Ambient (θ_{JA}) ..... +78°C/W

Operating Ambient Temperature Range ..... -40 to +85°C

Storage Temperature Range ..... -55 to +150°C

ESD Rating - All pins - HBM 2000V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

Note:	The Package Power Dissipation specification assumes a recommended thermal via design consisting of a 2 x 2 matrix of 0.3 mm (12 mil) vias at 1.0 mm pitch connected to the ground plane with a 1.6 mm x 2.3 mm thermal landing.

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TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise specified, maximum values are at T_A = -40°C to +85°C, V_{DD} = 3V to 5.5V, V_{BUS} = 0V to 32V; typical values are at T_A = +25°C, V_{DD} = 3.3V, V_{BUS} = 24V, V_{SENSE} = (SENSE+ – SENSE-) = 0V						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Power Supply						
V_{DD} Range	V_{DD}	3.0	—	5.5	V	
V_{DD} Integrate Current	I_{DD}	—	450	900	µA	Output unloaded
V_{DD} Read Current	I_{READ}	—	300	450	µA	Output unloaded
V_{DD} Sleep Current	I_{SLEEP}	—	3.5	15	µA	
V_{DD} Rise Rate	V_{DD_RISE}	0.05	—	1000	V/ms	0 to 3V in 60 ms
Analog Input Characteristics						
Bus Voltage Range	V_{BUS}	0	—	32	V	Common-mode voltage on SENSE pins, referenced to ground
V_{SENSE} Differential Input Voltage Range	V_{SENSE_DIF}	0	—	100	mV	
ADC Data Resolution	ADC_RES	—	—	14	bits	
V_{SENSE} LSB Step Size	V_{SENSE}_LSB	—	6.1	—	µV	14-bit resolution
		—	48.8	—	µV	11-bit resolution
V_{BUS} LSB Step Size	V_{BUS}_LSB	—	1.95	—	mV	14-bit resolution
		—	15.6	—	mV	11-bit resolution
V_{SENSE} Gain Accuracy	$V_{SENSE_GAIN_ERR}$	—	±0.2	±0.4	%	Gain = 1
V_{SENSE} Offset Accuracy, Referenced to Input	$V_{SENSE_OFFSET_ERR}$	—	±25	±100	µV	14-bit resolution
V_{BUS} Gain Accuracy	$V_{BUS_GAIN_ERR}$	—	—	±0.4	%	Measured at ADC output, Gain = 1
SENSE+, SENSE- Pin Leakage Current	I_{SENSE+}, I_{SENSE-}	—	—	1.0	µA	V_{BUS} = 24V, V_{SENSE} = 0V Sleep state
SENSE+, SENSE- Pin Leakage Current	I_{SENSE+}, I_{SENSE-}	—	—	1.0	µA	V_{DD} = 0V
SENSE+ Pin Bias Current	I_{SENSE+_BIAS}	—	34	—	µA	V_{BUS} = 24V, V_{SENSE} = 100 mV Integrate state, Power measurement
SENSE- Pin Bias Current	I_{SENSE-_BIAS}	—	—	1.0	µA	V_{BUS} = 24V, V_{SENSE} = 0 to 100 mV Integrate state

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TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, maximum values are at T_A = -40°C to +85°C, V_{DD} = 3V to 5.5V, V_{BUS} = 0V to 32V; typical values are at T_A = +25°C, V_{DD} = 3.3V, V_{BUS} = 24V, V_{SENSE} = (SENSE+ – SENSE-) = 0V						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
DAC and OUT Amplifier Characteristics						
Output Voltage Swing	V_{OUT}	0	3.0	V_{DD}-0.15	V	3V FSR maximum equation in effect when V_{DD} falls below 3.15V
Output Gain Error	OUT_{GAIN_ERR}	—	—	±0.2	%	
Output Offset Error, Referenced to Output	OUT_{OFFSET_ERR}	—	±3	±6	mV	3V FSR
Output Settling Time	t_{SETTLE}	—	—	42	µs	Output swing from 0V to 3.0V driving up to 50 pF
Output Load	C_{OUT}	—	—	50	pF	
Output Current Drive	I_{OUT}	—	—	±3	mA	DC
OUT Short Circuit	I_{OUT_SHORT}	—	—	20	mA	Device cannot be damaged when OUT pin is short circuited to GND
OUT Power Supply Rejection Ratio, DC, Referenced to Input	OUT_{PSRR_DC}	—	69	—	dB	
Integration and Read Timing						
Time to First Communications	t_{INT_T}	—	14.25	20	ms	Time after power-up before ready to begin communications and measurement
Update Pulse	t_{UPDATE}	1.25	—	9.2	µs	$\overline{READ}$/INT pin low pulse width range to guarantee transfer of digital value to DAC and not enter Read state
Read Pulse	t_{READ}	9.8	—	—	µs	$\overline{READ}$/INT pin minimum low pulse width to guarantee entry into Read state
Read State Time for Auto-Sleep State	t_{SLEEP}	1.088	1.14	1.203	s	
Transition From Sleep State to Start of Integration Period	$t_{SLEEP_TO_INT}$	—	—	86	µs	
Transition From Read State to Start of Integration Period	$t_{READ_TO_INT}$	—	—	30	µs	

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, maximum values are at T_A = -40°C to +85°C, V_{DD} = 3V to 5.5V, V_{BUS} = 0V to 32V; typical values are at T_A = +25°C, V_{DD} = 3.3V, V_{BUS} = 24V, V_{SENSE} = (SENSE+ – SENSE-) = 0V						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Digital I/O Pins ($\overline{\text{READ}}$/INT, SMBus pins)						
Output Low Voltage	V_{OL}	—	—	0.4	V	Sinking 8 mA
Input High Voltage	V_{IH}	2.0	—	—	V	
Input Low Voltage	V_{IL}	—	—	0.8	V	
Leakage Current	I_{LEAK}	-5	—	+5	µA	Powered or unpowered, T_A < +85°C maximum

TABLE 1-2: SMBUS MODULE SPECIFICATIONS

Electrical Characteristics: Unless otherwise specified, maximum values are at T_A = -40°C to +85°C, V_{DD} = 3V to 5.5V, V_{BUS} = 0V to 32V; typical values are at T_A = +25°C, V_{DD} = 3.3V, V_{BUS} = 24V, V_{SENSE} = (SENSE+ – SENSE-) = 0V						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
SMBus Interface						
Input Capacitance	C_{IN}	—	4	10	pF	
SMBus Timing						
Clock Frequency	f_{SMB}	10	—	400	kHz	
Spike Suppression	t_{SP}	0	—	50	ns	Pulse width of spikes that must be suppressed by the input filter
Bus Free Time Stop to Start	t_{BUF}	1.3	—	—	µs	
Start Setup Time	$t_{SU:STA}$	0.6	—	—	µs	
Start Hold Time	$t_{HD:STA}$	0.6	—	—	µs	
Stop Setup Time	$t_{SU:STO}$	0.6	—	—	µs	
Data Hold Time	$t_{HD:DAT}$	0	—	—	µs	When transmitting to the master
Data Hold Time	$t_{HD:DAT}$	0.3	—	—	µs	When receiving from the master
Data Setup Time	$t_{SU:DAT}$	0.6	—	—	µs	
Clock Low Period	t_{LOW}	1.3	—	—	µs	
Clock High Period	t_{HIGH}	0.6	—	—	µs	
Clock/Data Fall Time	t_{FALL}	—	—	300	ns	Minimum = 20 + 0.1 C_{LOAD} ns
Clock/Data Rise Time	t_{RISE}	—	—	300	ns	Minimum = 20 + 0.1 C_{LOAD} ns
Capacitive Load	C_{LOAD}	—	—	400	pF	Total per bus line
Time Out	$t_{TIMEOUT}$	25	—	35	ms	Disabled by default
Idle Reset	t_{IDLE_RESET}	350	—	—	µs	Disabled by default (see **Section 5.2 "SMBus Timeout"**)

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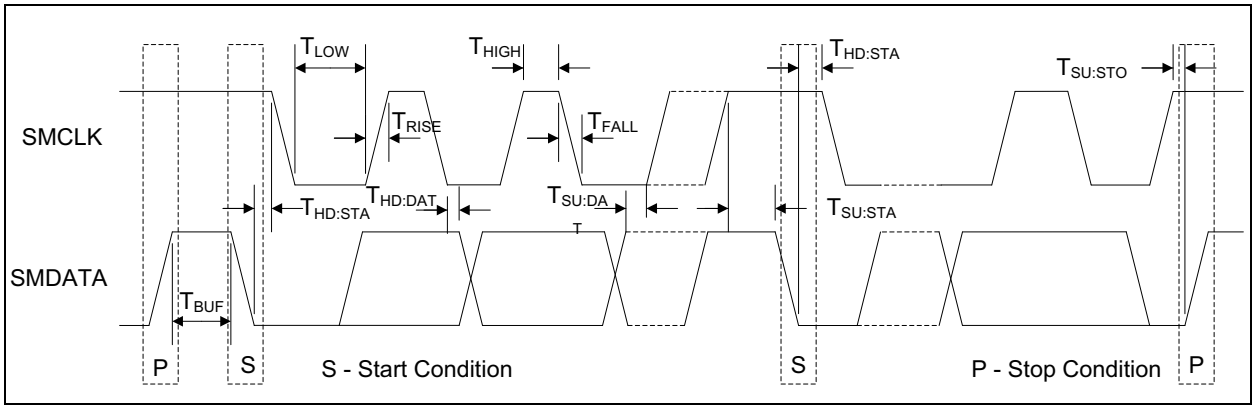

FIGURE 1-1: *SMBus Timing.*

NOTES:

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2.0 TYPICAL OPERATING CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise specified, maximum values are at T_A = -40°C to 85°C, V_{DD} = 3V to 5.5V, V_{BUS} = 0V to 32V; typical values are at T_A = 25°C, V_{DD} = 3.3V, V_{BUS} = 24V, V_{SENSE} = (SENSE+ - SENSE-) = 0V

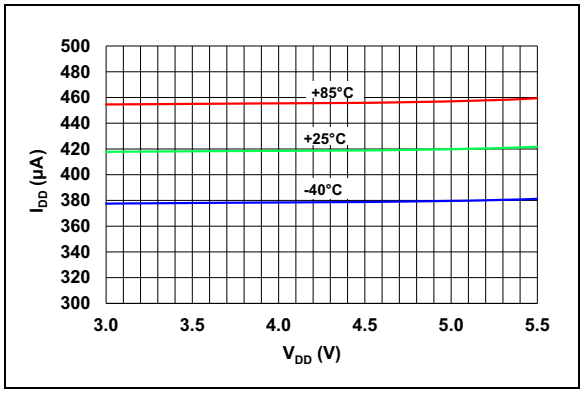

FIGURE 2-1: *Integrate State I_{DD} vs. V_{DD} (V_{BUS} = 24V, V_{SENSE} = 0V).*

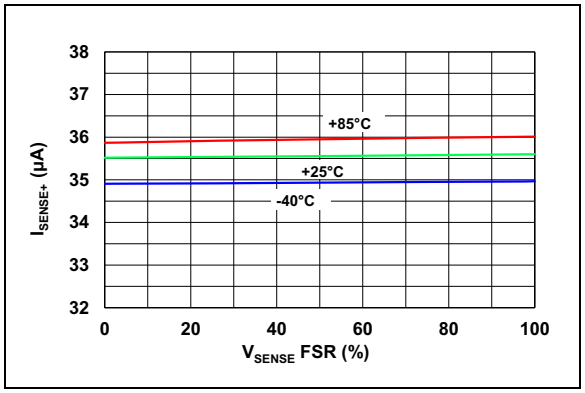

FIGURE 2-4: *I_{SENSE+} Input Current vs. V_{SENSE} - Integrate State.*

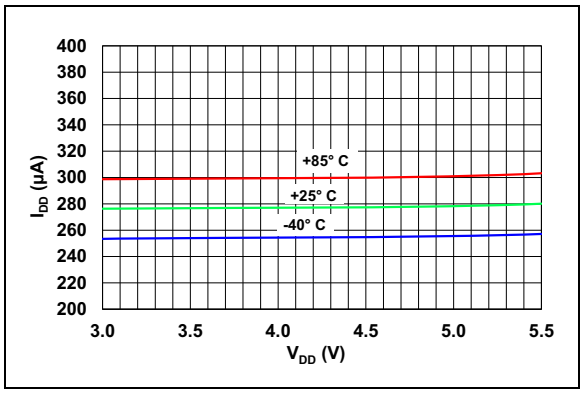

FIGURE 2-2: *Read State I_{DD} vs. V_{DD} (V_{BUS} = 24, V_{SENSE} = 0V).*

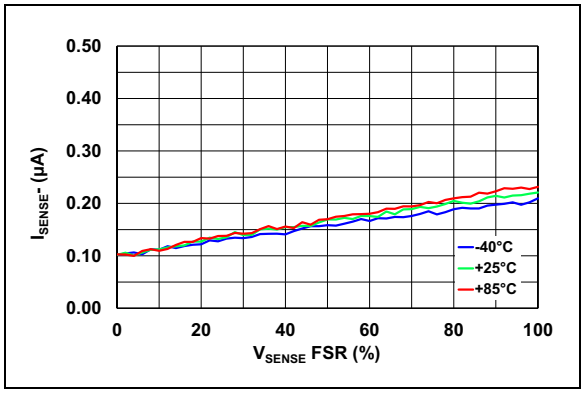

FIGURE 2-5: *I_{SENSE-} Input Current vs. V_{SENSE} - Integrate State (V_{BUS} = 24V, V_{SENSE} = 100 mV).*

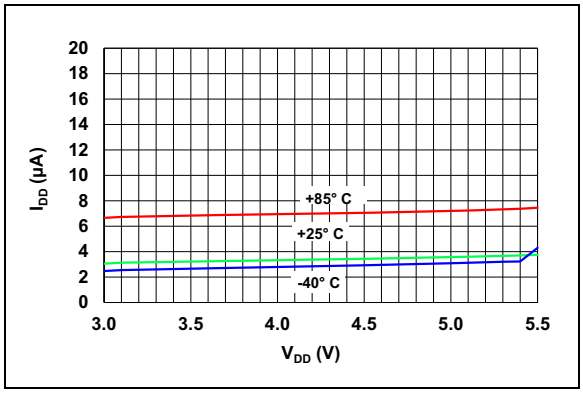

FIGURE 2-3: *Sleep State I_{DD} vs. V_{DD} (V_{BUS} = 24, V_{SENSE} = 0V).*

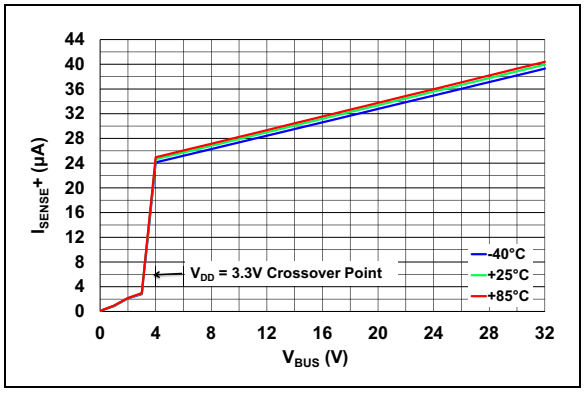

FIGURE 2-6: *I_{SENSE+} Input Current vs. Common-Mode Voltage (V_{BUS}) Integrate State (V_{DD} = 3.3V, V_{SENSE} = 100 mV).*

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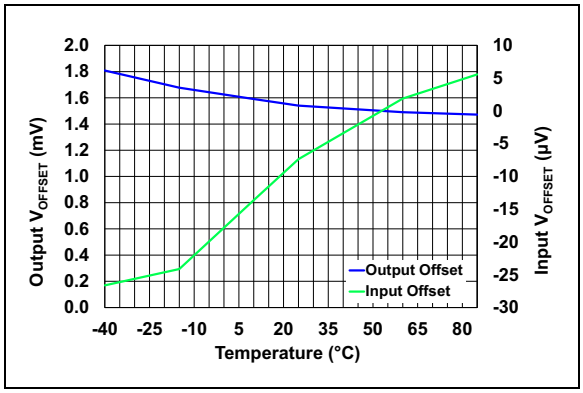

FIGURE 2-7: *Current Sense Offset vs. Temperature (V_{BUS} = 24V, V_{SENSE} = 100 mV).*

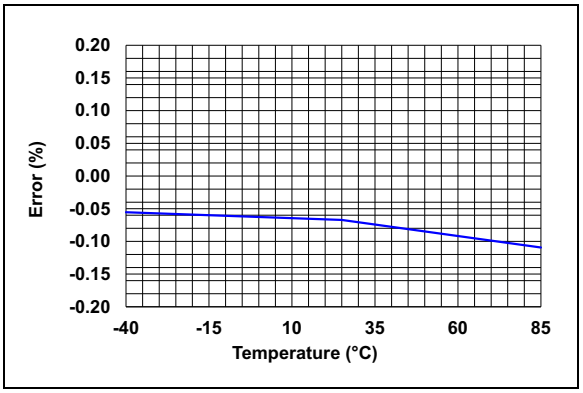

FIGURE 2-10: *Current Sense Offset vs. Temperature (V_{BUS} = 32V, V_{SENSE} = 98 mV).*

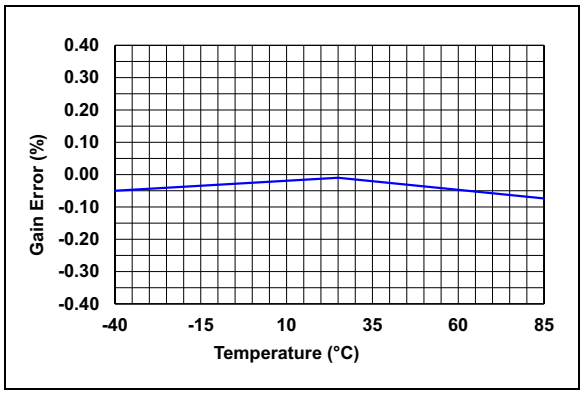

FIGURE 2-8: *Current Sense Gain Error vs. Temperature (V_{BUS} = 24V, V_{SENSE} = 98 mV).*

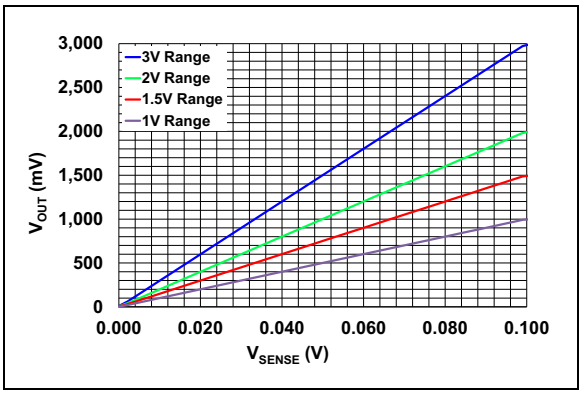

FIGURE 2-11: *V_{OUT} vs. V_{SENSE} (V_{DD} = 3.3V, V_{BUS} = 24V).*

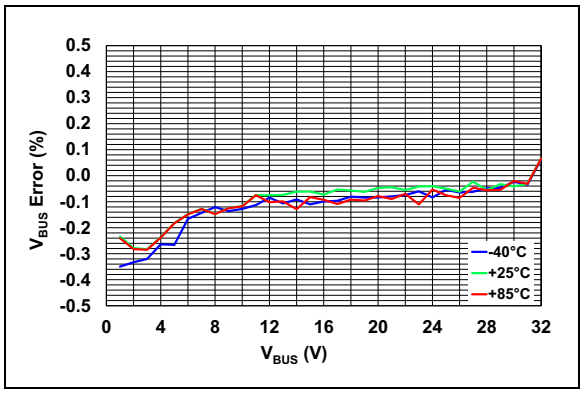

FIGURE 2-9: *V_{BUS} Voltage Measurement Accuracy vs. Temperature (V_{DD} = 3.3V, V_{SENSE} = 98 mV).*

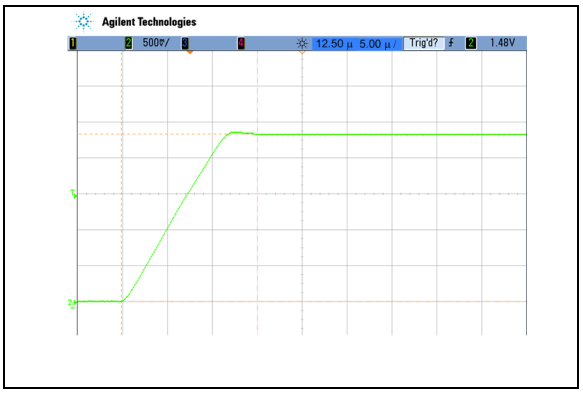

FIGURE 2-12: *DAC Setting Time.*

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN DESCRIPTION

PAC1921 3x3 VDFN	Symbol	Type (See Table 3-2)	Function
1	V_{DD}	Power	Positive Power Supply Voltage
2	SENSE+	AIO40	V_{BUS}/V_{SENSE+} input
3	SENSE–	AIO40	$V_{SENSE–}$ input
4	OUT	AIO5	Measurement Output Voltage
5	GND	Power	Ground
6	ADDR_SEL	AIO2	Selects SMBus/I^2C Address
7	RESERVED	DI (5V)	Reserved for future use. Connect to V_{DD} for SMBus functionality.
8	$\overline{\text{READ}}$/INT	DI	Controls power states
9	SM_DATA	DIOD	SM_DATA: SMBus/I^2C Data - requires pull-up resistor
10	SM_CLK	DI (5V)	SM_CLK: SMBus/I^2C Clock - requires pull-up resistor
11	EP	-	Not internally connected, but recommend grounding

TABLE 3-2: PIN TYPES DESCRIPTION

Pin Type	Description
Power	This pin is used to power to the device.
AIO40	Analog Input/Output - this pin is used as an I/O for analog signals. Maximum voltage is 40V.
AIO5	Analog Input Output - this pin is used as an I/O for analog signals. Maximum voltage is 5V.
AIO2	Analog Input/Output - this pin is used as an I/O for analog signals. Maximum voltage is 2V.
DI	Digital Input - this pin is used for digital inputs.
DIOD	Digital Input/Output Open-Drain - this pin is used for digital I/O and is open-drain.

3.1 Positive Power Supply Voltage (V_{DD})

Power supply input Voltage ranging from 3.0 to 5.5 V_{DC}.

3.2 V_{BUS}/V_{SENSE+} Input/$V_{SENSE–}$ Input (SENSE+/SENSE-)

These two pins form the differential input for measuring voltage across a sense resistor in the application. The positive input (Sense+) also acts as the input pin for bus voltage.

3.3 Measurement Output Voltage (Out)

The OUT pin provides an analog voltage based on the upper 10 bits of the latest calculation. This pin can be programmed for 1.0, 1.5, 2.0 and 3.0V output swings.

3.4 Ground (GND)

System ground.

3.5 SMBus/I^2C Address (ADDR_SEL)

Address selection for the SMBus Slave address, based on the pull-down resistor.

3.6 COMM_SEL

Reserved for future use, connect to V_{DD} for SMBus operability.

3.7 Power States ($\overline{\text{READ}}$/INT)

This pin controls the current state of the device, either in the INTEGRATE state, or in the READ state.

3.8 SMBus/I^2C Data (SM_DATA)

This is the bidirectional SMBus data pin. This pin is open-drain and requires a pull-up resistor.

3.9 SMBus/I^2C Clock (SM_CLK)

This is the SMBus clock pin. This pin is open-drain and requires a pull-up resistor.

3.10 Exposed Thermal Pad (EP)

This pad should be connected to ground for noise immunity.

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NOTES:

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4.0 GENERAL DESCRIPTION

The PAC1921 is a dedicated power monitoring device with a configurable output: Power, Current, or Voltage. The OUT pin supplies data for systems that cannot tolerate the latencies inherent in embedded communications buses. MCU-based systems equipped with ADC inputs can sample the value presented on the OUT pin for immediate use in thermal or power control algorithms. Output values are also available in a digital format via the SMBus interface. The PAC1921 contains a high-side precision current-sensing circuit and a precision bus voltage measurement circuit. The current-sensing circuit contains a differential amplifier that continuously measures the voltage (V_{SENSE}) developed across an external sense resistor to represent the high-side supply current. The full-scale range of V_{SENSE} is from 0 mV to 100 mV. For power, the current and voltage data is multiplied and accumulated, scaled with two digital gain parameters, then applied to the OUT pin through a 10-bit DAC and a gain output buffer for the output FSR.

The integration time is variable depending on the measurement type, the resolution setting (11-bit or 14-bit), the post filter settings and the number of samples. A system diagram using the PAC1921 in SMBus mode is shown in Figure 4-1.

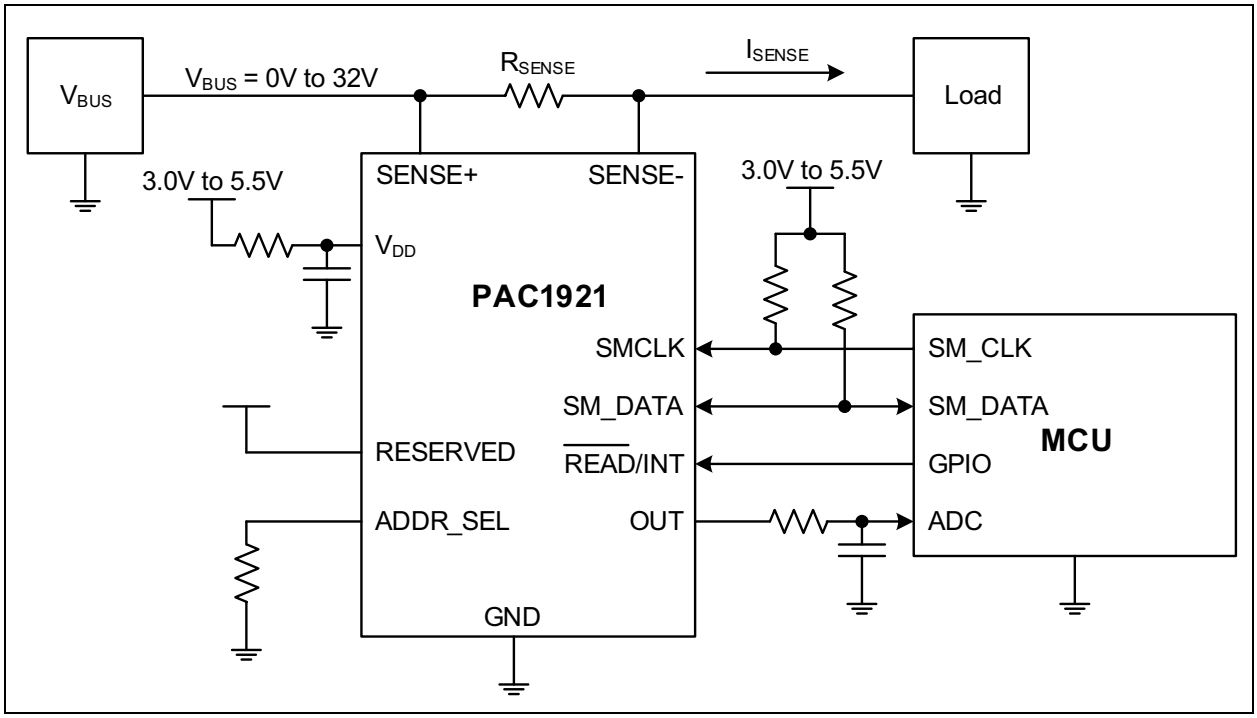


FIGURE 4-1: *PAC1921 System Diagram – SMBus Mode.*

4.1 V_{DD} Pin RC Filter

For optimal rejection of AC power supply noise, an RC filter comprised of a 100Ω resistor and a 1 µF capacitor is required on the 3.3V V_{DD} pin.

4.2 OUT Pin RC Filter

To minimize the effect of circuit noise induced on the OUT signal trace between the PAC1921 and the receiving ADC, an RC filter comprised of a 100-150Ω resistor and a 1 nF capacitor is recommended on the OUT pin. This RC filter should ideally be placed near the measurement ADC input.

4.3 Use Cases

The following examples illustrate application of the PAC1921 device. Figure 4-2 demonstrates how to synchronize the power measurement of multiple supply rails using a single GPIO to control the $\overline{\text{READ}}$/INT pins.

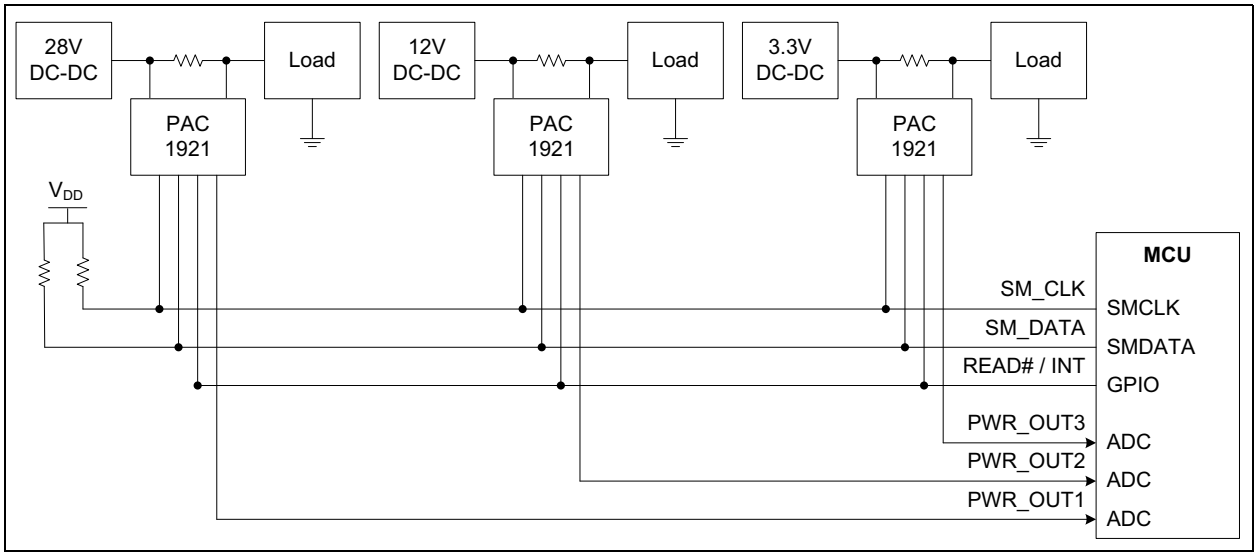
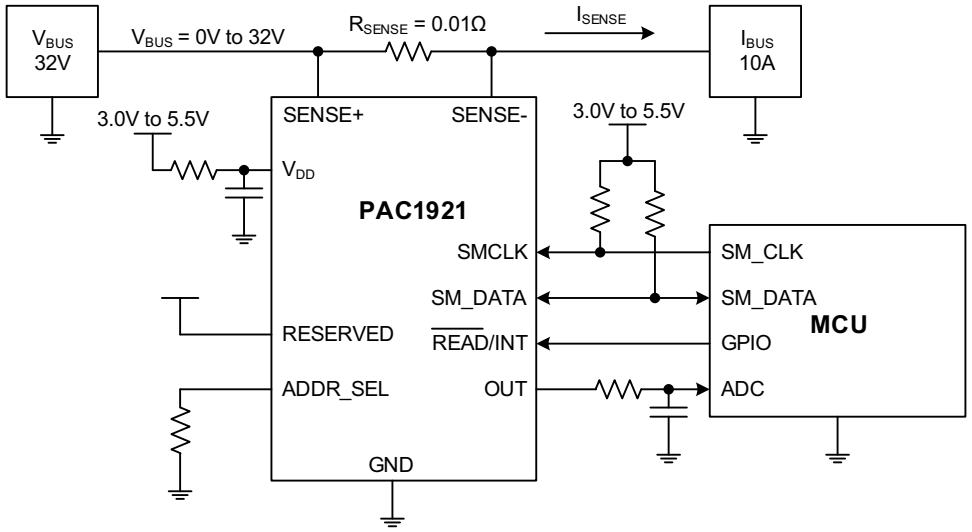


FIGURE 4-2: *Usage Model.*

Figure 4-3 shows some of the math when filling the registers with maximum values.



I_{MAX} = 10A

V_{SENSE} = 0.01Ω x 10A = 0.10V = 100 mV (max I_{LOAD})

V_{SENSE} Result Registers (12h, 13h) = FF80h

V_{MAX} = 32V

V_{BUS} = 32V (max V_{BUS})

V_{BUS} Result Registers (10h, 11h) = FF80h

Power = 10A x 32V = 320W

V_{POWER} Result Registers (1Dh, 1Eh) = FF80h (Upper 10 bits of V_{POWER} Result)

OUT Pin (3V FSR) = V_{POWER} Result 65472 x OUT Pin FSR

= FF80h/65472 x 3.0V

= 2.997V

Calculated Power using OUT pin = OUT Pin/OUT Pin FSR x I_{MAX} x V_{MAX}

= 2.997/3.0 x 10 x 32

= 319.68W

FIGURE 4-3: *Maximum Value Example.*

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Figure 4-4 illustrates dynamic operating conditions by changing the DI_GAIN value.

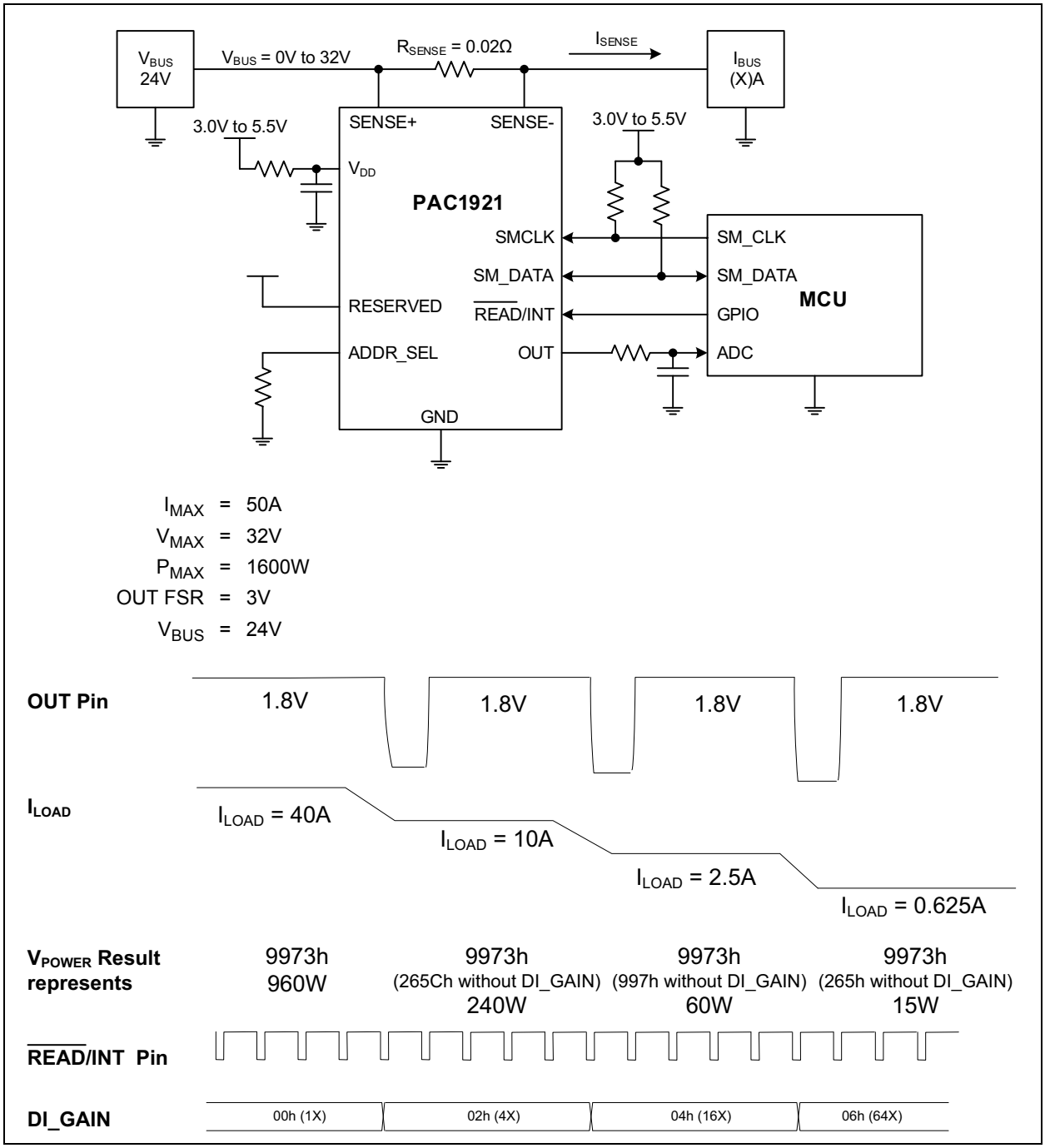

FIGURE 4-4: *DI_GAIN Effects on OUT Voltage.*

In this example, the load current decreases from 40A to less than 1A over time. The user is notified of a change through the change in the OUT voltage. The DI_GAIN value is then adjusted to center the measurements again. In this example, the changes in current were factors of four apart. Using the DI_GAIN parameter to adjust the Full Scale value, the analog output maintains good resolution throughout the entire range.

4.4 Power States

The PAC1921 has three power states, as described in the following paragraphs.

4.4.1 INTEGRATE STATE

In the Integrate state, the device is fully active and integrating in one of two modes: pin-controlled or free-run (see **Section 4.7 "Integration"**). When the $\overline{\text{READ}}$/INT pin is driven high, the device is in the Integrate state. Alternatively, when using SMBus, the device can be placed in the Integrate state by enabling the pin override (READ/INT_OVR = 1) and setting the INT_EN bit to '1'.

4.4.2 READ STATE

The Read state is a lower-power state. When the $\overline{\text{READ}}$/INT pin is driven low for at least t_{READ} time (see **Section 1.0 "Electrical Characteristics"**), the device is in the Read state. When using SMBus, the device can also be placed in the Read state by enabling the pin override (READ/INT_OVR = 1) and setting the INT_EN bit to '0'. The Read state terminates integration, starts the internal sleep timer, transfers the selected measurement to the output DAC, and places the device in a low-power state. The OUT pin will output the latest measurement voltage in the voltage range defined by V_{OUT} until the next time the device enters the Read state (next falling edge of $\overline{\text{READ}}$/INT, or INT_EN set to '1' and then back to '0') or until the sleep timer expires and the device enters the Sleep state.

4.4.3 SLEEP STATE

The Sleep state is the lowest-power state. While in this state, the device will draw a supply current of I_{SLEEP} from the V_{DD} pin. By default, the device enters the Sleep state automatically when the $\overline{\text{READ}}$/INT pin (or INT_EN bit if READ/INT_OVR = 1) is held low for longer than t_{SLEEP}. In SMBus mode, the device can also be put in the Sleep state by setting the SLEEP bit (see Register 6-3). When entering the Sleep state, the device will reset all measurement registers and turn off unnecessary internal biasing and drive circuits to reduce quiescent current to I_{SLEEP}. The device will stay in the Sleep state until it is placed in the Integrate state. The device will transition from Sleep to the start of integration in $t_{SLEEP_TO_INT}$ and start accumulating current and voltage information again. An example of the timing required to enter the Sleep state is shown in Figure 4-5.

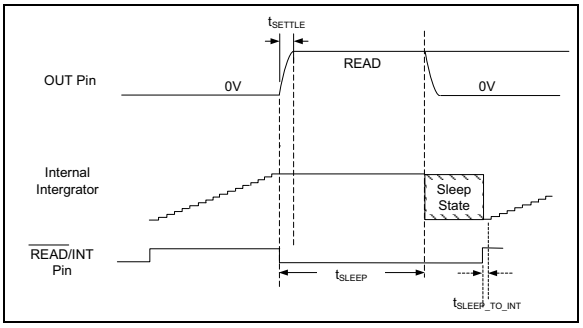

FIGURE 4-5: *Sleep State Timing.*

4.5 Measurement Modes

The PAC1921 can measure the source-side voltage, V_{BUS}, and the voltage across an external current sense resistor, V_{SENSE}. The device can be configured to perform one of three sets of calculations: Power (see **Section 4.5.1 "Power Measurement"**), V_{SENSE} (see **Section 4.5.2 "V_{SENSE} Measurement"**) or V_{BUS} (see **Section 4.5.3 "V_{BUS} Measurement"**). The results of these digital calculations are applied to the analog OUT pin as well as stored in registers available via the communications bus. Figure 4-6 shows the data flow.

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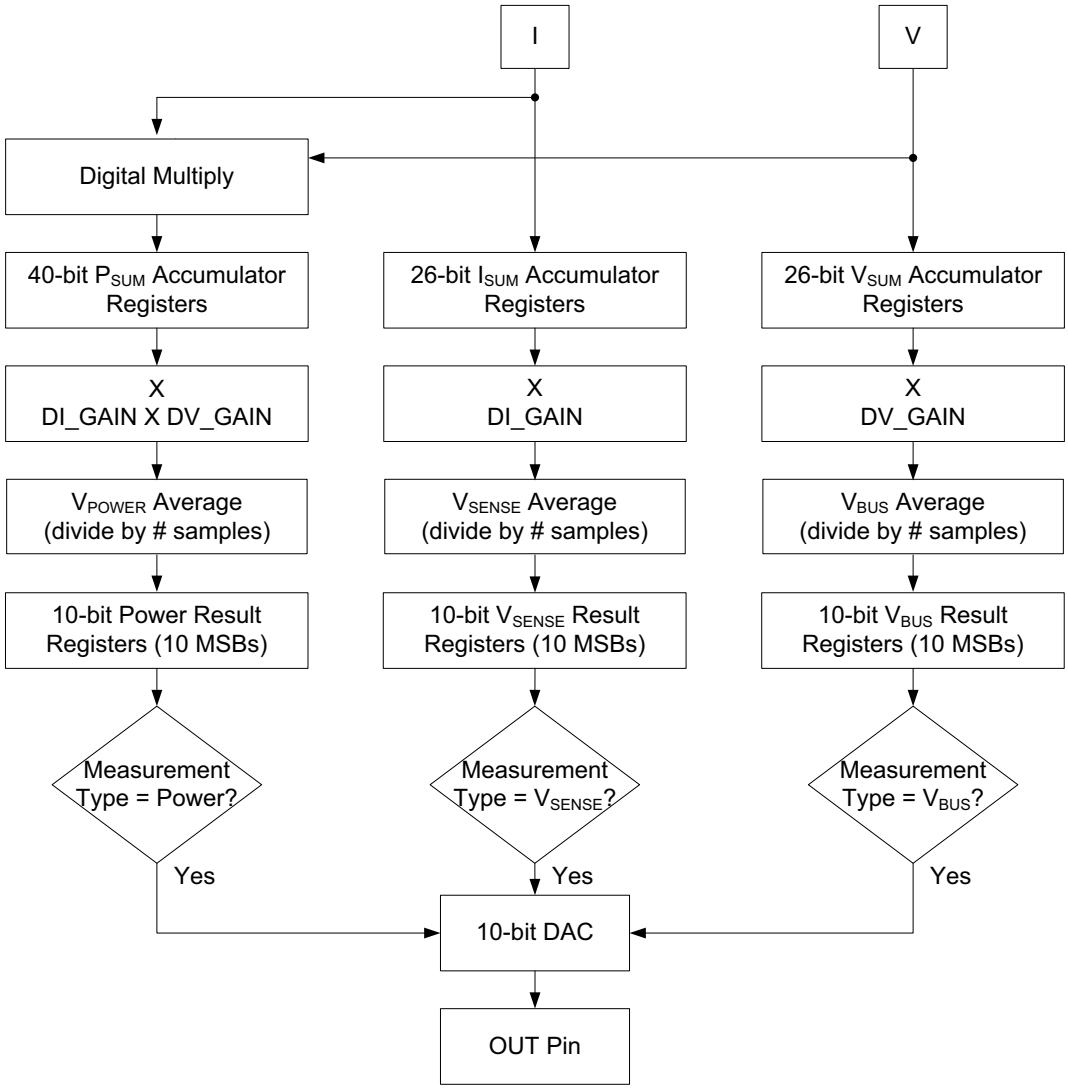

Note: Registers not required for the selected measurement type are not populated.

FIGURE 4-6: *PAC1921 Data Flow.*

4.5.1 POWER MEASUREMENT

V_{BUS} and V_{SENSE} are sampled and multiplied during the integration period, resulting in the sum of power for all samples. The power full-scale range is defined in Equation 4-1. The instantaneous values are summed over the integration period. The summed value is then divided by the number of samples, and stored in the V_{POWER} Results registers.

The V_{POWER} Results registers result can be converted directly to watts using the conversion described in Equation 4-2 for 1 LSB. This result is also sent to the DAC which drives the proportional voltage output on the OUT pin, if it is the selected output.

EQUATION 4-1: POWER FSR CALCULATION

$$PowerFSR = \left(\frac{(0.1V)/R\Omega}{DI_GAIN}\right) \times \left(\frac{32V}{DV_GAIN}\right)$$

Where:

0.1V	=	Maximum V_{SENSE} voltage input
RΩ	=	R_{SENSE} resistor value
DI_GAIN	=	Digital current gain
32V	=	Maximum device bus voltage input
DV_GAIN	=	Digital voltage gain

EQUATION 4-2: POWER LSB WEIGHT

$$1_{LSB} = \frac{\frac{0.1V}{R\Omega \times DI_GAIN} \times \frac{32V}{DV_GAIN}}{1023 \times 2^6}$$

Where:

0.1V	=	Maximum V_{SENSE} voltage input
RΩ	=	R_{SENSE} resistor value
DI_GAIN	=	Digital current gain
32V/DV_GAIN	=	Maximum device bus voltage input
DV_GAIN	=	Digital voltage gain

4.5.2 V_{SENSE} MEASUREMENT

When V_{SENSE} is selected as the measurement type, free-run integration is used (see **Section 4.7.3 "Free-Run Integration"**). The V_{SENSE} voltage is digitized and summed in the I_{SUM} Accumulator Registers. The average is then taken at the end of the integration period. Finally, digital gain is applied by adjusting the parameter DI_GAIN. The upper 10-bit resultant value represents the average V_{SENSE} voltage measured and is used to drive the DAC. The PAC1921 should be kept in the Integrate state for continuous output in this mode. The value of one LSB in amps can be calculated according to Equation 4-3.

EQUATION 4-3: V_{SENSE} LSB VALUE IN AMPS

$$1_{LSB} = \frac{\frac{0.1V}{R\Omega \times DI_GAIN}}{1023 \times 2^6}$$

Where:

0.1V	=	Maximum V_{SENSE} voltage input
RΩ	=	R_{SENSE} resistor value
DI_GAIN	=	Digital current gain
1023 x 2^6	=	FSR x scale offset

The value of one LSB in volts can be calculated according to Equation 4-4.

EQUATION 4-4: V_{SENSE} LSB VALUE IN VOLTS

$$1_{LSB} = \frac{\frac{0.1V}{DI_GAIN}}{1023 \times 2^6}$$

Where:

0.1V	=	Maximum V_{SENSE} voltage input
DI_GAIN	=	Digital current gain
1023 x 2^6	=	FSR x scale offset

4.5.3 V_{BUS} MEASUREMENT

When V_{BUS} is selected as the measurement type, free-run integration is used (see **Section 4.7.3 "Free-Run Integration"**). The V_{BUS} voltage is digitized and summed in the V_{SUM} Accumulator Registers. The average is taken at the end of the integration period and digital gain is applied by adjusting the parameter DV_GAIN. The upper 10-bit resultant value represents the average V_{BUS} voltage measured and is used to drive the DAC. The PAC1921 should be kept in the Integrate state for continuous output in this mode. The value of one LSB in volts can be calculated according to Equation 4-5.

EQUATION 4-5: V_{BUS} LSB VALUE IN VOLTS

$$1_{LSB} = \frac{\frac{32V}{DV_GAIN}}{1023 \times 2^6}$$

Where:

1LSB	=	LSB value in volts
32/DV_GAIN	=	Maximum voltage
1023 x 2^6	=	FSR shifted 6 bits

4.6 OUT Pin and Measurement Type

The OUT pin is driven by a buffered 10-bit DAC. The OUT pin signal is typically sent to an MCU with ADC inputs to supply data for algorithms that cannot tolerate the latencies inherent in embedded communications buses. After a DAC update, the OUT pin can be polled after t_{SETTLE}. The output voltage can also be expressed as a result of the DAC, as shown in Equation 4-6.

EQUATION 4-6: OUT PIN VALUE

$$OUT = \frac{DAC}{1023 \times 2^6} \times OUTFSR$$

Where:

OUT	=	Output on OUT pin
DAC	=	value of the selected measurement result registers
1023 x 2^6	=	FSR x scale offset
OUTFSR	=	Output FSR

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The OUT Pin can represent Power, Voltage or Current. This measurement type is selected by the MXSL[1:0] bits shown in Table 4-1.

TABLE 4-1: MUX_SEL MULTIPLEXER DECODE

MXSL[1:0]		Selected Output
1	0	
0	0	V_{POWER} pin-controlled (default)
0	1	V_{SENSE} free-run
1	0	V_{BUS} free-run
1	1	V_{POWER} free-run

To change the MUX_SEL parameter, see **Section 4.7.8 "Changing Integration Parameter Settings"**.

The OUT buffer FSR is configurable. The OUT FSR is set by the OFSR[1:0] bits in Control Register 02h, as shown in Table 4-2.

TABLE 4-2: OFSR DECODE - SMBUS MODE

OFSR[1:0]		FSR for OUT Pin
1	0	
0	0	0 to 3V (default)
0	1	0 to 2V
1	0	0 to 1.5V
1	1	0 to 1V

4.7 Integration

The PAC1921 has two Integrate state (see **Section 4.4.1 "Integrate State"**) operating modes: pin-controlled and free-run. In pin-controlled mode, the measurement type is Power. In free-run mode, the measurement type is Power by default and can be changed in SMBus mode to Voltage or Current.

If pin-controlled integration mode is selected, the OUT pin will update to the latest Power value when the PAC1921 is placed in the Read state or when the $\overline{\text{READ}}$/INT pin is held low for t_{UPDATE}. If free-run is chosen, the OUT pin will update at the conclusion of each integration period. The integration mode is selected by the MXSL[1:0] bits (see Table 4-1).

TABLE 4-3: INT_SEL PIN DECODE

INT_SEL Pin Voltage	Integration Mode
GND	Pin-controlled
V_{DD}	Free-run

4.7.1 PIN-CONTROLLED INTEGRATION

In pin-controlled integration mode, the integration period is the time the PAC1921 is in the Integrate state less the state transition time, as shown in Figure 4-7. The power integration period can be any time between ~0.9 ms and ~1s with 11-bit resolution and between ~2.7 ms and ~2.9s with 14-bit resolution. When the PAC1921 is placed in the Read state, measurement is stopped, calculations are made, and the result is latched into the DAC.

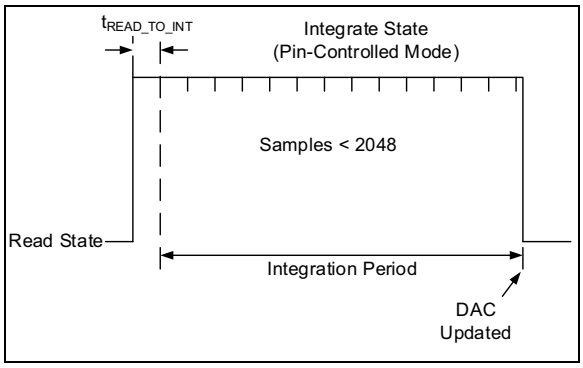

***FIGURE 4-7:** Pin-Controlled Integration Period.*

To obtain an update to the DAC without entering the Read state, the $\overline{\text{READ}}$/INT pin can be held low for t_{UPDATE}. This eliminates the $t_{READ_TO_INT}$ delay at the start of the next integration period which occurs when transitioning from Read to Integrate, as shown in Figure 4-8.

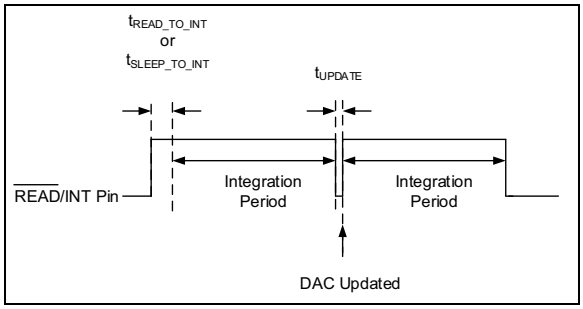

***FIGURE 4-8:** Pin-Controlled Measurement Time.*

4.7.2 MAXIMUM SAMPLES

The number of samples is limited to 2048. When the Samples Registers reach their maximum value (2048), integration stops, the calculations are performed, the registers are updated and the results are sent to the OUT pin.

4.7.3 FREE-RUN INTEGRATION

In free-run integration mode, the integration period is controlled by the selected measurement type, resolution, filtering, and number of samples (see **Section 4.7.4 "ADC Resolution, Filtering and Sampling"**). The number of samples is controlled by the SMPL bits in the configuration register. The legend for these bits is shown in Table 4-4.

TABLE 4-4: SAMPLES IN FREE-RUN MODE

SMPL[3:0]				Number of Samples
3	2	1	0	
0	0	0	0	1 (default)
0	0	0	1	2
0	0	1	0	4
0	0	1	1	8
0	1	0	0	16
0	1	0	1	32
0	1	1	0	64
0	1	1	1	128
1	0	0	0	256
1	0	0	1	512
1	0	1	0	1024
1	0	1	1	2048
1	1	0	0	2048
1	1	0	1	2048
1	1	1	0	2048
1	1	1	1	2048

After each integration period is completed, the output value is calculated and the result is latched into the DAC. As long as the device is still in the Integrate state, the next integration period starts after the calculations are complete. Integration is disabled whenever the device enters the Read state.

When the device enters the Read state during an integration period, that data is discarded, as shown in Figure 4-9.

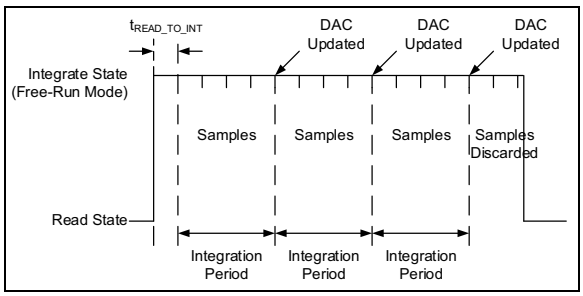

FIGURE 4-9: *Incomplete Integration Time.*

4.7.4 ADC RESOLUTION, FILTERING AND SAMPLING

ADC resolution can be specified at 11 or 14 bits. In SMBus mode, the resolution is set independently for V_{SENSE} and V_{BUS} by using the I_RES and V_RES bits (see Register 6-1).

ADC post filtering improves signal quality and increases conversion time by 50%. In SMBus mode, ADC post filtering can be enabled or disabled by using the VSFEN and VBFEN bits (see Register 6-2).

When Power is selected as the OUT measurement type, the bus voltage and sense resistor voltage are sampled an equal number of times during the integration period in a round-robin scheme (e.g., a V_{BUS} measurement is taken and then a V_{SENSE} measurement is taken for each power sample). When V_{BUS} or V_{SENSE} is selected as the OUT measurement type, only the selected channel is sampled and digitized.

In free-run integration, the number of samples is selectable. In free-run SMBus mode, the number of samples is set by the SMPL[3:0] bits (see Register 6-2).

The free-run integration period is determined by the selected measurement type, number of samples, resolution and filtering as shown in Table 4-5.

11-bit resolution is recommended if the fastest integration time is required. 14-bit resolution will provide more accurate and highly averaged measurements.

TABLE 4-5: FREE RUN INTEGRATION PERIODS

Samples	Integration Period Power measurement			Integration Period V_{SENSE} or V_{BUS} Measurement	
	14-bit ADC Post Filter On	11-Bit ADC Post Filter Off	Mixed ADC Post Filter On	14-bit ADC Post Filters On	11-Bit ADC Post Filters Off
1	2.72 ms	0.93 ms	2.1 ms	1.41 ms	0.51 ms
2	4.05 ms	1.46 ms	3.1 ms	2.02 ms	0.72 ms
4	6.79 ms	2.41 ms	5.1 ms	3.43 ms	1.24 ms
8	12.2 ms	4.32 ms	9.2 ms	6.06 ms	2.08 ms
16	23 ms	8.05 ms	17.5 ms	11.5 ms	3.95 ms
32	46 ms	16.1 ms	34.9 ms	22.9 ms	7.89 ms
64	92 ms	32.1 ms	70 ms	45.7 ms	15.7 ms
128	184 ms	64.2 ms	139 ms	91.3 ms	31.4 ms
256	368 ms	128.3 ms	278 ms	183 ms	62.7 ms
512	736 ms	257 ms	556 ms	365 ms	126 ms
1024	1471 ms	513 ms	1112 ms	730 ms	251 ms
2048	2941ms	1026 ms	2223 ms	1460 ms	502 ms

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4.7.5 DI_GAIN SETTING

The DI_GAIN parameter acts as a digital multiplier to control the effective current gain, as described in Equation 4-3. DI_GAIN 1X is the setting for the full-scale range. DI_GAIN can be increased when the system is designed for a lower V_{SENSE} range. It can also be used to provide a larger signal when the system is in a low-power mode.

TABLE 4-6: DI_GAIN DECODE

DI_GAIN[2:0]			DI_GAIN Multiplier	Effective V_{SENSE} Range
2	1	0		
0	0	0	1X (default)	0 to 100 mV (default)
0	0	1	2X	0 to 50 mV
0	1	0	4X	0 to 25 mV
0	1	1	8X	0 to 12.5 mV
1	0	0	16X	0 to 6.25 mV
1	0	1	32X	0 to 3.125 mV
1	1	0	64X	0 to 1.56 mV
1	1	1	128X	0 to 0.78 mV

DI_GAIN is set in the Gain Configuration Register (see Register 6-1) based on Table 4-6.

4.7.6 DI_GAIN OVERFLOW

If DI_GAIN is set too high for the input magnitude when V_{SENSE} or V_{POWER} is selected as the measurement type, it will cause an overflow in the results registers (P_{SUM_GAINED} and I_{AVG}). To provide an indication that the selected gain is too high, the following occurs:

Overflow status register 1Ch bit 2 (VSOV) is set to 1b and bit 0 (VPOV) is set to 1b if the power calculation overflowed, too.

V_{SENSE} Result Registers are set to the maximum value (12h is set to FFh and 13h is set to C0h).

V_{POWER} Result Registers are set to the maximum value (1Dh is set to FFh and 1Eh is set to C0h).

The values in the I_{SUM} Accumulator Registers and P_{SUM} Accumulator Registers will be accurate. In SMBus mode, change the DI_GAIN selection (see Register 6-1), set the RDAC bit (see Register 6-3) and check the results until an effective current gain is selected.

4.7.7 DV_GAIN SETTING

The DV_GAIN parameter acts as a digital multiplier to control the effective bus voltage gain. DV_GAIN 1X is the setting for the full-scale voltage range. DV_GAIN can be increased when the system is designed for a lower V_{BUS} range. It can also be used to provide a larger signal when the system is in a low-power mode.

TABLE 4-7: DV_GAIN DECODE

DV_GAIN[2:0]			DV_GAIN Multiplier	Effective V_{BUS} Range
2	1	0		
0	0	0	1X (default)	0 to 32V (default)
0	0	1	2X	0 to 16V
0	1	0	4X	0 to 8V
0	1	1	8X	0 to 4V
1	0	0	16X	0 to 2V
1	0	1	32X	0 to 1V
1	1	0	32X	0 to 1V
1	1	1	32X	0 to 1V

DV_GAIN is set in the Gain Configuration Register (see Register 6-1) as shown in Table 4-7.

4.7.7.1 DV_GAIN Overflow

If DV_GAIN is too high for the range being measured when V_{BUS} or V_{POWER} is selected as the measurement type, it will cause an overflow in the results registers. To provide an indication that the selected gain is too high, the following occurs:

Overflow status register 1Ch bit 1 (VBOV) is set to 1b and bit 0 (VPOV) is set to 1b if the power calculation overflowed, too.

V_{BUS} Result Register 10h is set to FFh and V_{BUS} Result Register 11h is set to C0h.

V_{POWER} Result Register 1Dh is set to FFh and V_{POWER} Result Register 1Eh is set to C0h.

The values in the V_{SUM} Accumulator Registers and P_{SUM} Accumulator Registers will be accurate. In SMBus mode, change the DV_GAIN selection in Register 6-1 to match the range of the bus being measured. Set the RDAC bit in the same register and check the results.

4.7.8 CHANGING INTEGRATION PARAMETER SETTINGS

The integration parameter settings I_RES, V_RES, SMPL, VSFEN and VBFEN can be changed by first putting the device in the Read state (see **Section 4.4 "Power States"**), then changing the applicable registers. If one of these parameters is changed while the device is in the Integrate state, the change will not take effect until after the device has been placed into the Read state and then back into the Integrate state. DI_GAIN and DV_GAIN can also be updated in the Read state; however, the effects can be seen while in Read by setting the RDAC bit to recalculate the last measurement using the new gain settings.

If the integration mode is changed from V_{POWER} pin-controlled while the device is in the Integrate state, the device will terminate the Power measurement, update the OUT pin and then switch to the new measurement/integration mode. If the integration mode is changed from V_{POWER} free-run, V_{SENSE} or V_{BUS} while the device is in the Integrate state, the device will complete the integration period, update the OUT pin and then switch to the new measurement/integration mode.

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5.0 COMMUNICATIONS PROTOCOL

The PAC1921 communicates with a host controller, such as an PIC MCU, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 1-1.

For the first 15 ms after power-up, the device may not respond to SMBus communications.

5.1 SMBus Control Bits

The interaction between clock and data creates special function bits within the data stream.

5.1.1 SMBUS START BIT

The SMBus Start bit is defined as a transition of the SMBus Data line from a logic '1' state to a logic '0' state while the SMBus Clock line is in a logic '1' state.

5.1.2 SMBUS ADDRESS AND RD/$\overline{WR}$ BIT

The SMBus Address Byte consists of the 7-bit client address followed by the RD/$\overline{WR}$ indicator bit. If this RD/$\overline{WR}$ bit is a logic '0', the SMBus Host is writing data to the client device. If this RD/$\overline{WR}$ bit is a logic '1', the SMBus Host is reading data from the client device. The PAC1921 SMBus address is determined by a single pull-down resistor connected between ground and the ADDR_SEL pin as shown in Table 5-1.

TABLE 5-1: ADDR_SEL RESISTOR SETTING

Resistor (5%)	SMBus Address
0	1001_100(r/w)
120	1001_101(r/w)
220	1001_110(r/w)
330	1001_111(r/w)
470	1001_000(r/w)
620	1001_001(r/w)
820	1001_010(r/w)
1000	1001_011(r/w)
1300	0101_000(r/w)
1800	0101_001(r/w)
2200	0101_010(r/w)
3000	0101_011(r/w)
4300	0101_100(r/w)
6800	0101_101(r/w)
12000	0101_110(r/w)
open	0011_000((r/w)

5.1.3 SMBUS DATA BYTES

All SMBus Data bytes are sent most significant bit first and composed of eight bits of information.

5.1.4 SMBUS ACK AND NACK BITS

The SMBus client will acknowledge all data bytes that it receives. This is done by the client device pulling the SMBus data line low after the 8th bit of each byte that is transmitted.

The host will NACK (not acknowledge) the last data byte to be received from the client by holding the SMBus data line high after the 8th data bit has been sent.

5.1.5 SMBUS STOP BIT

The SMBus Stop bit is defined as a transition of the SMBus Data line from a logic '0' state to a logic '1' state while the SMBus clock line is in a logic '1' state. When the device detects an SMBus Stop bit and it has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

5.2 SMBus Timeout

The PAC1921 supports SMBus Timeout. If the clock line is held low for longer than $t_{TIMEOUT}$, the device will reset its SMBus protocol. This function can be enabled by setting the TIMEOUT bit (see Register 6-3).

5.3 SMBus and I²C Compatibility

The PAC1921 is compatible with SMBus and I²C. The major differences between SMBus and I²C devices are highlighted here. For more information, refer to the SMBus 2.0 and I²C specifications. For information on using the PAC1921 in an I²C system, refer to AN 14.0 – *"Microchip Dedicated Slave Devices in I²C Systems"* (DS00001853).

- PAC1921 supports I²C fast mode at 400 kHz. This covers the SMBus max time of 100 kHz.
- Minimum frequency for SMBus communications is 10 kHz.
- The SMBus client protocol will reset if the clock is held at a logic '0' for longer than 30 ms. This time-out functionality is disabled by default in the PAC1921 and can be enabled by writing to the TIMEOUT bit. I²C does not have a time out.
- I²C devices do not support the Alert Response Address functionality (which is optional for SMBus).
- I²C devices support Block Read and Block Write differently. I²C protocol allows for an unlimited number of bytes to be sent in either direction. The SMBus protocol requires that an additional data byte indicating number of bytes to read/write is transmitted. The PAC1921 supports I²C formatting only.

Attempting to communicate with the PAC1921 SMBus interface with an invalid slave address or invalid protocol will result in no response from the device and will not affect its register contents. Stretching of the SMCLK signal is supported, provided other devices on the SMBus control the timing.

5.4 SMBus Protocols

The device supports Send Byte, Read Byte, Write Byte, Receive Byte, and the Alert Response Address as valid protocols as shown below.

All of the below protocols use the convention in Table 5-2.

TABLE 5-2: PROTOCOL FORMAT

Data Sent to Device	Data Sent to the Host
# of bits sent	# of bits sent

5.4.1 WRITE BYTE

The Write Byte is used to write one byte of data to the registers, as shown in Table 5-3.

TABLE 5-3: WRITE BYTE PROTOCOL

START	Slave Address	WR	ACK	Register Address	ACK	Register Data	ACK	STOP
1 → 0	YYYY_YYY	0	0	XXh	0	XXh	0	0 → 1

5.4.2 READ BYTE

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 5-4.

TABLE 5-4: READ BYTE PROTOCOL

START	Slave Address	WR	ACK	Register Address	ACK	START	Slave Address	RD	ACK	Register Data	NACK	STOP
1→ 0	YYYY_YYY	0	0	XXh	0	1 → 0	YYYY_YYY	1	0	XXh	1	0 → 1

5.4.3 SEND BYTE

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 5-5.

TABLE 5-5: SEND BYTE PROTOCOL

START	Slave Address	WR	ACK	Register Address	ACK	STOP
1 → 0	YYYY_YYY	0	0	XXh	0	0 → 1

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5.4.4 RECEIVE BYTE

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 5-6.

TABLE 5-6: RECEIVE BYTE PROTOCOL

START	Slave Address	RD	ACK	Register Data	NACK	STOP
1 → 0	YYYY_YYY	1	0	XXh	1	0 → 1

5.5 I²C Protocols

The PAC1921 supports I²C Block Read and Block Write.

The protocols listed below use the convention in Table 5-2.

5.5.1 BLOCK WRITE

The Block Write protocol is used to write multiple data bytes to a group of contiguous registers, as shown in Table 5-7.

TABLE 5-7: BLOCK WRITE PROTOCOL

START	Slave Address	WR	ACK	Register Address	ACK	Register Data	ACK
1 → 0	YYYY_YYY	0	0	XXh	0	XXh	0
Register Data	**ACK**	**Register Data**	**ACK**		**Register Data**	**ACK**	**STOP**
XXh	0	XXh	0		XXh	0	0 → 1

5.5.2 BLOCK READ

The Block Read protocol is used to read multiple data bytes from a group of contiguous registers, as shown in Table 5-8.

TABLE 5-8: BLOCK READ PROTOCOL

START	Slave Address	WR	ACK	Register Address	ACK	START	Slave Address	RD	ACK	Register Data
1 → 0	YYYY_YYY	0	0	XXh	0	1 → 0	YYYY_YYY	1	0	XXh
ACK	**Register Data**	**ACK**	**Register Data**	**ACK**	**Register Data**	**ACK**		**Register Data**	**NACK**	**STOP**
0	XXh	0	XXh		0	0		XXh	1	0 → 1

NOTES:

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6.0 REGISTER DESCRIPTION

The registers shown in Table 6-1 are accessible through the SMBus. In the individual register tables that follow, an entry of '—' indicates that the bit is not used and will always read '0'.

TABLE 6-1: REGISTER SET IN HEXADECIMAL ORDER

Register Address	Register Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	Default Value
00h	Gain Configuration	I_RES	V_RES	DIGN2	DIGN1	DIGN0	DVGN2	DVGN1	DVGN0	00h
01h	Integration Configuration	SMPL3	SMPL2	SMPL1	SMPL0	VSFEN	VBFEN	RIOV	INTEN	0Ch
02h	Control	MXSL1	MXSL0	OFSR1	OFSR0	TOUT	SLEEP	SLPOV	RDAC	00h
10h	V_{BUS} Result High Byte	VBR9	VBR8	VBR7	VBR6	VBR5	VBR4	VBR3	VBR2	00h
11h	V_{BUS} Result Low Byte	VBR1	VBR0	—	—	—	—	—	—	00h
12h	V_{SENSE} Result High Byte	VSR9	VSR8	VSR7	VSR6	VSR5	VSR4	VSR3	VSR2	00h
13h	V_{SENSE} Result Low Byte	VSR1	VSR0	—	—	—	—	—	—	00h
14h	V_{SUM} Accumulator High Byte	VSM24	VSM23	VSM22	VSM21	VSM20	VSM19	VSM18	VSM17	00h
15h	V_{SUM} Accumulator Middle High Byte	VSM16	VSM15	VSM14	VSM13	VSM12	VSM11	VSM10	VSM9	00h
16h	V_{SUM} Accumulator Middle Low Byte	VSM8	VSM7	VSM6	VSM5	VSM4	VSM3	VSM2	VSM1	00h
17h	V_{SUM} Accumulator Low Byte	VSM0	—	—	—	—	—	—	—	00h
18h	I_{SUM} Accumulator High Byte	ISM24	ISM23	ISM22	ISM21	ISM20	ISM19	ISM18	ISM17	00h
19h	I_{SUM} Accumulator Mid-high Byte	ISM16	ISM15	ISM14	ISM13	ISM12	ISM11	ISM10	ISM9	00h
1Ah	I_{SUM} Accumulator Mid-low Byte	ISM8	ISM7	ISM6	ISM5	ISM4	ISM3	ISM2	ISM1	00h
1Bh	I_{SUM} Accumulator Low Byte	ISM0	—	—	—	—	—	—	—	00h
1Ch	Overflow Status	—	—	—	—	—	VSOV	VBOV	VPOV	00h
1Dh	V_{POWER} Result High Byte	VPR9	VPR8	VPR7	VPR6	VPR5	VPR4	VPR3	VPR2	00h
1Eh	V_{POWER} Result Low Byte	VPR1	VPR0	—	—	—	—	—	—	00h
21h	Samples High Byte	SMP11	SMP10	SMP9	SMP8	SMP7	SMP6	SMP5	SMP4	00h
22h	Samples Low Byte	SMP3	SMP2	SMP1	SMP0	—	—	—	—	00h
23h	P_{SUM} Accumulator High Byte	PSM38	PSM37	PSM36	PSM35	PSM34	PSM33	PSM32	PSM31	00h
24h	P_{SUM} Accumulator Middle-High Byte	PSM30	PSM29	PSM28	PSM27	PSM26	PSM25	PSM24	PSM23	00h

TABLE 6-1: REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)

Register Address	Register Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	Default Value
25h	P_{SUM} Accumulator Middle Byte	PSM22	PSM21	PSM20	PSM19	PSM18	PSM17	PSM16	PSM15	00h
26h	P_{SUM} Accumulator Middle-Low Byte	PSM14	PSM13	PSM12	PSM11	PSM10	PSM9	PSM8	PSM7	00h
27h	P_{SUM} Accumulator Low Byte	PSM6	PSM5	PSM4	PSM3	PSM2	PSM1	PSM0	—	00h
FDh	Product ID	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0	5Bh
FEh	Manufacturer ID	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0	5Dh
FFh	Revision	RID7	RID6	RID5	RID4	RID3	RID2	RID1	RID0	82h

6.1 Read Multiple Data Bytes

Data represented by multiple byte data registers are ensured to be synchronized and stable in the Read and Sleep states after transitioning from the Integrate state and waiting for t_{SETTLE} time (see Table 1-2). During the Integrate state, the data bytes will be changing dynamically.

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6.2 Detailed Register Description

REGISTER 6-1: GAIN CONFIGURATION REGISTER (ADDRESS 00H)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
I_RES	V_RES	DI_GAIN[2:0]			DV_GAIN[2:0]		
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **I_RES**: Sets the V_{SENSE} ADC measurement resolution
1 = V_{SENSE} ADC measurement resolution is 11-bit
0 = V_{SENSE} ADC measurement resolution is 14-bit

bit 6 **V_RES**: Sets the V_{BUS} ADC measurement resolution
1 = V_{BUS} ADC measurement resolution is 11-bit
0 = V_{BUS} ADC measurement resolution is 14-bit

bit 5-3 **DI_GAIN[2:0]**: Selects the digital current gain,
000b = 1x
001b = 2x
010b = 4x
011b = 8x
100b = 16x
101b = 32x
110b = 64x
111b = 128x

bit 2-0 **DV_GAIN[2:0]**: Selects the digital bus voltage gain.
000b = 1x
001b = 2x
010b = 4x
011b = 8x
100b = 16x
101b = 32x
110b = 32x
111b = 32x

REGISTER 6-2: INTEGRATION CONFIGURATION REGISTER (ADDRESS 01H)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
SMPL[3:0]				VSFEN	VBFEN	RIOV	INTEN
bit 7							bit 0

Legend:			
RC = Read-then-clear bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **SMPL[3:0]**: Controls the number of samples of the selected measurement type.
0000b = 1
0001b = 2
0010b = 4
0011b = 8
0100b = 16
0101b = 32
0110b = 64
0111b = 128
1000b = 256
1001b = 512
1010b = 1024
1011b = 2048
1100b = 2048
1101b = 2048
1110b = 2048
1111b = 2048

bit 3 **VSFEN**: enables the ADC post filter for V_{SENSE} samples. When the filter is enabled, conversion time is increased by 50%
1 = Filter enabled
0 = Filter disabled

bit 2 **VBFEN**: enables the ADC post filter for V_{BUS} samples. When the filter is enabled, conversion time is increased by 50%
1 = Filter enabled
0 = Filter disabled

bit 1 **RIOV**: enables the INT_EN bit to override the $\overline{\text{READ}}$/INT pin.
1 = Override enabled
0 = Override not enabled

bit 0 **INTEN**: forces the device into integrate mode, overriding the $\overline{\text{READ}}$/INT pin.
1 = Forced Integrate mode
0 = Forced Read State

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REGISTER 6-3: CONTROL REGISTER (ADDRESS 02H)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MXSL[1:0]		OFSR[1:0]		TOUT	SLEEP	SLPOV	RDAC
bit 7							bit 0

Legend:			
RC = Read-then-clear bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **MXSL[1:0]**: Selects which digital value is used for input to the OUT DAC and the integration mode
00 = V_{POWER} pin-controlled (default)
01 = V_{SENSE} free-run
10 = V_{BUS} free-run
11 = V_{POWER} free-run

bit 5-4 **OFSR[1:0]**: Determines the OUT pin full-scale range
00b = 3V FSR
01b = 2V FSR
10b = 1.5V FSR
11b = 1.0V FSR

bit 3 **TOUT**: Enables the time out and idle reset functionality of the communications protocol (see **Section 5.2 "SMBus Timeout"**).
1 = Time out enabled
0 = Time out disabled

bit 2 **SLEEP**: When the device is in the Read state, writing this bit to a '1' places the device in Sleep state.
1 = Sleep State
0 = Normal operation

bit 1 **SLPOV**: Sleep override. Writing a '1' disables the Sleep state timer, allowing the PAC1921 to remain in the Read state after t_{SLEEP}.
1 = Forced Read mode
0 = Normal operation

bit 0 **RDAC**: Forces the device to recalculate the selected measurement, and output immediately to the DAC
1 = Forced recalculate/DAC update mode
0 = Normal operation

REGISTER 6-4: V_{BUS} RESULT REGISTER (ADDRESSES 10H AND 11H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VBR[9:2]							
bit 15							bit 8

R-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
VBR[1:0]		—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **VBR[9:0]**: These registers contain the most recent digitized value of the average of V_{BUS} samples.
bit 5-0 **Unimplemented**: Read as '0'

REGISTER 6-5: V_{SENSE} RESULT REGISTER (ADDRESSES 12H AND 13H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VSR[9:2]							
bit 15							bit 8

R-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
VSR[1:0]		—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **VBR[9:0]**: These registers contain the most recent digitized value of the average of V_{SENSE} samples

bit 5-0 **Unimplemented**: Read as '0'

REGISTER 6-6: V_{SUM} ACCUMULATOR REGISTER (ADDRESSES 14H THROUGH 17H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VSM[24:17]							
bit 31							bit 24

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VSM[16:9]							
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VSM[8:1]							
bit 15							bit 8

R-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
VSM0	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-7 **VSM[24:0]**: These registers contain the accumulated sum of V_{BUS} samples (V_{SUM}) This is the number of 14-bit ADC counts. For 11-bit ADC resolution, the bits are shifted left by 3, so 1 count has a bit weighting of 8 and the lowest 3 bits will not be populated. The register value is only valid in the Read state.

bit 6-0 **Unimplemented**: Read as '0'

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REGISTER 6-7: ISUM ACCUMULATOR REGISTER (ADDRESSES 18H THROUGH 1BH)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
ISM[24:17]							
bit 31							bit 24

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
ISM[16:9]							
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
ISM[8:1]							
bit 15							bit 8

R-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
ISM0	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-7 **ISM[24:0]**: These registers contain the accumulated sum of V_{SENSE} samples (I_{SUM}). This is the number of 14-bit ADC counts. For 11-bit ADC resolution, the bits are shifted left by 3, so 1 count has a bit weighting of 8 and the lowest 3 bits will not be populated. The register value is only valid in the Read state.

bit 6-0 **Unimplemented**: Read as ‘0’

REGISTER 6-8: OVERFLOW STATUS REGISTER (ADDRESS 1CH)

U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
—	—	—	—	—	VSOV	VBOV	VPOV
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-3 **Unimplemented**: Read as ‘0’

bit 2 **VSOV**: This bit is set to ‘1’ when the DI_GAIN setting causes the V_{SENSE} Result register to overflow
1 = Overflow occurred
0 = Normal operation

bit 1 **VBOV**: This bit is set to ‘1’ when the DV_GAIN setting causes the V_{BUS} Result register to overflow.
1 = Overflow occurred
0 = Normal operation

bit 0 **VPOV**: This bit is set to ‘1’ when the DI_GAIN and/or DV_GAIN settings cause the V_{POWER} Result register to overflow
1 = Overflow occurred
0 = Normal operation

REGISTER 6-9: V_{POWER} RESULT REGISTER (ADDRESSES 1DH AND 1EH)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VPR[9:2]							
bit 15							bit 8

R-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
VPR[1:0]		—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-6 **VPR[9:0]**: These registers store the digitized value of the latest representation of the power relative to maximum power.

bit 5-0 **Unimplemented**: Read as ‘0’

REGISTER 6-10: SAMPLES REGISTERS (ADDRESSES 21H AND 22H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP[11:4]							
bit 15							bit 8

R-0	R-0	R-0	R-0	U-0	U-0	U-0	U-0
SMP[3:0]				—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-4 **SMP[11:0]**: These register values indicate the number of voltage samples (pairs of samples for power) taken during the integration period.

bit 3-0 **Unimplemented**: Read as ‘0’

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REGISTER 6-11: P_{SUM} ACCUMULATOR REGISTER (ADDRESSES 23H THROUGH 27H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
PSM[38:31]							
bit 39							bit 32

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
PSM[30:23]							
bit 31							bit 24

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
PSM[22:15]							
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
PSM[14:7]							
bit 15							bit 8

R-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
PSM[5:1]							—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 39-1 **PSM[38:1]**: These registers contain the accumulated sum of power samples (P_{SUM}). This is the number of 14-bit ADC counts. For 11-bit ADC resolution, the bits are shifted left by 6, so 1 count has a bit weighting of 64 and the lowest 6 bits will not be populated. The register value is only valid in the Read state.

bit 0 **Unimplemented**: Read as ‘0’

REGISTER 6-12: PRODUCT ID REGISTER (ADDRESS FDH)

R-0	R-1	R-0	R-1	R-1	R-0	R-1	R-1
PID[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **PID[7:0]**: This register contains the Product ID for the PAC1921.

REGISTER 6-13: MANUFACTURER ID REGISTER (ADDRESS FEH)

R-0	R-1	R-0	R-1	R-1	R-1	R-0	R-1
MID[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **MID[7:0]**: The Manufacturer ID register identifies Microchip as the manufacturer of the PAC1921

REGISTER 6-14: REVISION ID REGISTER (ADDRESS FFH)

R-1	R-0	R-0	R-0	R-0	R-0	R-1	R-0
RID[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **RID[7:0]**: The Revision register identifies the die revision.

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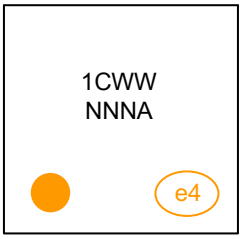
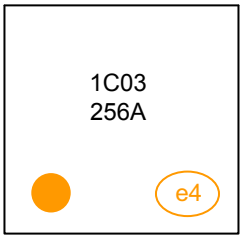
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

10-Lead VDFN (3x3x0.9 mm)



Example

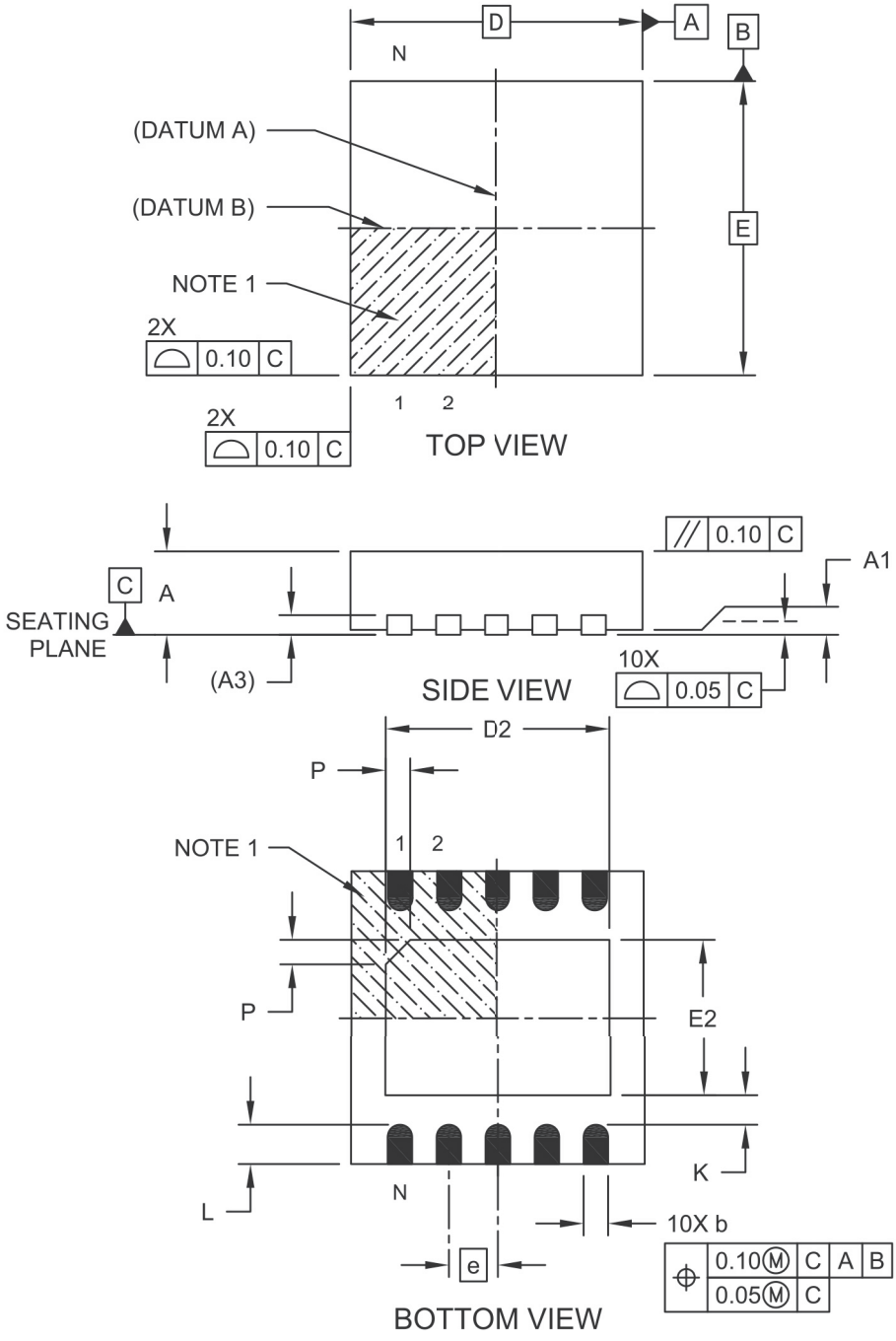


Legend:	Y	Year code (last digit of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	<R>	Package
	<COO>	Country of origin

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

10-Lead Very Thin Plastic Dual Flat, No Lead Package (9Q) - 3x3 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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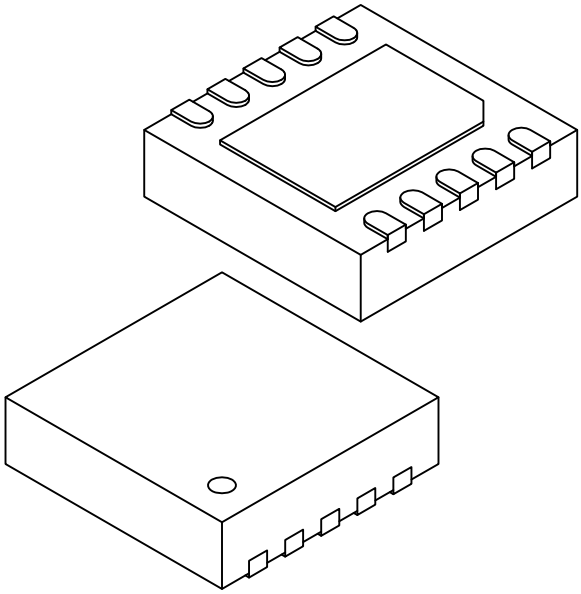
10-Lead Very Thin Plastic Dual Flat, No Lead Package (9Q) - 3x3 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	(A3)		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	2.20	2.30	2.40
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.60	1.70
Exposed Pad Chamfer	P	-	0.25	-
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.25	0.30	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-206 Rev B Sheet 2 of 2

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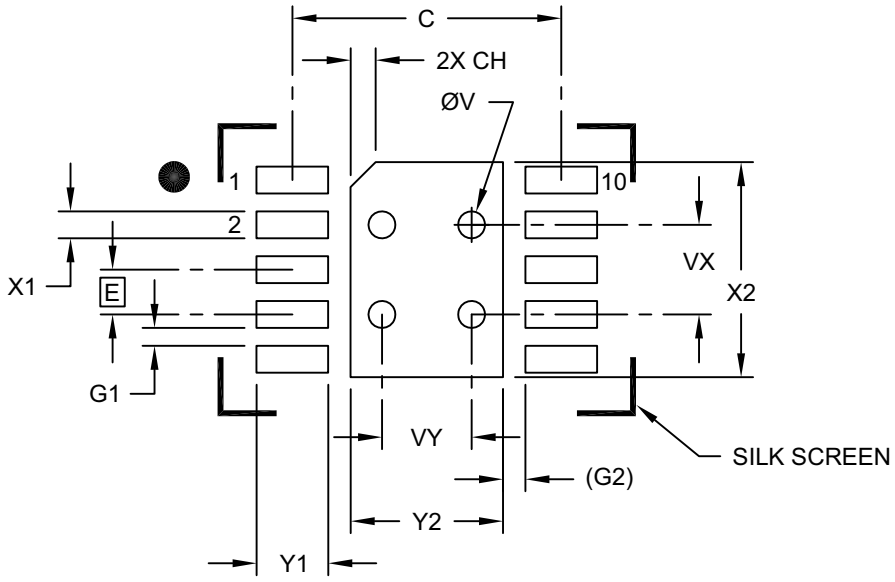
10-Lead Very Thin Plastic Dual Flat, No Lead Package (9Q) - 3x3 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	Y2			1.70
Optional Center Pad Length	X2			2.40
Contact Pad Spacing	C		3.00	
Center Pad Chamfer	CH		0.28	
Contact Pad Width (X10)	X1			0.30
Contact Pad Length (X10)	Y1			0.80
Contact Pad to Contact Pad (X8)	G1	0.20		
Contact Pad to Center Pad (X10)	G2		0.25 REF	
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	VX		1.00	
Thermal Via Pitch	VY		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerances, for reference only.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2206 Rev A

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APPENDIX A: REVISION HISTORY

Revision E (August 2019)

- Updated **Section 7.0, Packaging Information**.

Revision D (October 2016)

- Fixed minor typographical errors.

Revision C (June 2016)

- Modified the matrix description from the note in **Section "Absolute Maximum Ratings(†)"**.
- Fixed various typographical errors for consistency.

Revision B (April 2015)

- The document has been restructured to comply with the latest Microchip data sheet standards.
- Removed notes from **Section 1.1 "Electrical Specifications"**.
- Created separate **Section 2.0 "Typical Operating Curves"** chapter; updated plots.
- Fixed minor typographical errors.

Revision A (May 2014)

Replaced former SMSC version 1.2 (12-21-12).

- All sections updated to Microchip format.
- References to "stand-alone mode" removed.
- References to "lead-free" removed.

Rev 1.2 (December 2012)

- Modified under features in **"Ordering Information"** section.

Rev. 1.0 (April 2012)

- Initial document release.

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NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-X	-XXX	-XX
Device	SMBus Address	Package	Tape and Reel

Device:	PAC1921: High-Side Power/Current Monitor with Analog Output	
SMBus Address:	-1	= selectable address
Package:	AIA	= 10-lead 3 mm x 3 mm VDFN
Tape and Reel Option:	TR	= 4,000 piece Tape and Reel

Example:

a) PAC1921-1-AIA-TR: High-Side Current Monitor, 3 x 3 10 Lead VDFN package, Tape and Reel

NOTES:

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