

# MC33771B_SDS

## Battery cell controller IC

Rev. 7.0 — 10 May 2021 Product short data sheet

## 1 General description

The 33771 is a SMARTMOS lithium-ion battery cell controller IC designed for automotive applications, such as hybrid electric (HEV) and electric vehicles (EV) along with industrial applications, such as energy storage systems (ESS) and uninterruptible power supply (UPS) systems.

The device performs ADC conversions of the differential cell voltages and current, as well as battery coulomb counting and battery temperature measurements. The information is digitally transmitted through the Serial Peripheral Interface (SPI) or Transformer Isolation (TPL) to a microcontroller for processing.

## 2 Features

- 9.6 V ≤ $V_{PWR}$ ≤ 63 V operation, 75 V transient
- 7 to 14 cells management
- Isolated 2.0 Mbps differential communication or 4.0 Mbps SPI
- Addressable on initialization
- 0.8 mV maximum total voltage measurement error
- Synchronized cell voltage/current measurement with coulomb count
- Total stack voltage measurement
- Seven GPIO/temperature sensor inputs
- 5.0 V at 5.0 mA reference supply output
- Automatic over/undervoltage and temperature detection routable to fault pin
- Integrated sleep mode over/undervoltage and temperature monitoring
- Onboard 300 mA passive cell balancing with diagnostics
- Hot plug capable
- Detection of internal and external faults, as open lines, shorts, and leakages
- Designed to support ISO 26262, up to ASIL D safety system
- Fully compatible with the MC33772 for a maximum of six cells
- Qualified in compliance with AEC–Q100

## 3 Simplified application diagram

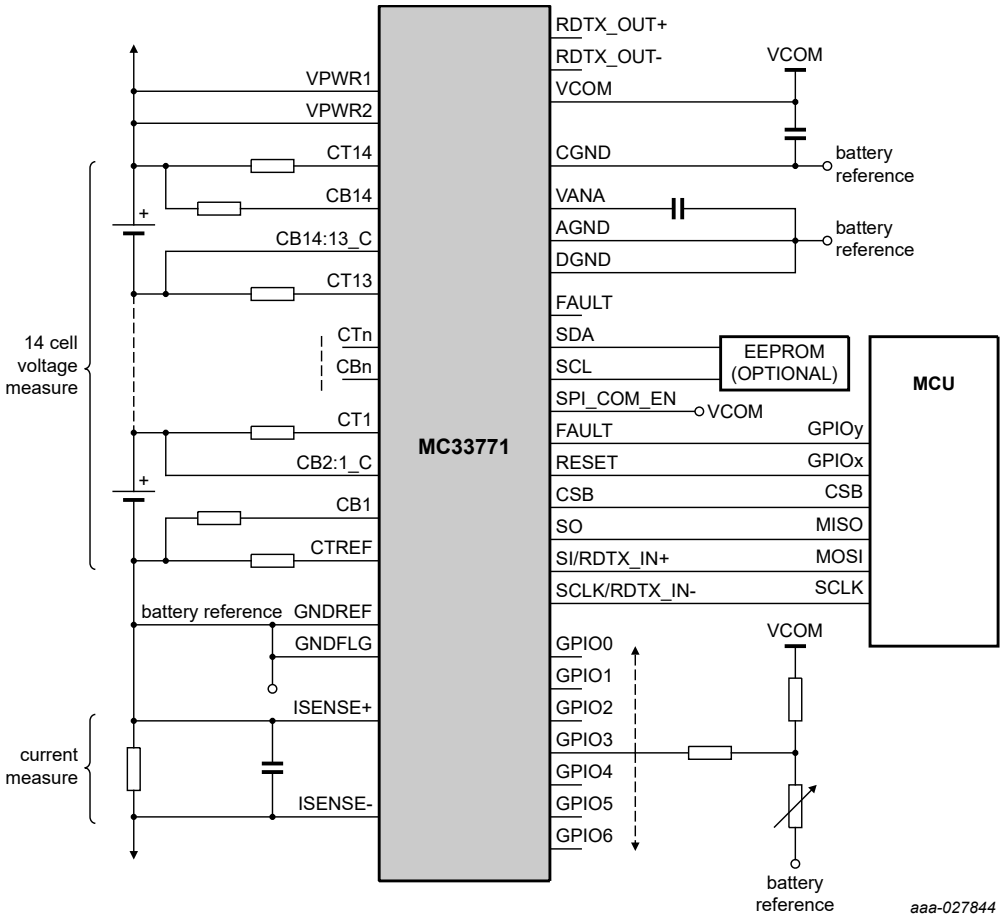


**Figure 1. Simplified application diagram, SPI use case**


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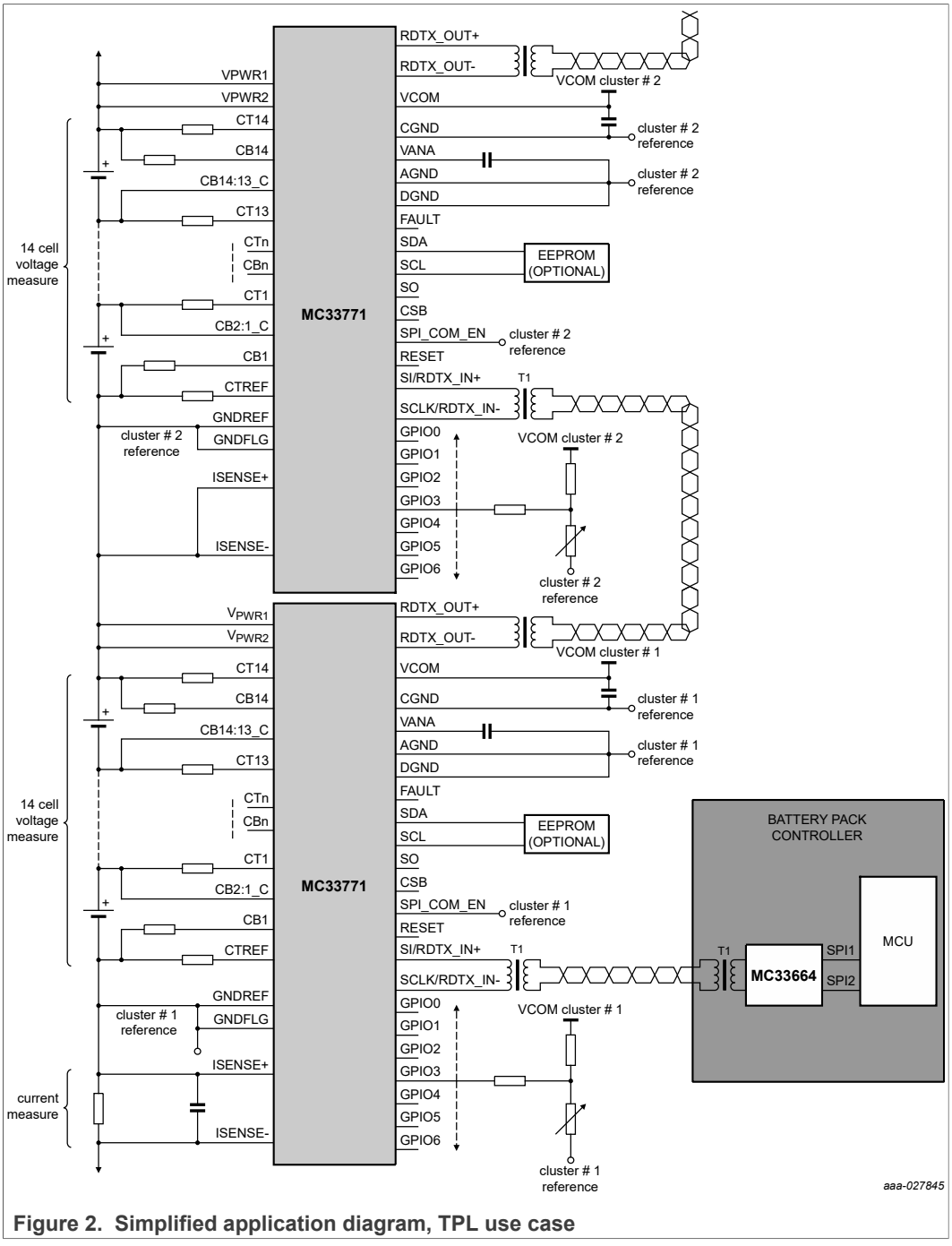


**Figure 2. Simplified application diagram, TPL use case**

# 4 Applications

- Automotive: 48 V and high-voltage battery packs
- E-bikes, e-scooters
- Energy storage systems
- Uninterruptible power supply (UPS)


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# 5 Ordering information

## 5.1 Part numbers definition

**MC33771B x y z AE/R2**

**Table 1. Part number breakdown**

| Code | Option | Description |
|---|---|---|
| x | S | x = S (SPI communication type) |
| | T | x = T (TPL communication type) |
| y | A | y = A (Advanced) |
| | B | y = B (Basic) |
| | P | y = P (Premium) |
| z | 1 | z = 1 (7 to 14 channels) |
| | 2 | z = 2 (7 to 8 channels) |
| | AE | Package suffix |
| | R2 | Tape and reel indicator |


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## 5.2 Part numbers list

This section describes the part numbers available to be purchased along with their differences. Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.nxp.com.

**Table 2. Advanced orderable part table**

*Temperature range is −40 to 105 °C*

*Package type is 64-pin LQFP-EP*

| Orderable part | Number of channels | OV/UV | Precision GPIO as temperature channels and OT/UT | Current channel or coulomb count |
|---|---|---|---|---|
| **SPI communication protocol** | | | | |
| MC33771BSA1AE | 7 to 14 | Yes | Yes | No |
| MC33771BSA2AE | 7 to 8 | Yes | Yes | No |
| **TPL differential communication protocol** | | | | |
| MC33771BTA1AE | 7 to 14 | Yes | Yes | No |
| MC33771BTA2AE | 7 to 8 | Yes | Yes | No |

**Table 3. Basic orderable part table**

*Temperature range is −40 to 105 °C*

*Package type is 64-pin LQFP-EP*

| Orderable part | Number of channels | OV/UV | Precision GPIO as temperature channels and OT/UT | Current channel or coulomb count |
|---|---|---|---|---|
| **SPI communication protocol** | | | | |
| MC33771BSB1AE | 7 to 14 | Yes | No | No |
| MC33771BSB2AE | 7 to 8 | Yes | No | No |
| **TPL differential communication protocol** | | | | |
| MC33771BTB1AE | 7 to 14 | Yes | No | No |
| MC33771BTB2AE | 7 to 8 | Yes | No | No |

**Table 4. Premium orderable part table**

*Temperature range is −40 to 105 °C*

*Package type is 64-pin LQFP-EP*

| Orderable part | Number of channels | OV/UV | Precision GPIO as temperature channels and OT/UT | Current channel or coulomb count |
|---|---|---|---|---|
| **SPI communication protocol** | | | | |
| MC33771BSP1AE | 7 to 14 | Yes | Yes | Yes |
| MC33771BSP2AE | 7 to 8 | Yes | Yes | Yes |
| **TPL differential communication protocol** | | | | |
| MC33771BTP1AE | 7 to 14 | Yes | Yes | Yes |
| MC33771BTP2AE | 7 to 8 | Yes | Yes | Yes |


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# 6 Pinning information

## 6.1 Pinout diagram

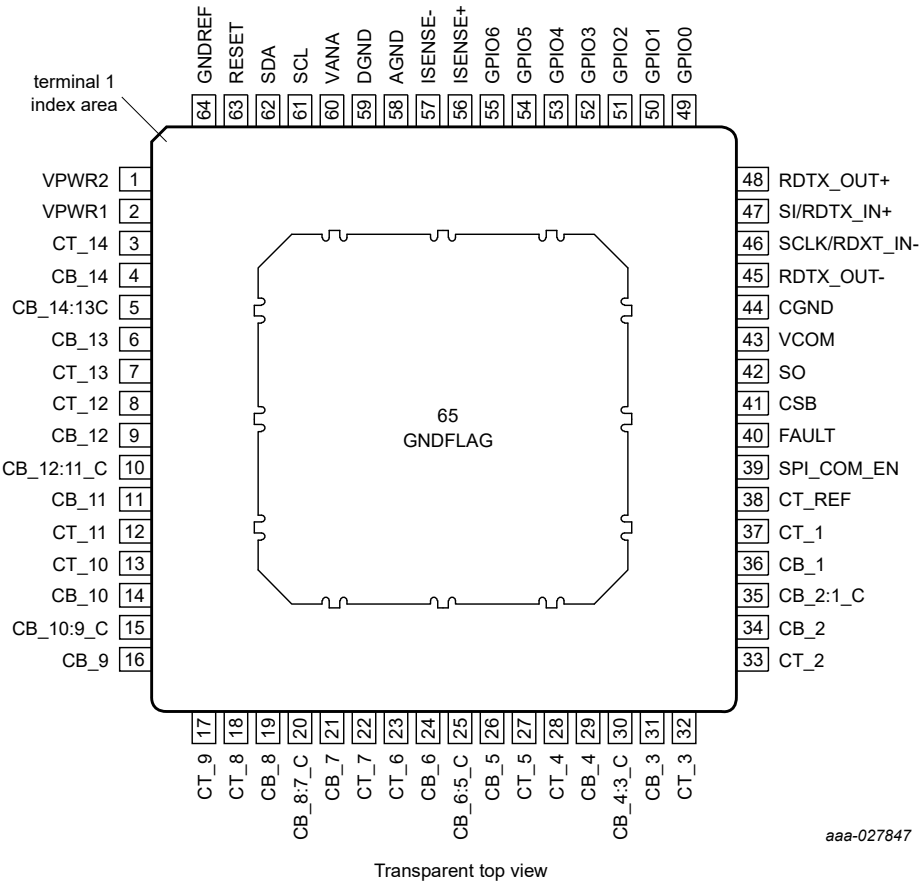


**Figure 3. Pinout diagram**

## 6.2 Pin definitions

**Table 5. Pin definitions**

| Number | Name | Function | Definition |
|---|---|---|---|
| 1 | VPWR2 | Input | Power input to the 33771 |
| 2 | VPWR1 | Input | Power input to the 33771 |
| 3 | CT_14 | Input | Cell pin 14 input. Terminate to LPF resistor. |
| 4 | CB_14 | Output | Cell balance driver. Terminate to cell 14 cell balance load resistor. |
| 5 | CB_14:13_C | Output | Cell balance 14:13 common. Terminate to cell 14 and 13 common pin. |
| 6 | CB_13 | Output | Cell balance driver. Terminate to cell 13 cell balance load resistor. |
| 7 | CT_13 | Input | Cell pin 13 input. Terminate to LPF resistor. |
| 8 | CT_12 | Input | Cell pin 12 input. Terminate to LPF resistor. |


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**Table 5. Pin definitions***...continued*

| Number | Name | Function | Definition |
|---|---|---|---|
| 9 | CB_12 | Output | Cell balance driver. Terminate to cell 12 cell balance load resistor. |
| 10 | CB_12:11_C | Output | Cell balance 12:11 common. Terminate to cell 12 and 11 common pin. |
| 11 | CB_11 | Output | Cell balance driver. Terminate to cell 11 cell balance load resistor. |
| 12 | CT_11 | Input | Cell pin 11 input. Terminate to LPF resistor. |
| 13 | CT_10 | Input | Cell pin 10 input. Terminate to LPF resistor. |
| 14 | CB_10 | Output | Cell balance driver. Terminate to cell 10 cell balance load resistor. |
| 15 | CB_10:9_C | Output | Cell balance 10:9 common. Terminate to cell 10 and 9 common pin. |
| 16 | CB_9 | Output | Cell balance driver. Terminate to cell 9 cell balance load resistor. |
| 17 | CT_9 | Input | Cell pin 9 input. Terminate to LPF resistor. |
| 18 | CT_8 | Input | Cell pin 8 input. Terminate to LPF resistor. |
| 19 | CB_8 | Output | Cell balance driver. Terminate to cell 8 cell balance load resistor. |
| 20 | CB_8:7_C | Output | Cell balance 8:7 common. Terminate to cell 8 and 7 common pin. |
| 21 | CB_7 | Output | Cell balance driver. Terminate to cell 7 cell balance load resistor. |
| 22 | CT_7 | Input | Cell pin 7 input. Terminate to LPF resistor. |
| 23 | CT_6 | Input | Cell pin 6 input. Terminate to LPF resistor. |
| 24 | CB_6 | Output | Cell balance driver. Terminate to cell 6 cell balance load resistor. |
| 25 | CB_6:5_C | Output | Cell balance 6:5 common. Terminate to cell 6 and 5 common pin. |
| 26 | CB_5 | Output | Cell balance driver. Terminate to cell 5 cell balance load resistor. |
| 27 | CT_5 | Input | Cell pin 5 input. Terminate to LPF resistor. |
| 28 | CT_4 | Input | Cell pin 4 input. Terminate to LPF resistor. |
| 29 | CB_4 | Output | Cell balance driver. Terminate to cell 4 cell balance load resistor. |
| 30 | CB_4:3_C | Output | Cell balance 4:3 common. Terminate to cell 4 and 3 common pin. |
| 31 | CB_3 | Output | Cell balance driver. Terminate to cell 3 cell balance load resistor. |
| 32 | CT_3 | Input | Cell pin 3 input. Terminate to LPF resistor. |
| 33 | CT_2 | Input | Cell pin 2 input. Terminate to LPF resistor. |
| 34 | CB_2 | Output | Cell balance driver. Terminate to cell 2 cell balance load resistor. |


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**Table 5. Pin definitions***...continued*

| Number | Name | Function | Definition |
|---|---|---|---|
| 35 | CB_2:1_C | Output | Cell Balance 2:1 common. Terminate to cell 2 and 1 common pin. |
| 36 | CB_1 | Output | Cell balance driver. Terminate to cell 1 cell balance load resistor. |
| 37 | CT_1 | Input | Cell pin 1 input. Terminate to LPF resistor. |
| 38 | CT_REF | Input | Cell pin REF input. Terminate to LPF resistor. |
| 39 | SPI_COM_EN | Input | SPI communication enable, pin must be high for the SPI to be active |
| 40 | FAULT | Output | Fault output dependent on user defined internal or external faults. If not used, it must be left open. |
| 41 | CSB | Input | SPI chip select |
| 42 | SO | Output | SPI serial output |
| 43 | VCOM | Output | Communication regulator output. Decouple with 2.2 µF ceramic. |
| 44 | CGND | Ground | Communication decoupling ground. Terminate to GNDREF |
| 45 | RDTX_OUT- | I/O | Receive/transmit output negative |
| 46 | SCLK/RDTX_IN- | I/O | SPI clock or receive/transmit input negative |
| 47 | SI/RDTX_IN+ | I/O | SPI serial input or receiver/transmit input positive |
| 48 | RDTX_OUT+ | I/O | Receive/transmit output positive |
| 49 | GPIO0 | I/O | General purpose analog input or GPIO or wake-up or fault daisy chain |
| 50 | GPIO1 | I/O | General purpose analog input or GPIO |
| 51 | GPIO2 | I/O | General purpose analog input or GPIO or conversion trigger |
| 52 | GPIO3 | I/O | General purpose analog input or GPIO |
| 53 | GPIO4 | I/O | General purpose analog input or GPIO |
| 54 | GPIO5 | I/O | General purpose analog input or GPIO |
| 55 | GPIO6 | I/O | General purpose analog input or GPIO |
| 56 | ISENSE+ | Input | Current measurement input+ |
| 57 | ISENSE- | Input | Current measurement input− |
| 58 | AGND | Ground | Analog ground, terminate to GNDREF |
| 59 | DGND | Ground | Digital ground, terminate to GNDREF |
| 60 | VANA | Output | Precision ADC analog supply. Decouple with ceramic 47 nF ceramic capacitor to AGND. |
| 61 | SCL | I/O | $I^2C$ clock |
| 62 | SDA | I/O | $I^2C$ data |


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**Table 5. Pin definitions**...*continued*

| Number | Name | Function | Definition |
|---|---|---|---|
| 63 | RESET | Input | RESET is an active high input. RESET has an internal pull down. If not used, it can be tied to GND. |
| 64 | GNDREF | Ground | Ground reference for device. Terminate to reference of battery cluster. |
| 65 | GNDFLAG | Ground | Device flag. Terminate to lowest potential of battery cluster. |

# 7 General product characteristics

## 7.1 Ratings and operating requirements relationship

The operating voltage range pertains to the VPWR pins referenced to the AGND pins.

**Table 6. Ratings vs. operating requirements**

| Fatal range<br>• Permanent failure might occur | Handling range – no permanent failure | | | Fatal range<br>• Permanent failure might occur |
|---|---|---|---|---|
| | Lower limited operating range<br>• No permanent failure, but IC functionality is not guaranteed | Normal operating range<br>• 100 % functional | Upper limited operating range<br>• IC parameters might be out of specification<br>• Detection of $V_{PWR}$ overvoltage is functional | |
| $V_{PWR}$ < −0.3 V | 7.6 V ≤ $V_{PWR}$ < 9.6 V<br>**Reset range:**<br>–0.3 V ≤ $V_{PWR}$ < 7.6 V | 9.6 V ≤ $V_{PWR}$ ≤ 63 V | 63 V < $V_{PWR}$ ≤ 75 V | 75 V < $V_{PWR}$ |

In both upper and lower limited operating range, no information can be provided about IC performance. Only the detection of $V_{PWR}$ overvoltage is guaranteed in the upper limited operating range.

Performance in normal operating range is guaranteed only if there is a minimum of seven battery cells in the stack.

## 7.2 Maximum ratings

**Table 7. Maximum ratings**

*All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.*

| Symbol | Description (rating) | Min | Max | Unit |
|---|---|---|---|---|
| **Electrical ratings** | | | | |
| VPWR1, VPWR2 | Supply input voltage | −0.3 | 75 | V |
| CT14 | Cell terminal voltage | −0.3 | 75 | V |
| VPWR to CT14 | Voltage across VPWR1,2 pins pair and CT14 pin | −10 | 10.5 | V |
| $CT_N$ to $CT_{N-1}$ | Cell terminal differential voltage [1] | −0.3 | 6.0 | V |
| $CT_{N(CURRENT)}$ | Cell terminal input current | — | ±500 | µA |
| $CB_N$ to $CB_{N:N-1_C}$<br>$CB_{N:N-1_C}$ to $CB_{N-1}$ | Cell balance differential voltage | — | 10 | V |


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**Table 7. Maximum ratings**...*continued*

*All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.*

| Symbol | Description (rating) | Min | Max | Unit |
|---|---|---|---|---|
| $CB_{N-1_C}$ to CTn-1 | Cell balance input to cell terminal input | −10 | +10 | V |
| VISENSE | ISENSE+ and ISENSE– pin voltage | −0.3 | 2.5 | V |
| VCOM | Maximum voltage may be applied to VCOM pin from external source | — | 5.8 | V |
| VANA | Maximum voltage may be applied to VANA pin | — | 3.1 | V |
| $V_{GPIO0}$ | GPIO0 pin voltage | –0.3 | 6.5 | V |
| $V_{GPIOx}$ | GPIOx pins (x = 1 to 6) voltage | –0.3 | VCOM + 0.5 | V |
| $V_{DIG}$ | Voltage $I^2C$ pins (SDA, SCL) | –0.3 | VCOM + 0.5 | V |
| $V_{RESET}$ | RESET pin | –0.3 | 6.5 | V |
| $V_{CSB}$ | CSB pin | –0.3 | 6.5 | V |
| $V_{SPI_COMM_EN}$ | SPI_COMM_EN | –0.3 | 6.5 | V |
| $V_{SO}$ | SO pin | –0.3 | VCOM + 0.5 | V |
| $V_{GPIO5,6}$ | Maximum voltage for GPIO5 and GPIO6 pins used as current input | −0.3 | 2.5 | V |
| FAULT | Maximum applied voltage to pin | −0.3 | 7.0 | V |
| $V_{COMM}$ | Maximum voltage to pins RDTX_OUT+, RDTX_OUT–, SI/RDTX_IN+, CLK/RDTX_IN– | −10.0 | 10.0 | V |
| $f_{SPI}$ | SPI frequency (SPI mode) | — | 4.2 | MHz |
| $BR_{TPL}$ | Transformer communication bit rate (TPL mode) | 1.9 | 2.1 | Mbps |
| $f_{TPL}$ | Transformer signal frequency (TPL mode) | 3.8 | 4.2 | MHz |
| $V_{ESD}$ | ESD voltage<br>Human body model (HBM)<br>Charge device model (CDM)<br>Charge device model corner pins (CDM) | <br>—<br>—<br>— | <br>±2000<br>±500<br>±750 | V |
| $V_{ESD}$ | ESD voltage (VPWR1, VPWR2, CTx, CBx, GPIOx, ISENSE+, ISENSE−, RDTX_OUT+, RDTX_OUT−, SI/RDTX_IN+, SCLK/ RDTX_IN−) [2]<br>Human body model (HBM) | <br>— | <br>±4000 | V |
| $V_{ESD}$ | ESD voltage (CTREF, CTx, CBx, GPIOx, ISENSE+, ISENSE−, RDTX_OUT+, RDTX_OUT−, SI/RDTX_IN+, SCLK/ RDTX_IN−)<br>IEC 61000-4-2, Unpowered (Gun configuration: 330Ω / 150pF)<br>HMM, Unpowered (Gun configuration: 330Ω / 150pF)<br>ISO 10605:2009, Unpowered (Gun configuration: 2 kΩ / 150pF)<br>ISO 10605:2009, Powered (Gun configuration: 2 kΩ / 150pF) | <br>—<br>—<br>—<br>— | <br>±8000<br>±8000<br>±8000<br>±8000 | V |

[1] Adjacent CT pins may experience an overvoltage that exceeds their maximum rating during OV/UV functional verification test or during open line diagnostic test. Nevertheless, the IC is completely tolerant to this special situation.

[2] ESD testing is performed in accordance with the human body model (HBM) ($C_{ZAP}$ = 100 pF, $R_{ZAP}$ = 1500 Ω), and the charge device model (CDM) ($C_{ZAP}$ = 4.0 pF).


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## 7.3 Thermal characteristics

**Table 8. Thermal ratings**

*All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.*

| Symbol | Description (rating) | | Min | Max | Unit |
|---|---|---|---|---|---|
| **Thermal ratings** | | | | | |
| | Operating temperature | | | | °C |
| $T_A$ | Ambient | | −40 | +105 | |
| $T_J$ | Junction | | −40 | +150 | |
| $T_{STG}$ | Storage temperature | | −55 | +150 | °C |
| $T_{PPRT}$ | Peak package reflow temperature | [1] [2] | — | 260 | °C |
| **Thermal resistance and package dissipation ratings** | | | | | |
| $R_{\Theta JB}$ | Junction-to-board (bottom exposed pad soldered to board) 64 LQFP EP | [3] | — | 10 | °C/W |
| $R_{\Theta JA}$ | Junction-to-ambient, natural convection, single-layer board (1s) 64 LQFP EP | [4] [5] | — | 59 | °C/W |
| $R_{\Theta JA}$ | Junction-to-ambient, natural convection, four-layer board (2s2p) 64 LQFP EP | [4] [5] | — | 27 | °C/W |
| $R_{\Theta JCTOP}$ | Junction-to-case top (exposed pad) 64 LQFP EP | [6] | — | 14 | °C/W |
| $R_{\Theta JCBOTTOM}$ | Junction-to-case bottom (exposed pad) 64 LQFP EP | [7] | — | 0.97 | °C/W |
| ΨJT | Junction to package top, natural convection | [8] | — | 3 | °C/W |

[1] Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
[2] NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts (MC33xxxD enter 33xxx), and review parametrics.
[3] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
[4] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
[5] Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
[6] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1), with the cold plate temperature used for the case temperature.
[7] Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.
[8] Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letter (Ψ) is not available, the thermal characterization parameter is written as Psi-JT.

## 7.4 Electrical characteristics

**Table 9. Static and dynamic electrical characteristics**

*Characteristics noted under conditions 9.6 V ≤ $V_{PWR}$ ≤ 63 V, −40 °C ≤ $T_A$ ≤ 105 °C, GND = 0 V, unless otherwise stated. Typical values refer to $V_{PWR}$ = 56 V, $T_A$ = 25 °C, unless otherwise noted.*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Power management** | | | | | |
| $V_{PWR(FO)}$ | Supply voltage | | | | V |
| | Full parameter specification | 9.6 | — | 63 | |


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**Table 9. Static and dynamic electrical characteristics**...*continued*

*Characteristics noted under conditions 9.6 V ≤ $V_{PWR}$ ≤ 63 V, −40 °C ≤ $T_A$ ≤ 105 °C, GND = 0 V, unless otherwise stated. Typical values refer to $V_{PWR}$ = 56 V, $T_A$ = 25 °C, unless otherwise noted.*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $I_{VPWR}$ | Supply current (base value)<br>Normal mode, cell balance OFF, ADC inactive, SPI communication inactive, IVCOM = 0 mA<br>Normal mode, cell balance OFF, ADC inactive, TPL communication inactive, IVCOM = 0 mA | <br>—<br>— | <br>5.4<br>8.0 | <br>—<br>— | mA |
| $I_{VPWR(TPL_TX)}$ | Supply current adder when TPL communication active | — | 50 | — | mA |
| $I_{VPWR(CBON)}$ | Supply current adder to set all 14 cell balance switches ON | — | 0.97 | — | mA |
| $I_{VPWR(ADC)}$ | Delta supply current to perform ADC conversions (addend)<br>ADC1-A,B continuously converting<br>ADC2 continuously converting | <br>—<br>— | <br>3.0<br>1.4 | <br>—<br>— | mA |
| $I_{VPWR(SS)}$ | Supply current in sleep mode and in idle mode, communication inactive, cell balance off, cyclic measurement off, oscillator monitor on<br>SPI mode (25 °C)<br>TPL mode (25 °C) | <br>—<br>— | <br>40<br>68 | <br>—<br>— | µA |
| $I_{VPWR(CKMON)}$ | Clock monitor current consumption | — | 5 | — | µA |
| $V_{PWR(OV_FLAG)}$ | $V_{PWR}$ overvoltage fault threshold (flag) | — | 65 | — | V |
| $V_{PWR(LV_FLAG)}$ | $V_{PWR}$ low-voltage warning threshold (flag) | — | 12 | — | V |
| $V_{PWR(UV_POR)}$ | $V_{PWR}$ undervoltage shutdown threshold (POR) | — | 8.5 | — | V |
| $V_{PWR(HYS)}$ | $V_{PWR}$ UV hysteresis voltage | — | 200 | — | mV |
| $t_{VPWR(FILTER)}$ | $V_{PWR}$ OV, LV filter | — | 50 | — | µs |
| **VCOM power supply** | | | | | |
| $V_{COM}$ | VCOM output voltage | — | 5.0 | — | V |
| $I_{VCOM}$ | VCOM output current allocated for external use | — | — | 5.0 | mA |
| $V_{COM(UV)}$ | VCOM undervoltage fault threshold | — | 4.4 | — | V |
| $V_{COM_HYS}$ | VCOM undervoltage hysteresis | — | 100 | — | mV |
| $t_{VCOM(FLT_TIMER)}$ | VCOM undervoltage fault timer | — | 10 | — | µs |
| $t_{VCOM(RETRY)}$ | VCOM fault retry timer | — | 10 | — | ms |
| $V_{COM(OV)}$ | VCOM overvoltage fault threshold | 5.4 | — | 5.9 | V |
| $I_{LIM(OC)}$ | VCOM current limit | 65 | — | 140 | mA |
| $R_{VCOM(SS)}$ | VCOM sleep mode pull-down resistor | — | 2.0 | — | kΩ |
| **VANA power supply** | | | | | |
| $V_{ANA}$ | VANA output voltage (not used by external circuits)<br>Decouple with 47 nF X7R 0603 or 0402 | <br>— | <br>2.65 | <br>— | V |
| $V_{ANA(UV)}$ | VANA undervoltage fault threshold | — | 2.4 | — | V |
| $V_{ANA_HYS}$ | VANA undervoltage hysteresis | — | 50 | — | mV |
| $V_{ANA(FLT_TIMER)}$ | VANA undervoltage fault timer | — | 11 | — | µs |
| $V_{ANA(OV)}$ | VANA overvoltage fault threshold | — | 2.8 | — | V |
| $t_{VANA(RETRY)}$ | VANA fault retry timer | — | 10 | — | ms |
| $I_{LIM(OC)}$ | VANA current limit | 5.0 | — | 10 | mA |
| $R_{VANA_RPD}$ | VANA sleep mode pull-down resistor | — | 1.0 | — | kΩ |


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**Table 9. Static and dynamic electrical characteristics**...*continued*

*Characteristics noted under conditions 9.6 V ≤ $V_{PWR}$ ≤ 63 V, −40 °C ≤ $T_A$ ≤ 105 °C, GND = 0 V, unless otherwise stated. Typical values refer to $V_{PWR}$ = 56 V, $T_A$ = 25 °C, unless otherwise noted.*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{VANA}$ | VANA rise time (CL = 47 nF ceramic X7R only) | — | — | 100 | µs |
| **ADC1-A, ADC1-B** | | | | | |
| $CTn_{(LEAKAGE)}$ | Cell terminal input leakage current (except in SLEEP mode when cell balancing is ON) | — | 10 | — | nA |
| $CTn_{(FV)}$ | Cell terminal input current - functional verification | — | 0.365 | — | mA |
| $CT_N$ | Cell terminal input current during conversion | — | 50 | — | nA |
| $R_{PD}$ | Cell terminal open load detection pull-down resistor | — | 950 | — | Ω |
| $V_{VPWR_RES}$ | VPWR terminal measurement resolution | — | 2.44141 | — | mV/LSB |
| $V_{VPWR_RNG}$ | VPWR terminal measurement range | 9.6 | — | 75 | V |
| $VPWR_{TERM_ERR}$ | VPWR terminal measurement accuracy | −0.5 | — | 0.5 | % |
| $V_{CT_RNG}$ | ADC differential input voltage range for CTn to CTn-1 | 0.0 | — | 4.85 | V |
| $V_{CT_ANx_RES}$ | Cell voltage and ANx resolution in 15-bit MEAS_xxxx registers | — | 152.58789 | — | µV/LSB |
| $V_{ERR33RT}$ | Cell voltage measurement error $V_{CELL}$ = 3.3 V, $T_A$ = 25 °C | −0.8 | ±0.4 | 0.8 | mV |
| $V_{ERR}$ | Cell voltage measurement error<br>0.1 V ≤ $V_{CELL}$ ≤ 4.8 V, −40 °C ≤ $T_A$ ≤ 105 °C (or −40 °C ≤ $T_J$ ≤ 125 °C) | — | ±0.7 | — | mV |
| $V_{ERR_1}$ | Cell voltage measurement error<br>0 V ≤ $V_{CELL}$ ≤ 1.5 V, −40 °C ≤ $T_A$ ≤ 60 °C (or −40 °C ≤ $T_J$ ≤ 85 °C) | — | ±0.4 | — | mV |
| $V_{ERR_2}$ | Cell voltage measurement error<br>1.5 V ≤ $V_{CELL}$ ≤ 2.7 V, −40 °C ≤ $T_A$ ≤ 60 °C (or −40 °C ≤ $T_J$ ≤ 85 °C) | — | ±0.4 | — | mV |
| $V_{ERR_3}$ | Cell voltage measurement error<br>2.7 V ≤ $V_{CELL}$ ≤ 3.7 V, −40 °C ≤ $T_A$ ≤ 60 °C (or −40 °C ≤ $T_J$ ≤ 85 °C) | — | ±0.5 | — | mV |
| $V_{ERR_4}$ | Cell voltage measurement error<br>3.7 V ≤ $V_{CELL}$ ≤ 4.3 V, −40 °C ≤ $T_A$ ≤ 60 °C (or −40 °C ≤ $T_J$ ≤ 85 °C) | — | ±0.7 | — | mV |
| $V_{ERR_5}$ | Cell voltage measurement error<br>1.5 V ≤ $V_{CELL}$ ≤ 4.5 V, −40 °C ≤ $T_A$ ≤ 105 °C (or −40 °C ≤ $T_J$ ≤ 125 °C) | — | ±0.7 | — | mV |
| $V_{ANx_ERR}$ | Magnitude of ANx error in the entire measurement range:<br>Ratiometric measurement<br>Absolute measurement after soldering and aging, input in the range [1.0, 4.5] V<br>Absolute measurement after soldering and aging, input in the range [0, 4.85] V, for −40 °C < $T_A$ < 60 °C)<br>Absolute measurement after soldering and aging, input in the range [0, 4.85] V, for −40 °C < $T_A$ < 105 °C) | <br>—<br>—<br>−8.0<br>−11 | <br>—<br>—<br>—<br>— | <br>16<br>10<br>8.0<br>11 | mV |
| $t_{VCONV}$ | Single channel net conversion time<br>13-bit resolution<br>14-bit resolution<br>15-bit resolution<br>16-bit resolution | <br>—<br>—<br>—<br>— | <br>6.77<br>9.43<br>14.75<br>25.36 | <br>—<br>—<br>—<br>— | µs |


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**Table 9. Static and dynamic electrical characteristics**...*continued*

*Characteristics noted under conditions 9.6 V ≤ $V_{PWR}$ ≤ 63 V, −40 °C ≤ $T_A$ ≤ 105 °C, GND = 0 V, unless otherwise stated. Typical values refer to $V_{PWR}$ = 56 V, $T_A$ = 25 °C, unless otherwise noted.*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{V_NOISE}$ | Conversion noise | | | | µVrms |
| | 13-bit resolution | — | 1800 | — | |
| | 14-bit resolution | — | 1000 | — | |
| | 15-bit resolution | — | 600 | — | |
| | 16-bit resolution | — | 400 | — | |
| **ADC2/current sense module** | | | | | |
| $V_{INC}$ | ISENSE+/ISENSE− input voltage (reference to AGND) | −300 | — | 300 | mV |
| $V_{IND}$ | ISENSE+/ISENSE− differential input voltage range | −150 | — | 150 | mV |
| $V_{ISENSEX(OFFSET)}$ | ISENSE+/ISENSE− input voltage offset error | — | — | 0.5 | µV |
| $I_{GAINERR}$ | ISENSE error including nonlinearities | −0.5 | — | 0.5 | % |
| $I_{ISENSE_OL}$ | ISENSE open load injected current | — | 130 | — | µA |
| $V_{ISENSE_OL}$ | ISENSE open load detection threshold | — | 460 | — | mV |
| $V_{2RES}$ | Current sense user register resolution | — | 0.6 | — | µV/LSB |
| $V_{PGA_SAT}$ | PGA saturation half-range | | | | mV |
| | Gain = 256 | — | 4.9 | — | |
| | Gain = 64 | — | 19.5 | — | |
| | Gain = 16 | — | 78.1 | — | |
| | Gain = 4 | — | 150.0 | — | |
| $V_{PGA_ITH}$ | Voltage threshold for PGA gain increase | | | | mV |
| | Gain = 256 | — | — | — | |
| | Gain = 64 | — | 2.344 | — | |
| | Gain = 16 | — | 9.375 | — | |
| | Gain = 4 | — | 37.50 | — | |
| $V_{PGA_DTH}$ | Voltage threshold for PGA gain decrease | | | | mV |
| | Gain = 256 | — | 4.298 | — | |
| | Gain = 64 | — | 17.188 | — | |
| | Gain = 16 | — | 68.750 | — | |
| | Gain = 4 | — | — | — | |
| $t_{AZC_SETTLE}$ | Time to perform auto-zero procedure after enabling the current channel | — | 200 | — | µs |
| $t_{ICONV}$ | ADC conversion time including PGA settling time | | | | µs |
| | 13 bit resolution | — | 19.00 | — | |
| | 14 bit resolution | — | 21.67 | — | |
| | 15 bit resolution | — | 27.00 | — | |
| | 16 bit resolution | — | 37.67 | — | |
| $V_{I_NOISE}$ | Noise error at 16-bit conversion | — | 3.01 | — | µVrms |
| $V_{I_NOISE}$ | Noise error at 13-bit conversion | — | 8.33 | — | µVrms |
| $ADC_{CLK}$ | ADC2 and ADC1-A,B clocking frequency | — | 6.0 | — | MHz |
| **Cell balance drivers** | | | | | |
| $V_{DS(CLAMP)}$ | Cell balance driver VDS active clamp voltage | — | 11 | — | V |
| $V_{OUT(FLT_TH)}$ | Output fault detection voltage threshold | | | | V |
| | Balance off (open load)<br>Balance on (shorted load) | — | 0.55 | — | |
| $R_{PD_CB}$ | Output OFF open load detection pull-down resistor | | | | kΩ |
| | Balance off, open load detect disabled | — | 2.0 | — | |


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**Table 9. Static and dynamic electrical characteristics**...*continued*

*Characteristics noted under conditions 9.6 V ≤ $V_{PWR}$ ≤ 63 V, −40 °C ≤ $T_A$ ≤ 105 °C, GND = 0 V, unless otherwise stated. Typical values refer to $V_{PWR}$ = 56 V, $T_A$ = 25 °C, unless otherwise noted.*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $I_{OUT(LKG)}$ | Output leakage current<br>Balance off, open load detect disabled at $V_{DS}$ = 4.0 V | <br>— | <br>— | <br>1.0 | µA |
| $R_{DS(on)}$ | Drain-to-source on resistance<br>$I_{OUT}$ = 300 mA, $T_J$ = 105 °C<br>$I_{OUT}$ = 300 mA, $T_J$ = 25 °C<br>$I_{OUT}$ = 300 mA, $T_J$ = −40 °C | <br>—<br>—<br>— | <br>—<br>0.5<br>0.4 | <br>0.80<br>—<br>— | Ω |
| $I_{LIM_CB}$ | Driver current limitation (shorted resistor) | 310 | — | 950 | mA |
| $t_{CB_AUTOP}$ | CB_AUTO_PAUSE timing | — | 4.0 | — | µs |
| $t_{ON}$ | Cell balance driver turn on<br>$R_L$ = 15 Ω | <br>— | <br>350 | <br>— | µs |
| $t_{OFF}$ | Cell balance driver turn off<br>$R_L$ = 15 Ω | <br>— | <br>200 | <br>— | µs |
| $t_{BAL_DEGLICTH}$ | Short/open detect filter time | — | 20 | — | µs |
| **Internal temperature measurement** | | | | | |
| IC_TEMP1_ERR | IC temperature measurement error | −3.0 | — | 3.0 | K |
| IC_TEMP1_RES | IC temperature resolution | — | 0.032 | — | K/LSB |
| TSD_TH | Thermal shutdown | — | 170 | — | °C |
| TSD_HYS | Thermal shutdown hysteresis | — | 10 | — | °C |
| **Default operational parameters** | | | | | |
| $V_{CTOV(TH)}$ | Cell overvoltage threshold (8 bits), typical value is default value after reset | 0.0 | 4.2 | 5.0 | V |
| $V_{CTOV(RES)}$ | Cell overvoltage threshold resolution | — | 19.53125 | — | mV/LSB |
| $V_{CTUV(TH)}$ | Cell undervoltage threshold (8 bits), typical value is default value after reset | 0.0 | 2.5 | 5.0 | V |
| $V_{CTUV(RES)}$ | Cell undervoltage threshold resolution | — | 19.53125 | — | mV/LSB |
| $V_{GPIO_OT(TH)}$ | GPIOx configured as ANx input overtemperature threshold from POR | — | 1.16 | — | V |
| $V_{GPIO_OT(RES)}$ | Temperature voltage threshold resolution | — | 4.8828125 | — | mV/LSB |
| $V_{GPIO_UT(TH)}$ | GPIOx configured as ANx input undertemperature threshold from POR | — | 3.82 | — | V |
| $V_{GPIO_UT(RES)}$ | Temperature voltage threshold resolution | — | 4.8828125 | — | mV/LSB |
| **General purpose input/output GPIOx** | | | | | |
| $V_{IH}$ | Input high-voltage (3.3 V compatible) | 2.0 | — | — | V |
| $V_{IL}$ | Input low-voltage (3.3 V compatible) | — | — | 1.0 | V |
| $V_{HYS}$ | Input hysteresis | — | 100 | — | mV |
| $I_{IL}$ | Input leakage current<br>Pins tristate, $V_{IN}$ = $V_{COM}$ or AGND | <br>−100 | <br>— | <br>100 | nA |
| $I_{IDL}$ | Differential Input Leakage Current GPIO 5,6<br>GPIO 5,6 configured as digital inputs for current measurement | <br>−30 | <br>— | <br>30 | nA |
| $V_{OH}$ | Output high-voltage $I_{OH}$ = −0.5 mA | $V_{COM}$ − 0.8 | — | — | V |
| $V_{OL}$ | Output low-voltage $I_{OL}$ = +0.5 mA | — | — | 0.8 | V |
| $V_{ADC}$ | Analog ADC input voltage range for ratiometric measurements | AGND | — | $V_{COM}$ | V |


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**Table 9. Static and dynamic electrical characteristics**...*continued*

*Characteristics noted under conditions 9.6 V ≤ $V_{PWR}$ ≤ 63 V, −40 °C ≤ $T_A$ ≤ 105 °C, GND = 0 V, unless otherwise stated. Typical values refer to $V_{PWR}$ = 56 V, $T_A$ = 25 °C, unless otherwise noted.*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL(TH)}$ | Analog input open pin detect threshold | — | 0.15 | — | V |
| $R_{OPENPD}$ | Internal open detection pull-down resistor | 3.8 | 5.0 | — | kΩ |
| $t_{GPIO0_WU}$ | GPIO0 WU de-glitch filter | — | 50 | — | µs |
| $t_{GPIO0_FLT}$ | GPIO0 daisy chain de-glitch filter both edges | — | 20 | — | µs |
| $t_{GPIO2_SOC}$ | GPIO2 convert trigger de-glitch filter | — | 2.0 | — | µs |
| $t_{GPIOx_DIN}$ | GPIOx configured as digital input de-glitch filter | 2.5 | — | 5.6 | µs |
| **Reset input** | | | | | |
| $V_{IH_RST}$ | Input high-voltage (3.3 V compatible) | 2.0 | — | — | V |
| $V_{IL_RST}$ | Input low-voltage (3.3 V compatible) | — | — | 1.0 | V |
| $V_{HYS}$ | Input hysteresis | — | 0.6 | — | V |
| $t_{RESETFLT}$ | RESET de-glitch filter | — | 100 | — | µs |
| $R_{RESET_PD}$ | Input logic pull down (RESET) | — | 100 | — | kΩ |
| **SPI_COM_EN input** | | | | | |
| $V_{IH}$ | Input high-voltage (3.3 V compatible) | 2.0 | — | — | V |
| $V_{IL}$ | Input low-voltage (3.3 V compatible) | — | — | 1.0 | V |
| $V_{HYS}$ | Input hysteresis | — | 450 | — | mV |
| $R_{SPI_COM_EN_PD}$ | Input pull-down resistor (SPI_COM_EN) | — | 100 | — | kΩ |
| **Bus switch for TPL communication** | | | | | |
| $RX_{TERM}$ | Bus termination resistor (open resistor when bus switch is closed) | — | 150 | — | Ω |
| Remark: If the bus switch is closed, then the termination resistor is open, else the termination resistor is connected. At the end of the daisy chain, the switch must be open, so that the transmission line is properly terminated. | | | | | |
| **Digital interface** | | | | | |
| $V_{FAULT_HA}$ | FAULT output (high active, IOH = 1.0 mA) | 4.0 | 4.9 | 6.0 | V |
| $I_{FAULT_CL}$ | FAULT output current limit | 3.0 | — | 40 | mA |
| $R_{FAULT_PD}$ | FAULT output pull-down resistance | — | 100 | — | kΩ |
| $V_{IH_COMM}$ | Voltage threshold to detect the input as high<br>SI/RDTX_IN+, SCLK/RDTX_IN–, CSB, SDA, SCL (NOTE: needs to be 3.3 V compatible) | — | — | 2.0 | V |
| $V_{IL_COMM}$ | Voltage threshold to detect the input as low<br>SI/RDTX_IN+, SCLK/RDTX_IN–, CSB, SDA, SCL | 0.8 | — | — | V |
| $V_{HYS}$ | Input hysteresis<br>SI/RDTX_IN+, SCLK/RDTX_IN−, CSB, SDA, SCL | — | 80 | — | mV |
| $I_{LOGIC_SS}$ | Sleep state input logic current<br>CSB | −100 | — | 100 | nA |
| $R_{SCLK_PD}$ | Input logic pull-down resistance (SCLK/RDTX_IN–, SI/RDTX+) | — | 20 | — | kΩ |
| $R_{I_PU}$ | Input logic pull-up resistance to $V_{COM}$ (CSB, SDA, SCL) | — | 100 | — | kΩ |
| $I_{SO_TRI}$ | Tristate SO input current 0 V to $V_{COM}$ | −2.0 | — | 2.0 | µA |
| $V_{SO_HIGH}$ | SO high-state output voltage with $I_{SO(HIGH)}$ = −2.0 mA | $V_{COM}$ − 0.4 | — | — | V |
| $V_{SO_LOW}$ | SO, SDA, SLK low-state output voltage with $I_{SO(HIGH)}$ = −2.0 mA | — | — | 0.4 | V |
| $CSB_{WU_FLT}$ | CSB wake-up de-glitch filter, low to high transition | — | 50 | — | µs |


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**Table 9. Static and dynamic electrical characteristics**...*continued*

*Characteristics noted under conditions 9.6 V ≤ $V_{PWR}$ ≤ 63 V, −40 °C ≤ $T_A$ ≤ 105 °C, GND = 0 V, unless otherwise stated. Typical values refer to $V_{PWR}$ = 56 V, $T_A$ = 25 °C, unless otherwise noted.*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **System timing** | | | | | |
| $t_{CELL_CONV}$ | Time needed to acquire all 14 cell voltages and the current after an on demand conversion | | | | µs |
| | 13-bit resolution | — | 59 | — | |
| | 14-bit resolution | — | 80 | — | |
| | 15-bit resolution | — | 123 | — | |
| | 16-bit resolution | — | 208 | — | |
| $t_{SYNC}$ | V/I synchronization time | | | | µs |
| | ADC1-A,B at 13 bit, ADC2 at 13 bit | — | 48.16 | — | |
| | ADC1-A,B at 14 bit, ADC2 at 13 bit | — | 53.50 | — | |
| | ADC1-A,B at 15 bit, ADC2 at 13 bit | — | 64.16 | — | |
| | ADC1-A,B at 16 bit, ADC2 at 13 bit | — | 85.50 | — | |
| $t_{SYNC}$ | V/I synchronization time | | | | µs |
| | ADC1-A,B at 13 bit, ADC2 at 14 bit | — | 52.14 | — | |
| | ADC1-A,B at 14 bit, ADC2 at 14 bit | — | 57.48 | — | |
| | ADC1-A,B at 15 bit, ADC2 at 14 bit | — | 68.14 | — | |
| | ADC1-A,B at 16 bit, ADC2 at 14 bit | — | 89.48 | — | |
| $t_{SYNC}$ | V/I synchronization time | | | | µs |
| | ADC1-A,B at 13 bit, ADC2 at 15 bit | — | 62.12 | — | |
| | ADC1-A,B at 14 bit, ADC2 at 15 bit | — | 65.46 | — | |
| | ADC1-A,B at 15 bit, ADC2 at 15 bit | — | 76.12 | — | |
| | ADC1-A,B at 16 bit, ADC2 at 15 bit | — | 97.46 | — | |
| $t_{SYNC}$ | V/I synchronization time | | | | µs |
| | ADC1-A,B at 13 bit, ADC2 at 16 bit | — | 120.51 | — | |
| | ADC1-A,B at 14 bit, ADC2 at 16 bit | — | 117.84 | — | |
| | ADC1-A,B at 15 bit, ADC2 at 16 bit | — | 112.51 | — | |
| | ADC1-A,B at 16 bit, ADC2 at 16 bit | — | 113.39 | — | |
| $t_{VPWR(READY)}$ | Time after VPWR connection for the IC to be ready for initialization | — | — | 5.0 | ms |
| $t_{WAKE-UP}$ | Sleep mode to normal mode device ready | | | | µs |
| | Wake-up from fault | — | — | 400 | |
| | Wake-up from GPIO | — | — | 400 | |
| | Wake-up from network | — | — | 400 | |
| | Wake-up from CSB | — | — | 400 | |
| | Sleep mode to normal mode time after TPL bus wake-up | — | — | 1.0 | ms |
| $t_{WAKE_DELAY}$ | Time between wake pulses | — | 600 | — | µs |
| $t_{NOWUP}$ | Time, starting from the first SOM received, to go back to Sleep/Idle mode time after receiving incomplete TPL bus wake-up sequence | — | — | 1.3 | ms |
| $t_{IDLE}$ | Idle timeout after POR | — | 60 | — | s |
| $t_{WAKE_INIT}$ | Wake-up signaling timeout after POR | — | 0.65 | — | s |
| $t_{BALANCE}$ | Cell balance timer range | 0.5 | — | 511 | min |
| $t_{CYCLE}$ | Cyclic acquisition timer range | 0.0 | — | 8.5 | s |
| $t_{FAULT}$ | Fault detection to activation of fault pin | | | | µs |
| | Normal mode | — | — | 56 | |
| $t_{DIAG}$ | Diagnostic mode timeout | 0.047 | 1.0 | 8.5 | s |


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**Table 9. Static and dynamic electrical characteristics**...*continued*

*Characteristics noted under conditions 9.6 V ≤ $V_{PWR}$ ≤ 63 V, −40 °C ≤ $T_A$ ≤ 105 °C, GND = 0 V, unless otherwise stated. Typical values refer to $V_{PWR}$ = 56 V, $T_A$ = 25 °C, unless otherwise noted.*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{EOC}$ | SOC to data ready (includes post processing of data) | | | | µs |
| | 13-bit resolution | — | 148 | — | |
| | 14-bit resolution | — | 201 | — | |
| | 15-bit resolution | — | 307 | — | |
| | 16-bit resolution | — | 520 | — | |
| $t_{SETTLE}$ | Time after SOC to begin converting with ADC1-A,B | — | 12.28 | — | µs |
| $t_{SYS_MEAS1}$ | Time needed to send an SOC command and read back 96 cell voltages, 48 temperatures, 1 current, and 1 coulomb counter and ADC1-A,B configured as follows: | | | | ms |
| | 13-bit resolution | — | 3.73 | — | |
| | 14-bit resolution | — | 3.78 | — | |
| | 15-bit resolution | — | 3.89 | — | |
| | 16-bit resolution | — | 4.10 | — | |
| $t_{SYS_MEAS2}$ | Time needed to send an SOC command and read back 96 cell voltages, 1 current, and 1 coulomb counter and ADC1-A,B configured as follows: | | | | ms |
| | 13-bit resolution | — | 2.64 | — | |
| | 14-bit resolution | — | 2.69 | — | |
| | 15-bit resolution | — | 2.80 | — | |
| | 16-bit resolution | — | 3.01 | — | |
| $t_{CLST_TPL}$ | Time needed to send an SOC command and read back 14 cell voltages, 7 temperatures, 1 current, and 1 coulomb counter with TPL communication working at 2.0 Mbps and ADC1-A,B configured as follows: | | | | ms |
| | 13-bit resolution | — | 0.79 | — | |
| | 14-bit resolution | — | 0.85 | — | |
| | 15-bit resolution | — | 0.95 | — | |
| | 16-bit resolution | — | 1.16 | — | |
| $t_{CLST_SPI}$ | Time needed to send an SOC command and read back 14 cell voltages, 7 temperatures, 1 current, and 1 coulomb counter with SPI communication working at 4.0 Mbps and ADC1-A,B configured as follows: | | | | ms |
| | 13-bit resolution | — | 0.48 | — | |
| | 14-bit resolution | — | 0.54 | — | |
| | 15-bit resolution | — | 0.64 | — | |
| | 16-bit resolution | — | 0.86 | — | |
| $t_{I2C_DOWNLOAD}$ | Time to download EEPROM calibration after POR | — | — | 1.0 | ms |
| $t_{I2C_ACCESS}$ | EEPROM access time, EEPROM write (depends on device selection) | — | 5.0 | — | ms |
| $t_{WAVE_DC_BITx}$ | Daisy chain duty cycle off time | | | | µs |
| | $t_{WAVE_DC_BITx = 00}$ | — | 500 | — | |
| $t_{WAVE_DC_BITx}$ | Daisy chain duty cycle off time | | | | ms |
| | $t_{WAVE_DC_BITx = 01}$ | — | 1.0 | — | |
| $t_{WAVE_DC_BITx}$ | Daisy chain duty cycle off time | | | | ms |
| | $t_{WAVE_DC_BITx = 10}$ | — | 10 | — | |
| $t_{WAVE_DC_BITx}$ | Daisy chain duty cycle off time | | | | ms |
| | $t_{WAVE_DC_BITx = 11}$ | — | 100 | — | |
| $t_{WAVE_DC_ON}$ | Daisy chain duty cycle on time | — | 500 | 550 | µs |


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**Table 9. Static and dynamic electrical characteristics**...*continued*

*Characteristics noted under conditions 9.6 V ≤ $V_{PWR}$ ≤ 63 V, −40 °C ≤ $T_A$ ≤ 105 °C, GND = 0 V, unless otherwise stated. Typical values refer to $V_{PWR}$ = 56 V, $T_A$ = 25 °C, unless otherwise noted.*

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{COM_LOSS}$ | Time out to reset the IC in the absence of communication | | — | 1024 | — | ms |
| **SPI interface** | | | | | | |
| $F_{SCK}$ | CLK/RDTX_IN– frequency | [1] | — | — | 4.0 | MHz |
| $t_{SCK_H}$ | SCLK/RDTX_IN– high time (A) | [1] | 125 | — | — | ns |
| $t_{SCK_L}$ | SCLK/RDTX_IN– high time (B) | [1] | 125 | — | — | ns |
| $t_{SCK}$ | SCLK/RDTX_IN− period (A+B) | [1] | 250 | — | — | ns |
| $t_{FALL}$ | SCLK/RDTX_IN− falling time | | — | — | 15 | ns |
| $t_{RISE}$ | SCLK/RDTX_IN− rising time | | — | — | 15 | ns |
| $t_{SET}$ | SCLK/RDTX_IN− setup time (O) | [1] | 20 | — | — | ns |
| $t_{HOLD}$ | SCLK/RDTX_IN– hold time (P) | [1] | 20 | — | — | ns |
| $t_{SI_SETUP}$ | SI/RDTX_IN+ setup time (F) | [1] | 40 | — | — | ns |
| $t_{SI_HOLD}$ | SI/RDTX_IN+ hold time (G) | [1] | 40 | — | — | ns |
| $t_{SO_VALID}$ | SO data valid, rising edge of SCLK/RDTX_IN− to SO data valid (I) | [1] | — | — | 40 | ns |
| $t_{SO_EN}$ | SO enable time (H) | [1] | — | — | 40 | ns |
| $t_{SO_DISABLE}$ | SO disable time (K) | [1] | — | — | 40 | ns |
| $t_{CSB_LEAD}$ | CSB lead time (L) | [1] | 100 | — | — | ns |
| $t_{CSB_LAG}$ | CSB lag time (M) | [1] | 100 | — | — | ns |
| $t_{TD}$ | Sequential data transfer delay (N) | [1] | 1.0 | — | — | µs |
| **TPL interface** | | | | | | |
| $V_{RDTX\ INTH}$ | Differential receiver threshold | | — | 580 | — | mV |
| $V_{RDTX\ INHYS}$ | Differential receiver threshold hysteresis | | — | 100 | — | mV |
| $t_{RES}$ | Slave response after write command (echo) | | — | 2.35 | — | µs |

[1] See the timing diagram in Figure 4

## 7.5 Timing diagrams

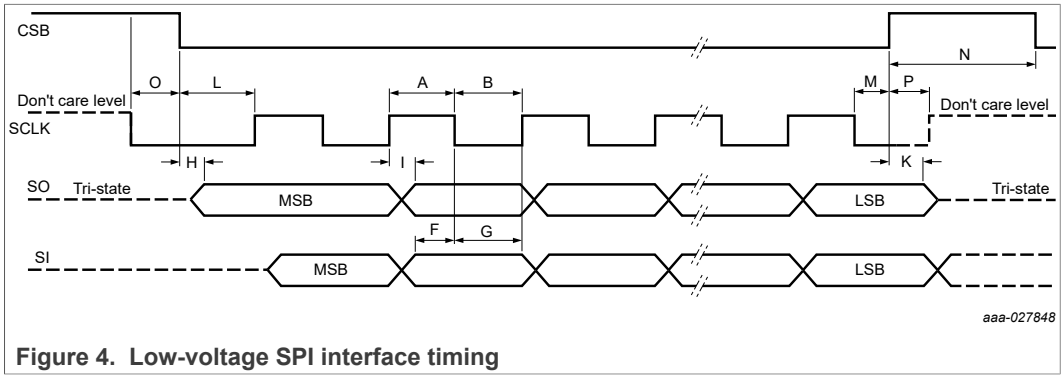


**Figure 4. Low-voltage SPI interface timing**


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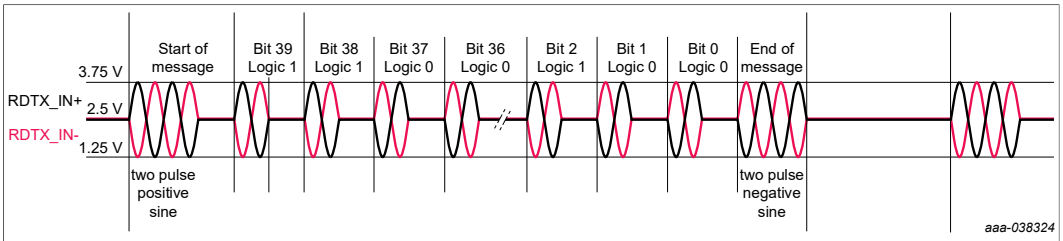


**Figure 5. Transformer communication signaling**


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# 8 Packaging

## 8.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

**Table 10. Package Outline**

| Package | Suffix | Package outline drawing number |
|---|---|---|
| 64-pin LQFP-EP | AE | 98ASA10763D |


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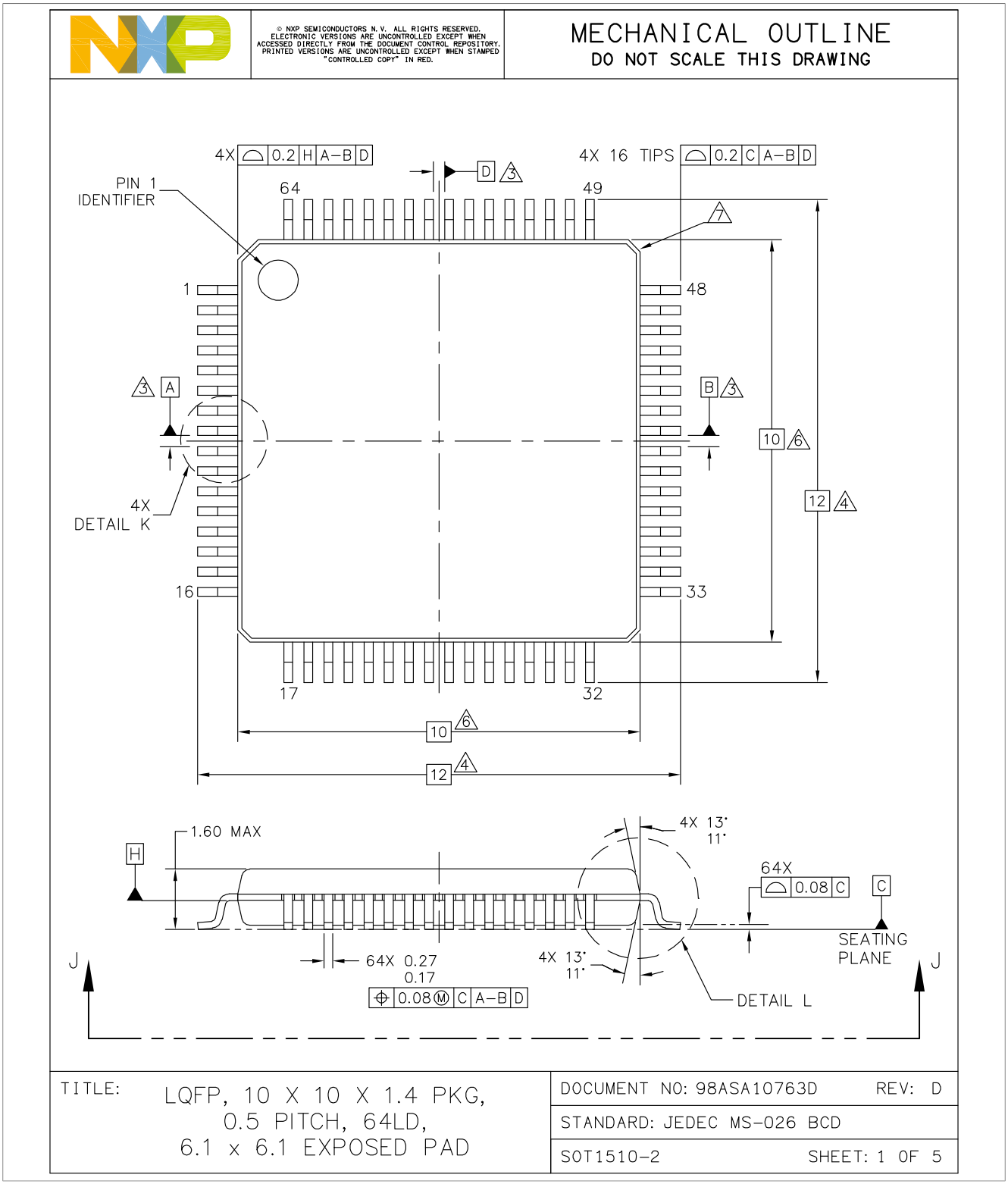



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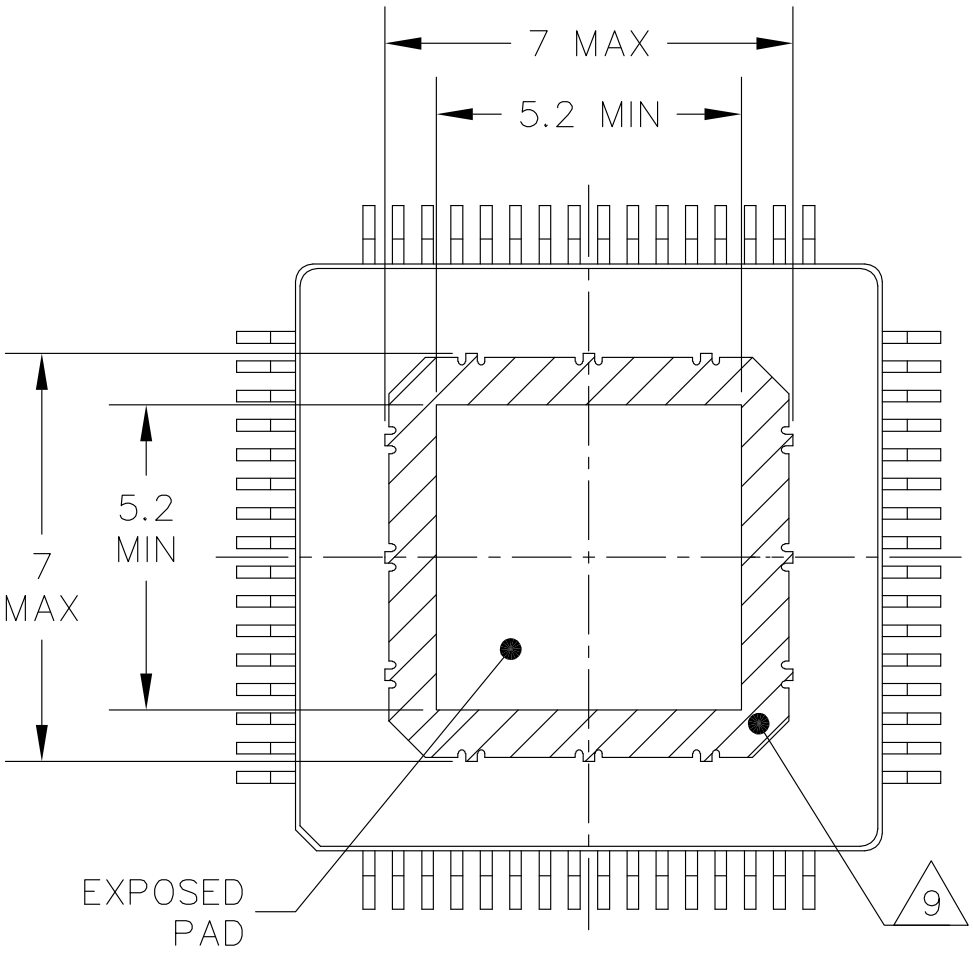
MECHANICAL OUTLINE
DO NOT SCALE THIS DRAWING




VIEW J–J

| | | |
|---|---|---|
| TITLE: LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD | DOCUMENT NO: 98ASA10763D | REV: D |
| | STANDARD: JEDEC MS-026 BCD | |
| | SOT1510-2 | SHEET: 2 |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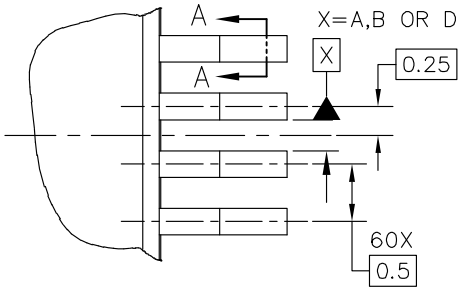
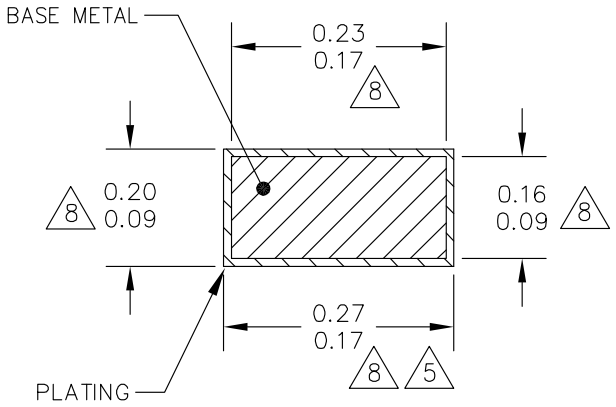
# MECHANICAL OUTLINE

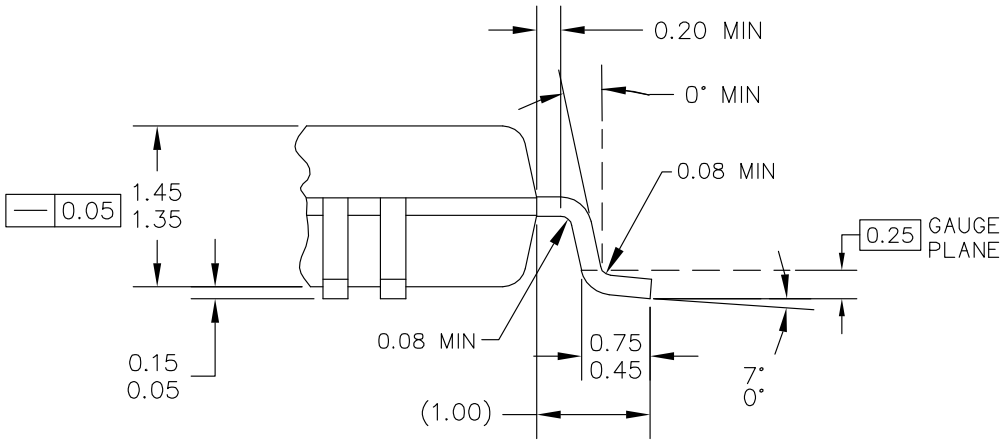
DO NOT SCALE THIS DRAWING




DETAIL K




SECTION A–A
64 PLACES
ROTATED 90° CLOCKWISE




DETAIL L

| | |
|---|---|
| TITLE: LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD | DOCUMENT NO: 98ASA10763D REV: D |
| | STANDARD: JEDEC MS-026 BCD |
| | SOT1510-2 SHEET: 3 |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MECHANICAL OUTLINE

DO NOT SCALE THIS DRAWING

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 MM.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.25 MM FROM THE LEAD TIP.
9. HATCHED AREA TO BE KEEP OUT ZONE FOR PCB ROUTING.

| | | |
|---|---|---|
| TITLE: | LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD | DOCUMENT NO: 98ASA10763D REV: D |
| | | STANDARD: JEDEC MS-026 BCD |
| | | SOT1510-2 SHEET: 4 |

**Figure 6. Package outline**


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# 9 Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| MC33771BSDS v.7.0 | 20210503 | Product data sheet | — | MC33771BSDS v.6.0 |
| Modifications: | Updated to align with full data sheet, MC33771B v.7.0 | | | |
| MC33771BSDS v.6.0 | 20200622 | Product data sheet | — | MC33771BSDS v.5.0 |
| Modifications: | Updated to align with full data sheet, MC33771B v.6.0 | | | |
| MC33771BSDS v.5.0 | 20180502 | Technical data | — | MC33771BSDS v.1 |
| Modifications: | Updated to align with full data sheet, MC33771B v.5.0 | | | |
| MC33771BSDS v.1 | 20180419 | Product preview | — | — |


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# 10 Legal information

## 10.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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**Date of release: 10 May 2021**
**Document identifier: MC33771BSDS**

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