# MC33665A

## Battery management communication gateway

Rev. 3 — 29 July 2022 Product short data sheet

# 1 Product profile

## 1.1 General description

The MC33665A is a general-purpose battery management communication gateway and transport protocol link (TPL) transceiver. The device forwards messages upcoming from different TPL (isolated daisy chain protocol of NXP) ports through a standard communication protocol. The standard communication protocol ensures compatibility with microcontrollers available in the market. The MC33665A is designed as a gateway for serial peripheral interface (SPI), CAN (FD) or universal asynchronous receiver transmitter (UART) to TPL.

In the SPI or UART variant, the device communicates directly to the MCU by using SPI or UART. The MC33665A transfers messages between MCU and battery management system (BMS) devices connected to integrated TPL ports.

In the CAN FD variant, the MC33665A can be communicated with controller area network (CAN) and CAN FD to send and receive messages to BMS devices connected on TPL ports. The device powers an external CAN transceiver to be a part of a CAN bus.

The MC33665A provides four TPL ports to communicate with other isolated BMS devices in the daisy chain. Each daisy chain port supports capacitive and inductive isolated communication, based on device capabilities use NXP battery cell controllers like MC33771C, MC33772C, and MC33775A. The MC33665A was developed following AEC-Q100 grade 1, automotive quality management (QM) device. The MC33665A is suitable to be used in safety critical applications up to ASIL D level.

## 1.2 Features and benefits

- MCU host interface supporting SPI, CAN (FD) or UART
  - SPI
    - Single or dual SPI mode
    - Up to 10 Mbit/s data rate
  - CAN (FD)
    - CAN up to 1 Mbit/s data rate
    - CAN FD up to 5 Mbit/s data rate
  - UART
    - Full duplex operation
    - Auto baud rate detection
    - Up to 6 MBd data rate
  - Selectable IO voltage of 5 V or 3.3 V
- Message buffering
  - Configurable response and request buffers

  - Status/handshake signals for data flow control
- Communication management unit
  - Error detection and reporting
- Multi-port TPL interface
  - Four independent TPL daisy chain ports
  - Automatic message routing based on address of TPL message
  - Support up to four TPL daisy chains and 62 nodes per chain
  - Each daisy chain features:
    - 2 Mbit/s data rate
    - Two-wire daisy chain supporting capacitive or inductive isolation
    - Loopback support
  - Compatible with TPL2 based products (for example MC33771C or MC33772C)
  - Compatible with TPL3 based products (for example MC33775A)
- Message synchronization
  - Enables synchronization of messages across all TPL daisy chain ports
  - Transmission of messages triggered by external event (SYNC)
  - Programmable time delay between messages
- Power supply options
  - Supply via external 5 V regulator or integrated 5 V regulator
  - Power mode management of the external CAN (FD) transceiver
- Operation modes
  - Active mode
  - Sleep mode (25 µA typ.)
- Wake-up of the device by
  - TPL daisy chain
  - MCU communication
  - Wake-up input
- Supports internal oscillator with or without external crystal
- General-purpose inputs/outputs (GPIOs) with assignable status and events
- $I^2C$-bus master interface to control external devices, for example, EEPROMs and security ICs
- Unique device ID
- AEC-Q100 grade 1 qualified: −40 °C to +125 °C ambient temperature range
- Suitable to be used in safety critical applications up to ASIL D level


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# 2 Ordering information

**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| MC33665ATS4AE | LQFP48 | plastic, low profile quad flat leaded package; 48 terminals; 0.50 mm pitch; 7 × 7 × 1.4 mm body | SOT1571-1 |
| MC33665ATU4AE | LQFP48 | plastic, low profile quad flat leaded package; 48 terminals; 0.50 mm pitch; 7 × 7 × 1.4 mm body | SOT1571-1 |
| MC33665ATF4AE | LQFP48 | plastic, low profile quad flat leaded package; 48 terminals; 0.50 mm pitch; 7 × 7 × 1.4 mm body | SOT1571-1 |

## 2.1 Ordering options

**Table 2. Type numbers**

| Type number | Description |
|---|---|
| MC33665ATS4AE | SPI gateway with four TPL ports |
| MC33665ATU4AE | UART gateway with four TPL ports |
| MC33665ATF4AE | CAN FD gateway with four TPL ports |


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# 3 Block diagram

Figure 1 shows the general architecture of the MC33665A.

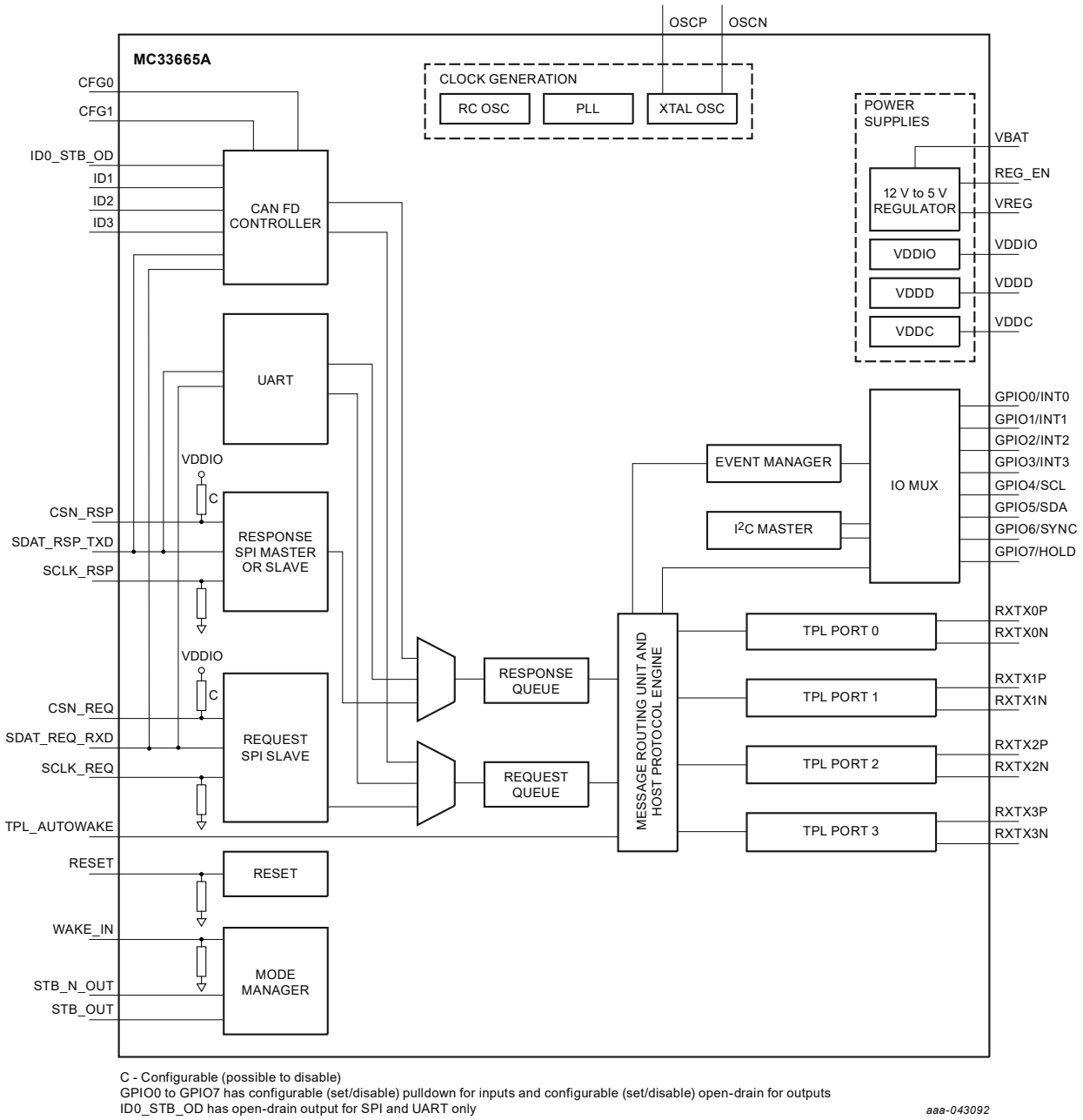


**Figure 1. Block diagram**


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# 4 Limiting values

**Table 3. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

*$T_{amb}$ = −40 °C to +125 °C; $T_j$ = −40 °C to +150 °C; all voltages are defined with respect to ground; positive currents flow into the IC.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{i(VBAT)}$ | input voltage on pin VBAT | | −0.3 | - | +40 | V |
| $V_{REG_EN}$ | voltage on pin REG_EN | | −0.3 | - | min ($V_{i(VBAT)}$ + 0.5, +40) | V |
| $V_{O(VREG)}$ | output voltage on pin VREG | | −0.3 | - | +5.8 | V |
| $V_{I(VDDD)}$ | input voltage on pin VDDD | | −0.3 | - | +5.8 | V |
| $V_{I(VDDC)}$ | input voltage on pin VDDC | | −0.3 | - | +5.8 | V |
| $V_{I(VDDIO)}$ | input voltage on pin VDDIO | | −0.3 | - | +5.8 | V |
| $V_{I(dig)}$ | digital input voltage | GPIO0 to GPIO7, ID1 to ID3, CFG0, CFG1, SDAT_REQ_ RXD, SDAT_RSP_TXD, CSN_ RSP, CSN_ REQ, SCLK_REQ, SCLK_RSP, STB_N_OUT, STB_OUT, TPL_AUTOWAKE | −0.3 | - | min ($V_{VDDIO}$ + 0.5, 5.8) | V |
| | | ID0_STB_OD for CAN FD | −0.3 | - | min ($V_{VDDIO}$ + 0.5, +5.8) | V |
| | | ID0_STB_OD for SPI or UART | −0.3 | - | +5.8 | V |
| $V_{I(WAKE_IN)}$ | input voltage on pin WAKE_IN | maximum limits | −0.3 | - | +40 | V |
| $V_{i(OSCP)}$ | input voltage on pin OSCP | | −0.3 | - | +5.8 | V |
| $V_{i(OSCN)}$ | input voltage on pin OSCN | | −0.3 | - | +2.75 | V |
| $V_{bus(TPL)}$ | voltage on TPL communication bus pins | RXTX0N, RXTX0P, RXTX1N, RXTX1P, RXTX2N, RXTX2P, RXTX3N, RXTX3P; Relative to VSSC | −10 | - | +10 | V |
| $V_{I(RESET)}$ | input voltage on pin RESET | maximum limits | −0.3 | - | +5.8 | V |
| $T_j$ | junction temperature | | −40 | - | +165 | °C |
| $T_{stg}$ | storage temperature | | −55 | - | +150 | °C |
| $T_{reflow(peak)}$ | peak reflow temperature | pin soldering temperature limit is maximum 10 s duration; not designed for immersion soldering; exceeding these limits may cause a malfunction or permanent damage to the device [1] | - | - | 260 | °C |


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[1] Package reflow capability of NXP meets Pb-free requirements for JEDEC standard J-STD-020C. For peak package reflow temperature and moisture sensitivity level (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts, and review parametrics.

# 5 Revision history

**Table 4. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| MC33665A_SDS v.3 | 20220729 | Product short data sheet | - | MC33665A_SDS v.2 |
| MC33665A_SDS v.2 | 20220414 | Product short data sheet | - | MC33665A_SDS v.1 |
| MC33665A_SDS v.1 | 20211216 | Preliminary short data sheet | - | - |


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|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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