InnoSwitch3-MX Family

Off-Line Multiple Output QR Flyback Switcher IC with Integrated 650 V, 725 V or 750 V Switch, Synchronous Rectification and FluxLink Feedback

Product Highlights

Based on InnoSwitch3

- High efficiency across full load range
- Incorporates a multi-mode Quasi-Resonant (QR) / CCM flyback controller, 650 V, 725 V or 750 V switch, secondary-side sensing and synchronous rectification driver
- PowiGaN™ technology – up to 85 W without heat sink (INN3478C, INN3479C and INN3470C)
- Integrated FluxLink™, HIPOT-isolated, feedback link
- Instantaneous transient response ±5% CV with 0%-100%-0% load step
- Partner IC to InnoMux

EcoSmart™ – Energy Efficient

- Easily meets all global energy efficiency regulations
- Low heat dissipation

Advanced Protection / Safety Features

- Primary sensed output OVP
- Open SR FET gate detection
- Hysteretic thermal shutdown
- Input voltage monitor with accurate brown-in/brown-out and overvoltage protection

Full Safety and Regulatory Compliance

- Reinforced insulation
- Isolation voltage >4000 VAC
- 100% production HIPOT compliance testing
- UL1577 and TUV (EN60950) safety approved
- Enables designs that have "A" performance criteria for EN61000-4 suite of test standards, including EN61000-4-2, 4-3 (30 V/m), 4-4, 4-5, 4-6, 4-8 (100 A/m) and 4-9 (1000 A/m)

Green Package

- Halogen free and RoHS compliant

Applications

- Use with InnoMux for Energy Star 8, CEC, and 2021/2023 EU labeling for monitors and TVs

Description

The InnoSwitch™3-MX together with InnoMux dramatically improves system efficiency by eliminating the boost and buck converter stages. It also simplifies the development and manufacturing of multiple output power supplies, particularly those in compact enclosures or with high efficiency requirements. The InnoSwitch3-MX architecture is revolutionary in that the devices incorporate both primary and secondary controllers, with sense elements and a safety-rated feedback mechanism into a single IC.

Close component proximity and innovative use of the integrated communication link, FluxLink, permit accurate control of a secondary-side synchronous rectification MOSFET with Quasi-Resonant switching of primary integrated high-voltage switch to maintain high efficiency across the entire load range.

This version of InnoSwitch3 is intended to be used with InnoMux for multiple output, single-stage power supplies for monitors and TVs. This enables very high system efficiency on a small PCB foot print.

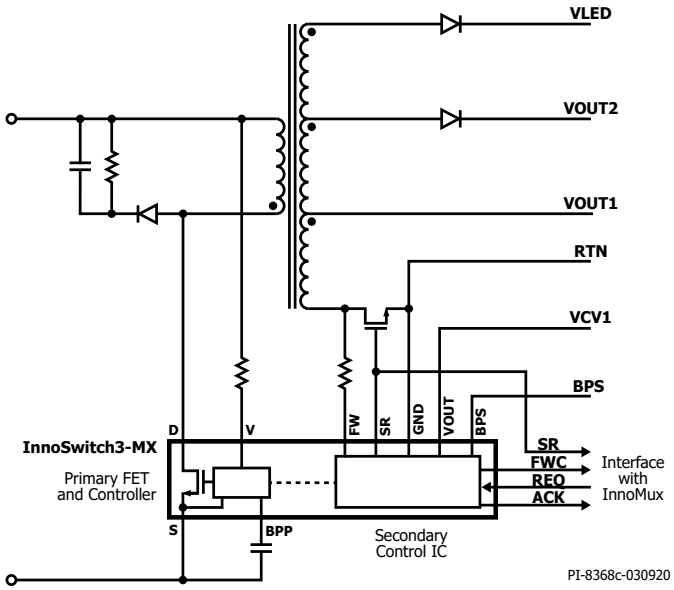


Figure 1. Typical Application/Performance.



Figure 2. High Creepage, Safety-Compliant InSOP-24D Package. Wave Solder or Reflow Process.

Output Power Table

Product[3]	BV Rating	85-265 VAC	
		Nominal Continuous[1]	Max Continuous[2]
INN3464C	650 V	18 W	23 W
INN34x5C	650 / 725 V	22 W	28 W
INN34x6C	650 / 725 V	28 W	35 W
INN34x7C	650 / 725 V	35 W	44 W
INN3468C	650 V	40 W	50 W
INN3478C	750 V	55 W	65 W
INN3479C	750 V	65 W	75 W
INN3470C	750 V	75 W	85 W

Table 1. Output Power Table.
Notes:
1. Continuous power using nominal primary current limit in a typical open frame application at +50 °C ambient with adequate PCB thermal design to ensure package temperature <125 °C.
2. Continuous power using maximum primary current limit in a typical open frame application at +50 °C ambient with adequate heat sinking to ensure package temperature <125 °C.
3. Package: InSOP-24D.

This Product is Covered by Patents and/or Pending Patent Applications.

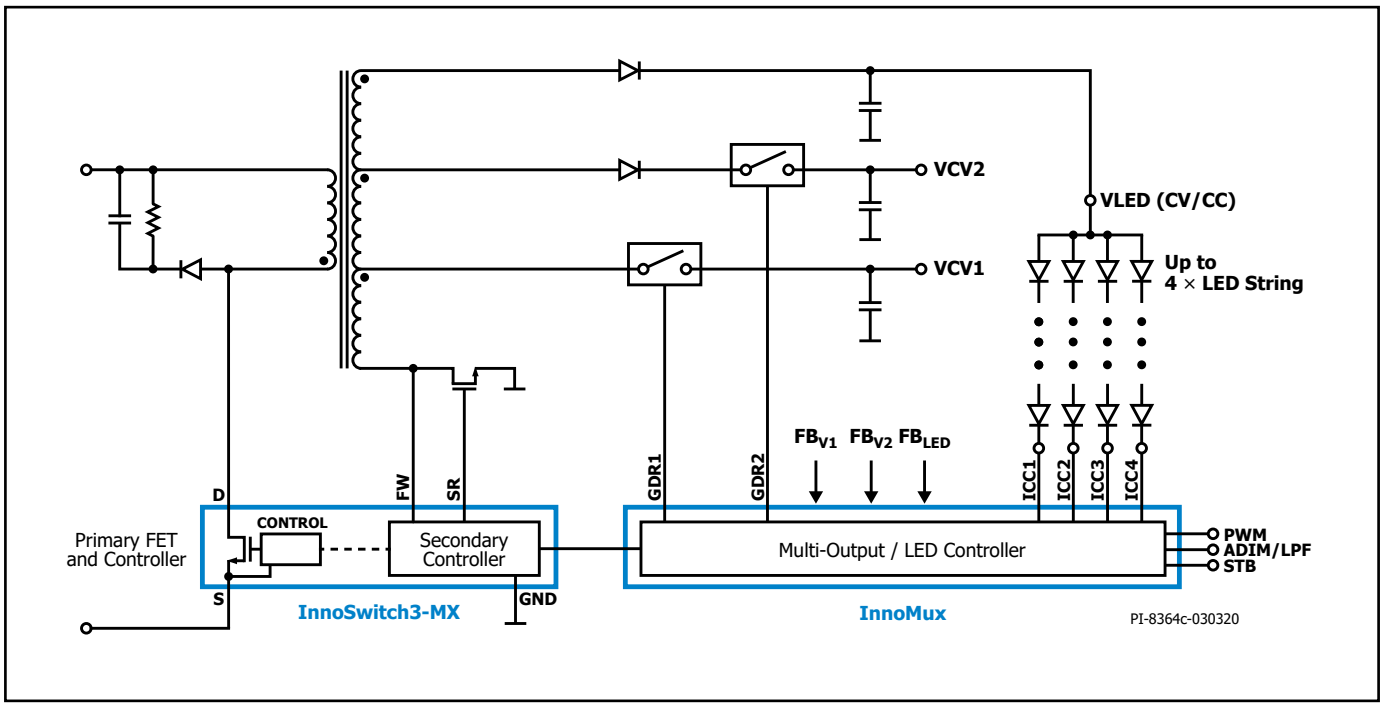


Figure 3. Simplified Schematic for Monitor / TV Application.

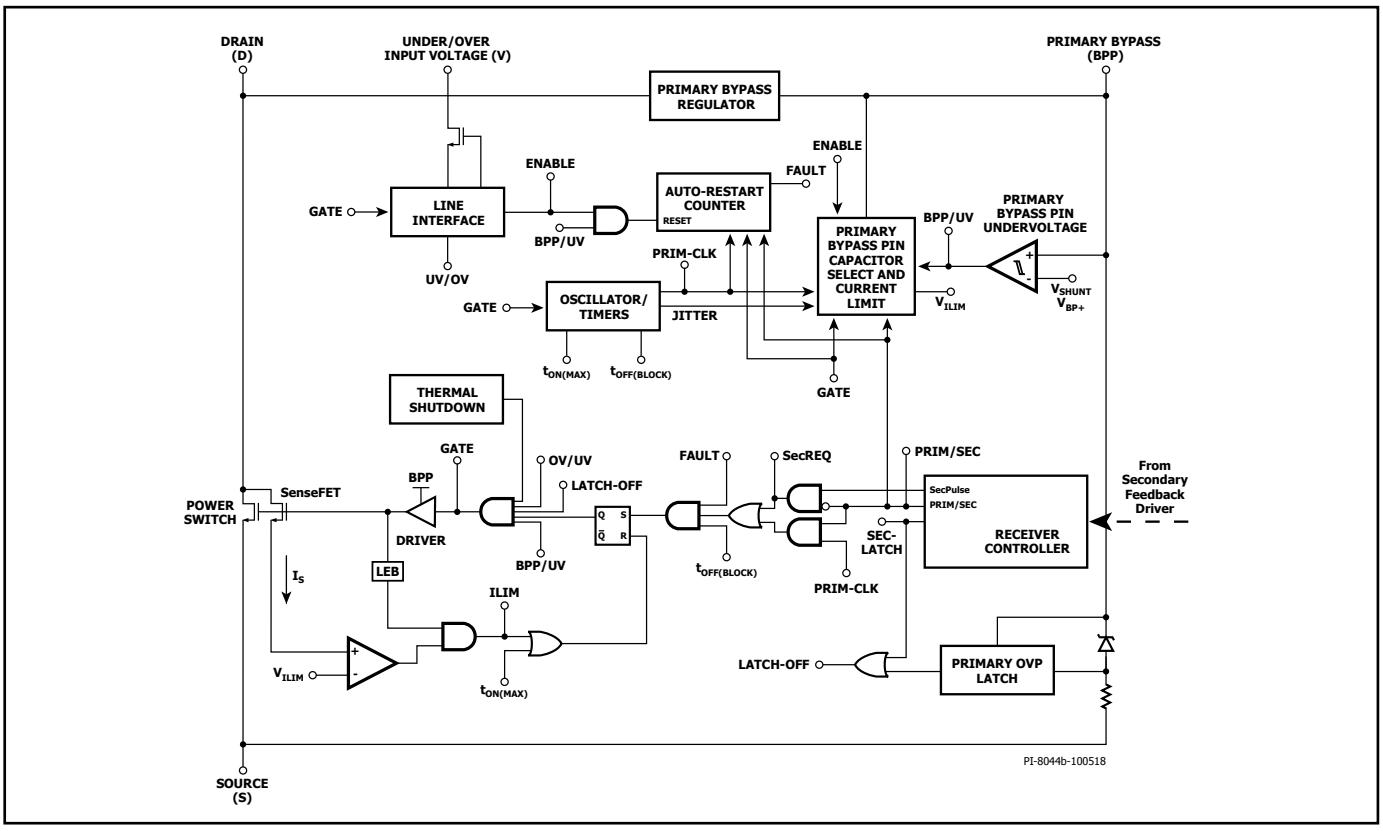


Figure 4. InnoSwitch3-MX Primary Block Diagram.

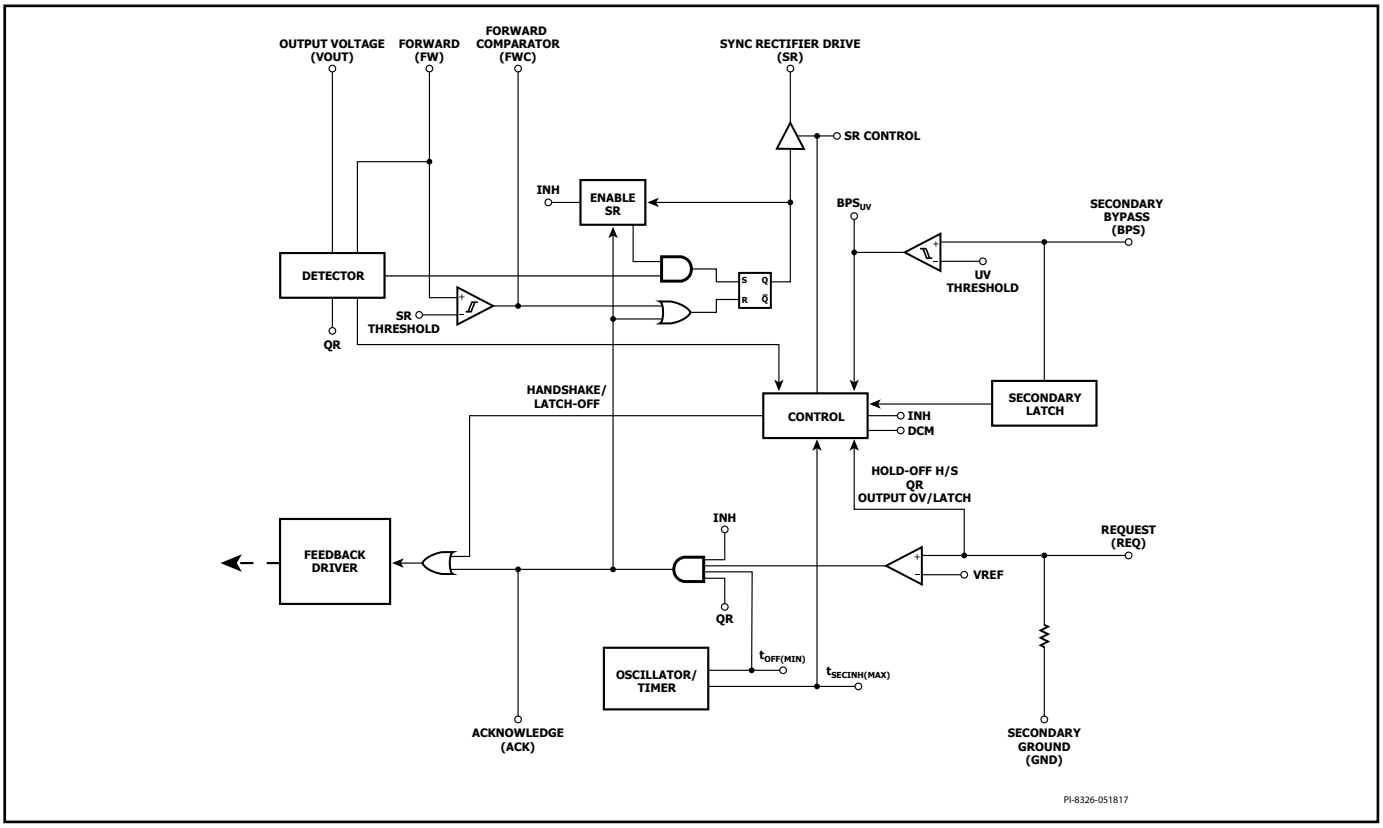


Figure 5. InnoSwitch3-MX Secondary Block Diagram.

Pin Functional Description

InnoSwitch3-MX

REQUEST (REQ) Pin (Pin 1)
Pulse request input. Should be connected to the InnoMux REQ output.

GROUND (GND) Pin (Pins 2 & 3)
All ground pins should be connected to secondary ground.

ACKNOWLEDGE (ACK) Pin (Pin 4)
Acknowledge to InnoMux that a request has been issued to the primary-side. Should be connected to the InnoMux ACK input.

FORWARD COMPARATOR (FWC) Pin (Pin 5)
Forward comparator output to InnoMux. Should be connected to the InnoMux FWC input.

SECONDARY BYPASS (BPS) Pin (Pin 6)
Supply pin for InnoSwitch3-MX. Must connect to BYPASS pin of InnoMux controller.

SYNCHRONOUS RECTIFIER DRIVE (SR) Pin (Pin 7)
SR drive output for synchronous rectifier. Should also be connected to InnoMux SR input.

OUTPUT VOLTAGE (VOUT) Pin (Pin 8)
Should be connected to VCV1 output.

FORWARD (FW) Pin (Pin 9)
Switching node of transformer for sensing.

NOT CONNECTED (NC) Pins (Pins 10, 11, and 12)
These pins are not connected and should be left floating.

UNDER/OVER INPUT VOLTAGE (V) Pin (Pin 13)
Input voltage sense.

PRIMARY BYPASS (BPP) Pin (Pin 14)
Internal voltage supply for primary-side controller.

NOT CONNECTED (NC) Pin (Pin 15)
This pin is not connected and should be left floating.

SOURCE (S) (Pins 16-19)
Internal power switch source connection.

DRAIN (D) (Pin 24)
High-voltage drain connection to internal power switch.

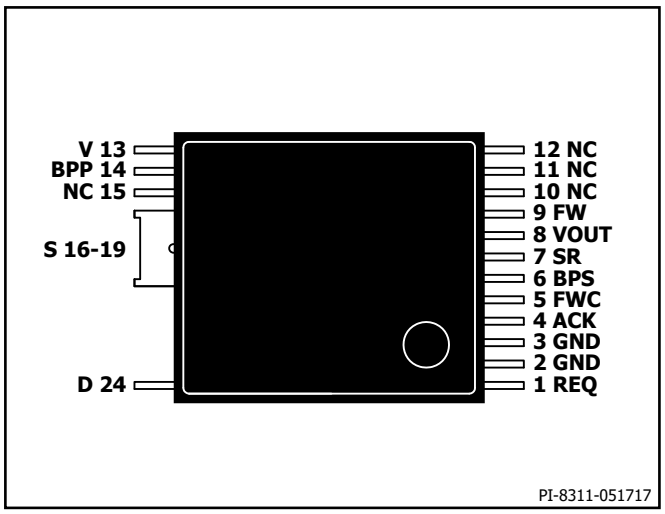


Figure 6. InnoSwitch3-MX Pin Configuration.

InnoSwitch3-MX Functional Description

The InnoSwitch3-MX combines a high-voltage power switch, along with both primary-side and secondary-side controllers in one device. The InnoSwitch3-MX is intended to be paired with an InnoMux controller.

The InnoSwitch3-MX architecture incorporates a novel inductive coupling feedback scheme using the package leadframe and bond wires to provide a safe, reliable, and low-cost means to accurately communicate power requests from the InnoMux controller to the primary controller.

The primary controller on InnoSwitch3-MX is a quasi-resonant (QR) flyback controller that has the ability to operate in continuous conduction mode (CCM). The controller uses a variable current control scheme. The primary consists of a jitter oscillator; a receiver circuit magnetically coupled to the secondary controller, a current limit controller, 5 V regulator on the PRIMARY BYPASS pin, audible noise reduction engine, bypass overvoltage detection circuit, a lossless input line sensing circuit, current limit selection circuitry, overvoltage protection, leading edge blanking, secondary output diode / SR MOSFET short protection circuit and a 650 V / 725 V / 750 V power switch.

The secondary controller consists of a transmitter circuit that is magnetically coupled to the primary receiver, synchronous rectifier (SR) MOSFET driver, timing functions and a host of integrated protection features.

Figures 4 and 5 show the functional block diagrams of the primary and secondary controllers with the most important features.

Primary Controller
InnoSwitch3-MX has variable frequency QR controller plus CCM/CrM/DCM operation for enhanced efficiency and extended output power capability.

PRIMARY BYPASS Pin Regulator
The PRIMARY BYPASS pin has an internal regulator that charges the PRIMARY BYPASS pin capacitor to V_{BPP} by drawing current from the DRAIN pin whenever the power switch is off. The PRIMARY BYPASS pin is the internal supply voltage node. When the power switch is on, the device operates from the energy stored in the PRIMARY BYPASS pin capacitor.

In addition, a shunt regulator clamps the PRIMARY BYPASS pin voltage to V_{SHUNT} when current is provided to the PRIMARY BYPASS pin through an external resistor. This allows the InnoSwitch3-MX to be powered externally through a bias winding, decreasing the no-load consumption and allowing meeting typical TV/Display application stand-by power requirements of 275 mW input power with 100 mW output load.

Primary Bypass ILIM Programming
InnoSwitch3-MX ICs allow the user to adjust primary current limit (I_{LIM}) settings through the selection of the PRIMARY BYPASS pin capacitor value. A ceramic capacitor can be used. There are 2 selectable capacitor sizes – 0.47 μF and 4.7 μF for setting standard and increased ILIM settings respectively. More information on which InnoSwitch3-MX support the adjustable current limit can be found in the parameters table.

Primary Bypass Undervoltage Threshold
The PRIMARY BYPASS pin undervoltage circuitry disables the power switch when the PRIMARY BYPASS pin voltage drops below ~4.5 V ($=V_{BPP} - V_{BPP(H)}$) in steady-state operation. Once the PRIMARY BYPASS pin voltage falls below this threshold, it must rise to $V_{BPP(SHUNT)}$ to re-enable turn-on of the power switch.

Primary Bypass Output Overvoltage Function
The PRIMARY BYPASS pin has an OV protection feature with either a latching or an auto-reset response. A Zener diode in parallel with the resistor in series with the PRIMARY BYPASS pin capacitor is typically used to detect an overvoltage on the primary bias winding and activate the protection mechanism. In the event that the current into the PRIMARY BYPASS pin exceeds I_{SD}, the device will latch-off or disable the power switch for a time $t_{AR(OFF)}$, after which time the controller will restart and attempt to return to regulation.

Output OV protection is also included as an integrated feature on the InnoMux controller.

Over-Temperature Protection

The thermal shutdown circuitry senses the primary switch die temperature. The threshold is set to T_{SD} with either a hysteretic or latch-off response.

Hysteretic response: If the die temperature rises above the threshold, the power switch is disabled and remains disabled until the die temperature falls by $T_{SD(H)}$ at which point switching is re-enabled. A large amount of hysteresis is provided to prevent over-heating of the PCB due to a continuous fault condition.

Latch-off response: If the die temperature rises above the threshold the power switch is disabled. The latching condition is reset by bringing the PRIMARY BYPASS pin below $V_{BPP(RESET)}$ or by going below the UNDER/OVER INPUT VOLTAGE pin UV (I_{UV-}) threshold.

Over-temperature protection is also included as an integrated feature on the InnoMux controller.

Current Limit Operation
The primary-side controller has a current limit threshold ramp that is inversely proportional to the time from the end of the previous primary switching cycle (i.e. from the time the primary switch turns off at the end of a switching cycle).

This characteristic produces a primary current limit that increases as the switching frequency (load) increases (Figure 7).

This algorithm enables the most efficient use of the primary switch with the benefit that this algorithm responds to digital feedback information immediately when a feedback switching cycle request is received.

At high load, switching cycles have a maximum current approaching 100% I_{LIM}. This gradually reduces to 30% of the full current limit as load decreases. Once 30% current limit is reached, there is no further reduction in current limit (since this is low enough to avoid audible noise). The time between switching cycles will continue to increase as load reduces.

Jitter
The normalized current limit is modulated between 100% and 95% at a modulation frequency of f_M; this results in a frequency jitter of ~7 kHz with average frequency of ~100 kHz.

Auto-Restart
In the event a fault condition occurs (such as an output overload, output short-circuit, or external component/pin fault), the InnoSwitch3-MX enters auto-restart (AR) or latches off. This is typically initiated by the InnoMux controller.

The latching condition is reset by bringing the PRIMARY BYPASS pin below ~3 V or by going below the UNDER/OVER INPUT VOLTAGE pin UV (I_{UV-}) threshold.

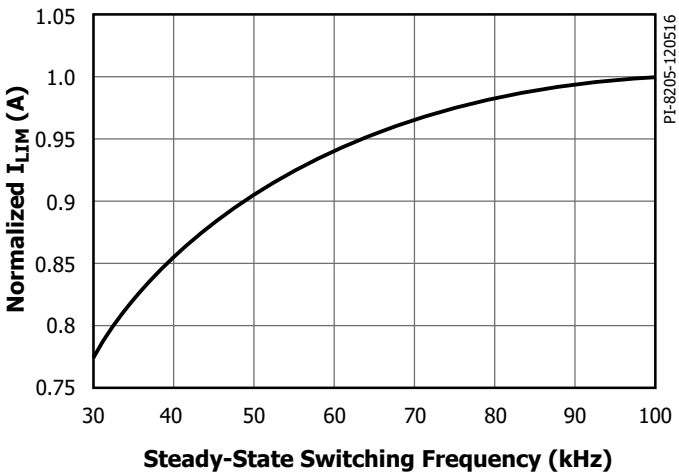


Figure 7. Normalized Primary Current vs. Frequency Jitter.

In auto-restart, switching of the power MOSFET is disabled for $t_{AR(OFF)}$. There are 2 ways to enter auto-restart:

1. Continuous secondary requests at above the overload detection frequency (~110 kHz) for longer than 82 ms (t_{AR}).
2. No requests for switching cycles from the secondary for >$t_{AR(SK)}$.

The InnoMux could initiate an auto-restart by no longer sending request cycles to the InnoMux3-MX secondary controller. The primary controller will then restart.

It is also possible that communication is lost, in which case the primary will also try to restart. Although this should never be the case in normal operation, it can be useful when system ESD events (for example) cause a loss of communication due to noise disturbing the secondary controller. The issue is resolved when the primary restarts after an auto-restart off-time.

The first auto-restart off-time is short ($t_{AR(OFF)SH}$). This short auto-restart time is to provide quick recovery under fast reset conditions. The short auto-restart off-time allows the controller to quickly check to determine whether the auto-restart condition is maintained beyond $t_{AR(OFF)SH}$.

The auto-restart is reset as soon as an AC reset occurs.

SOA Protection

In the event that there are two consecutive cycles where the I_{LIM} is reached within ~500 ns (the blanking time + current limit delay time), the controller will skip 2.5 cycles or ~25 µs (based on full frequency of 100 kHz). This provides sufficient time for the transformer to reset with large capacitive loads without extending the start-up time.

Input Line Voltage Monitoring

The UNDER/OVER INPUT VOLTAGE pin is used for input undervoltage and overvoltage sensing and protection.

A 4 MΩ resistor is tied between the high-voltage DC bulk capacitor after the bridge (or to the AC side of the bridge rectifier for fast AC reset) and the UNDER/OVER INPUT VOLTAGE pin to enable this functionality. This function can be disabled by shorting the UNDER/OVER INPUT VOLTAGE pin to primary GND.

At power-up, after the primary bypass capacitor is charged and the I_{LIM} state is latched, and prior to switching, the state of the UNDER/OVER INPUT VOLTAGE pin is checked to confirm that it is above the brown-in and below the overvoltage shutdown thresholds.

In normal operation, if the UNDER/OVER INPUT VOLTAGE pin current falls below the brown-out threshold and remains below brown-in for longer than t_{UV-}, the controller enters auto-restart. Switching will only resume once the UNDER/OVER INPUT VOLTAGE pin current is above the brown-in threshold.

In the event that the UNDER/OVER INPUT VOLTAGE pin current is above the overvoltage threshold, the controller will also enter auto-restart. Again, switching will only resume once the UNDER/OVER INPUT VOLTAGE pin current has returned to within its normal operating range.

The input line UV/OV function makes use of an internal high-voltage MOSFET on the UNDER/OVER INPUT VOLTAGE pin (V_V) to reduce power consumption. The controller samples the input line at light load conditions when the time between switching cycles is 50 µs or more. At <50 µs between switching cycles, the high-voltage MOSFET will remain on making sensing continuous.

Primary-Secondary Handshake

At start-up, the primary-side initially switches without any feedback information (this is very similar to the operation of a standard TOPSwitch™, TinySwitch™, LinkSwitch™ and other InnoSwitch3™ controllers).

If no feedback signals are received during the auto-restart time (t_{AR}), the primary goes into auto-restart mode. Under normal conditions, the InnoMux controller will power-up from the output voltage within the auto-restart time and will then provide power to the secondary controller in the InnoSwitch3-MX. The InnoMux will then direct InnoSwitch3 MX secondary to take over control. From this point onwards the secondary controls switching.

If the primary controller stops switching or does not respond to cycle requests from the secondary during normal operation (when the secondary has control), the handshake protocol is initiated to ensure that the secondary is ready to assume control once the primary begins to switch again. An additional handshake is also triggered if the secondary detects that the primary is providing more cycles than were requested.

The most likely event that could require an additional handshake is when the primary stops switching as the result of a momentary line brown-out event. When the primary resumes operation, it will default to a start-up condition and attempt to detect handshake pulses from the secondary.

If secondary does not detect that the primary responds to switching requests, or if the secondary detects that the primary is switching without cycle requests, the secondary controller will initiate a second handshake sequence. This provides additional protection against cross conduction of the SR FET while the primary is switching. This protection mode also prevents an output overvoltage condition in the event that the primary is reset while the secondary is still in control.

Wait and Listen

When the primary resumes switching after initial power-up recovery from an input line voltage fault (UV or OV) or an auto-restart event, it will assume control and require a successful handshake to relinquish control to the secondary controller.

As an additional safety measure the primary will pause for an auto-restart on-time period, t_{AR} (~82 ms), before switching. During this "wait" time, the primary will "listen" for secondary requests. If it sees two consecutive secondary requests, separated by ~30 µs, the primary will infer secondary control and begin switching in slave mode. If no pulses occur during the t_{AR} "wait" period, the primary will begin switching under primary control until handshake pulses are received.

Audible Noise Reduction Engine

The InnoSwitch3-MX features an active audible noise reduction mode whereby the controller (via a "frequency skipping" mode of operation) avoids the resonant band (where the mechanical structure of the power supply is most likely to resonate – increasing noise amplitude) between 7 kHz and 12 kHz – 142 µs and 83 µs. If a secondary controller switch request occurs within this time window from the last conduction cycle, the gate drive to the power switch is inhibited.

Secondary Controller

The IC is powered by the SECONDARY BYPASS (BPS) pin. This pin is normally connected to the InnoMux which, will provide power to the secondary controller.

The interface to InnoMux consists of four pins; the REQ pin receives requests for a new primary switching cycle. These requests are sent to the primary using the flux link. The ACK pin acknowledges the request when the pulse is sent over the flux link. The FWC and the SR pins provide further handshaking and timing signals for the InnoMux.

The FORWARD pin connects to the negative edge detection block used for both handshaking and timing to turn on the SR FET connected to the SYNCHRONOUS RECTIFIER DRIVE pin. The FORWARD pin is used to sense when to turn off the SR FET in discontinuous mode operation when the voltage across the FET on resistance drops below the $V_{SR(TH)}$ threshold.

In continuous conduction mode (CCM); operation of the SR FET is turned off when the pulse to demand the next switching cycle is sent to the primary controller, providing excellent synchronous operation, free of any overlap for the FET turn-off while operating in continuous mode.

Minimum Off-Time

The secondary controller initiates a cycle request using the inductive connection to the primary. The maximum frequency of secondary cycle requests is limited by a minimum cycle off-time of $t_{OFF(MIN)}$. This is in order to ensure that there is sufficient reset time after primary conduction to deliver energy to the load.

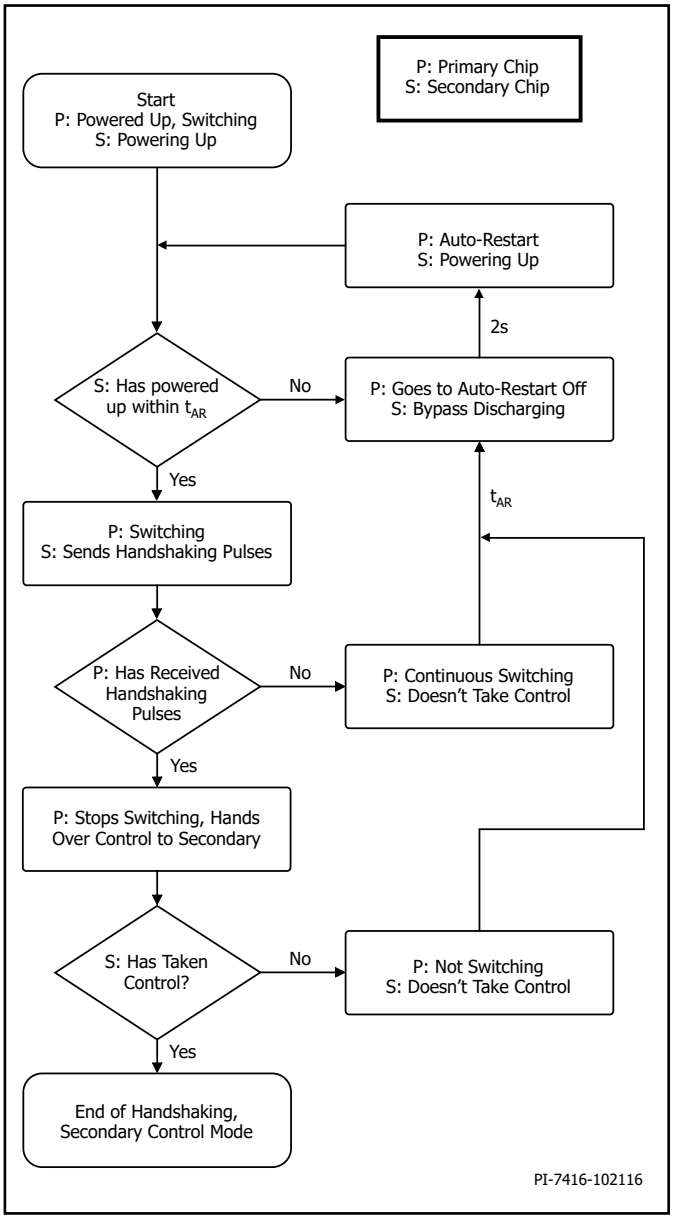


Figure 8. Primary-Secondary Handshake Flow Chart.

Maximum Secondary Inhibit Period
Secondary requests to initiate primary switching are inhibited to maintain operation below maximum frequency and ensure minimum off-time. Besides these constraints, secondary-cycle requests are also inhibited during the "ON" time cycle of the primary switch (time between the cycle request and detection of FORWARD pin falling edge). The maximum time-out in the event that a FORWARD pin falling edge is not detected after a cycle requested is ~30 µs.

SR Disable Protection
In each cycle SR is only engaged if a set cycle was requested by the secondary controller and the negative edge is detected on the FORWARD pin.

SR Static Pull-Down
To ensure that the SR gate is held low when the secondary is not in control, the SYNCHRONOUS RECTIFIER DRIVE pin has a nominally "ON" device to pull the pin low and reduce any voltage on the SR gate due to capacitive coupling from the FORWARD pin.

Open SR Protection
In order to protect against an open SYNCHRONOUS RECTIFIER DRIVE pin system fault the secondary controller has a protection mode to ensure the SYNCHRONOUS RECTIFIER DRIVE pin is connected to an external FET. At start-up the controller will apply a current to the SYNCHRONOUS RECTIFIER DRIVE pin; an internal threshold will correlate to a capacitance of 100 pF. If the external capacitance on the SYNCHRONOUS RECTIFIER DRIVE pin is below 100 pF the resulting voltage is above the reference voltage, and the device will assume the SYNCHRONOUS RECTIFIER DRIVE pin is "open" and there is no FET to drive. If the pin capacitance detected is above 100 pF (the resulting voltage is below the reference voltage), the controller will assume an SR FET is connected.

In the event the SYNCHRONOUS RECTIFIER DRIVE pin is detected to be open or the SYNCHRONOUS RECTIFIER DRIVE pin is tied to ground at start-up, the secondary controller will stop requesting pulses from the primary to initiate auto-restart.

It is possible to use a normal diode instead of an SR MOSFET. In that case, a 220 pF capacitor should be connected to the SR pin.

Intelligent Quasi-Resonant Mode Switching
In order to improve conversion efficiency and reduce switching losses, the InnoSwitch3-MX features a means to force switching when the voltage across the primary switch is near its minimum voltage when the converter operates in discontinuous conduction mode (DCM). This mode of operation is automatically engaged in DCM and disabled once the converter moves to continuous conduction mode (CCM). See Figure 9.

Rather than detecting the magnetizing ring valley on the primary side, the peak voltage of the FORWARD pin voltage as it rises above the output voltage level is used to gate secondary requests to initiate the switch "ON" cycle in the primary controller. The output voltage (VOUT) typically is the VCV1 application output voltage as regulated by the InnoMux controller.

The secondary controller detects when the controller enters in discontinuous-mode and opens secondary cycle request windows corresponding to minimum switching voltage across the primary power switch.

Quasi-Resonant (QR) mode is enabled for 20 µs after DCM is detected. QR switching is disabled after 20 µs, at which point switching may occur at any time a secondary request is initiated.

The secondary controller includes blanking of ~1 µs to prevent false detection of primary "ON" cycle when the FORWARD pin rings below ground.

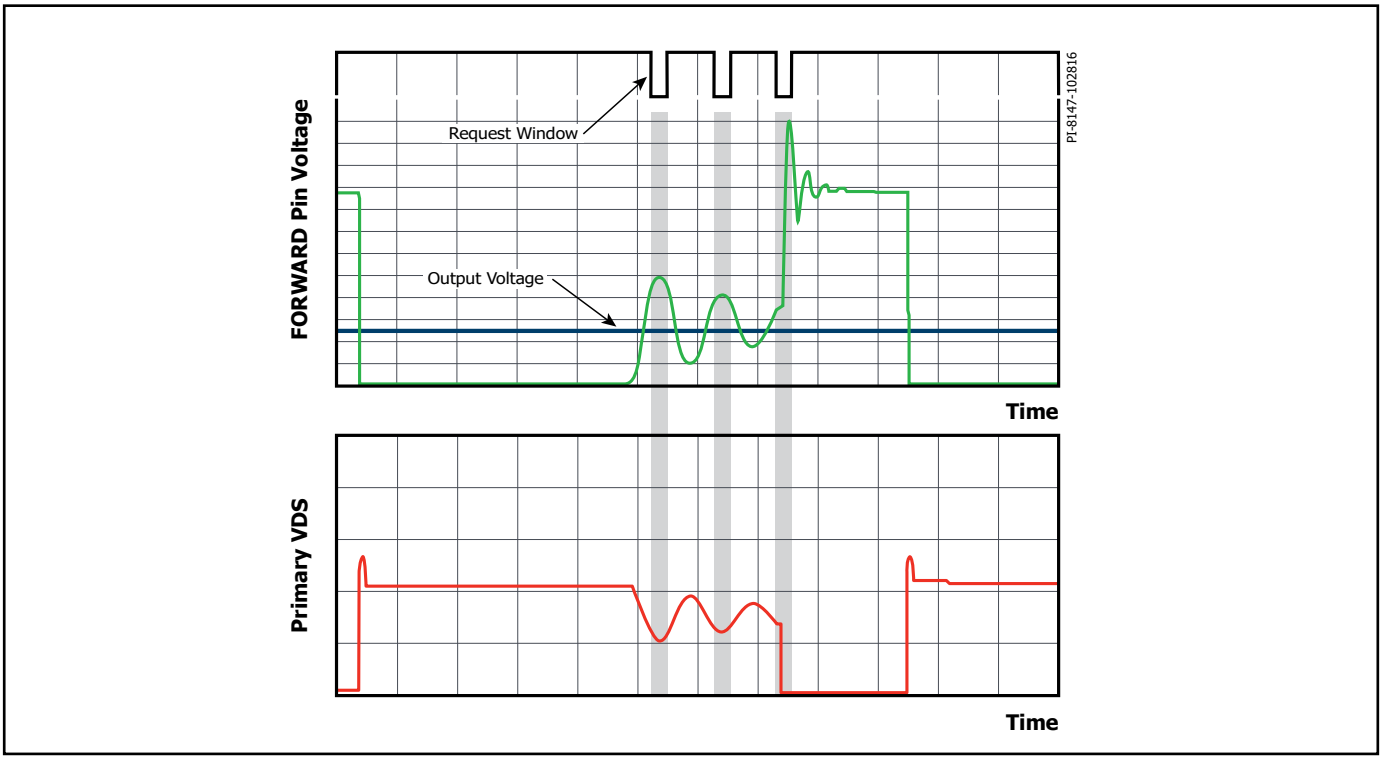


Figure 9. Intelligent Quasi-Resonant Mode Switching.

Design Considerations When Using PowiGaN Devices (INN3478C, INN3479C and INN3470C)

For a flyback converter configuration, typical voltage waveform at the DRAIN pin of the IC is shown in Figure 10.

V_{OR} is the reflected output voltage across the primary winding when the secondary is conducting. V_{BUS} is the DC voltage connected to one end of the transformer primary winding.

In addition to V_{BUS}+V_{OR}, the drain also sees a large voltage spike at turn off that is caused by the energy stored in the leakage inductance of the primary winding. To keep the drain voltage from exceeding the rated maximum continuous drain voltage, a clamp circuit is needed across the primary winding. The forward recovery of the clamp diode will add a spike at the instant of turn-OFF of the primary switch. V_{CLM} in Figure 22 is the combined clamp voltage including the spike. The peak drain voltage of the primary switch is the total of V_{BUS}, V_{OR} and V_{CLM}.

V_{OR} and the clamp voltage V_{CLM} should be selected such that the peak drain voltage is lower than 650 V for all normal operating conditions. This provides sufficient margin to ensure that occasional increase in voltage during line transients such as line surges will maintain the peak drain voltage well below 750 V under abnormal transient operating conditions. This ensures excellent long term reliability and design margin.

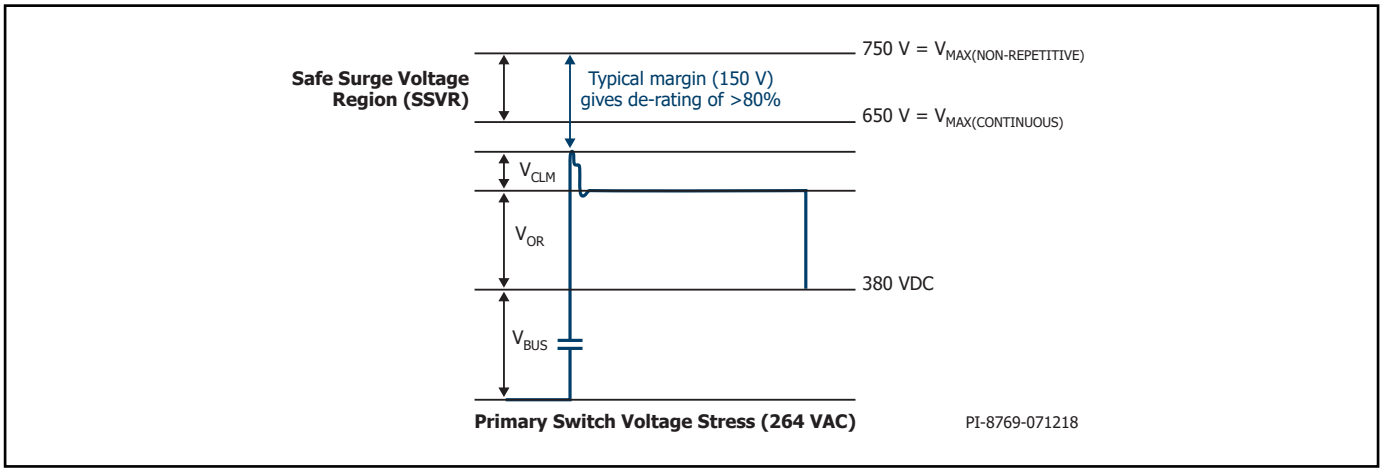


Figure 10. Peak Drain Voltage for 264 VAC Input Voltage.

Absolute Maximum Ratings[1,2]

D Pin Voltage: INN346x ..... -0.3 V to 650 V
D Pin Voltage: INN3475/3476/3477 ..... -0.3 V to 725 V
D Pin Voltage: INN3478/3479/3470 ..... -0.3 V to 750 V[6]
DRAIN Pin Peak Current: INN3464C ..... 1.52 A (2.85 A)[3]
INN34x5C ..... 1.84 A (3.45 A)[3]
INN34x6C ..... 2.32 A (4.35 A)[3]
INN34x7C ..... 2.64 A (4.95 A)[3]
INN3468C ..... 2.96 A (5.55 A)[3]
PowiGaN device INN3478C ..... 6.5 A[7]
PowiGaN device INN3479C ..... 10 A[7]
PowiGaN device INN3470C ..... 14A[7]
V Pin Voltage ..... -0.3 V to 725 V
FW Pin Voltage ..... 250 V
SR Pin Voltage ..... -0.3 V to 6 V
VOUT PIN Voltage ..... -0.3 V to 25 V
BPP/BPS Pin Voltage ..... -0.3 V to 6 V
Storage Temperature ..... -65 °C to 150 °C
Operating Junction Temperature[4] ..... -40 °C to 150 °C
Ambient Temperature ..... -40 °C to 105 °C
Lead Temperature[5] ..... 260 °C

Notes:
1. All voltages referenced to SOURCE and Secondary GROUND, T_A = 25 °C.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
3. Higher peak Drain current is allowed while the Drain voltage is simultaneously less than 400 V.
4. Normally limited by internal circuitry.
5. 1/16" from case for 5 seconds.
6. Maximum drain voltage (non-repetitive pulse) ..... -0.3 V to 750 V
   Maximum continuous drain voltage ..... -0.3 to 650 V
7. Please refer to Figure 11 for maximum allowable voltage and current combinations.

Thermal Resistance

Thermal Resistance: INN3464C to INN3468C & INN3475C to INN3477C
(θ_{JA}) ..... 76 °C/W[1], 65 °C/W[2]
(θ_{JC}) ..... 8 °C/W[3]
PowiGaN devices INN3478C, INN3479C, INN3470C
(θ_{JC}) ..... 10 °C/W[3]

Notes:
1. Soldered to 0.36 sq. inch (232 mm²) 2 oz. (610 g/m²) copper clad.
2. Soldered to 1 sq. inch (645 mm²) 2 oz. (610 g/m²) copper clad.
3. The case temperature is measured on the top of the package.

Parameter	Conditions	Rating	Units
Ratings for UL1577			
Primary-Side Current Rating	Current from pin (16-19) to pin 24	1.5	A
Primary-Side Power Rating	T_{AMB} = 25 °C (device mounted in socket resulting in T_{CASE} = 120 °C)	1.35	W
Secondary-Side Power Rating	T_{AMB} = 25 °C (device mounted in socket)	0.125	W
Package Characteristics			
Clearance		12.1	mm (typ)
Creepage		11.7	mm (typ)
Distance Through Insulation (DTI)		0.4	mm (min)
Transient Isolation Voltage		6	kV (min)
Comparative Tracking Index (CTI)		600	-

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Startup Switching Frequency	f_{START}	T_J = 25 °C		22.5	25	27.5	kHz
Jitter Modulation Frequency	f_M	T_J = 25 °C f_{SW} = 100 kHz			1.25		kHz
Maximum On-Time	$t_{ON(MAX)}$	T_J = 25 °C		11.5	14.6	18	µs
Minimum Primary Feedback Block-Out Timer	t_{BLOCK}					$t_{OFF(MIN)}$	µs
BPP Supply Current	I_{S1}	V_{BPP} = V_{BPP} + 0.1 V (Not Switching) T_J = 25 °C	INN3464C INN34x5C INN34x6C INN34x7C INN3468C	145	200	300	µA
			INN3478C INN3479C INN3470C	145	266	425	
	I_{S2}	V_{BPP} = V_{BPP} + 0.1 V (Switching at 132 kHz) T_J = 25 °C	INN3464C	0.38	0.50	0.69	mA
			INN34x5C	0.45	0.65	1.05	
			INN34x6C	0.65	0.86	1.20	
			INN34x7C	0.70	1.03	1.40	
			INN3468C	0.90	1.20	1.75	
			INN3478C	1.15	1.3	1.45	
			INN3479C INN3470C	1.46	1.95	2.81	
BPP Pin Charge Current	I_{CH1}	V_{BPP} = 0 V, T_J = 25 °C		-1.7	-1.35	-0.90	mA
	I_{CH2}	V_{BPP} = 4 V, T_J = 25 °C		-6.0	-4.65	-3.30	
BPP Pin Voltage	V_{BPP}			4.64	4.9	5.3	V
BPP Pin Voltage Hysteresis	$V_{BPP(H)}$	T_J = 25 °C		0.2	0.39	0.6	V
BPP Shunt	$V_{BPP(SHUNT)}$	I_{BPP} = 2 mA		5.2	5.36	5.7	V
BPP Power-Up Reset Threshold Voltage	$V_{BPP(RESET)}$	T_J = 25 °C		2.8	3.15	3.6	V
UV/OV Pin Brown-In Threshold	I_{UV+}	T_J = 25 °C		22	24.5	28	µA
UV/OV Pin Brown-Out Threshold	I_{UV-}	T_J = 25 °C		19	22	26	µA
Brown-Out Delay Time	t_{UV-}	T_J = 25 °C			35		ms
UV/OV Pin Line Overvoltage Threshold	I_{OV+}	T_J = 25 °C		100	112	118	µA
UV/OV Pin Line Overvoltage Hysteresis	$I_{OV(H)}$	T_J = 25 °C		6	7	9	µA

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Line Fault Protection							
VOLTAGE Pin Line Over-voltage Deglitch Filter	t_{OV+}	T_J = 25 °C See Note B			3		µs
VOLTAGE Pin Voltage Rating	V_V	T_J = 25 °C		650			V
Circuit Protection							
Standard Current Limt (BPP) Capacitor = 0.47 µF **See Note C**	I_{LIM}	di/dt = 187.5 mA/µs T_J = 25 °C	INN3464C	0.69	0.75	0.81	A
		di/dt = 287.5 mA/µs T_J = 25 °C	INN34x5C	1.06	1.15	1.24	
		di/dt = 362.5 mA/µs T_J = 25 °C	INN34x6C	1.33	1.45	1.57	
		di/dt = 500 mA/µs T_J = 25 °C	INN3467C	1.84	2.00	2.16	
		di/dt = 550 mA/µs T_J = 25 °C	INN3468C	2.02	2.20	2.38	
		di/dt = 487.5 mA/µs T_J = 25 °C	INN3477C	1.79	1.95	2.11	
		di/dt = 660 mA/µs T_J = 25 °C	INN3478C	2.39	2.60	2.81	
		di/dt = 750 mA/µs T_J = 25 °C	INN3479C	2.76	3.00	3.24	
		di/dt = 850 mA/µs T_J = 25 °C	INN3470C	3.13	3.40	3.67	
Increased Current Limit (BPP) Capacitor = 4.7 µF **See Note C**	I_{LIM+1}	di/dt = 187.5 mA/µs T_J = 25 °C	INN3464C	0.86	0.95	1.04	A
		di/dt = 287.5 mA/µs T_J = 25 °C	INN34x5C	1.27	1.40	1.53	
		di/dt = 362.5 mA/µs T_J = 25 °C	INN34x6C	1.58	1.75	1.92	
		di/dt = 500 mA/µs T_J = 25 °C	INN3467C	2.08	2.30	2.52	
		di/dt = 550 mA/µs T_J = 25 °C	INN3468C	2.35	2.60	2.85	
		di/dt = 487.5 mA/µs T_J = 25 °C	INN3477C	1.94	2.15	2.35	
		di/dt = 660 mA/µs T_J = 25 °C	INN3478C	2.63	2.91	3.19	
		di/dt = 750 mA/µs T_J = 25 °C	INN3479C	3.03	3.35	3.67	
		di/dt = 850 mA/µs T_J = 25 °C	INN3470C	3.44	3.80	4.16	
Overload Detection Frequency	f_{OVL}	T_J = 25 °C		102	110	118	kHz

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Circuit Protection (cont.)							
BYPASS Pin Latching Shutdown Threshold Current	I_{SD}	T_J = 25 °C		5.5	7.3	9	mA
Auto-Restart On-Time	t_{AR}	T_J = 25 °C		74	82	90	ms
Auto-Restart Trigger Skip Time	$t_{AR(SK)}$	T_J = 25 °C See Note A			1.3		sec
Auto-Restart Off-Time	$t_{AR(OFF)}$	T_J = 25 °C		1.7		2.1	sec
Short Auto-Restart Off-Time	$t_{AR(OFF)SH}$	T_J = 25 °C			0.20		sec
Output							
ON-State Resistance	$R_{DS(ON)}$	INN3464C	T_J = 25 °C		3.20	3.68	Ω
			T_J = 100 °C		4.96	5.70	
		INN3465C	T_J = 25 °C		1.95	2.25	
			T_J = 100 °C		3.02	3.5	
		INN3466C	T_J = 25 °C		1.30	1.5	
			T_J = 100 °C		2.02	2.35	
		INN3467C	T_J = 25 °C		1.02	1.20	
			T_J = 100 °C		1.58	1.85	
		INN3468C	T_J = 25 °C		0.86	0.99	
			T_J = 100 °C		1.34	1.55	
		INN3475C	T_J = 25 °C		1.95	2.25	
			T_J = 100 °C		3.02	3.5	
		INN3476C	T_J = 25 °C		1.34	1.55	
			T_J = 100 °C		2.08	2.40	
		INN3477C	T_J = 25 °C		1.20	1.40	
			T_J = 100 °C		1.86	2.2	
		INN3478C	T_J = 25 °C		0.52	0.68	
			T_J = 100 °C		0.78	1.02	
		INN3479C	T_J = 25 °C		0.35	0.44	
			T_J = 100 °C		0.49	0.62	
		INN3470C	T_J = 25 °C		0.29	0.39	
			T_J = 100 °C		0.41	0.54	

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Output (cont.)						
OFF-State Drain Leakage Current	I_{DSS1}	V_{BPP} = V_{BPP} + 0.1 V V_{DS} = 150 V T_J = 25 °C		15		µA
	I_{DSS2}	V_{BPP} = V_{BPP} + 0.1 V V_{DS} = 325 V T_J = 25 °C			200	µA
Drain Supply Voltage			50			V
Thermal Shutdown	T_{SD}	See Note A	135	142	150	°C
Thermal Shutdown Hysteresis	$T_{SD(H)}$	See Note A		70		°C
Secondary						
Maximum Switching Frequency	f_{SREQ}	T_J = 25 °C	118	132	145	kHz
BPS Pin Current at No-Load	I_{SNL}	T_J = 25 °C		300		µA
BPS Pin Undervoltage Threshold	$V_{BPS(UVLO)(TH)}$		3.6	3.80	4.1	V
BPS Pin Undervoltage Hysteresis	$V_{BPS(UVLO)(H)}$	T_J = 25 °C		0.65		V
FWD Pin Breakdown Voltage	V_{FWD}		250			V
Minimum Off-Time	$t_{OFF(MIN)}$		2.48	3.38		µs

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Synchronous Rectifier @ T_J = 25 °C						
SR Pin Drive Voltage	V_{SR}	Relies on InnoMUX Supply		V_{BPS}		V
SR Pin Voltage Threshold	$V_{SR(TH)}$			-3		mV
SR Pin Pull-Up Current	$I_{SR(PU)}$	T_J = 25 °C C_{LOAD} = 2 nF, f_{SW} = 100 kHz		155		mA
SR Pin Pull-Down Current	$I_{SR(PD)}$	T_J = 25 °C C_{LOAD} = 2 nF, f_{SW} = 100 kHz		270		mA
Output Pull-Up Resistance	R_{PU}	T_J = 25 °C V_{BPS} = 5 V I_{SR} = 10 mA	6.5	8.7	11	Ω
Output Pull-Down Resistance	R_{PD}	T_J = 25 °C V_{BPS} = 5 V I_{SR} = 10 mA	3.5	4.5	5.5	Ω

NOTES:
A. This parameter is derived from characterization.
B. This parameter is guaranteed by design.
C. To ensure correct current limit it is recommended that nominal 0.47 µF / 4.7 µF capacitors are used. In addition, the BPP capacitor value tolerance should be equal or better than indicated below across the ambient temperature range of the target application. The minimum and maximum capacitor values are guaranteed by characterization.

Nominal BPP Pin Capacitor Value	Tolerance Relative to Nominal Capacitor Value	
	Minimum	Maximum
0.47 µF	-60%	+100%
4.7 µF	-50%	N/A

Typical Performance Curve

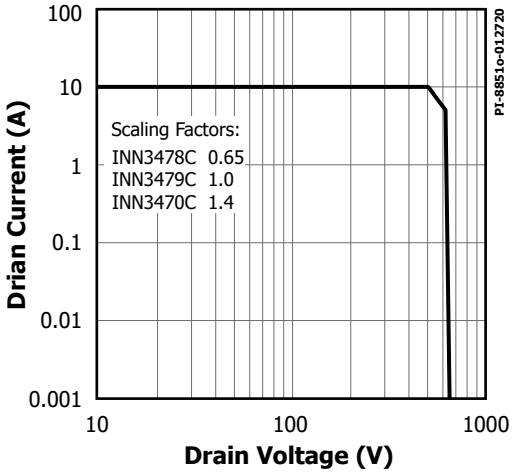
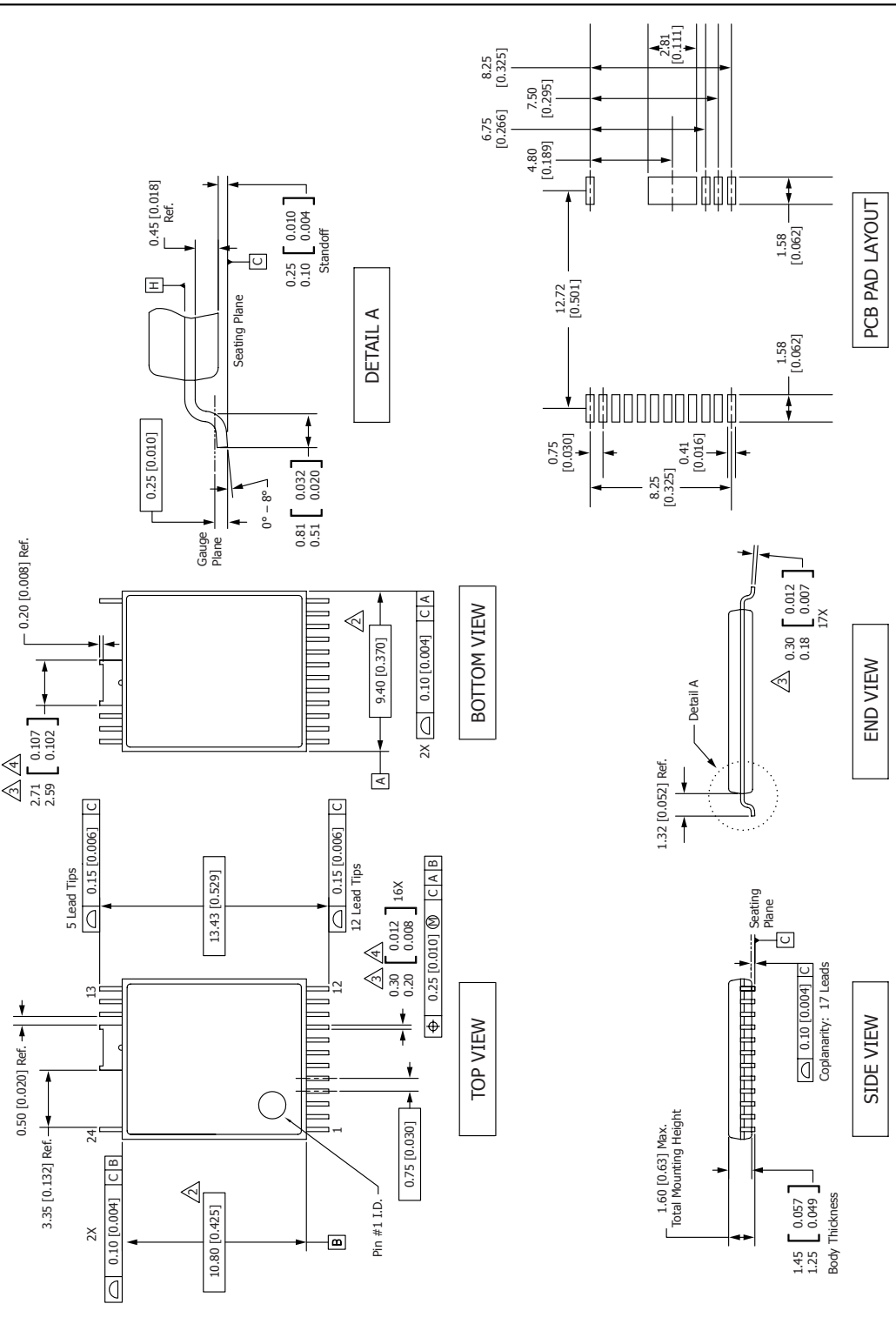


Figure 11. Maximum Allowable Drain Current vs. Drain Voltage (PowiGaN Devices INN3478C / INN3479C / INN3470C).

InSOP-24D



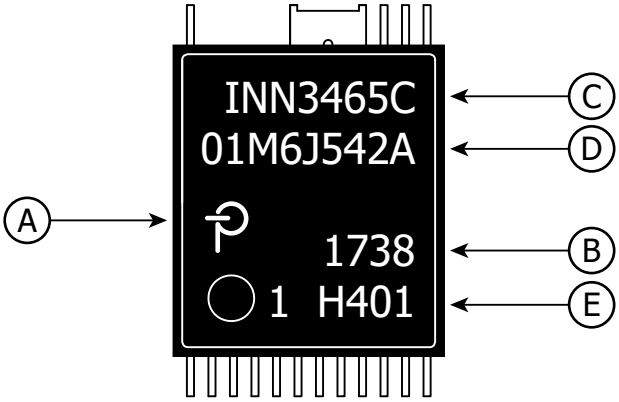
Notes:

1. Dimensioning and Tolerancing per ASME Y14.5M – 1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exculsive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.18 [0.007] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in millimeters [inches].
6. Datums A & B to be determined at Datum H.

PI-8106-051718
POD-InSOP-24D Rev B

PACKAGE MARKING

InSOP-24D



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code
E. Test Sublot and Feature Code

PI-8727e-011620

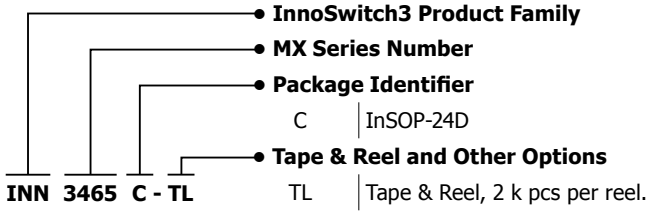
MSL Table

Part Number	MSL Rating
INN3464C	3
INN34x5C	3
INN34x6C	3
INN34x7C	3
INN3468C	3
INN3478C	3
INN3479C	3
INN3470C	3

ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	JESD78D	> ±100 mA or > 1.5 × V_{MAX} on all pins
Human Body Model ESD	ANSI/ESDA/JEDEC JS-001-2014	> ±2000 V on all pins
Charge Device Model ESD	ANSI/ESDA/JEDEC JS-002-2014	> ±500 V on all pins

Part Ordering Information



Revision	Notes	Date
B	Code L release.	03/19
C	Updated $R_{DS(ON)}$ Max value for INN3468C T_J = 25 °C. Updated I_{LIM} and I_{LIM+1} di/dt Condition values.	09/19
D	Code A release.	03/20
E	Updated Thermal Resistance table on page 10.	07/21
F	Updated Parameter name for V_{FWD}.	03/23

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