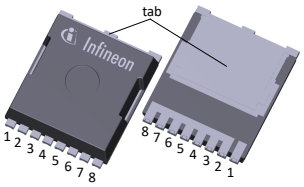
# MOSFET

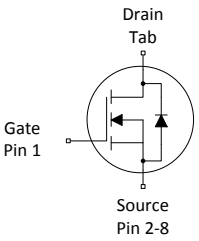
TOLL

## OptiMOS™ 6 Power-Transistor, 150 V




## Features

- N-channel, normal level
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- MSL 1 classified according to J-STD-020

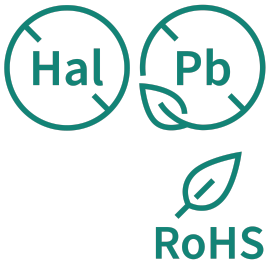



## Product validation

Fully qualified according to JEDEC for Industrial Applications

**Table 1 Key Performance Parameters**

| Parameter | Value | Unit |
|---|---|---|
| $V_{DS}$ | 150 | V |
| $R_{DS(on),max}$ | 2.5 | mΩ |
| $I_D$ | 263 | A |
| $Q_{oss}$ | 310 | nC |
| $Q_G$ | 105 | nC |
| $Q_{rr}$ (500A/µs) | 184 | nC |




| Type/Ordering Code | Package | Marking | Related Links |
|---|---|---|---|
| IPT025N15NM6 | PG-HSOF-8 | 025N15N6 | - |

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# 1 Maximum ratings

at $T_A$=25 °C, unless otherwise specified

**Table 2 Maximum ratings**

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Continuous drain current [1] | $I_D$ | - | - | 263<br>186<br>173<br>26 | A | $V_{GS}$=10 V, $T_C$=25 °C<br>$V_{GS}$=10 V, $T_C$=100 °C<br>$V_{GS}$=8 V, $T_C$=100 °C<br>$V_{GS}$=10 V, $T_A$=25 °C, $R_{thJA}$=40 °C/W [2] |
| Pulsed drain current [3] | $I_{D,pulse}$ | - | - | 1052 | A | $T_C$=25 °C |
| Avalanche current, single pulse [4] | $I_{AS}$ | - | - | 120 | A | $T_C$=25 °C |
| Avalanche energy, single pulse | $E_{AS}$ | - | - | 960 | mJ | $I_D$=63 A, $R_{GS}$=25 Ω |
| Gate source voltage | $V_{GS}$ | -20 | - | 20 | V | - |
| Power dissipation | $P_{tot}$ | - | - | 395<br>3.8 | W | $T_C$=25 °C<br>$T_A$=25 °C, $R_{thJA}$=40 °C/W [2] |
| Operating and storage temperature | $T_j$, $T_{stg}$ | -55 | - | 175 | °C | - |

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm$^2$ (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See Diagram 3 for more detailed information

[4] See Diagram 13 for more detailed information

# 2 Thermal characteristics

**Table 3 Thermal characteristics**

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | $R_{thJC}$ | - | - | 0.38 | °C/W | - |
| Thermal resistance, junction - ambient,<br>6 cm² cooling area [5] | $R_{thJA}$ | - | - | 40 | °C/W | - |
| Thermal resistance, junction - ambient,<br>minimal footprint | $R_{thJA}$ | - | - | 62 | °C/W | - |

[5] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm$^2$ (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

# 3 Electrical characteristics

at $T_j$=25 °C, unless otherwise specified

**Table 4 Static characteristics**

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 150 | - | - | V | $V_{GS}$=0 V, $I_D$=1 mA |
| Gate threshold voltage | $V_{GS(th)}$ | 3.0 | 3.5 | 4.0 | V | $V_{DS}$=$V_{GS}$, $I_D$=275 µA |
| Zero gate voltage drain current | $I_{DSS}$ | - | 0.1<br>10 | 1<br>100 | µA | $V_{DS}$=120 V, $V_{GS}$=0 V, $T_j$=25 °C<br>$V_{DS}$=120 V, $V_{GS}$=0 V, $T_j$=125 °C |
| Gate-source leakage current | $I_{GSS}$ | - | 10 | 100 | nA | $V_{GS}$=20 V, $V_{DS}$=0 V |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 1.9<br>2.1<br>2.4 | 2.4<br>2.5<br>2.9 | mΩ | $V_{GS}$=15 V, $I_D$=120 A<br>$V_{GS}$=10 V, $I_D$=120 A<br>$V_{GS}$=8 V, $I_D$=60 A |
| Gate resistance | $R_G$ | - | 1.06 | 1.59 | Ω | - |
| Transconductance | $g_{fs}$ | 102 | 200 | - | S | $\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, $I_D$=120 A |

**Table 5 Dynamic characteristics**

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance [6] | $C_{iss}$ | - | 7500 | 9800 | pF | $V_{GS}$=0 V, $V_{DS}$=75 V, $f$=1 MHz |
| Output capacitance [6] | $C_{oss}$ | - | 2300 | 3000 | pF | $V_{GS}$=0 V, $V_{DS}$=75 V, $f$=1 MHz |
| Reverse transfer capacitance [6] | $C_{rss}$ | - | 25 | 38 | pF | $V_{GS}$=0 V, $V_{DS}$=75 V, $f$=1 MHz |
| Turn-on delay time | $t_{d(on)}$ | - | 21 | - | ns | $V_{DD}$=75 V, $V_{GS}$=10 V, $I_D$=60 A, $R_{G,ext}$=1.6 Ω |
| Rise time | $t_r$ | - | 16 | - | ns | $V_{DD}$=75 V, $V_{GS}$=10 V, $I_D$=60 A, $R_{G,ext}$=1.6 Ω |
| Turn-off delay time | $t_{d(off)}$ | - | 34 | - | ns | $V_{DD}$=75 V, $V_{GS}$=10 V, $I_D$=60 A, $R_{G,ext}$=1.6 Ω |
| Fall time | $t_f$ | - | 19 | - | ns | $V_{DD}$=75 V, $V_{GS}$=10 V, $I_D$=60 A, $R_{G,ext}$=1.6 Ω |

[6] Defined by design. Not subject to production test.

**Table 6 Gate charge characteristics** [7)]

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge [8)] | $Q_{gs}$ | - | 41 | 53 | nC | $V_{DD}$=75 V, $I_D$=60 A, $V_{GS}$=0 to 10 V |
| Gate charge at threshold | $Q_{g(th)}$ | - | 26 | - | nC | $V_{DD}$=75 V, $I_D$=60 A, $V_{GS}$=0 to 10 V |
| Gate to drain charge [8)] | $Q_{gd}$ | - | 23 | 35 | nC | $V_{DD}$=75 V, $I_D$=60 A, $V_{GS}$=0 to 10 V |
| Switching charge | $Q_{sw}$ | - | 38 | - | nC | $V_{DD}$=75 V, $I_D$=60 A, $V_{GS}$=0 to 10 V |
| Gate charge total [8)] | $Q_g$ | - | 105 | 137 | nC | $V_{DD}$=75 V, $I_D$=60 A, $V_{GS}$=0 to 10 V |
| Gate plateau voltage | $V_{plateau}$ | - | 5.4 | - | V | $V_{DD}$=75 V, $I_D$=60 A, $V_{GS}$=0 to 10 V |
| Gate charge total, sync. FET | $Q_{g(sync)}$ | - | 89 | - | nC | $V_{DS}$=0.1 V, $V_{GS}$=0 to 10 V |
| Output charge [8)] | $Q_{oss}$ | - | 310 | 403 | nC | $V_{DS}$=75 V, $V_{GS}$=0 V |

7) See "Gate charge waveforms" for parameter definition

8) Defined by design. Not subject to production test.

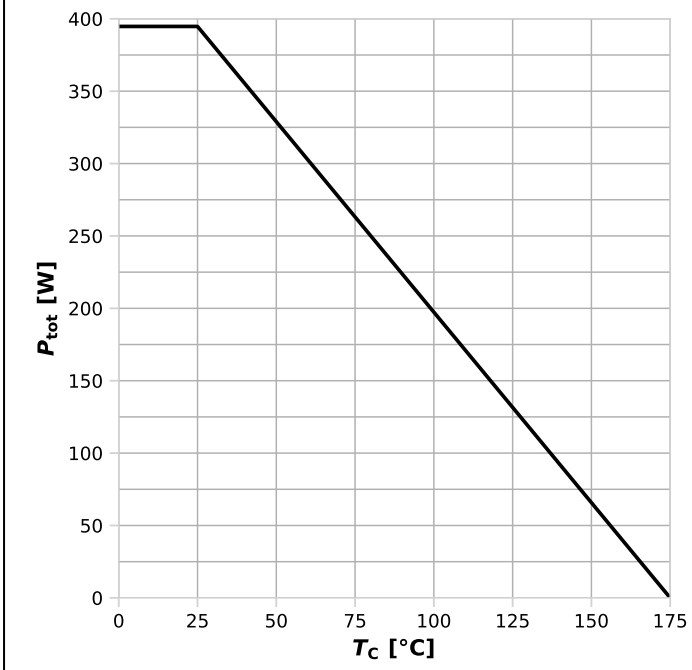
**Table 7 Reverse diode**

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Diode continuous forward current | $I_S$ | - | - | 263 | A | $T_C$=25 °C |
| Diode pulse current | $I_{S,pulse}$ | - | - | 1052 | A | $T_C$=25 °C |
| Diode forward voltage | $V_{SD}$ | - | 0.86 | 1.0 | V | $V_{GS}$=0 V, $I_F$=120 A, $T_j$=25 °C |
| Reverse recovery time [9)] | $t_{rr}$ | - | 40 | 80 | ns | $V_R$=75 V, $I_F$=60 A, d$i_F$/d$t$=500 A/µs |
| Reverse recovery charge [9)] | $Q_{rr}$ | - | 184 | 368 | nC | $V_R$=75 V, $I_F$=60 A, d$i_F$/d$t$=500 A/µs |
| Reverse recovery time [9)] | $t_{rr}$ | - | 37 | 74 | ns | $V_R$=75 V, $I_F$=60 A, d$i_F$/d$t$=1000 A/µs |
| Reverse recovery charge [9)] | $Q_{rr}$ | - | 334 | 668 | nC | $V_R$=75 V, $I_F$=60 A, d$i_F$/d$t$=1000 A/µs |

9) Defined by design. Not subject to production test.

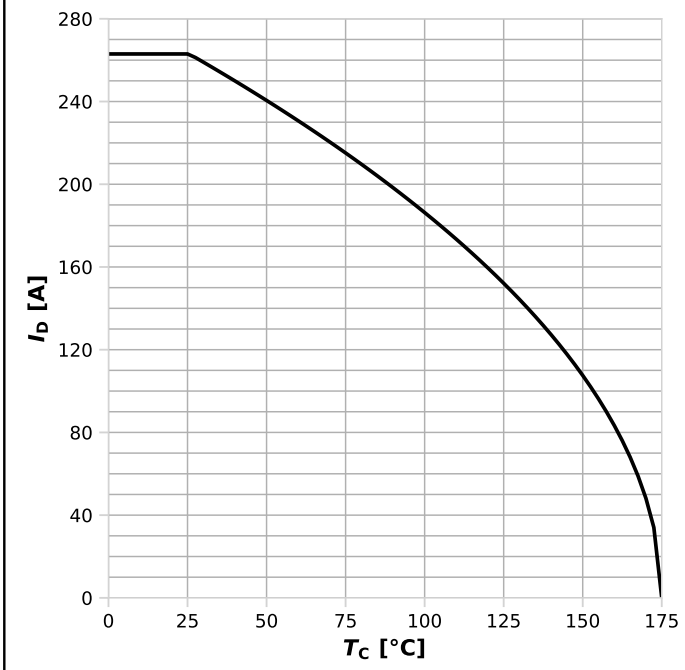
# 4 Electrical characteristics diagrams

**Diagram 1: Power dissipation**



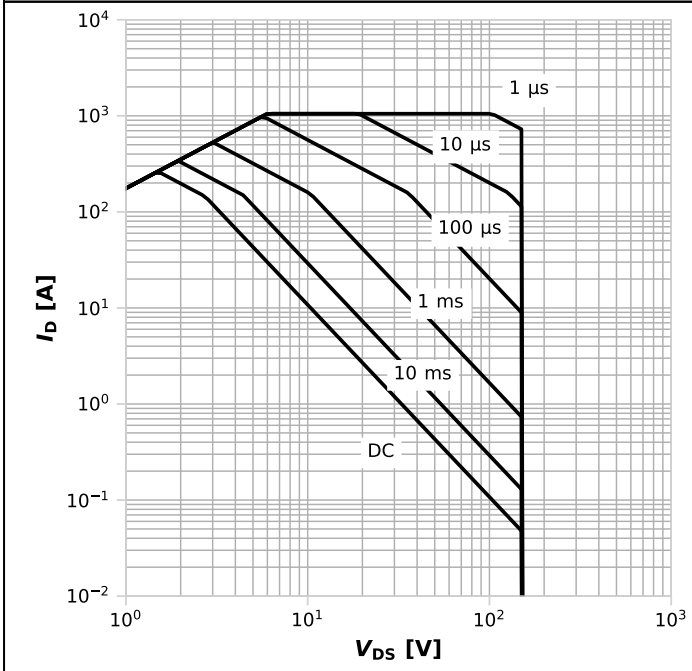

$P_{tot}$=f($T_C$)

**Diagram 2: Drain current**



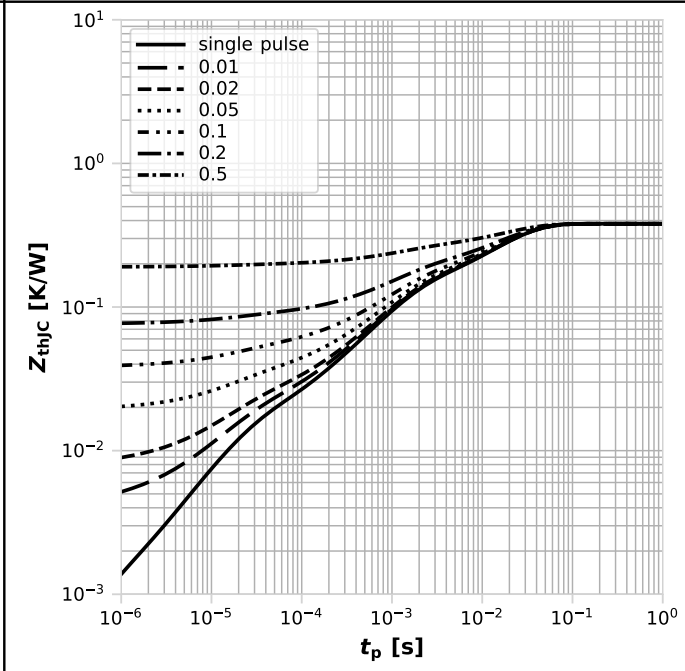

$I_D$=f($T_C$); $V_{GS}$≥10 V

**Diagram 3: Safe operating area**



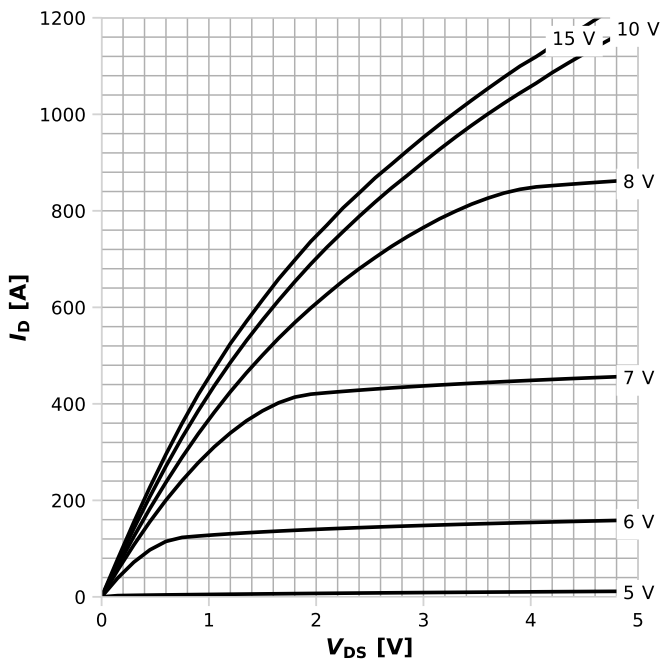

$I_D$=f($V_{DS}$); $T_C$=25 °C; $D$=0; parameter: $t_p$

**Diagram 4: Max. transient thermal impedance**



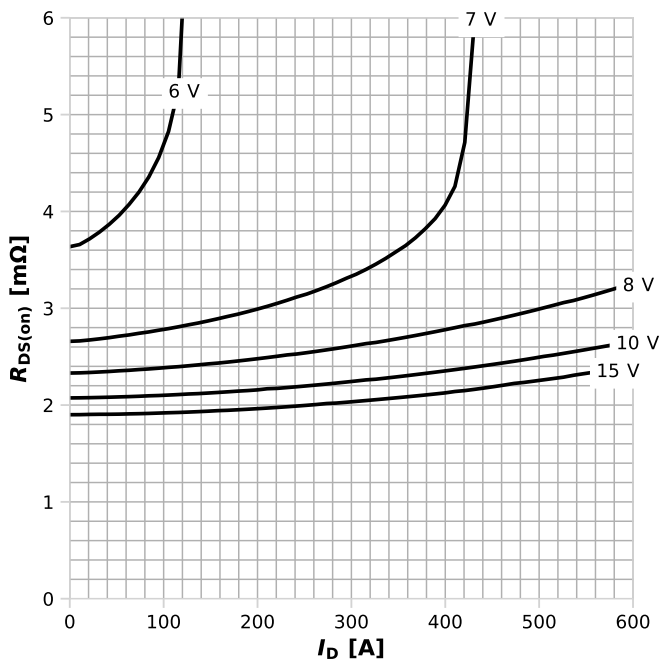

$Z_{thJC}$=f($t_p$); parameter: $D$=$t_p$/$T$

**Diagram 5: Typ. output characteristics**



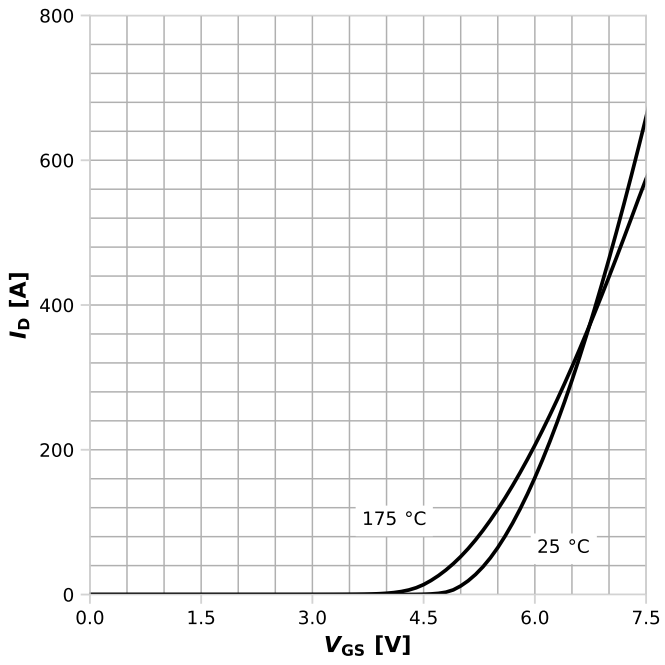

$I_D$=f($V_{DS}$), $T_j$=25 °C; parameter: $V_{GS}$

**Diagram 6: Typ. drain-source on resistance**



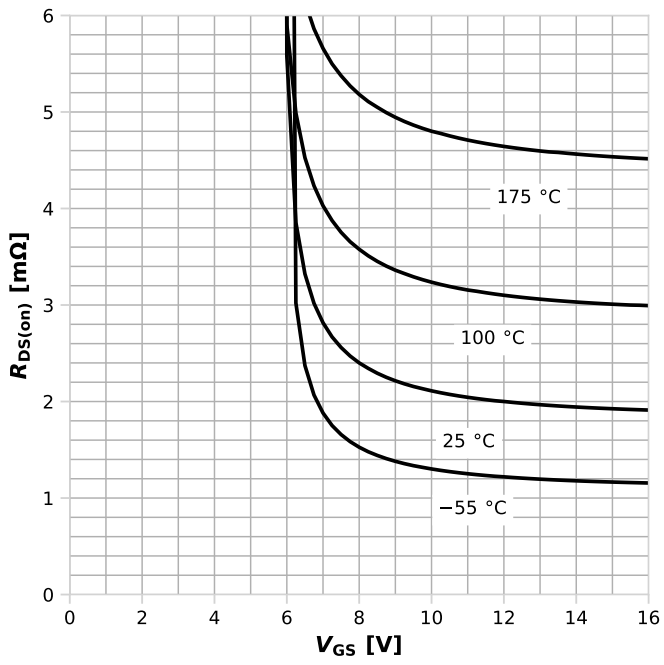

$R_{DS(on)}$=f($I_D$), $T_j$=25 °C; parameter: $V_{GS}$

**Diagram 7: Typ. transfer characteristics**



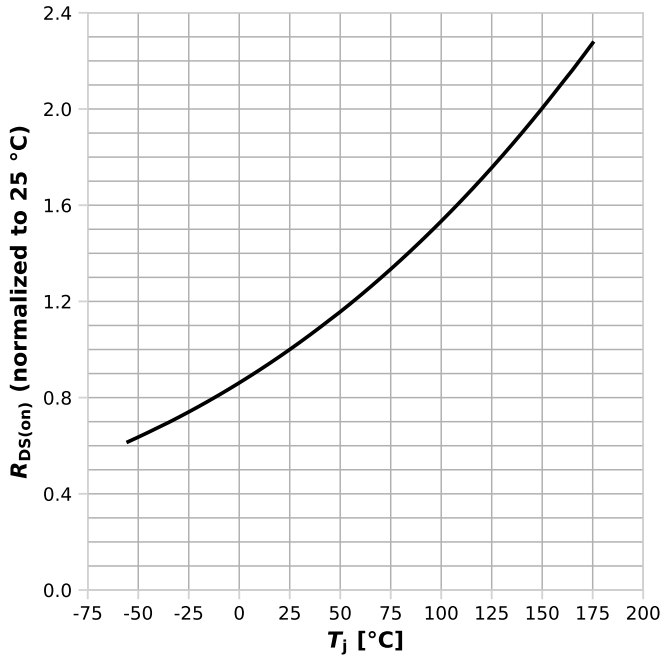

$I_D$=f($V_{GS}$), $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: $T_j$

**Diagram 8: Typ. drain-source on resistance**



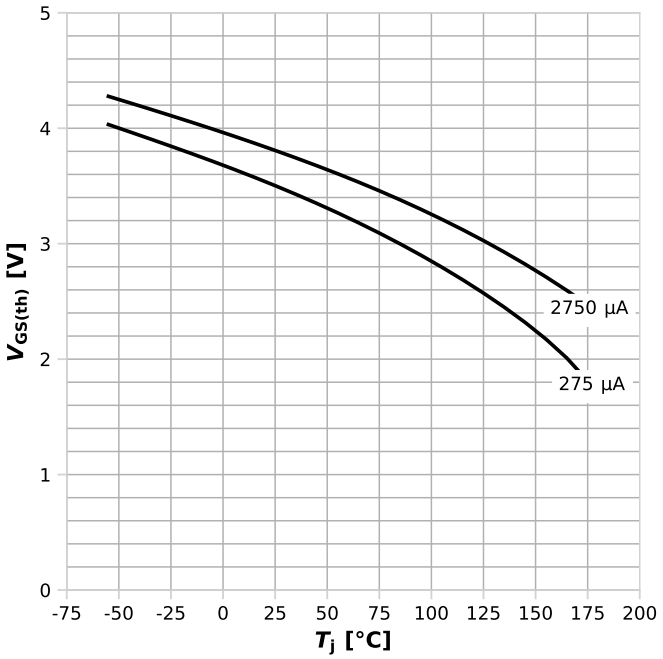

$R_{DS(on)}$=f($V_{GS}$), $I_D$=120 A; parameter: $T_j$

**Diagram 9: Normalized drain-source on resistance**



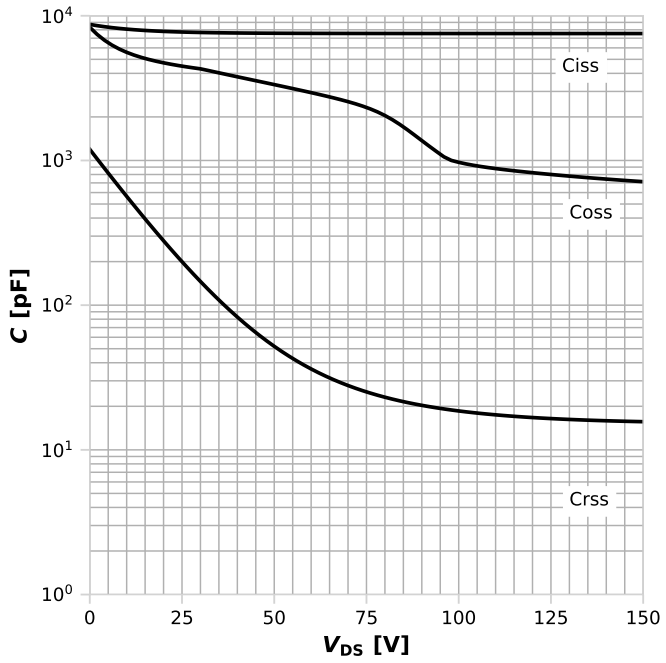

$R_{DS(on)}$=f($T_j$), $I_D$=120 A, $V_{GS}$=10 V

**Diagram 10: Typ. gate threshold voltage**



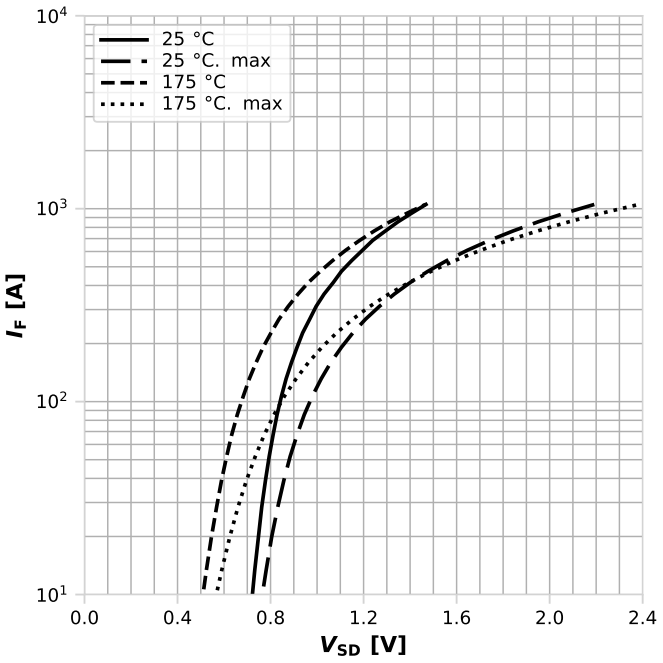

$V_{GS(th)}$=f($T_j$), $V_{GS}$=$V_{DS}$; parameter: $I_D$

**Diagram 11: Typ. capacitances**

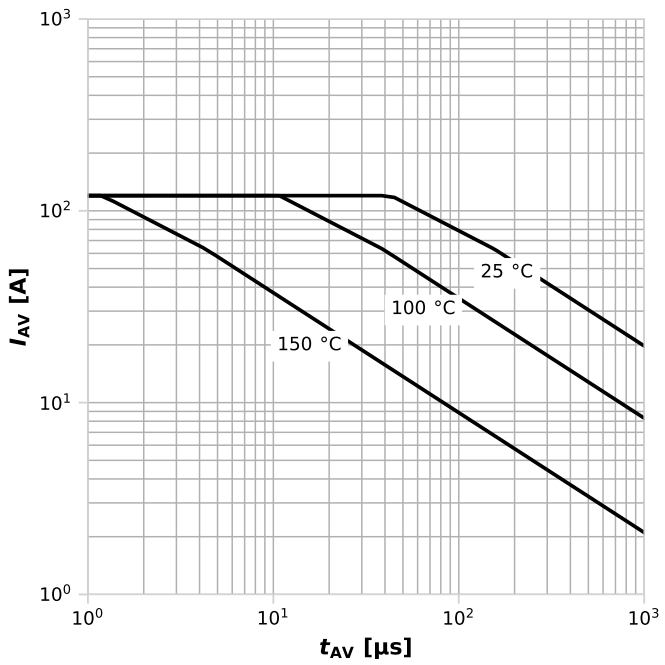
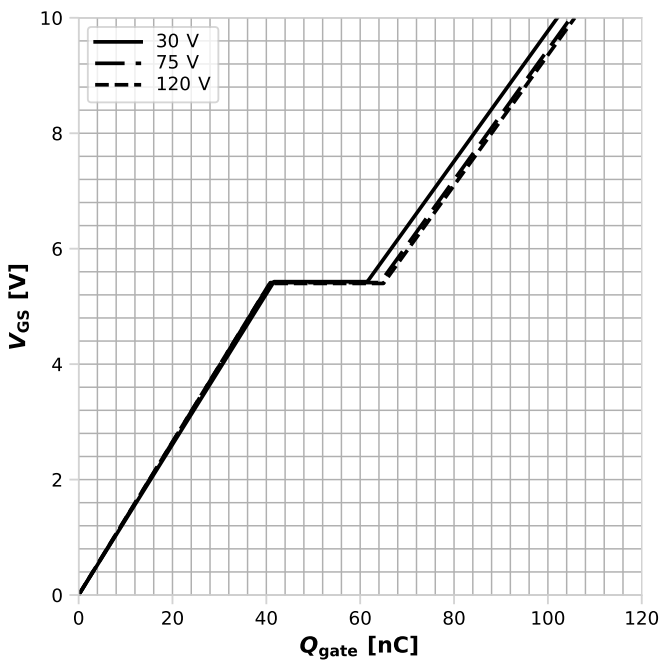


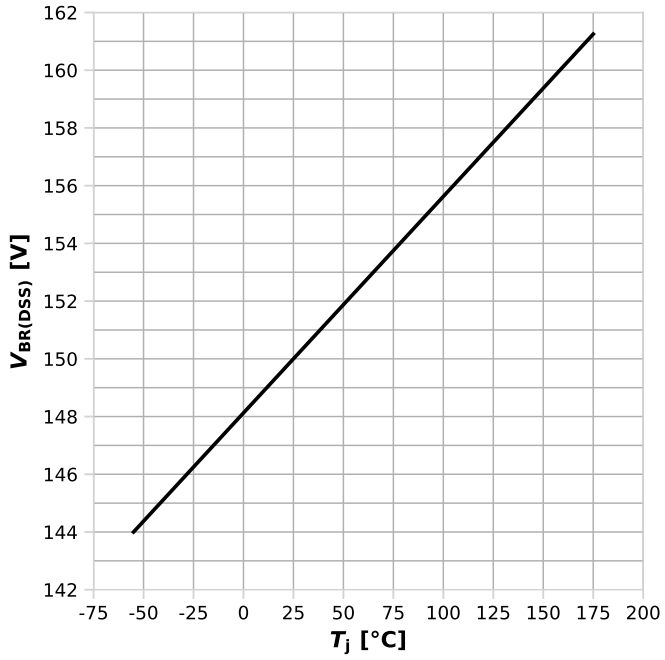
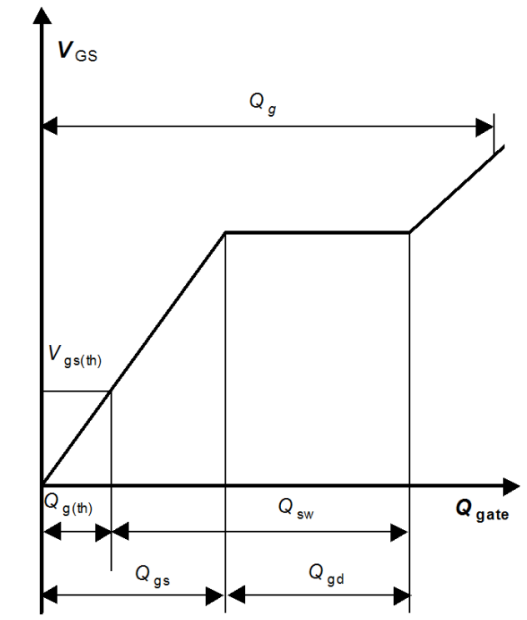

$C$=f($V_{DS}$); $V_{GS}$=0 V; $f$=1 MHz

**Diagram 12: Forward characteristics of reverse diode**

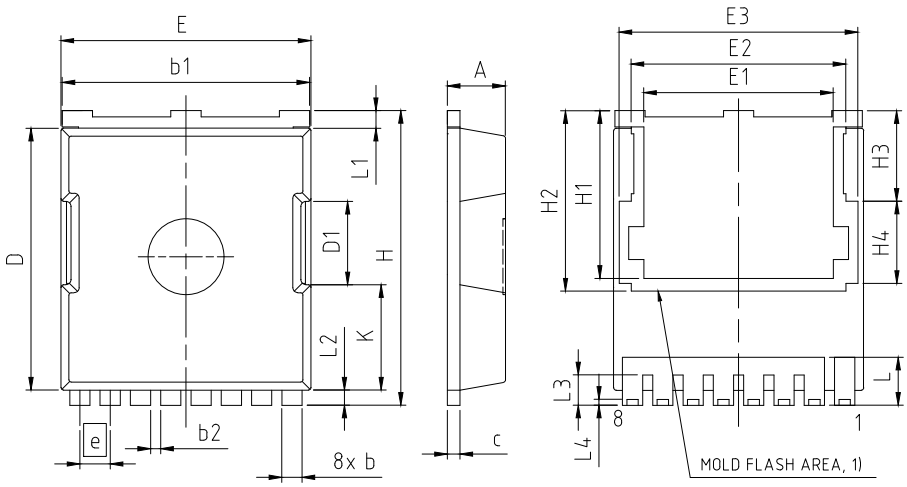



$I_F$=f($V_{SD}$); parameter: $T_j$

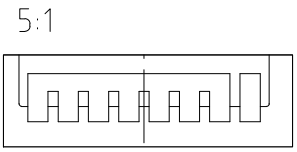
| Diagram 13: Avalanche characteristics | Diagram 14: Typ. gate charge |
|---|---|
|  |  |
| $I_{AS}$=f($t_{AV}$); $R_{GS}$=25 Ω; parameter: $T_{j,start}$ | $V_{GS}$=f($Q_{gate}$), $I_D$=60 A pulsed, $T_j$=25 °C; parameter: $V_{DD}$ |

| Diagram 15: Min. drain-source breakdown voltage | Gate charge waveforms |
|---|---|
|  |  |
| $V_{BR(DSS)}$=f($T_j$); $I_D$=1 mA | - |

# 5 Package Outlines




| PACKAGE - GROUP NUMBER: | PG-HSOF-8-U01 | |
|---|---|---|
| DIMENSIONS | MILLIMETERS | |
| | MIN. | MAX. |
| A | 2.20 | 2.40 |
| b | 0.70 | 0.90 |
| b1 | 9.70 | 9.90 |
| b2 | 0.42 | 0.50 |
| c | 0.40 | 0.60 |
| D | 10.28 | 10.58 |
| D1 | 3.30 | |
| E | 9.70 | 10.10 |
| E1 | 7.50 | |
| E2 | 8.50 | |
| E3 | 9.46 | |
| e | 1.20 (BSC) | |
| H | 11.48 | 11.88 |
| H1 | 6.55 | 6.95 |
| H2 | 7.15 | |
| H3 | 3.59 | |
| H4 | 3.26 | |
| N | 8 | |
| K | 4.18 | |
| L | 1.60 | 2.10 |
| L1 | 0.50 | 0.90 |
| L2 | 0.50 | 0.70 |
| L3 | 1.00 | 1.30 |
| L4 | 0.13 | 0.33 |




OPTIONAL LEAD FORM:
WITHOUT LTI OPTION

1) PATIALLY COVERED WITH MOLD FLASH

**Figure 1 Outline PG-HSOF-8, dimensions in mm**

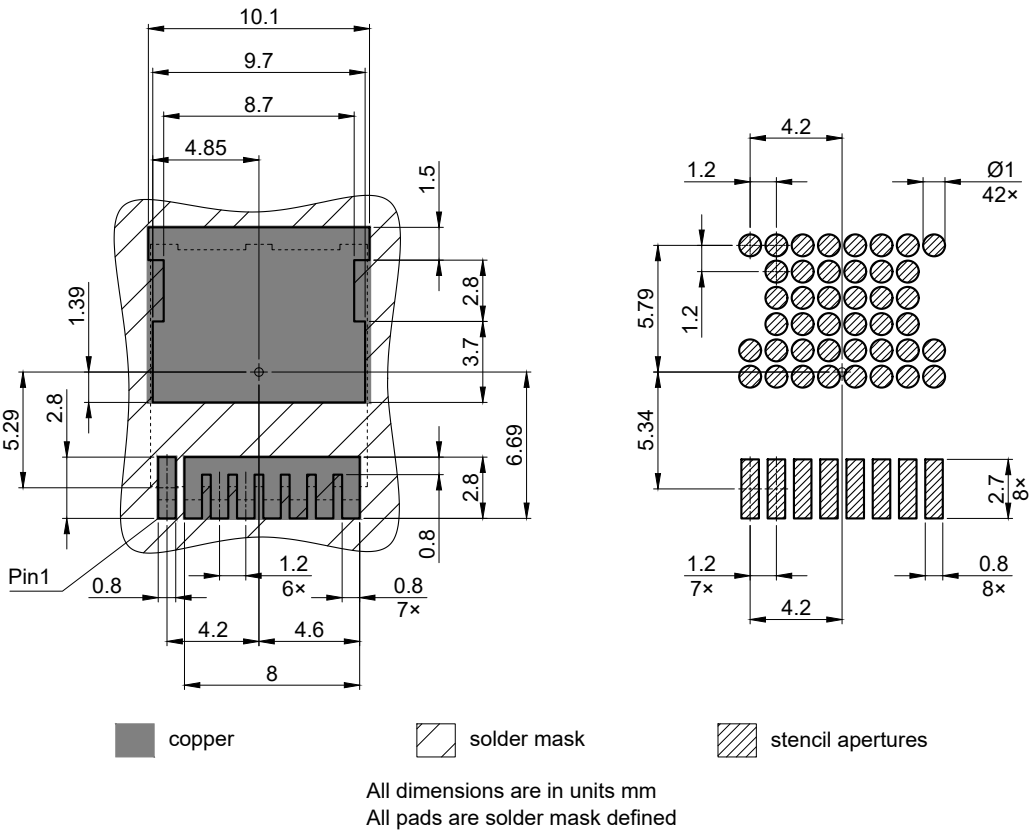



**Figure 2 Outline PG-HSOF-8, dimensions in mm**

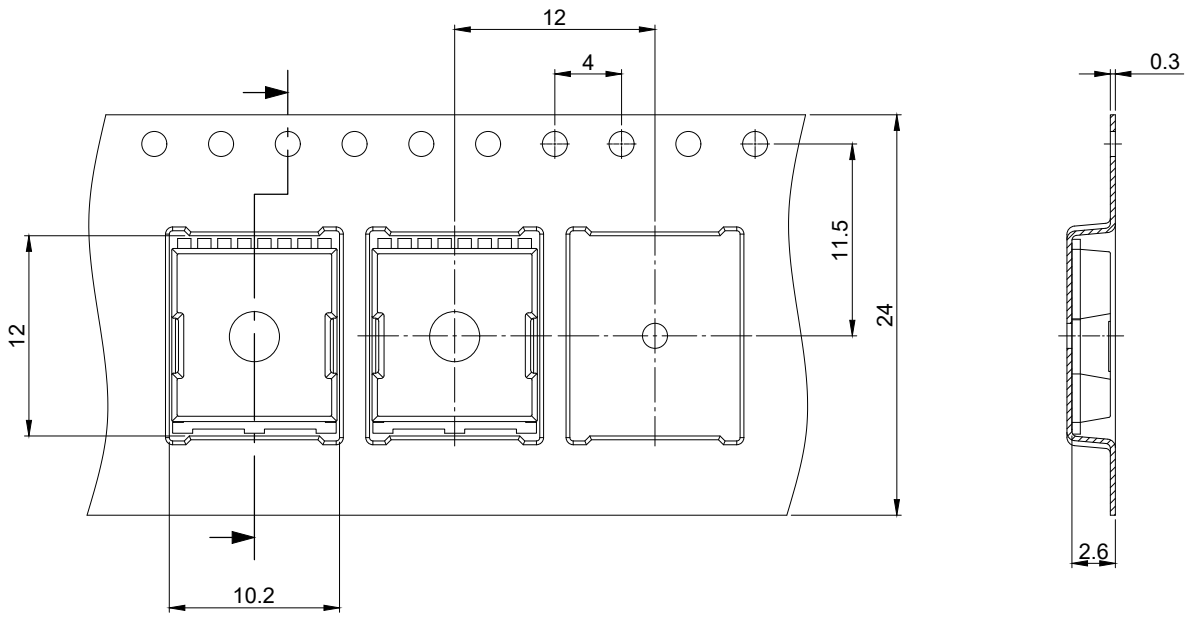



**Figure 3 Outline PG-HSOF-8, dimensions in mm**

## Revision History

IPT025N15NM6

### Revision 2024-04-22, Rev. 2.0

Previous Revision

| Revision | Date | Subjects (major changes since last revision) |
|---|---|---|
| 1.0 | 2024-03-15 | Release of preliminary version |
| 2.0 | 2024-04-22 | Release of final |

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### Parça koduyla arama

Üretici parça numarasını yazın; stok ve fiyatı hemen görün.

**www.entegreci.com**

### Ürün kategorileri

Entegreden kapasitöre tüm elektronik komponent kategorileri.

**Kategorilere göz atın**

### Üreticiler

Aradığınız üreticinin ürünlerini tek sayfada inceleyin.

**Üreticileri görün**

### Toplu alım ve teklif

Listede olmayan ya da yüksek adetli parçalar için teklif isteyin.

**Teklif isteyin**

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