# IRFZ14SPBF-VB Datasheet

## N-Channel 60V (D-S) MOSFET

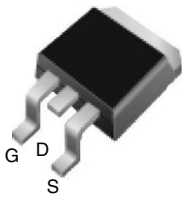
| PRODUCT SUMMARY | | | |
|---|---|---|---|
| $V_{DS}$ (V) | $R_{DS(on)}$ (Ω) | $I_D$ (A)[a, e] | $Q_g$ (Max) |
| 60 | 0.032 at $V_{GS}$ = 10 V | 50 | 66 nC |
| | 0.035 at $V_{GS}$ = 4.5 V | 40 | |

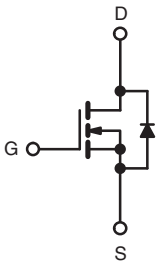
### FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Logic-Level Gate Drive
- Fast Switching
- Compliant to RoHS Directive 2002/95/EC

RoHS* COMPLIANT
HALOGEN FREE Available

**$D^2PAK$ (TO-263)**




N-Channel MOSFET

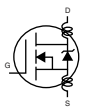
| ABSOLUTE MAXIMUM RATINGS ($T_C$ = 25 °C, unless otherwise noted) | | | | | |
|---|---|---|---|---|---|
| PARAMETER | | | SYMBOL | LIMIT | UNIT |
| Drain-Source Voltage | | | $V_{DS}$ | 60 | V |
| Gate-Source Voltage | | | $V_{GS}$ | ± 10 | |
| Continuous Drain Current[f] | $V_{GS}$ at 10 V | $T_C$ = 25 °C | $I_D$ | 50 | A |
| Continuous Drain Current | | $T_C$ = 100 °C | | 36 | |
| Pulsed Drain Current[a] | | | $I_{DM}$ | 200 | |
| Linear Derating Factor | | | | 1.0 | W/°C |
| Linear Derating Factor (PCB Mount)[e] | | | | 0.025 | |
| Single Pulse Avalanche Energy[b] | | | $E_{AS}$ | 400 | mJ |
| Maximum Power Dissipation | $T_C$ = 25 °C | | $P_D$ | 150 | W |
| Maximum Power Dissipation (PCB Mount)[e] | $T_A$ = 25 °C | | | 3.7 | |
| Peak Diode Recovery dV/dt[c] | | | dV/dt | 4.5 | V/ns |
| Operating Junction and Storage Temperature Range | | | $T_J$, $T_{stg}$ | - 55 to + 175 | °C |
| Soldering Recommendations (Peak Temperature)[d] | for 10 s | | | 300[d] | |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. $V_{DD}$ = 25 V, starting $T_J$ = 25 °C, L = 179 µH, $R_g$ = 25 Ω, $I_{AS}$ = 51 A (see fig. 12).
c. $I_{SD}$ ≤ 51 A, dI/dt ≤ 250 A/µs, $V_{DD}$ ≤ $V_{DS}$, $T_J$ ≤ 175 °C.
d. 1.6 mm from case.
e. When mounted on 1" square PCB (FR-4 or G-10 material).
f. Current limited by the package, (die current = 51 A).

| THERMAL RESISTANCE RATINGS | | | | |
|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TYP.** | **MAX.** | **UNIT** |
| Maximum Junction-to-Ambient | $R_{thJA}$ | - | 62 | °C/W |
| Maximum Junction-to-Ambient (PCB Mount)[a] | $R_{thJA}$ | - | 40 | |
| Maximum Junction-to-Case (Drain) | $R_{thJC}$ | - | 1.0 | |

**Note**
a. When mounted on 1" square PCB (FR-4 or G-10 material).

| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0, $I_D$ = 250 µA | | 60 | - | - | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D$ = 1 mA | | - | 0.070 | - | V/°C |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | | 1.0 | - | 3.0 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{GS}$ = ± 10 V | | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 60 V, $V_{GS}$ = 0 V | | - | - | 25 | µA |
| | | $V_{DS}$ = 48 V, $V_{GS}$ = 0 V, $T_J$ = 150 °C | | - | - | 250 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V | $I_D$ = 21 A[b] | - | 0.032 | - | Ω |
| | | $V_{GS}$ = 4.5 V | $I_D$ = 15 A[b] | - | 0.035 | - | |
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ = 25 V, $I_D$ = 21A [b] | | 23 | - | - | S |
| **Dynamic** | | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1.0 MHz, see fig. 5 | | - | 3000 | - | pF |
| Output Capacitance | $C_{oss}$ | | | - | 1000 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | - | 200 | - | |
| Total Gate Charge | $Q_g$ | $V_{GS}$ = 5.0 V | $I_D$ = 51 A, $V_{DS}$ = 48 V, see fig. 6 and 13[b] | - | 60 | - | nC |
| Gate-Source Charge | $Q_{gs}$ | | | - | 10 | - | |
| Gate-Drain Charge | $Q_{gd}$ | | | - | 40 | - | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 30 V, $I_D$ = 51 A, $R_g$ = 4.6 Ω, $R_D$ = 0.56 Ω, see fig. 10[b] | | - | 17 | - | ns |
| Rise Time | $t_r$ | | | - | 230 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | - | 42 | - | |
| Fall Time | $t_f$ | | | - | 110 | - | |
| Internal Drain Inductance | $L_D$ | Between lead, 6 mm (0.25") from package and center of die contact  | | - | 4.5 | - | nH |
| Internal Source Inductance | $L_S$ | | | - | 7.5 | - | |
| **Drain-Source Body Diode Characteristics** | | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | 50[c] | A |
| Pulsed Diode Forward Current[a] | $I_{SM}$ | | | - | - | 200 | |
| Body Diode Voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ = 51 A, $V_{GS}$ = 0 V[b] | | - | - | 2.5 | V |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $T_J$ = 25 °C, $I_F$ = 51 A, dI/dt = 100 A/µs[b] | | - | 130 | 180 | ns |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | | - | 0.84 | 1.3 | µC |
| Forward Turn-On Time | $t_{on}$ | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$) | | | | | |

**Notes**
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.
c. Current limited by the package, (Die Current = 51 A).

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

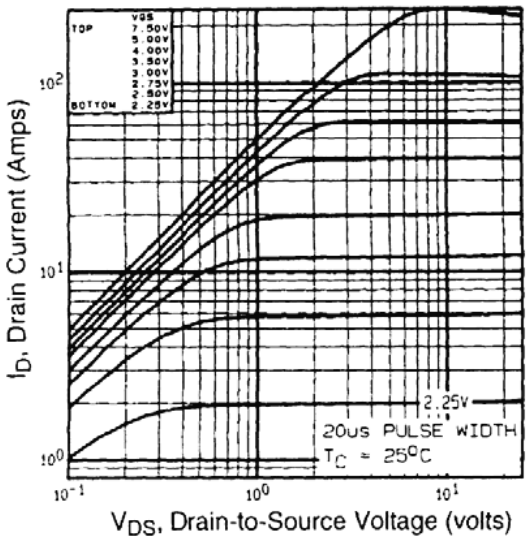



**Fig. 1 - Typical Output Characteristics, $T_C$ = 25 °C**

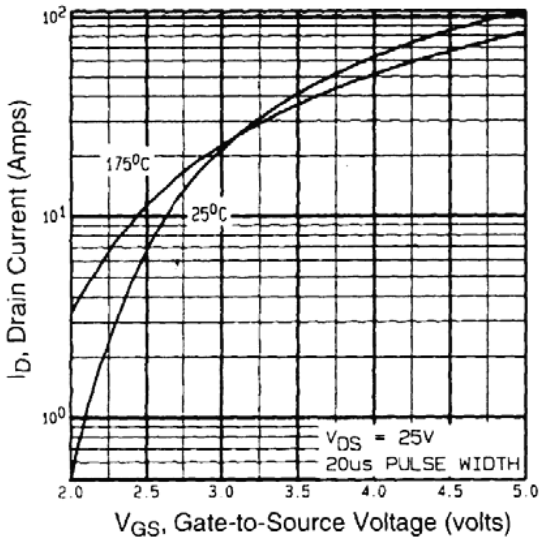



**Fig. 3 - Typical Transfer Characteristics**

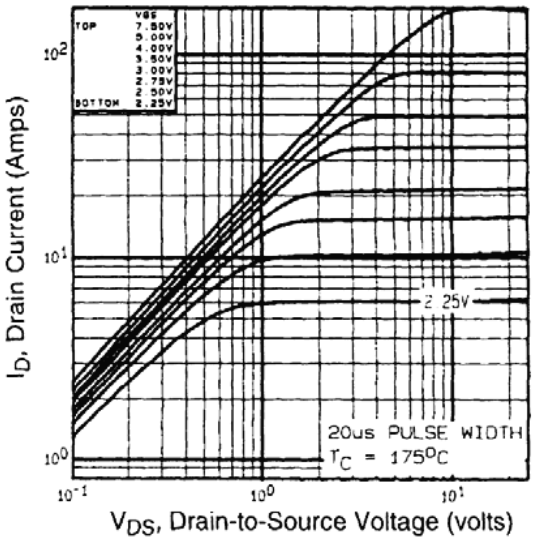



**Fig. 2 - Typical Output Characteristics, $T_C$ = 150 °C**

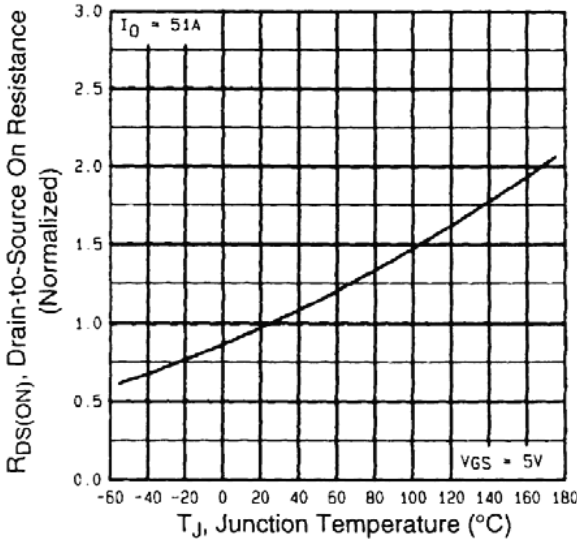



**Fig. 4 - Normalized On-Resistance vs. Temperature**

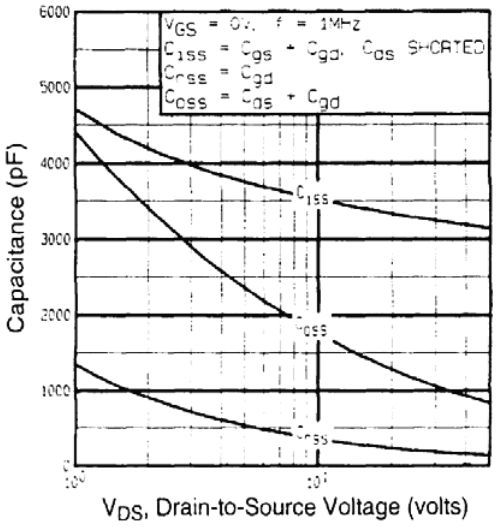



Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

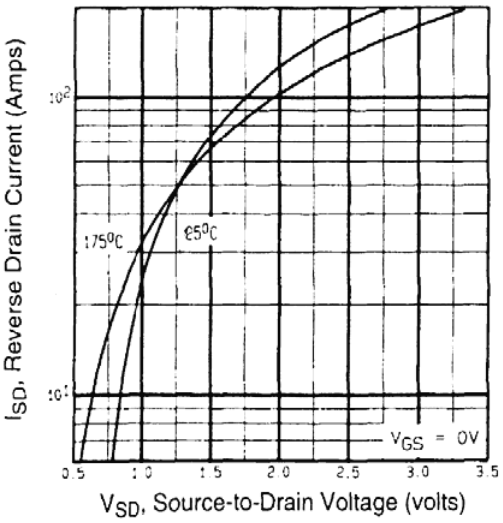



Fig. 7 - Typical Source-Drain Diode Forward Voltage

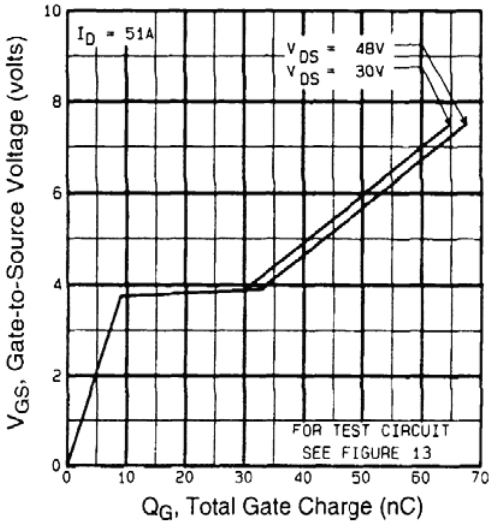



Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

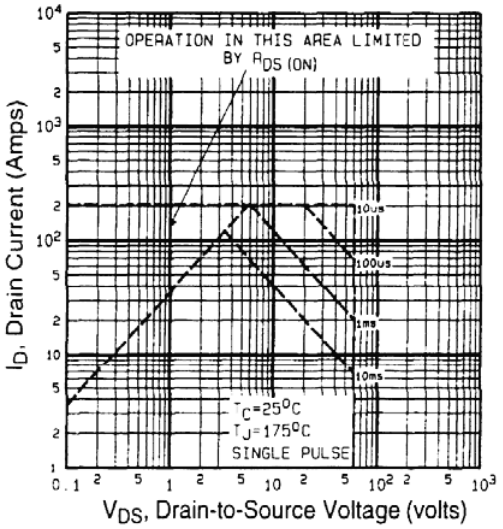



Fig. 8 - Maximum Safe Operating Area

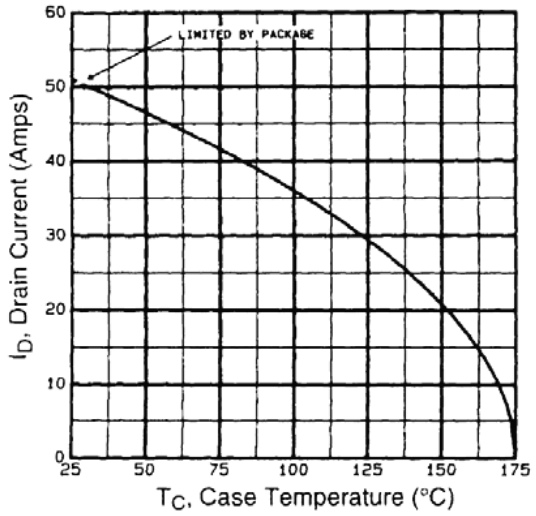



Fig. 9 - Maximum Drain Current vs. Case Temperature

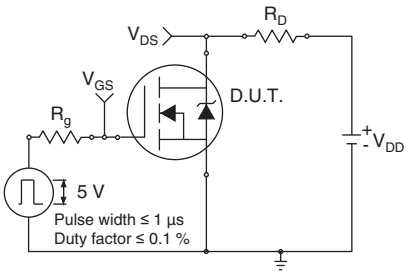



Fig. 10a - Switching Time Test Circuit

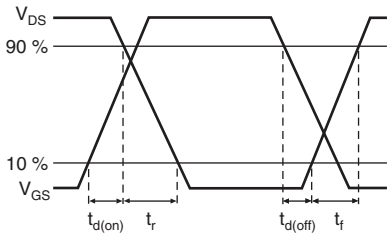



Fig. 10b - Switching Time Waveforms

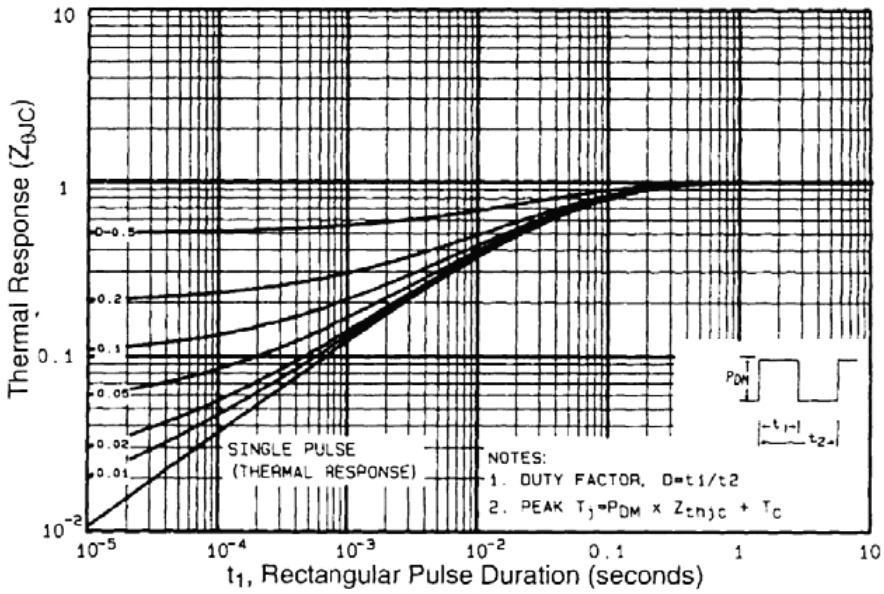



Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

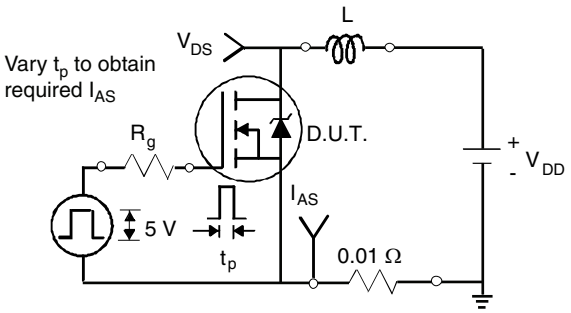



Fig. 12a - Unclamped Inductive Test Circuit

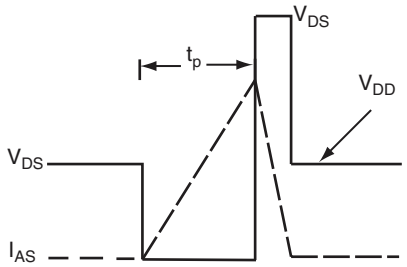



Fig. 12b - Unclamped Inductive Waveforms

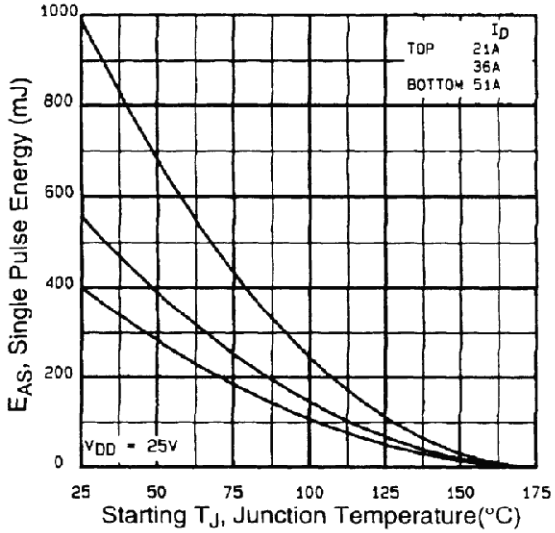



Fig. 12c - Maximum Avalanche Energy vs. Drain Current

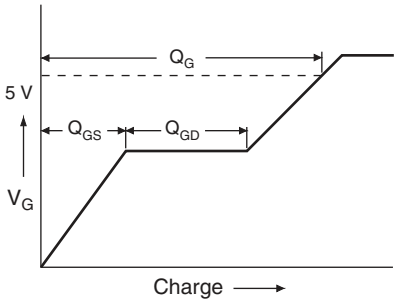



Fig. 13a - Basic Gate Charge Waveform

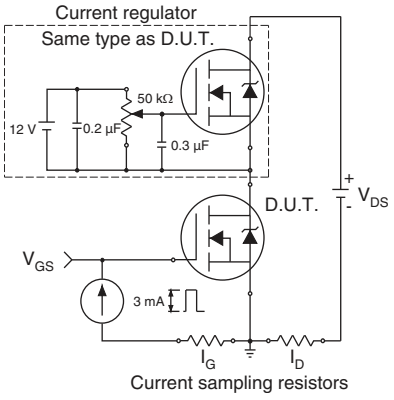
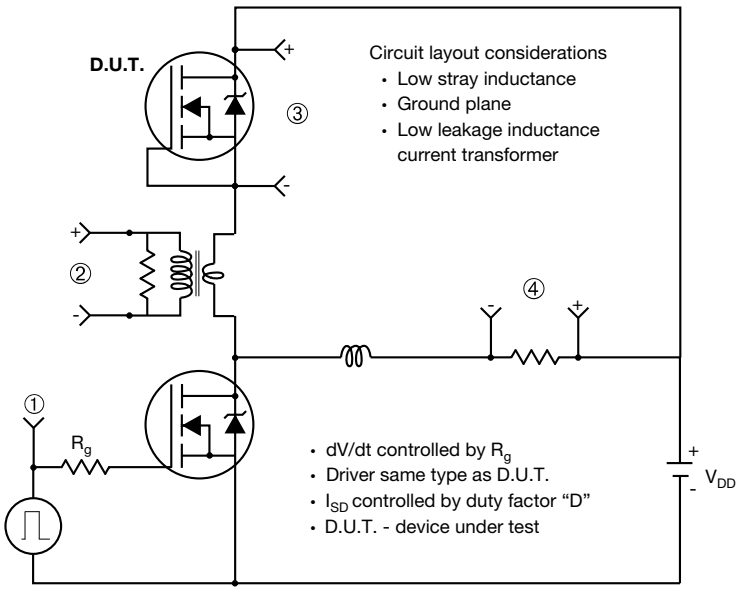
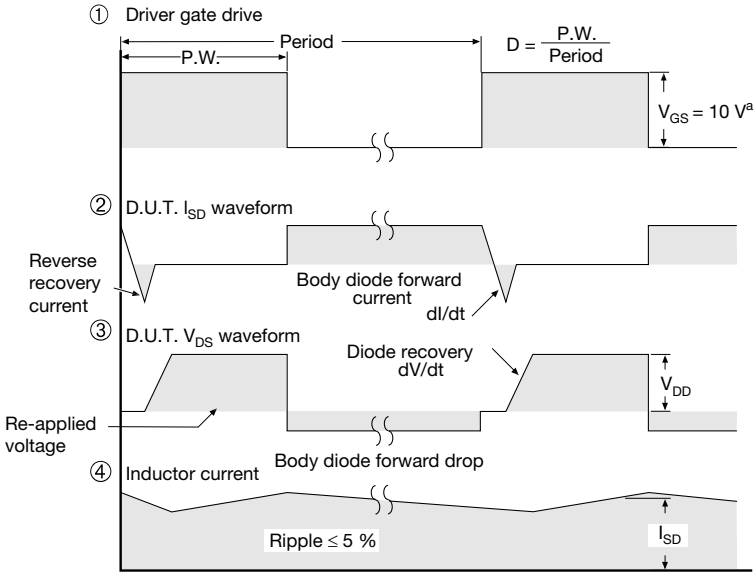



Fig. 13b - Gate Charge Test Circuit

**Peak Diode Recovery dV/dt Test Circuit**



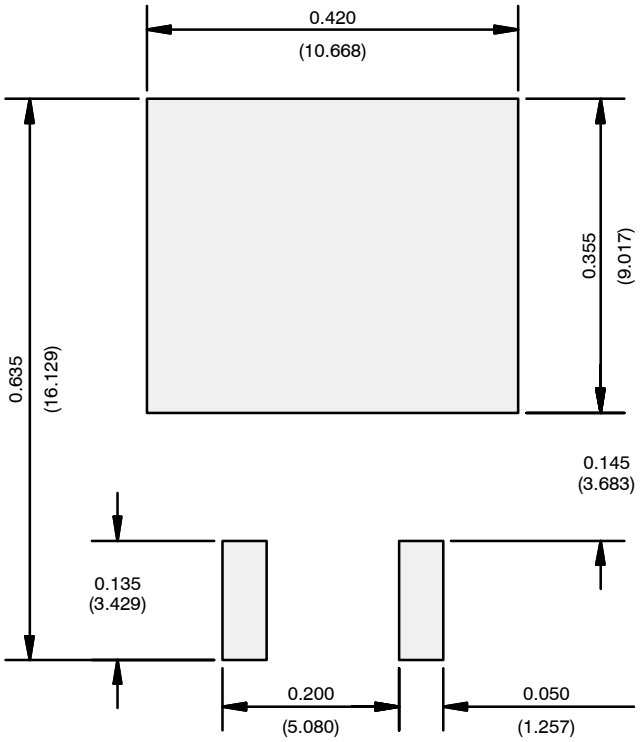




**Note**

a. $V_{GS}$ = 5 V for logic level devices

**Fig. 14 - For N-Channel**

## RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead




Recommended Minimum Pads
Dimensions in Inches/(mm)

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