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FAIRCHILD SEMICONDUCTOR®

FDMA7628

February 2026

Single N-Channel 1.5 V Specified PowerTrench® MOSFET
20 V, 9.4 A, 14.5 mΩ

Features

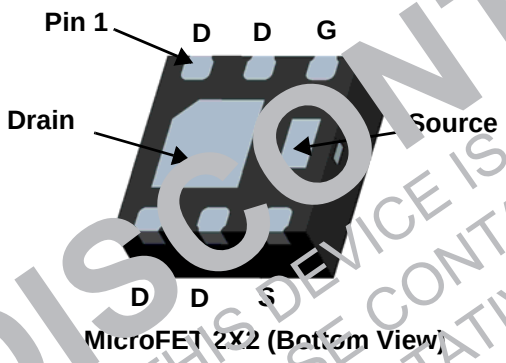
- Max $r_{DS(on)}$ = 14.5 mΩ at V_{GS} = 4.5 V, I_D = 9.4 A
- Max $r_{DS(on)}$ = 18.2 mΩ at V_{GS} = 2.5 V, I_D = 8.3 A
- Max $r_{DS(on)}$ = 23.3 mΩ at V_{GS} = 1.8 V, I_D = 7.3 A
- Max $r_{DS(on)}$ = 32.3 mΩ at V_{GS} = 1.5 V, I_D = 6.2 A
- Low Profile-0.8 mm maximum in the new package MicroFET 2x2 mm
- RoHS Compliant

General Description

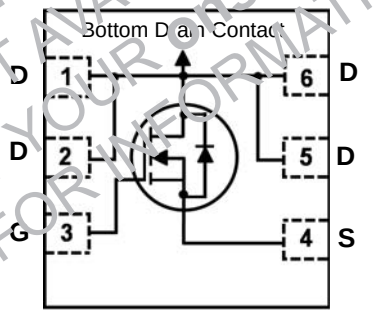
This Single N-Channel MOSFET has been designed using Fairchild Semiconductor's advanced Power Trench® process to optimize the $r_{DS(ON)}$ @ V_{GS} = 1.5 V on special MicroFET leadframe.

Applications

- Li-Ion Battery Pack
- DC-DC Buck Converter



MicroFET 2X2 (Bottom View)



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MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			20	V
V_{GS}	Gate to Source Voltage			±8	V
I_D	-Continuous	T_A = 25 °C	(Note 1a)	9.4	A
	-Pulsed			54	
P_D	Power Dissipation	T_A = 25 °C	(Note 1a)	1.9	W
	Power Dissipation	T_A = 25 °C	(Note 1b)	0.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	65	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	180	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
104	FDMA7628	MicroFET 2X2	7 ”	12 mm	3000 units

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Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		15		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	0.4	0.6	1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-3		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 4.5 V, I_D = 9.4 A		11.3	14.5	mΩ
		V_{GS} = 2.5 V, I_D = 8.3 A		12.7	18.2	
		V_{GS} = 1.8 V, I_D = 7.3 A			23.3	
		V_{GS} = 1.5 V, I_D = 6.2 A		18.3	32.3	
		V_{GS} = 4.5 V, I_D = 9.4 A, T_J = 125 °C		14.7	18.3	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 9.4 A		56		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz		1260	1680	pF
C_{oss}	Output Capacitance			180	240	pF
C_{rss}	Reverse Transfer Capacitance			122	185	pF
R_g	Gate Resistance			1.9		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 10 V, I_D = 9.4 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω		9	17	ns
t_r	Rise Time			6	11	ns
$t_{d(off)}$	Turn-Off Delay Time			37	58	ns
t_f	Fall Time			6	11	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 4.5 V, V_{DD} = 10 V, I_D = 9.4 A		17.5		nC
	Total Gate Charge	V_{GS} = 0 V to 2.5 V		10.0		nC
	Total Gate Charge	V_{GS} = 0 V to 1.8 V		7.4		nC
	Total Gate Charge	V_{GS} = 0 V to 1.5 V		6.2		nC
Q_{gs}	Gate to Source Charge			1.7		nC
Q_{gd}	Gate to Drain “Miller” Charge			2.7		nC
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain-Source Diode Forward Current				2.0	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.0 A (Note 2)		0.63	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 9.4 A, di/dt = 100 A/μs		16	29	ns
Q_{rr}	Reverse Recovery Charge			5	10	nC

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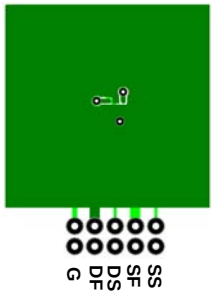
NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a.65 °C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 180 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

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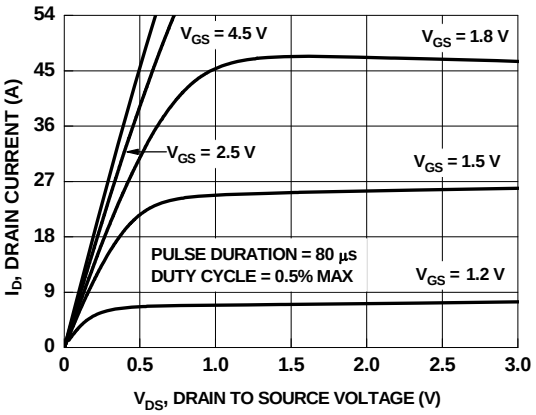

Figure 1. On Region Characteristics

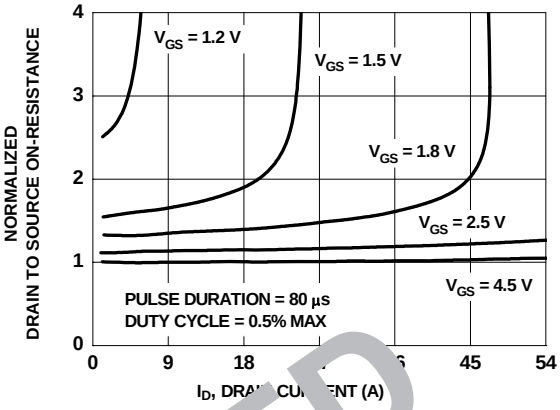

Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

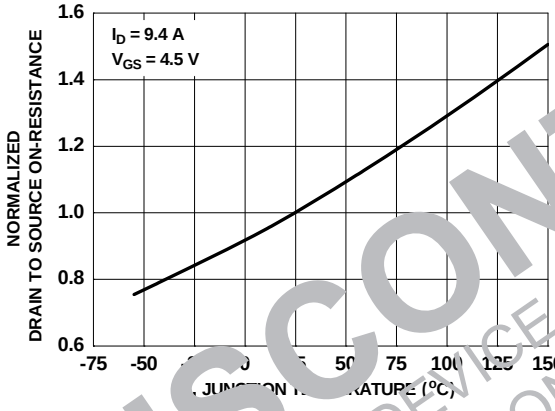

Figure 3. Normalized On Resistance vs Junction Temperature

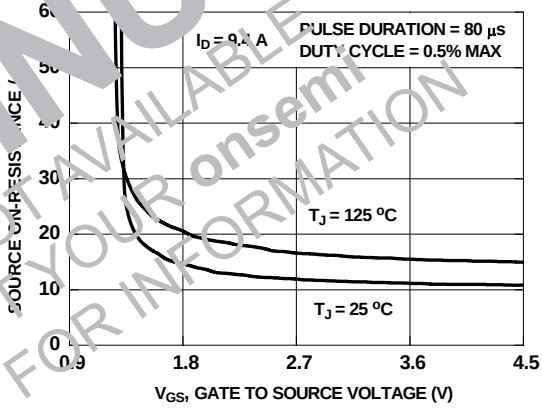

Figure 4. On-Resistance vs Gate to Source Voltage

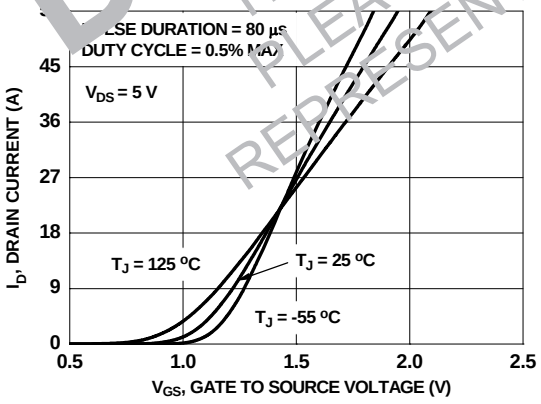

Figure 5. Transfer Characteristics

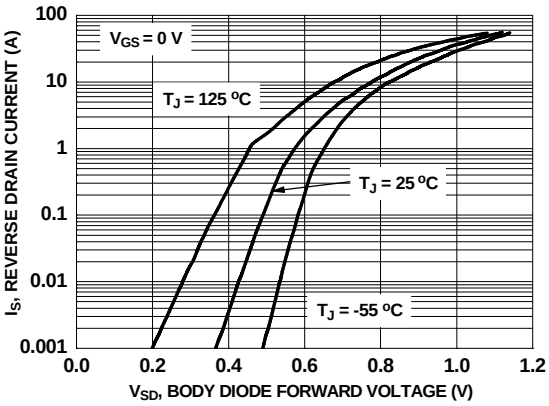

Figure 6. Source to Drain Diode Forward Voltage vs Source Current

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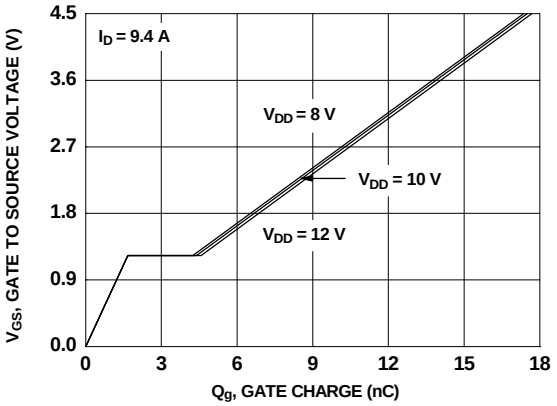

Figure 7. Gate Charge Characteristics

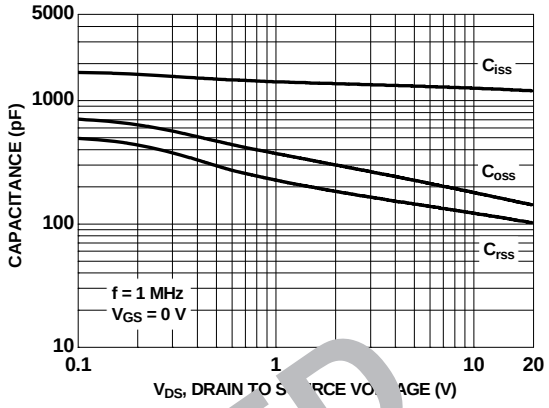

Figure 8. Capacitance vs Drain to Source Voltage

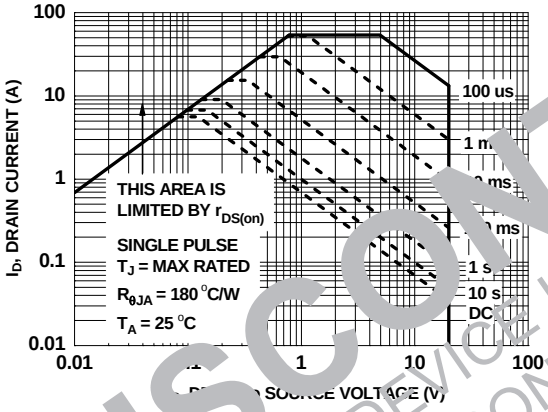

Figure 9. Forward Bias Safe Operating Area

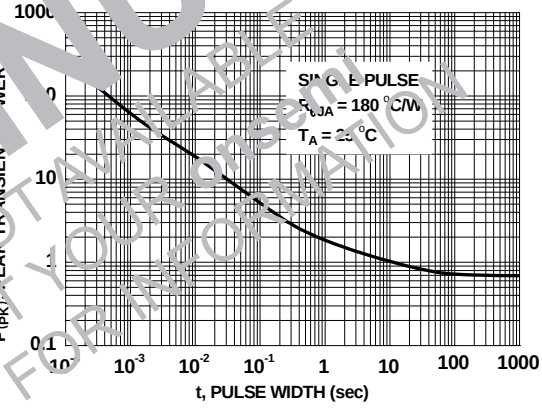

Figure 10. Single Pulse Maximum Power Dissipation

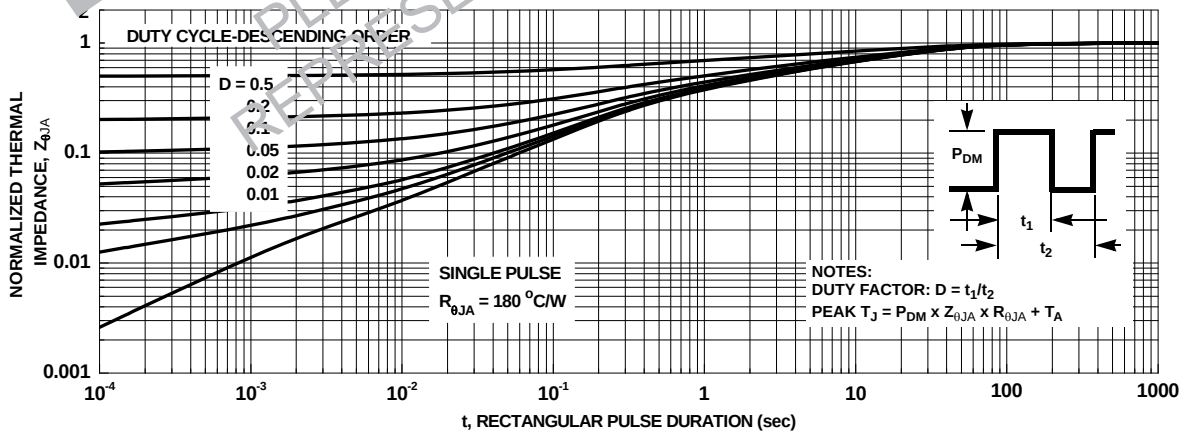

Figure 11. Junction-to-Ambient Transient Thermal Response Curve

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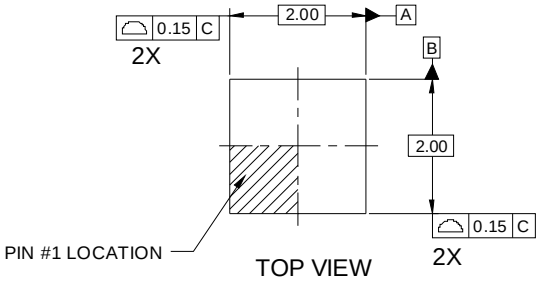
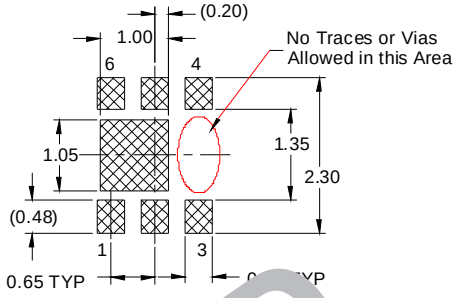
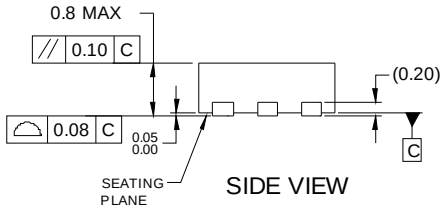
Dimensional Outline and Pad Layout



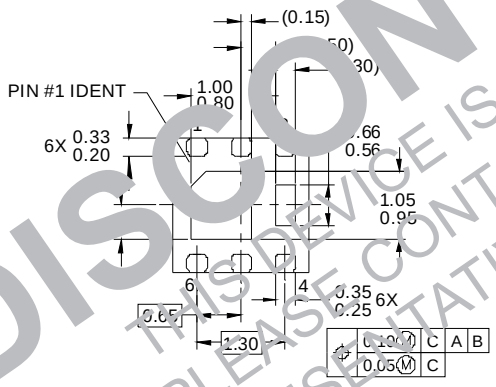
TOP VIEW



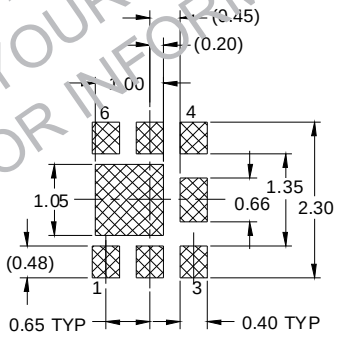
RECOMMENDED LAND PATTERN OPT 1



SIDE VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN OPT 2

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A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-229 DATED AUG/2003
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

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