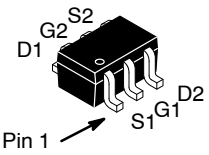
MOSFET - Dual N-Channel, POWERTRENCH®

20 V, 1.2 A, 175 mΩ

FDG1024NZ



SC−88/SC−70 6 Lead, 1.25 x 2
CASE 419AD

Description

This dual N−Channel logic level enhancement mode field effect transistors are produced using **onsemi**'s proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on−state resistance. This device has been designed especially for low voltage applications as a replacement for bipolar digital transistors and small signal MOSFETs. Since bias resistors are not required, this dual digital FET can replace several different digital transistors, with different bias resistor values.

Features

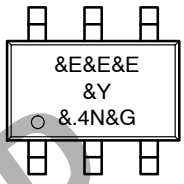
- Max $r_{DS(on)}$ = 175 mΩ at V_{GS} = 4.5 V, I_D = 1.2 A
- Max $r_{DS(on)}$ = 215 mΩ at V_{GS} = 2.5 V, I_D = 1.0 A
- Max $r_{DS(on)}$ = 270 mΩ at V_{GS} = 1.8 V, I_D = 0.9 A
- Max $r_{DS(on)}$ = 389 mΩ at V_{GS} = 1.5 V, I_D = 0.8 A
- HBM ESD Protection Level > 2 kV (Note 3)
- Very Low Level Gate Drive Requirements Allowing Operation in 1.5 V Circuits ($V_{GS(th)}$ < 1 V)
- Very Small Package Outline SC−88/SC−70 6 Lead
- RoHS Compliant
- These Device is Halogen Free

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter		Ratings	Unit
V_{DS}	Drain to Source Voltage		20	V
V_{GS}	Gate to Source Voltage		±8	V
I_D	Drain Current	Continuous T_A = 25°C (Note 1a)	1.2	A
		Pulsed	6	
P_D	Power Dissipation	T_A = 25°C (Note 1a)	0.36	W
		T_A = 25°C (Note 1b)	0.30	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150	°C

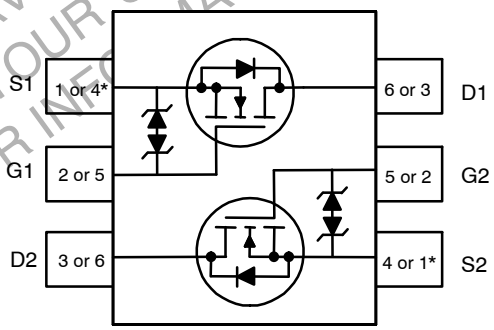
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAM



&E	= Designates Space
&Y	= Binary Calendar Year
&.4N	= Specific Device Code
&G	= 1−Digit Weekly Date Code

ELECTRICAL CONNECTION



N−Channel MOSFET

* The pinouts are symmetrical; pin 1 and 4 are interchangeable.
Units inside the carrier can be of either orientation and will not affect the functionality of the device.

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

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THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	350	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	415	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

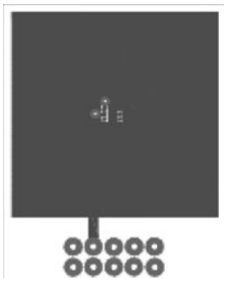
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	20	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	14	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8 V, V_{DS} = 0 V	–	–	±10	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	0.4	0.8	1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	–3	–	mV/°C
$r_{DS(ON)}$	Static Drain to Source On Resistance	V_{GS} = 4.5 V, I_D = 1.2 A	–	160	175	mΩ
		V_{GS} = 2.5 V, I_D = 1.0 A	–	185	215	
		V_{GS} = 1.8 V, I_D = 0.9 A	–	232	270	
		V_{GS} = 1.5 V, I_D = 0.8 A	–	321	389	
		V_{GS} = 4.5 V, I_D = 1.2 A, T_J = 125°C	–	220	259	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 1.2 A	–	4	–	S
DYNAMIC CHARACTERISTICS						
C_{iSS}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	–	115	150	pF
C_{OSS}	Output Capacitance		–	25	35	pF
Crss	Reverse Transfer Capacitance		–	20	25	pF
R_g	Gate Resistance		–	4.6	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 10 V, I_D = 1.2 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω	–	3.7	10	ns
t_r	Rise Time		–	1.7	10	ns
$t_{d(off)}$	Turn–Off Delay Time		–	11	19	ns
t_f	Fall Time		–	1.5	10	ns
Q_g	Total Gate Charge	V_{GS} = 4.5 V, V_{DD} = 10 V, I_D = 1.2 A	–	1.8	2.6	nC
Qgs	Gate to Source Charge		–	0.3	–	nC
Qgd	Gate to Drain “Miller” Charge		–	0.4	–	nC
DRAIN–SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Drain–Source Diode Forward Current		–	–	0.3	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.3 A (Note 2)	–	0.7	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 1.2 A, di/dt = 100 A/μs	–	10	20	ns
Q_{rr}	Reverse Recovery Charge		–	1.9	10	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

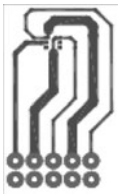
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NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a. 350°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 415°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

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PACKAGE MARKING AND ORDERING INFORMATION

ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Shipping†
.4N	FDG1024NZ	SC−88/SC−70 6 Lead (Halogen Free)	7”	8 mm	3000 / Tape and Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

(T_J = 25°C UNLESS OTHERWISE NOTED)

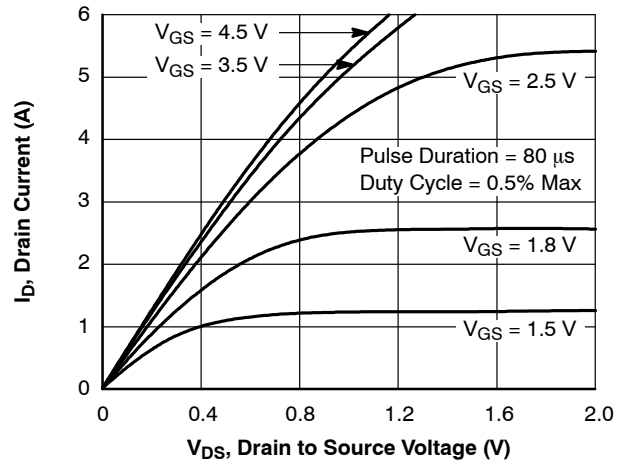


Figure 1. On−Region Characteristics

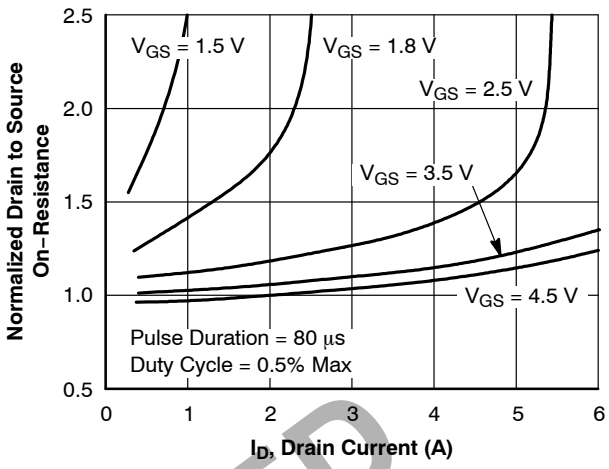


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

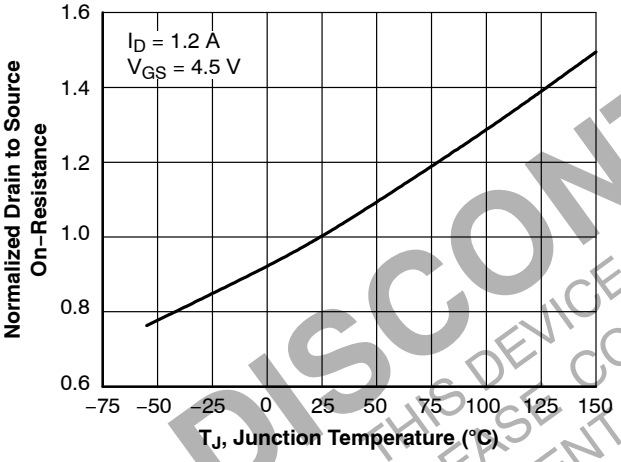


Figure 3. Normalized On−Resistance vs. Junction Temperature

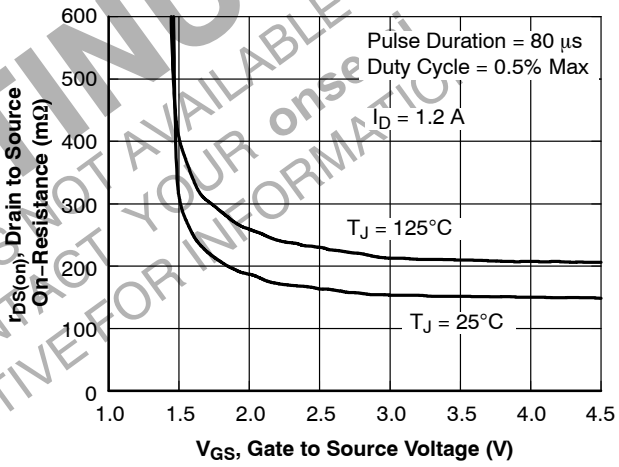


Figure 4. On−Resistance vs. Gate to Source Voltage

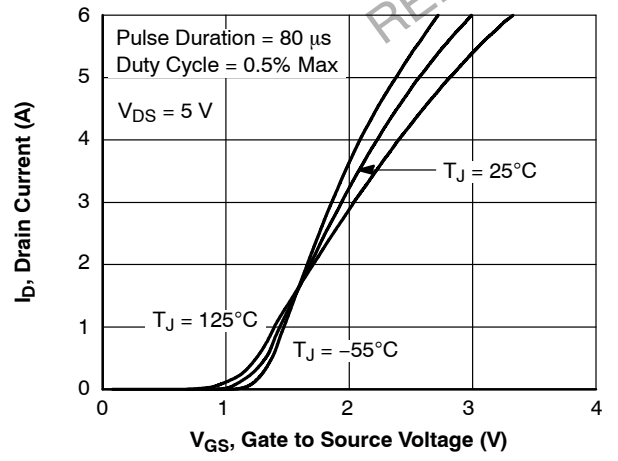


Figure 5. Transfer Characteristics

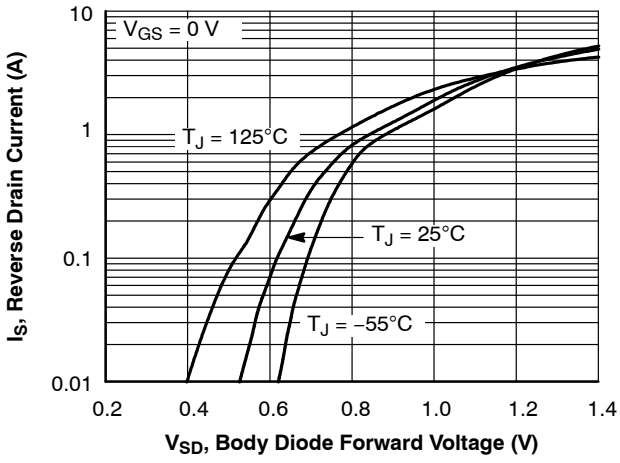


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

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TYPICAL CHARACTERISTICS (CONTINUED)

(T_J = 25°C UNLESS OTHERWISE NOTED)

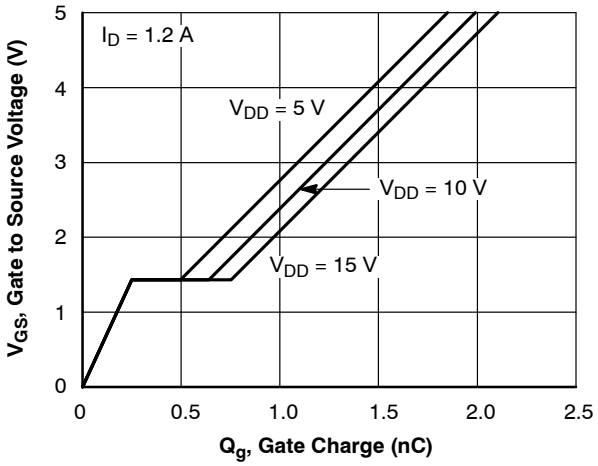


Figure 7. Gate Charge Characteristics

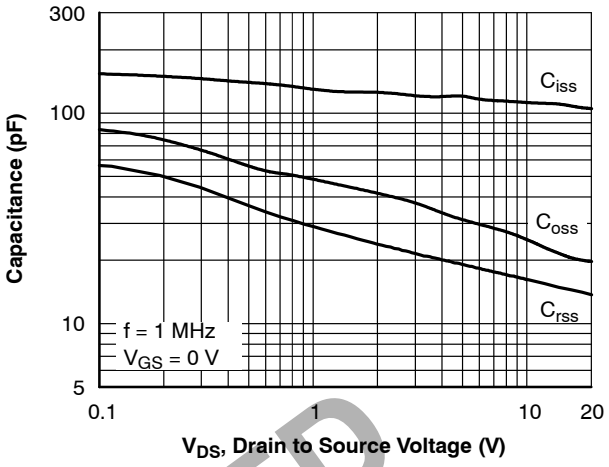


Figure 8. Capacitance vs. Drain to Source Voltage

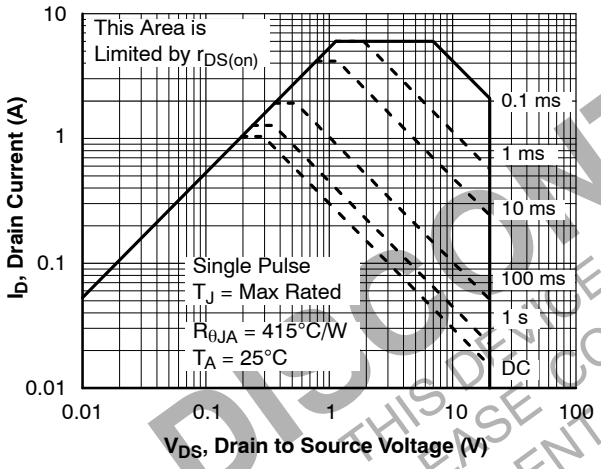


Figure 9. Forward Bias Safe Operating Area

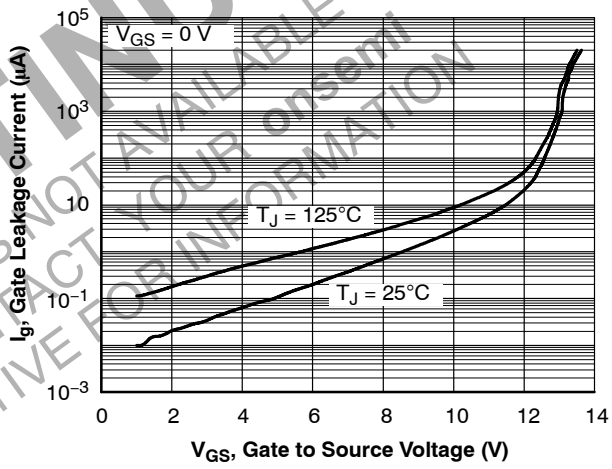


Figure 10. Gate Leakage Current vs. Gate to Source Voltage

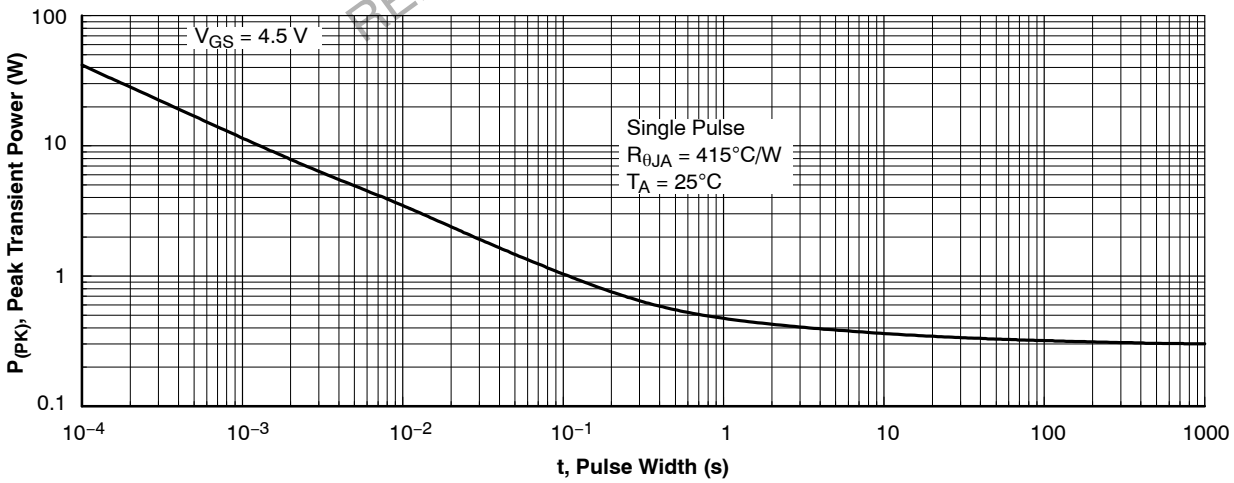


Figure 11. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS (CONTINUED)

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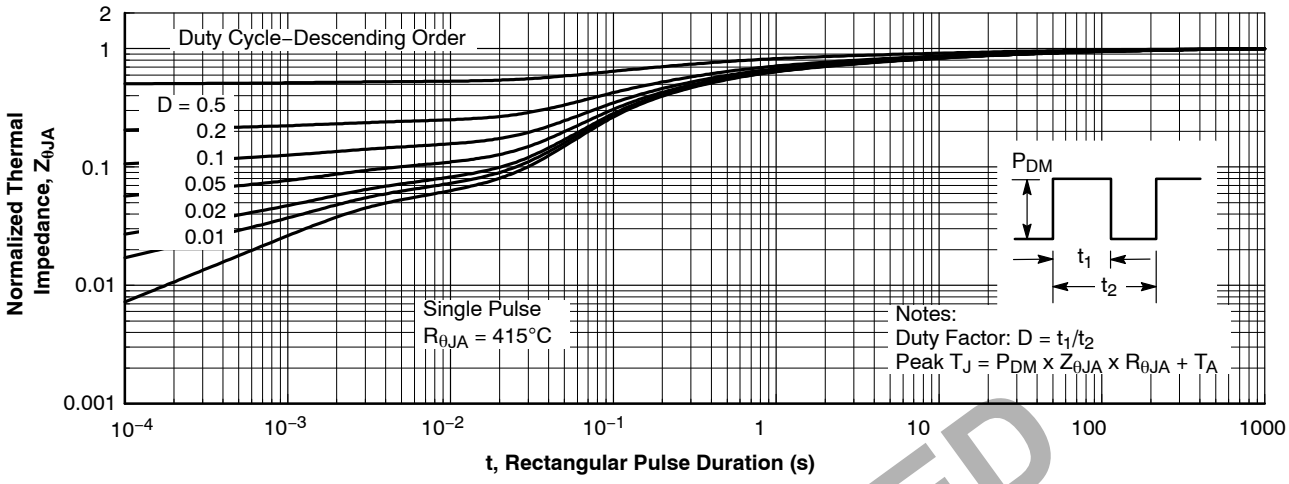


Figure 12. Transient Thermal Response Curve

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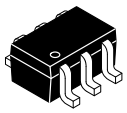
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REVISION HISTORY

Revision	Description of Changes	Date
3	Document Discontinued.	1/15/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

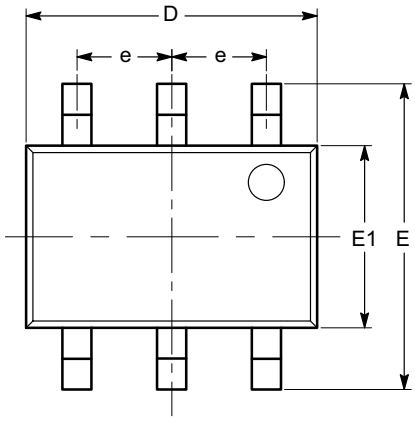
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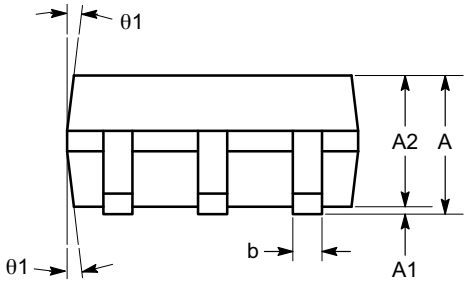
SC−88 (SC−70 6 Lead), 1.25x2
CASE 419AD
ISSUE A

DATE 07 JUL 2010

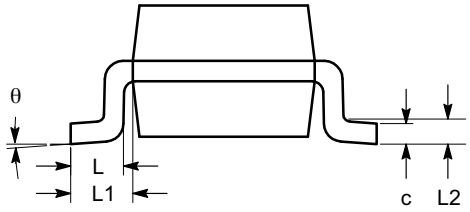


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.10
A1	0.00		0.10
A2	0.80		1.00
b	0.15		0.30
c	0.10		0.18
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e		0.65 BSC	
L	0.26	0.36	0.46
L1		0.42 REF	
L2		0.15 BSC	
θ	0°		8°
θ1	4°		10°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-203.

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DESCRIPTION:	**SC−88 (SC−70 6 LEAD), 1.25X2**		**PAGE 1 OF 1**

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Teklif isteyin

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