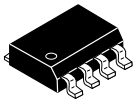
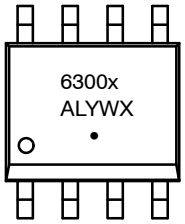
Highly Integrated Quasi-Resonant Current Mode PWM Controller

FAN6300A / FAN6300H



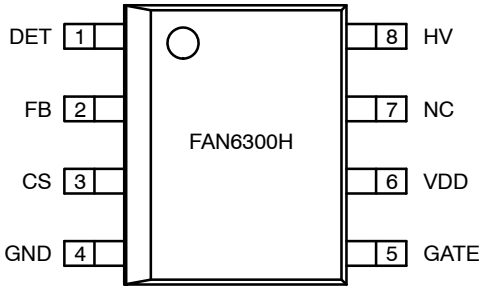
SOIC8
CASE 751EB

MARKING DIAGRAM



6300x = Specific Device Code (x = A or H)
A = Assembly Location
L = Wafer Lot Traceability
YW = Date Code
X = Manufacture Flow
• = Pb Free

PIN ASSIGNMENT



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

The highly integrated FAN6300A/H of PWM controller provides several features to enhance the performance of flyback converters. FAN6300A is applied on quasiresonant flyback converters where maximum operating frequency is below 100 kHz. FAN6300H is suitable for high−frequency operation (up to 190 kHz). A built−in HV startup circuit can provide more startup current to reduce the startup time of the controller. Once the V_{DD} voltage exceeds the turn−on threshold voltage, the HV startup function is disabled immediately to reduce power consumption. An internal valley voltage detector ensures power system operates at quasi−resonant operation over a wide−range of line voltage and any load conditions, as well as reducing switching loss to minimize switching voltage on drain of power MOSFET.

To minimize standby power consumption and light−load efficiency, a proprietary green−mode function provides off−time modulation to decrease switching frequency and perform extended valley voltage switching to keep to a minimum switching voltage. The operating frequency is limited by minimum t_{OFF} time, which is 38 μs to 8 μs in FAN6300A and 13 μs to 3 μs in FAN6300H, so FAN6300H can operate at higher switching frequency than FAN6300A.

FAN6300A/H controller also provides many protection functions. Pulse−by−pulse current limiting ensures the fixed−peak current limit level, even when a short circuit occurs. Once an open−circuit failure occurs in the feedback loop, the internal protection circuit disables PWM output immediately. As long as VDD drops below the turn−off threshold voltage, the controller also disables PWM output. The gate output is clamped at 18 V to protect the power MOS from high gate−source voltage conditions. The minimum t_{OFF} time limit prevents the system frequency from being too high. If the DET pin triggers OVP, internal OTP is triggered and the power system enters latch−mode until AC power is removed.

The FAN6300A/H controller is available in the 8−pin SOIC8 package.

Features

- High−Voltage Startup
- Quasi−Resonant Operation
- Cycle−by−Cycle Current Limiting
- Peak−Current−Mode Control
- Leading−Edge Blanking (LEB)
- Internal Minimum t_{OFF}
- Internal 5 ms Soft−Start
- Over Power Compensation
- GATE Output Maximum Voltage
- Auto−Recovery Over−Current Protection (FB Pin)
- Auto−Recovery Open−Loop Protection (FB Pin)
- VDD Pin and Output Voltage (DET Pin) OVP Latched
- Low Frequency Operation (below 100 kHz) for FAN6300A
- High Frequency Operation (up to 190 kHz) for FAN6300H

Applications

- AC/DC NB Adapters
- Open−Frame SMPS

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APPLICATION DIAGRAM

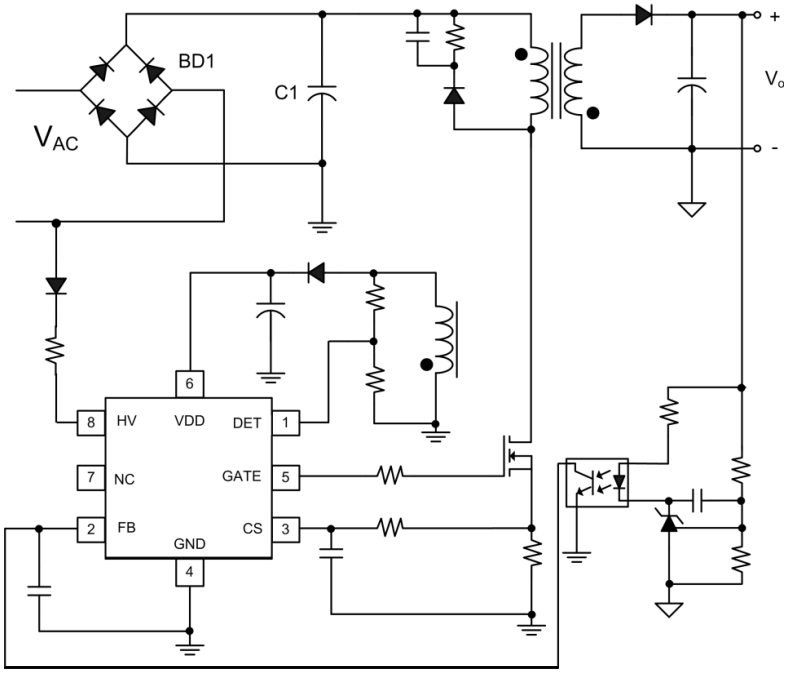


Figure 1. Typical Application

INTERNAL BLOCK DIAGRAM

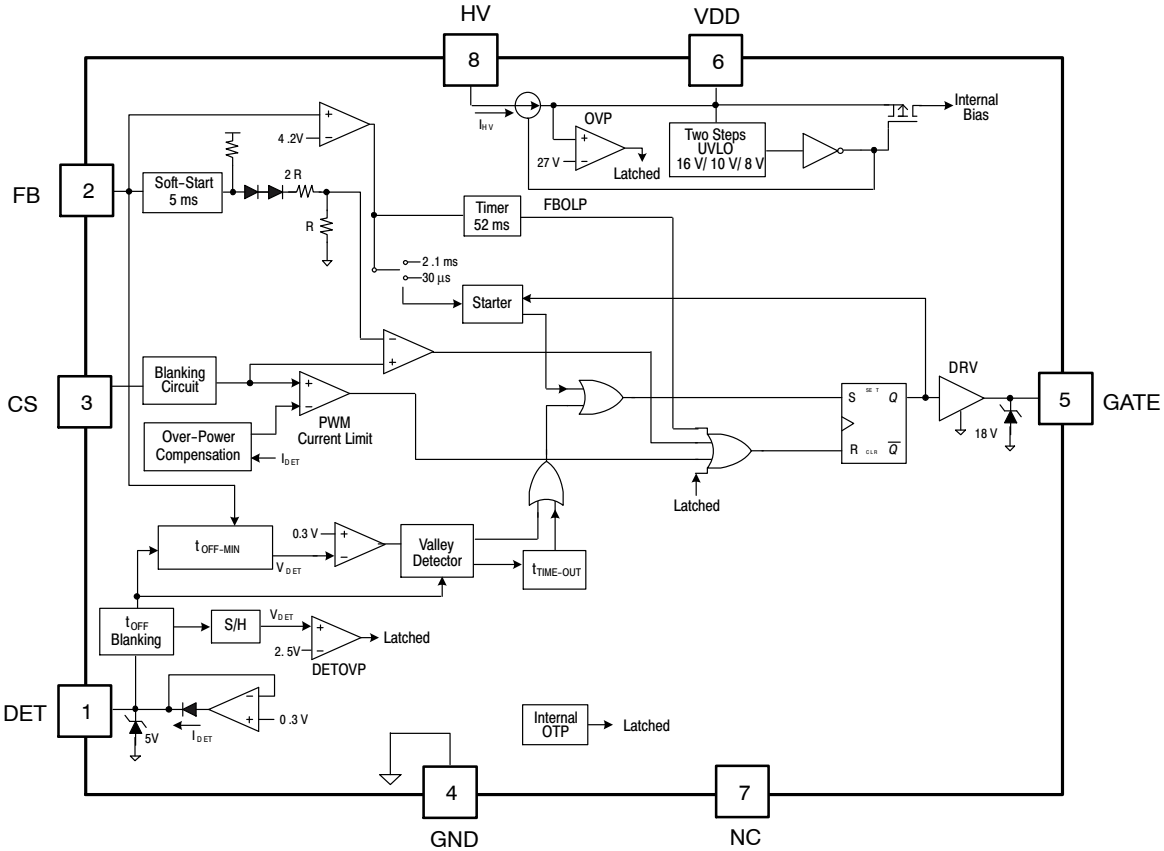


Figure 2. Functional Block Diagram

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PIN CONFIGURATION

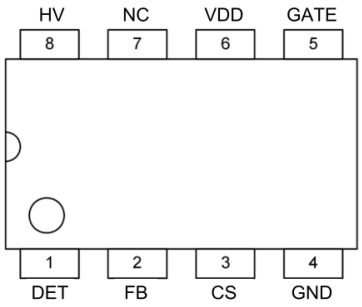


Figure 3. Pin Configuration

PIN DEFINITIONS

Pin #	Pin Name	Description
1	DET	This pin is connected to an auxiliary winding of the transformer via resistors of the divider for the following purposes: – Generates a ZCD signal once the secondary–side switching current falls to zero. – Produces an offset voltage to compensate the threshold voltage of the peak current limit to provide a constant power limit. The offset is generated in accordance with the input voltage when PWM signal is enabled. – Detects the valley voltage of the switching waveform to achieve the valley voltage switching and minimize the switching losses. A voltage comparator and a 2.5 V reference voltage develop a output OVP protection. The ratio of the divider decides what output voltage to stop gate, as an optical coupler and secondary shunt regulator are used.
2	FB	The feedback pin should to be connected to the output of the error amplifier for achieving the voltage control loop. The FB should be connected to the output of the optical coupler if the error–amplifier is equipped at the secondary–side of the power converter. The input impedance of this pin is a 5 kΩ equivalent resistance. A 1/3 attenuator connected between the FB and the PWM circuit is used for the loop–gain attenuation. FAN6300A/H performs an open–loop protection once the FB voltage is higher than a threshold voltage (around 4.2 V) more than 55 ms.
3	CS	Input to the comparator of the over–current protection. A resistor senses the switching current and the resulting voltage is applied to this pin for the cycle–by–cycle current limit.
4	GND	The power ground and signal ground. A 0.1 μF decoupling capacitor placed between VDD and GND is recommended.
5	GATE	Totem–pole output generates the PWM signal to drive the external power MOSFET. The clamped gate output voltage is 18 V.
6	VDD	Power Supply. The threshold voltages for startup and turn–off are 16 V and 10 V, respectively. The startup current is less than 20 μA and the operating current is lower than 4.5 mA.
7	NC	No connect
8	HV	High–voltage startup

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	DC Supply Voltage		30	V
V_{HV}	Maximum Voltage on HV Pin		500	V
V_H	Maximum Voltage on GATE Pin	−0.3	25.0	V
V_L	V_{FB}, V_{CS}, V_{DET} (Maximum Voltage on Low Power Pins)	−0.3	7.0	V
P_D	Power Dissipation		400	mW
T_J	Operating Junction Temperature		150	°C
T_{STG}	Storage Temperature Range	−55	150	°C
T_L	Lead Temperature (Soldering 10 seconds)		270	°C
ESD	Human Body Model, JEDEC:JESD22−A114		3.0	kV
	Charged Device Model, JEDEC:JESD22−C101		1.5	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltage values, except differential voltages, are given with respect to GND pin.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
T_A	Operating Ambient Temperature	−40	105	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{DD} = 10 ~ 25 V, T_A = −40 ~ +105°C (T_J = T_A))

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD} SECTION						
V_{OP}	Continuously Operating Voltage				25	V
V_{DD-ON}	Turn−On Threshold Voltage		15	16	17	V
$V_{DD-PWM-OFF}$	PWM Off Threshold Voltage		9	10	11	V
V_{DD-OFF}	Turn−Off Threshold Voltage		7	8	9	V
I_{DD-ST}	Startup Current	V_{DD} = V_{DD-ON} − 0.16 V, GATE Open		10	20	μA
I_{DD-OP}	Operating Current	V_{DD} = 15 V, f_S = 60 kHz, C_L = 2 nF		4.5	5.5	mA
$I_{DD-GREEN}$	Green−Mode Operating Supply Current (Average)	V_{DD} = 15 V, f_S = 2 kHz, C_L = 2 nF			3.5	mA
$I_{DD-PWM-OFF}$	Operating Current at PWM−Off Phase	V_{DD} = $V_{DD-PWM-OFF}$ − 0.5 V	70	80	90	μA
V_{DD-OVP}	V_{DD} Over−Voltage−Protection (Latch−Off)		26	27	28	V
$t_{VDD-OVP}$	V_{DD} OVP Debounce Time		100	150	200	μs
$I_{DD-LATCH}$	V_{DD} OVP Latch−Up Holding Current	V_{DD} = 5 V		42		μA
HV STARTUP CURRENT SOURCE SECTION						
V_{HV-MIN}	Minimum Startup Voltage on Pin HV				50	V
I_{HV}	Supply Current Drawn from Pin HV	V_{AC} = 90 V (V_{DC} = 120 V), V_{DD} = 0 V	1.5		4.0	mA
I_{HV-LC}	Leakage Current after Startup	V_{HV} = 500 V, V_{DD} = V_{DD-OFF} + 1 V		1	20	μA
FEEDBACK INPUT SECTION						
A_V	Internal Voltage to Current Sense Attenuation	A_V = $\Delta V_{CS}/\Delta V_{FB}$, 0 < V_{CS} < 0.9	1/2.75	1/3.00	1/3.25	V/V
Z_{FB}	Input Impedance		3	5	7	kΩ
I_{OZ}	Bias Current	FB = V_{OZ}		1.2	2	mA
V_{OZ}	Zero Duty−Cycle Input Voltage		0.8	1.0	1.2	V
V_{FB-OLP}	Open Loop Protection Threshold Voltage		3.9	4.2	4.5	V
t_{D-OLP}	Debounce Time for Open Loop/Overload Protection		46	52	62	ms
t_{SS}	Internal Soft−Start Time			5		ms
DET PIN OVP AND VALLEY DETECTION SECTION						
$V_{DET-OVP}$	Comparator Reference Voltage		2.45	2.50	2.55	V
A_V	Open−Loop Gain (Note 3)			60		dB
B_W	Gain Bandwidth (Note 3)			1		MHz
V_{V-HIGH}	Output High Voltage		4.5			V
V_{V-LOW}	Output Low Voltage				0.5	V
$t_{DET-OVP}$	Output OVP (Latched) Debounce Time		100	150	200	μs
$I_{DET-SOURCE}$	Maximum Source Current	V_{DET} = 0 V			1	mA
$V_{DET-HIGH}$	Upper Clamp Voltage	I_{DET} = −1 mA			5	V
$V_{DET-LOW}$	Lower Clamp Voltage	I_{DET} = 1 mA	0.1	0.3		V
$t_{VALLEY-DELAY}$	Delay Time from Valley−Signal Detected to Output Turn−On (Note 3)			200		ns
$t_{OFF-BNK}$	Leading−Edge−Blanking Time for DET when PWM MOS Turns Off (Note 3)	FAN6300A		4.0		μs
		FAN6300H		1.5		
$t_{TIME-OUT}$	Time−Out after $t_{OFF-MIN}$	FAN6300A		9		μs
		FAN6300H		5		

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ELECTRICAL CHARACTERISTICS (continued)
(Unless otherwise specified, V_{DD} = 10 ~ 25 V, T_A = −40 ~ +105°C (T_J = T_A)) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OSCILLATOR SECTION						
t_{ON-MAX}	Maximum On−Time		38	45	54	μs
$t_{OFF-MIN}$	Minimum Off−Time	$V_{FB} \geq V_N$, FAN6300A		8		μs
		$V_{FB} \geq V_N$, FAN6300H		3		μs
		$V_{FB} = V_G$, FAN6300A		38		μs
		$V_{FB} = V_G$, FAN6300H		13		μs
V_N	Beginning of Green Mode at FB Voltage Level		1.95	2.10	2.25	V
V_G	Beginning of Green Mode at FB Voltage Level		1.0	1.2	1.4	V
ΔV_{FBG}	Green Mode V_{FB} Hysteresis Voltage		0.05	0.10	0.20	V
$t_{STARTER}$	Start Timer (Time−Out Timer)	$V_{FB} < V_G$	1.8	2.1	2.4	ms
		$V_{FB} > V_{FB-OLP}$	25	30	45	μs
OUTPUT SECTION						
V_{OL}	Output Voltage Low	V_{DD} = 15 V, I_O = 150 mA			1.5	V
V_{OH}	Output Voltage High	V_{DD} = 12 V, I_O = 150 mA	7.5			V
t_r	Rising Time			145	200	ns
t_f	Falling Time			55	120	ns
V_{CLAMP}	Gate Output Clamping Voltage		16.7	18.0	19.3	V
CURRENT SENSE SECTION						
t_{PD}	Delay to Output		20	150	200	ns
V_{LIMIT}	Limit Voltage on CS Pin for Over−Power Compensation	I_{DET} < 74.41 μA	0.82	0.85	0.88	V
		I_{DET} = 550 μA	0.380	0.415	0.450	V
V_{SLOPE}	Slope Compensation (Note 3)	t_{ON} = 45 μs		0.3		V
		t_{ON} = 0 μs		0.1		V
t_{BNK}	Leading−Edge Blanking Time (MOS Turns ON)		525	625	725	ns
V_{CS-H}	V_{CS} Clamped High Voltage once CS Pin Floating	CS Pin Floating	4.5		5.0	V
t_{CS-H}	Delay Time once CS Pin Floating	CS Pin Floating		150		μs
INTERNAL OVER−TEMPERATURE PROTECTION SECTION						
T_{OTP}	Internal Threshold Temperature for OTP (Note 3)			125		°C
$T_{OTP-HYST}$	Hysteresis Temperature for Internal OTP (Note 3)			5		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Guaranteed by design.

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TYPICAL PERFORMANCE CHARACTERISTICS

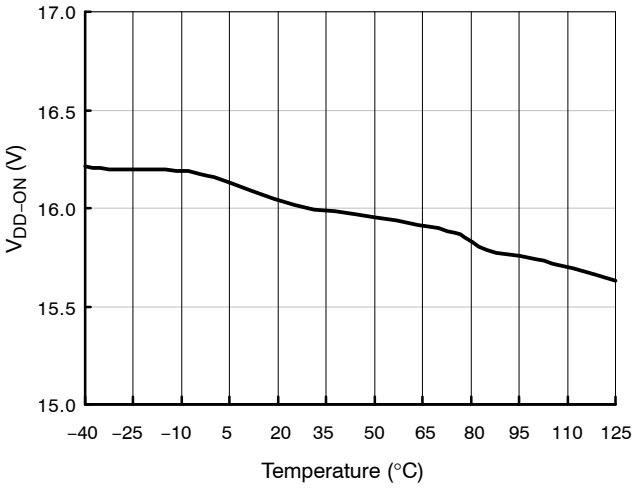


Figure 6. Turn−Off Threshold Voltage

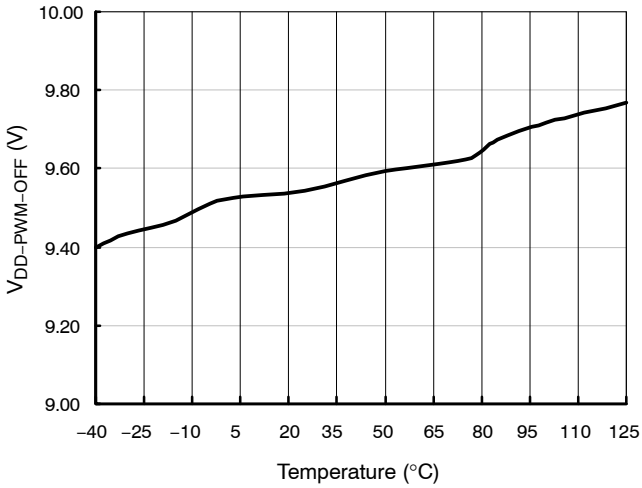


Figure 7. Startup Current

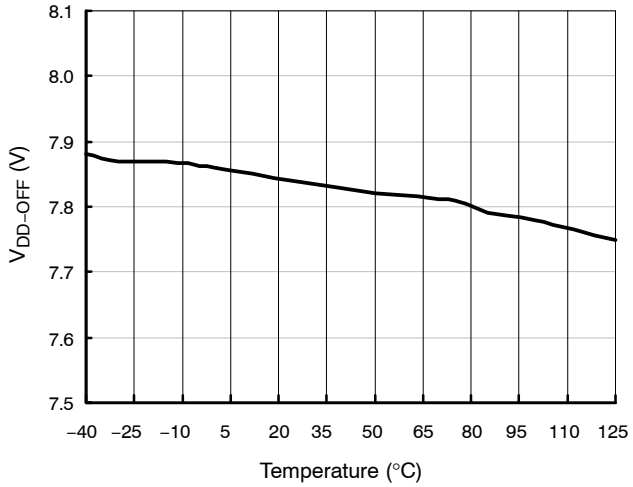


Figure 4. Turn−On Threshold Voltage

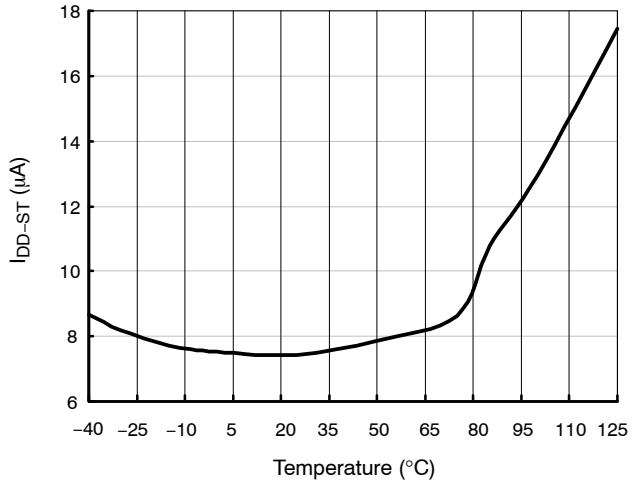


Figure 5. PWM−Off Threshold Voltage

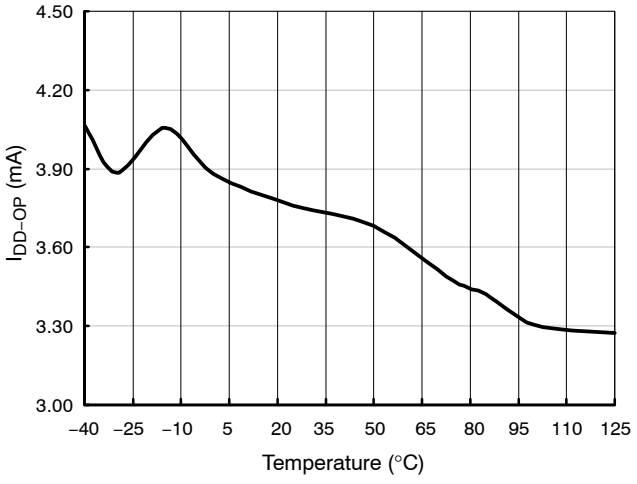


Figure 8. Operating Current

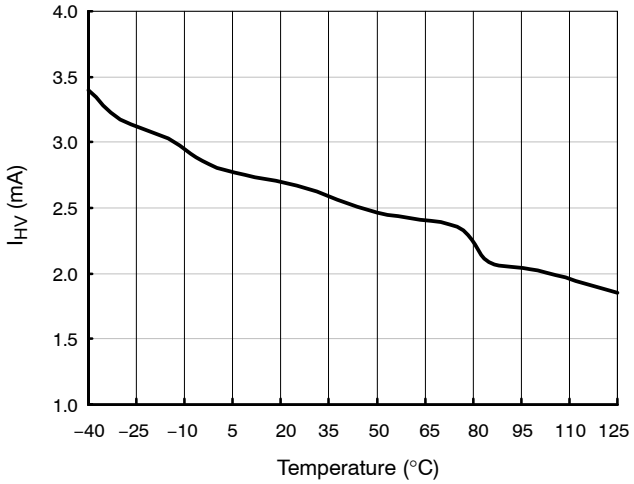


Figure 9. Supply Current Drawn from HV Pin

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

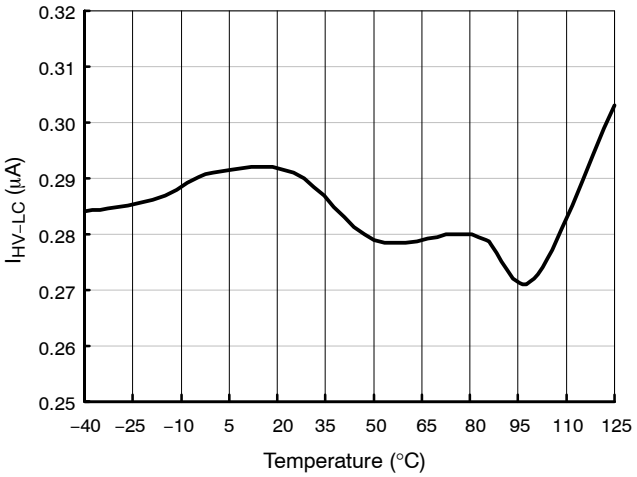


Figure 10. Leakage Current after Startup

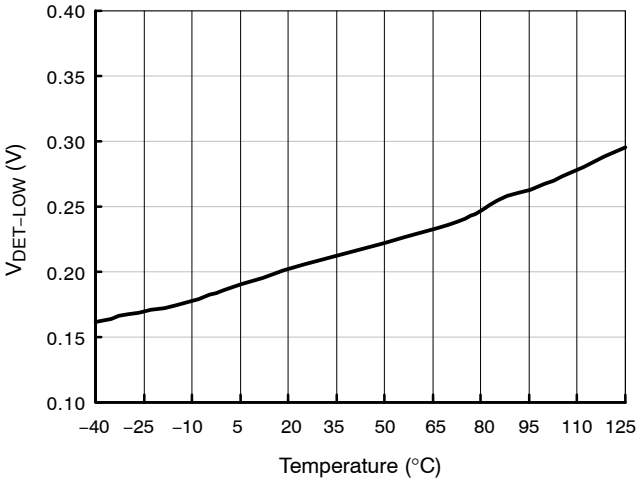


Figure 11. Lower Clamp Voltage

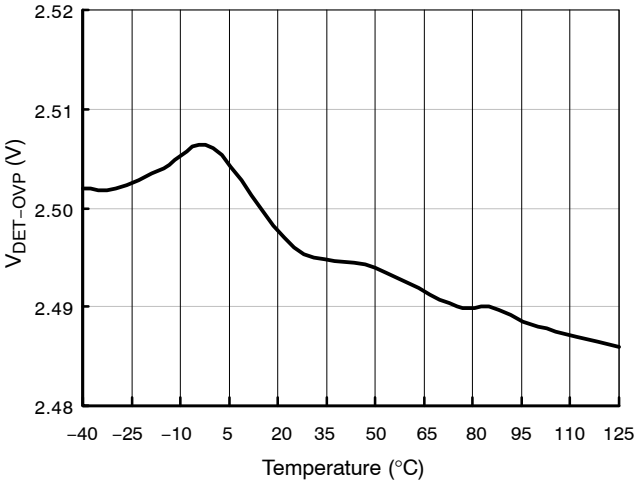


Figure 12. Comparator Reference Voltage

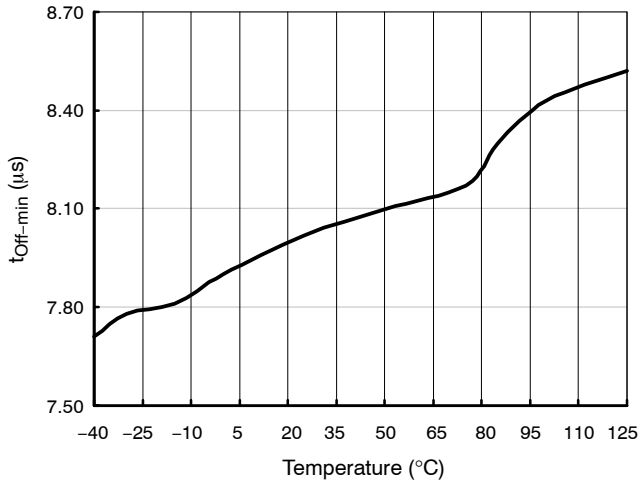


Figure 13. Minimum Off Time (V_{FB} > V_N)

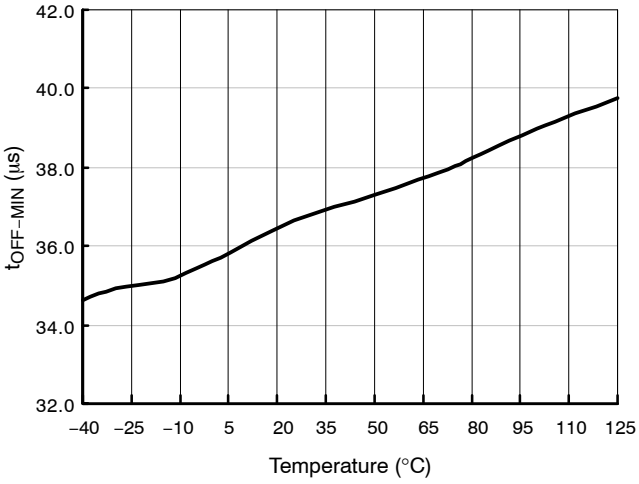


Figure 14. Minimum Off Time (V_{FB} = V_G)

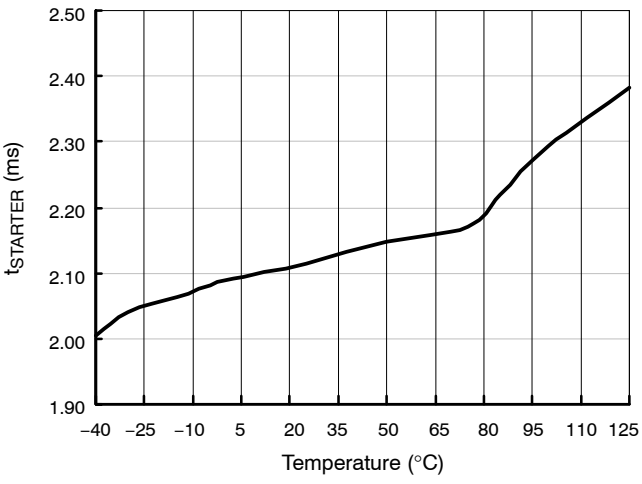


Figure 15. Start Timer (V_{FB} < V_G)

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OPERATION DESCRIPTION

The FAN6300A/H PWM controller integrates designs to enhance the performance of flyback converters. An internal valley voltage detector ensures power system operates at Quasi−Resonant (QR) operation across a wide range of line voltage. The following descriptions highlight some of the features of the FAN6300A/H.

Startup Current

For startup, the HV pin is connected to the line input or bulk capacitor through an external diode and resistor, R_{HV}, which are recommended as 1N4007 and 100 kΩ. Typical startup current drawn from the HV pin is 1.2 mA and it charges the hold−up capacitor through the diode and resistor. When the V_{DD} voltage level reaches V_{DD-ON}, the startup current switches off. At this moment, the V_{DD} capacitor only supplies the FAN6300A/H to maintain V_{DD} until the auxiliary winding of the main transformer provides the operating current.

Valley Detection

The DET pin is connected to an auxiliary winding of the transformer via resistors of the divider to generate a valley signal once the secondary−side switching current discharges to zero. It detects the valley voltage of the switching waveform to achieve the valley voltage switching. This ensures QR operation, minimizes switching losses, and reduces EMI. Figure 16 shows divider resistors R_{DET} and R_A. When V_{AUX} (in Figure 16) is negative, the DET pin voltage is clamped to $V_{DET-LOW}$ (0.3 V) by the sourcing current $I_{DET-SOURCE}$. The valley of the drain voltage of the main power switch is detected when the sourcing current exceeds 30 μA during off time of the GATE signal. Reducing R_{DET} makes the valley easier to be detected.

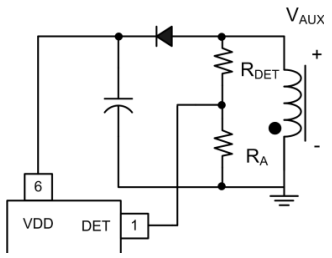


Figure 16. Valley Detect Section

The internal timer (minimum t_{OFF} time) prevents gate retriggering within 8 μs (3 μs for H version) after the gate signal going−low transition. The minimum t_{OFF} limit prevents system frequency being too high. Figure 17 shows a typical drain voltage waveform with first valley switching.

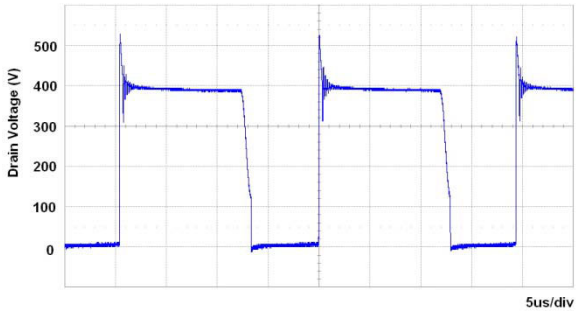


Figure 17. First Valley Switching

Green−Mode Operation

The proprietary green−mode function provides off−time modulation to linearly decrease the switching frequency under light−load conditions. V_{FB}, which is derived from the voltage feedback loop, is taken as the reference. In Figure 18, once V_{FB} is lower than V_N, $t_{OFF-MIN}$ increases linearly with lower VFB. The valley voltage detection signal does not start until $t_{OFF-MIN}$ finishes. Therefore, the valley detect circuit is activated after $t_{OFF-MIN}$ finishes, which decreases the switching frequency and provides extended valley voltage switching. However, in very light load condition, it might fail to detect the valley voltage due to too low of $I_{DET-SOURCE}$ after the $t_{OFF-MIN}$. Under this condition, an internal $t_{TIME-OUT}$ signal initiates a new cycle start after a 9 μs delay (with 5 μs delay for H version). Figure 19 and Figure 20 show the two different conditions.

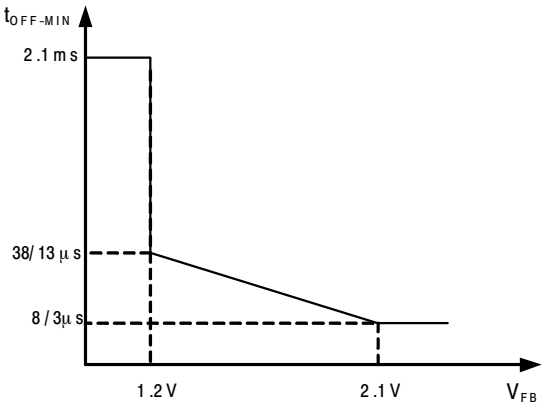


Figure 18. V_{FB} vs. $t_{OFF-MIN}$ Curve

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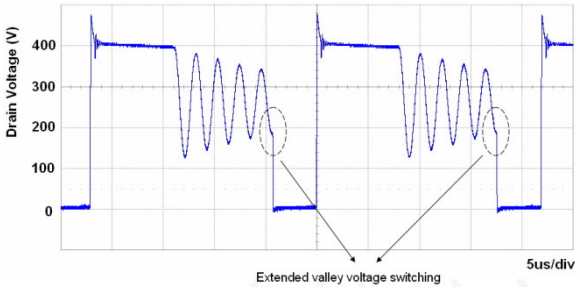


Figure 19. Operation in Extended Valley Voltage Detection Mode

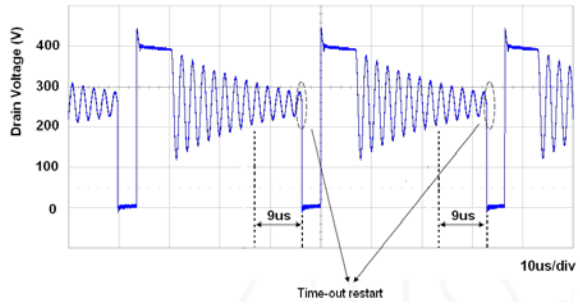


Figure 20. Internal $t_{TIME-OUT}$ Initiates New Cycle after Failure to Detect Valley Voltage (with 5 μs Delay for FAN6300H version)

Peak−Current−Mode PWM

Peak−current−mode control is utilized to regulate output voltage and provide pulse−by−pulse current limiting. The switch current is detected by a sense resistor into the CS pin. The PWM duty cycle is determined by this current sense signal and V_{FB}. When the voltage on CS reaches around (V_{FB}−1.2)/3, the PWM signal is turned off immediately.

Leading−Edge Blanking (LEB)

Each time the power MOFFET switches on, a turn−on spike occurs on the sense resistor. To avoid premature termination of the switching pulse, lead−edge blanking time is built in. During the blanking period, the current limit comparator is disabled; it cannot switch off the gate driver.

Under−Voltage Lockout (UVLO)

The turn−on, PWM−off, and turn−off thresholds are fixed internally at 16/10/8 V. During startup, the startup capacitor must be charged to 16 V through the startup resistor to enable the IC. The hold−up capacitor continues to supply V_{DD} until energy can be delivered from the auxiliary winding of the main transformer. V_{DD} must not drop below 10 V during this startup process. This UVLO hysteresis window ensures that hold−up capacitor is adequate to supply V_{DD} during startup.

Gate Output

The BiCMOS output stage is a fast totem−pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 18 V Zener diode to protect power MOSFET transistors against undesired over−voltage gate signals.

Over−Power Compensation

When CS pin signal hits a V_{LIMIT} threshold, GATE signal is terminated to limit the input power. To compensate the variation of over−power limit over wide AC input range, the current limit V_{LIMIT} is adjusted according to $I_{DET-SROUCE}$ during on time of the GATE signal. During the GATE−on time, the amplitude of V_{AUX} is proportional to V_{IN}. $I_{DET-SROUCE}$ is dominated by V_{AUX}/R_{DET} at this duration. V_{LIMIT} decreases linearly when $I_{DET-SROUCE}$ is higher than 74.41 μA. This results in a lower current limit at high−line input. Adjusting R_{DET} affects the variation of V_{LIMIT} across the input voltage range.

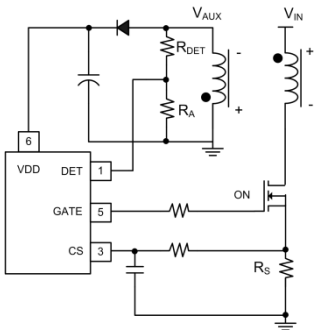


Figure 21. H/L Line Constant Power Limit Compensated by DET Pin

V_{DD} Over−Voltage Protection

V_{DD} over−voltage protection prevents damage due to abnormal conditions. Once the V_{DD} voltage is over the V_{DD} over−voltage protection voltage (V_{DD-OVP}) and lasts for $t_{VDD-OVP}$, the PWM pulse is disabled and the controller latches off.

Output Over−Voltage Protection

The output over−voltage protection works by the sampling voltage, as shown in Figure 22, after switch−off sequence. A 4 μs (1.5 μs for H version) blanking time ignores the leakage inductance ringing. A voltage comparator and a 2.5 V reference voltage develop an output OVP protection. The ratio of the divider determines the sampled voltage, as an optical coupler and secondary shunt

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regulator are used. If the DET pin OVP is triggered, the power system enters latch−mode until AC power is removed.

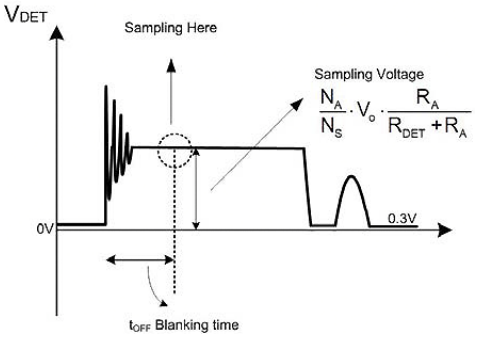


Figure 22. Voltage Sampled after 4 μs (1.5 μs for FAN6300H version) Blanking Time after Switch−Off Sequence

Short−Circuit and Open−Loop Protection

The FB voltage increases every time the output of the power supply is shorted or overloaded. If the FB voltage remains higher than a built−in threshold for longer than t_{D-OLP}, PWM output is turned off. As PWM output is turned off, the supply voltage V_{DD} begins decreasing.

When V_{DD} goes below 8 V, the controller is totally shut down. V_{DD} is charged up to the turn−on threshold voltage of 16 V through the startup resistor. This protection feature continues as long as the overloading condition persists. This prevents the power supply from overheating due to overloading.

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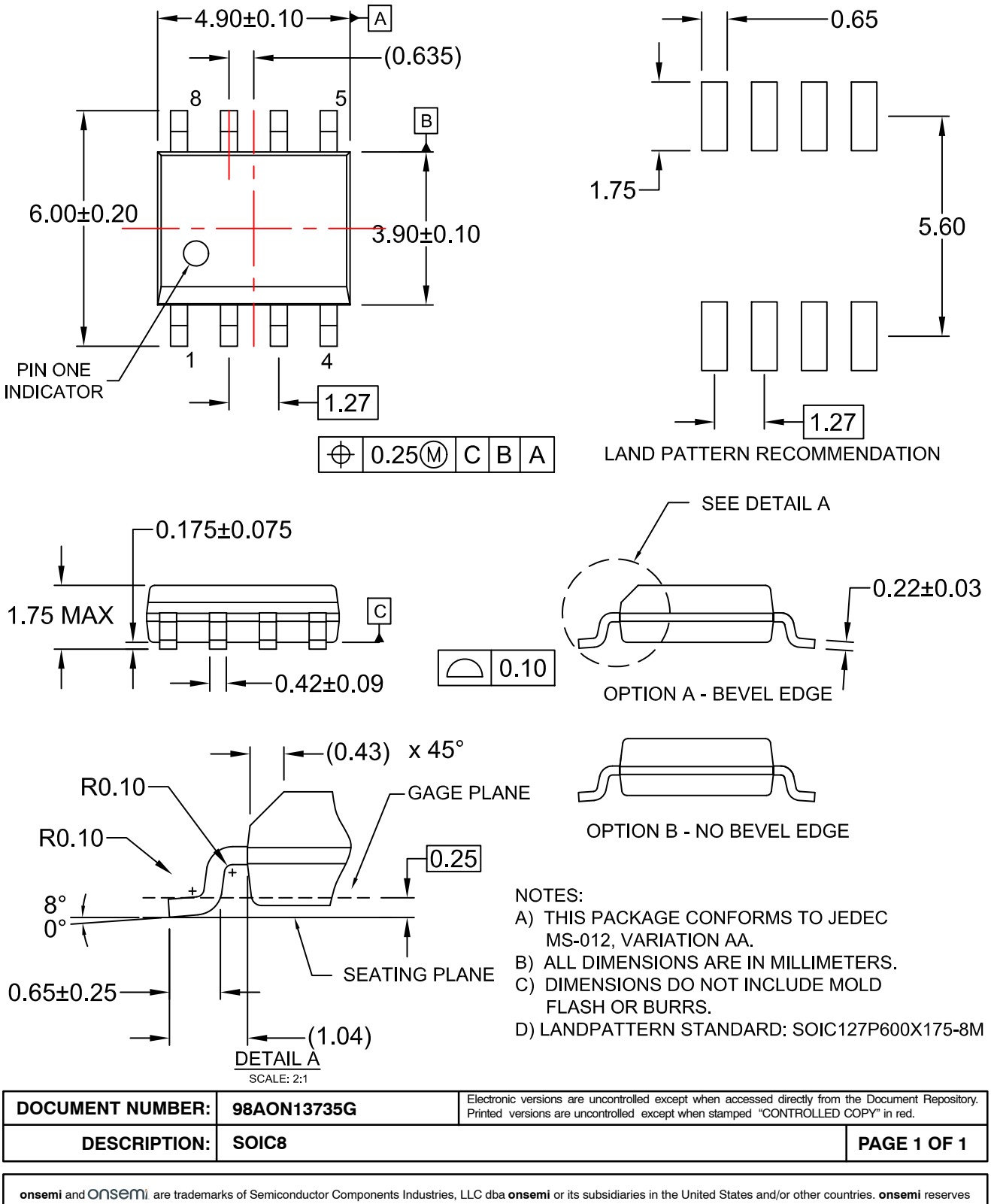
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