# Offline Quasi-Resonant PWM Controller

# FAN6080HMX

The FAN6080HMX is an advanced PWM controller aimed at achieving power density of ≥10 W/in$^3$ in universal input range AC/DC flyback isolated power supplies. It incorporates Quasi−Resonant (QR) control with proprietary valley switching. QR switching provides high efficiency by reducing switching losses.

FAN6080HMX features MWSAVER® burst mode operation with extremely low operating current (300 μA) and significantly reduces standby power consumption to meet the most stringent efficiency regulations such as Energy Star's 5−Star Level and CoC Tier II specifications.

FAN6080HMX includes several features aimed at optimizing efficiency, EMI and protections. FAN6080HMX has a wide blanking frequency range that improves light load efficiency. The maximum operating frequency is optimized to minimize components temperature while maximizing the full load efficiency. The minimum peak current is also set to optimize to balance the standby power consumption and the audio noise. It also includes several rich programmable protection features such as over−voltage protection (OVP) and precise constant output current regulation (CC).

FAN6080HMX is available in SOIC8 package.

### Features

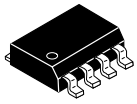
- High Efficiency Across Wide Input and Output Conditions in a Small Form Factor
- Quasi−Resonant Switching Operation with Wide Blanking Frequency Range (24 kHz~125 kHz)
- Optimization Transformer Design for Adaptive Charger Application
- Precise Constant Output Current Regulation with Programmable Line Compensation
- MWSAVER Technology for Ultra Low Standby Power Consumption (<20 mW)
- Forced and Inherent Frequency Modulation of Valley Switching for Low EMI Emissions and Common Mode Noise
- Built−In and User Configurable Over−Voltage Protection (OVP) and Under−Voltage Protection (UVP)
- Built−In Over−Temperature Protection (OTP)
- Fully Programmable Brown−In and Brownout Protection
- Built−In High−Voltage Startup to Reduce External Components

### Typical Applications

- Battery Charges for Smart Phones, Feature Phones, and Tablet PCs
- AC−DC Adapters for Portable Devices or Battery Chargers that Require CV/CC Control

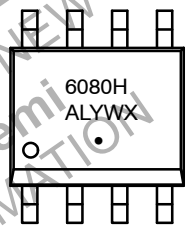
**ON Semiconductor®**

www.onsemi.com



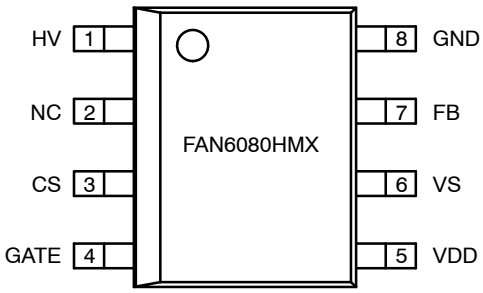
**SOIC8**
**CASE 751EB**

### MARKING DIAGRAM




6080H = Specific Device Code
A = Assembly Location
L = Wafer Lot Traceability
YW = Date Code
X = Manufacture Flow
• = Pb Free

### PIN ASSIGNMENT




(Top View)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

DISCONTINUED
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR onsemi REPRESENTATIVE FOR INFORMATION

© Semiconductor Components Industries, LLC, 2020

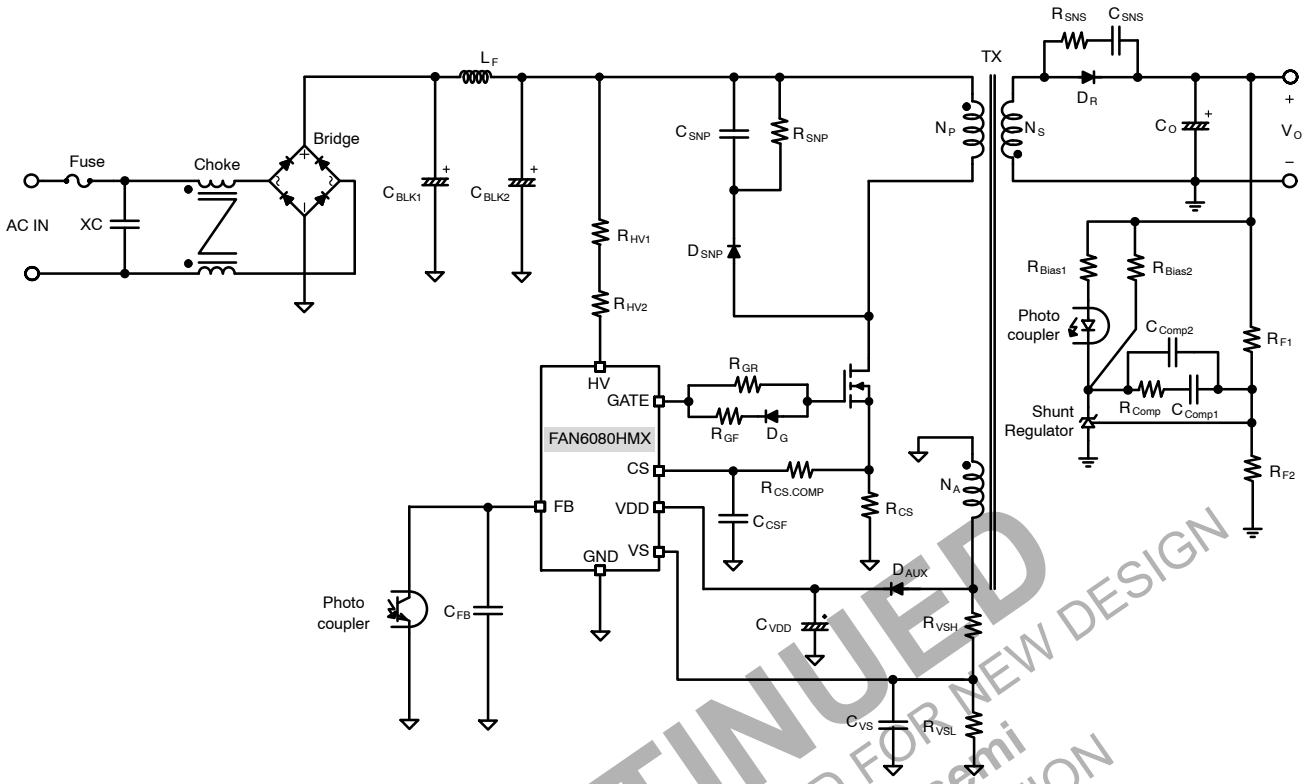



**Figure 1. FAN6080HMX Typical Application**

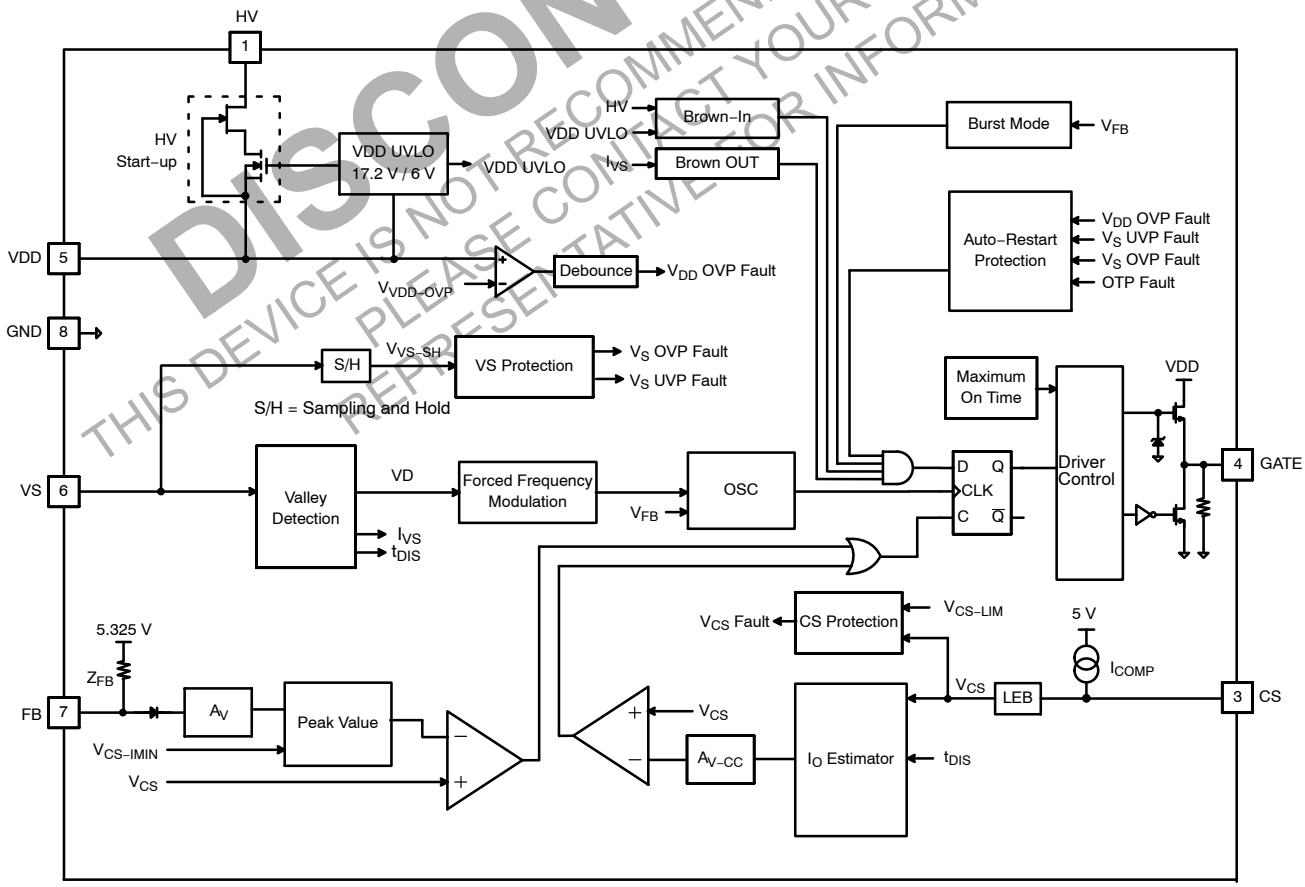



**Figure 2. FAN6080HMX Block Diagram**

DISCONTINUED
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR onsemi
REPRESENTATIVE FOR INFORMATION

## PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | HV | High Voltage. This pin connects to DC bus for high−voltage startup. |
| 2 | NC | No Connect. |
| 3 | CS | Current Sense. This pin connects to a current−sense resistor to sense the MOSFET current for Peak−Current−Mode control for output regulation. The current sense information is also used to estimate the output current for CC regulation. |
| 4 | GATE | PWM Signal Output. This pin has an internal totem−pole output driver to drive the power MOSFET. The gate driving voltage is internally clamped at 8 V. |
| 5 | VDD | Power Supply. IC operating current and MOSFET driving current are supplied through this pin. This pin is typically connected to an external VDD capacitor. |
| 6 | VS | Voltage Sense. The VS voltage is used to detect resonant valleys for quasi−resonant switching. This pin detects the output voltage information and diode current discharge time based on the auxiliary winding voltage. It also senses input voltage for Brown−out protection. |
| 7 | FB | Feedback. Typically Opto−Coupler is connected to this pin to provide feedback information to the internal PWM comparator. This feedback is used to control the duty cycle in CV regulation. |
| 8 | GND | Ground. |

## MAXIMUM RATINGS

| Symbol | Rating | Value | Unit |
|---|---|---|---|
| $V_{HV}$ | Maximum Voltage on HV Pin | 600 | V |
| $V_{VDD}$ | DC Supply Voltage | 60 | V |
| $V_{GATE}$ | Maximum Voltage on GATE Pin | −0.3 to 30 | V |
| $V_{FB}$ | Maximum Voltage on FB Pin | −0.3 to 6.5 | V |
| $V_{max}$ | Maximum Voltage on Low Power Pins (Except Pin 1, Pin 4, Pin 5, Pin 7) | −0.3 to 6 | V |
| $P_D$ | Power Dissipation (TA = 25°C) | 770 | mW |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) | 162 | °C/W |
| $\Psi_{JT}$ | Thermal Resistance (Junction−to−Top) | 20 | °C/W |
| $T_J$ | Operating Junction Temperature | −40 to +150 | °C |
| $T_{STG}$ | Storage Temperature Range | −40 to +150 | °C |
| ESD | Human Body Model, JEDEC:JESD22_A114 | 2.0 | kV |
| | Charged Device Model, JEDEC:JESD22_C101 | 0.5 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All voltage values, except differential voltages, are given with respect to GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

## RECOMMENDED OPERATING RANGES

| Symbol | Rating | Min | Max | Unit |
|---|---|---|---|---|
| $V_{HV}$ | HV Pin Supply Voltage | 50 | 500 | V |
| $V_{VDD}$ | VDD Pin Supply Voltage | 7 | 50 | V |
| $V_{VS}$ | VS Pin Supply Voltage | 0.7 | 2.9 | V |
| $V_{CS}$ | CS Pin Supply Voltage | 0 | 0.85 | V |
| $V_{FB}$ | FB Pin Supply Voltage | 0 | 4.55 | V |
| $T_A$ | Operating Temperature | −40 | +85 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DISCONTINUED
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR onsemi REPRESENTATIVE FOR INFORMATION

## ELECTRICAL CHARACTERISTICS

(For typical values $T_J$ = 25°C, for min/max values $T_J$ = −40°C to 125°C, $V_{DD}$ = 15 V; unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **HV SECTION** | | | | | | |
| $I_{HV}$ | Supply Current Drawn from HV Pin | $V_{HV}$ = 120 V, $V_{DD}$ = 0 V | 1.2 | 2.0 | 10 | mA |
| $I_{HV-LC}$ | Leakage Current Drawn from HV Pin | $V_{HV}$ = 600 V, $V_{DD}$ = $V_{DD-OFF}$ + 1 V | 0 | 0.8 | 10 | μA |
| $V_{Brown-IN}$ | Brown−In Threshold Voltage | $R_{HV}$ = 360 kΩ | 75 | 92 | 115 | V |
| **$V_{DD}$ SECTION** | | | | | | |
| $V_{DD-ON}$ | Turn−On Threshold Voltage | $V_{DD}$ Rising | 15.3 | 17.2 | 18.7 | V |
| $V_{DD-OFF}$ | Turn−Off Threshold Voltage | $V_{DD}$ Falling | 5.5 | 6 | 6.5 | V |
| $V_{DD-VS-DET}$ | Output Short Detection Threshold (Note 3) | | 6.0 | 6.5 | 7.0 | V |
| $I_{DD-ST}$ | Startup Current | $V_{DD}$ = $V_{DD-ON}$ − 0.16 V | − | − | 60 | μA |
| $I_{DD-OP}$ | Operating Supply Current | $V_{CS}$ = 5.0 V, $V_{VS}$ = 3 V, $V_{FB}$ = 3 V, $V_{DD}$ = 15 V, $C_{GATE}$ = 1 nF | − | 2 | 3 | mA |
| $I_{DD-Burst}$ | Burst−Mode Operating Supply Current | $V_{CS}$ = 0.3 V, $V_{VS}$ = 0 V, $V_{FB}$ = 0 V; $V_{DD}$ = $V_{DD-ON}$ → $V_{DD-OVP}$ → 10 V, $C_{GATE}$ = 1 nF | − | 300 | 600 | μA |
| $t_{IDD-Burst}$ | $I_{DD-Burst}$ Operation Enable Debounce Time | $V_{FB}$ < $V_{FB-Burst-L}$ | − | 100 | − | μs |
| $V_{VDD-OVP}$ | $V_{DD}$ Over−Voltage−Protection Level | | 56.2 | 57.2 | 58.2 | V |
| $t_{D-VDDOVP}$ | $V_{DD}$ Over−Voltage−Protection Debounce Time | | − | 70 | 150 | μs |
| **OSCILLATOR SECTION** | | | | | | |
| $f_{BNK-MAX}$ | Maximum Blanking Frequency | $V_{FB}$ > $V_{FB-BNK-HL-H}$, $V_{FB-BNK-LL-H}$ | 115 | 125 | 135 | kHz |
| $f_{BNK-MIN}$ | Minimum Blanking Frequency | $V_{FB}$ < $V_{FB-BNK-HL-L}$, $V_{FB-BNK-LL-L}$ | 21 | 24 | 27 | kHz |
| $f_{OSC-MIN-DCM}$ | Minimum Frequency for DCM | $V_{VS}$ = 0 V | 19 | 21.5 | 24 | kHz |
| $f_{OSC-MIN-CRM}$ | Minimum Frequency for CRM | $V_{VS}$ = 1 V | 19 | 21.5 | 24 | kHz |
| $F_{MAX-HL}$ | Maximum Blanking Frequency Limit for High Line | | 90 | 100 | 110 | kHz |
| $\Delta t_{FM-Range}$ | Forced Frequency Modulation Range | $V_{FB}$ > $V_{FB-Burst-H}$ | 215 | 270 | 325 | ns |
| $\Delta t_{FM-Period}$ | Forced Frequency Modulation Period (Note 3) | $V_{FB}$ > $V_{FB-Burst-H}$ | 2.1 | 2.5 | 2.9 | ms |
| **FEEDBACK INPUT SECTION** | | | | | | |
| $Z_{FB}$ | FB Pin Input Impedance | | 37.0 | 40.5 | 43.5 | kΩ |
| $A_V$ | Internal Voltage Attenuator of FB Pin (Note 3) | $V_{HV}$ = 120 V, $V_{DD}$ = 0 V | 1/3 | 1/3.5 | 1/4 | V/V |
| $V_{FB-Open}$ | FB Pin Pull−Up Voltage | FB Pin Open | 4.55 | 5.325 | 6.10 | V |
| $V_{FB-BNK-HL-H}$ | Modulated Blanking Frequency Upper/Lower $V_{FB}$ Limit for High Line | | 2.30 | 2.40 | 2.50 | V |
| $V_{FB-BNK-HL-L}$ | | | 1.90 | 2.00 | 2.10 | V |
| $V_{FB-BNK-LL-H}$ | Modulated Blanking Frequency Upper/Lower $V_{FB}$ Limit for Low Line | | 1.90 | 2.00 | 2.10 | V |
| $V_{FB-BNK-LL-L}$ | | | 1.50 | 1.60 | 1.70 | V |
| $V_{FB-Burst-H}$ | FB Threshold to Enable/Disable Gate Drive in Burst Mode | $V_{FB}$ Rising | 0.90 | 1.05 | 1.20 | V |
| $V_{FB-Burst-L}$ | | $V_{FB}$ Falling | 0.85 | 1.00 | 1.15 | V |
| **VOLTAGE−SENSE SECTION** | | | | | | |
| $I_{VS-MAX}$ | Maximum VS Source Current Capability | | − | − | 3 | mA |
| $t_{VS-BNK1}$ | VS Sampling Blanking Time 1 after GATE Pin Pull−Low | $V_{FB}$ < 2.0 V | 0.84 | 1.0 | 1.23 | μs |
| $t_{VS-BNK2}$ | VS Sampling Blanking Time 2 after GATE Pin Pull−Low | $V_{FB}$ > 2.2 V | 1.45 | 1.80 | 2.15 | μs |
| $V_{S-Clamp}$ | VS Clamping Voltage (Note 3) | | − | 0 | − | V |
| $t_{ZCD-to-PWM}$ | Delay from VS Voltage Zero Crossing to PWM ON (Note 3) | $V_{VS}$ = 0 V, $C_{GATE}$ = 1 nF | 100 | 175 | 250 | ns |
| $I_{VS-HL}$ | VS Source Current Threshold to Enable $V_{FB-BNK-HL-H/L}$ from Low to High Line | | 1.290 | 1.440 | 1.590 | mA |

DISCONTINUED
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR onsemi
REPRESENTATIVE FOR INFORMATION

## ELECTRICAL CHARACTERISTICS

(For typical values $T_J$ = 25°C, for min/max values $T_J$ = −40°C to 125°C, $V_{DD}$ = 15 V; unless otherwise noted) (continued)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VOLTAGE−SENSE SECTION** | | | | | | |
| $I_{VS-LH}$ | VS Source Current Threshold to Enable $V_{FB-BNK-LL-H/L}$ from High to Low Line | | 1.208 | 1.350 | 1.492 | mA |
| $t_{D-VS-LD}$ | Line Detection Debounce Time for $I_{VS-LH}$ | | 11 | 17 | 23 | ms |
| $I_{VS-Brown-Out}$ | VS Source Current Threshold to Enable Brown−out | Set $I_{VS}$ = 2.161 mA at 264 $V_{AC}$, brown out level = 55 $V_{AC}$ | 370 | 450 | 520 | μA |
| $t_{D-Brown-Out}$ | Brown−Out Debounce Time | | 12.5 | 16.5 | 21 | ms |
| $N_{Brown-Out}$ | Brown−Out Recheck Debounce Cycle Counts after No Gate Signal during $t_{D-Brown-Out}$ | | – | 3 | – | Cycle |
| $V_{VS-OVP}$ | Output Over−Voltage−Protection with Vs Sampling Voltage | | 2.9 | 3.0 | 3.1 | V |
| $V_{VS-UVP-L}$ | Output Under−Voltage−Protection with Vs Sampling Voltage | | 0.260 | 0.300 | 0.340 | V |
| $N_{VS-OVP}$ | Output Over−Voltage−Protection Debounce Cycle Counts | Enabled during $I_{DD-Burst}$ operation | – | 3 | – | Cycle |
| $N_{VS-UVP}$ | Output Under−Voltage−Protection Debounce Cycle Counts | Enabled during $I_{DD-Burst}$ operation | – | 3 | – | Cycle |
| $t_{VS-UVP-BLANK}$ | Output Under−Voltage Protection Blanking Time at start−up | | 25 | 40 | 55 | ms |
| $N_{VDD-Hiccup-L}$ | Auto−Restart 3 Cycles Mode Counts for Low Line | $V_{VS-SH} < V_{VS-UVP}$, $V_{VS-SH} > V_{VS-OVP}$, Initial state before startup, Enabled by $I_{VS} < I_{VS-LH}$ | – | 3 | – | Cycle |
| $N_{VDD-Hiccup-H}$ | Auto−Restart 6 Cycles Mode Counts for High Line | $V_{VS-SH} < V_{VS-UVP}$, $V_{VS-SH} > V_{VS-OVP}$ Enabled by $I_{VS} > I_{VS-HL}$ | – | 6 | – | Cycle |
| **OVER−TEMPERATURE PROTECTION SECTION** | | | | | | |
| $T_{OTP}$ | Threshold Temperature for Over−Temperature−Protection (Note 3) | | – | 140 | – | °C |
| **CURRENT−SENSE SECTION** | | | | | | |
| $V_{CS-LIM}$ | Current Limit Threshold Voltage | FB Pin Open | 0.85 | 0.90 | 0.95 | V |
| $V_{CS-IMIN}$ | Current Sense Threshold Voltage | | 0.18 | 0.20 | 0.22 | V |
| $t_{PD}$ | GATE Output Turn−Off Delay | | – | 50 | 100 | ns |
| $t_{LEB}$ | Leading−Edge Blanking Time | | – | 300 | – | ns |
| **CONSTANT CURRENT CORRECTION SECTION** | | | | | | |
| $I_{COMP-H}$ | High Line Compensation Current | $I_{VS}$ = 2.391 mA | 90 | 100 | 110 | μA |
| $I_{COMP-L}$ | Low Line Compensation Current | $I_{VS}$ = 814 μA | 32 | 36 | 40 | μA |
| **CONSTANT CURRENT ESTIMATOR SECTION** | | | | | | |
| $V_{REF-CC}$ | Constant Current Control Reference Voltage | | – | 1.60 | – | V |
| $V_{REF-CC-CL}$ | Closed Loop of Constant Current Control Reference Voltage | $V_{REF-CC-CL} \times A_{V-CC} \times A_{PK} \times T_{DIS} / T = V_{REF-CC}$ | 2.118 | 2.184 | 2.250 | V |
| $A_{PK}$ | Peak Value Amplifying Gain (Note 3) | | – | 3.3 | – | V/V |
| **GATE SECTION** | | | | | | |
| $V_{GATE-L}$ | Gate Output Voltage Low | | 0 | – | 1.5 | V |
| $t_r$ | Rising Time | $V_{CS}$ = 0 V, $V_{VS}$ = 0 V, $C_{GATE}$ = 1 nF | 100 | 135 | 180 | ns |
| $t_f$ | Falling Time | $V_{CS}$ = 0 V, $V_{VS}$ = 0 V, $C_{GATE}$ = 1 nF $T_J$ = 25°C | 30 | 50 | 70 | ns |
| $V_{GATE-CLAMP}$ | Gate Output Clamping Voltage | $V_{DD}$ = 25 V | 6.8 | 8.0 | 8.5 | V |
| $t_{ON-MAX}$ | Maximum On Time | $V_{FB}$ = 3 V, $V_{CS}$ = 0.3 V | 18.5 | 22 | 25.5 | μs |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Design guaranteed.

DISCONTINUED
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR onsemi REPRESENTATIVE FOR INFORMATION

## TYPICAL PERFORMANCE CHARACTERISTICS

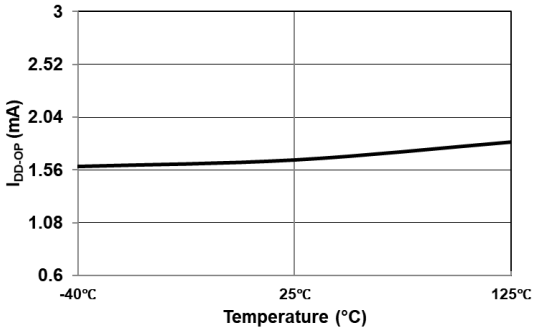



**Figure 3. Operating Supply Current ($I_{DD-OP}$) vs. Temperature**

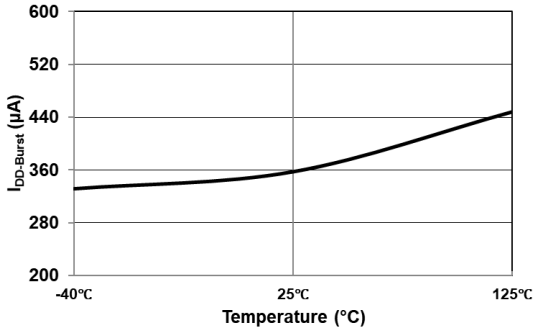



**Figure 4. Burst Mode Operating Supply Current ($I_{DD-Burst}$) vs. Temperature**

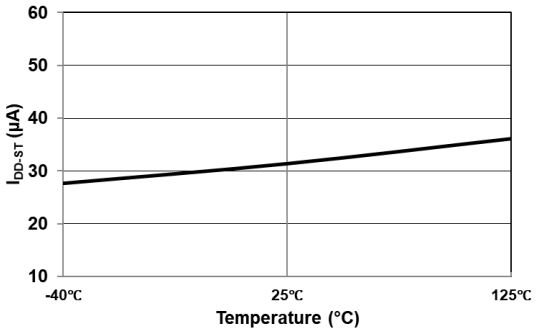



**Figure 5. Startup Current ($I_{DD-ST}$) vs. Temperature**

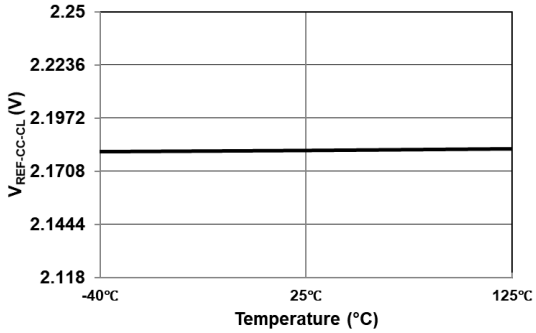



**Figure 6. Closed Loop of Constant Current Control Reference Voltage ($V_{REF-CC-CL}$) vs. Temperature**

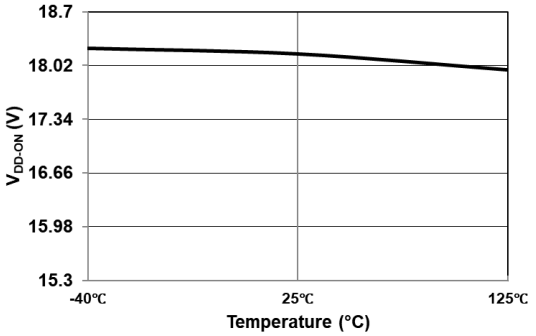



**Figure 7. Turn−ON Threshold Voltage ($V_{DD-ON}$) vs. Temperature**

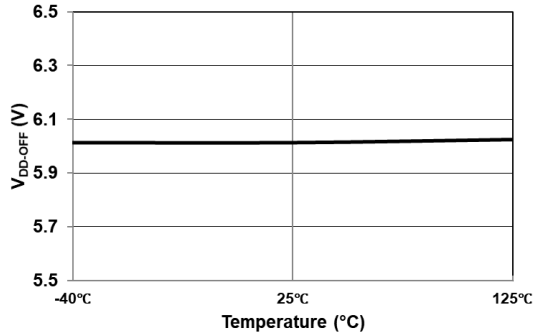



**Figure 8. Turn−Off Threshold Voltage ($V_{DD-OFF}$) vs. Temperature**

DISCONTINUED
IS NOT RECOMMENDED
PLEASE CONTACT
TATIVE FOR
DESIGN

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

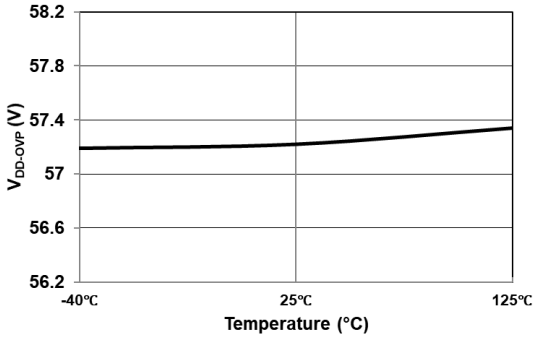



**Figure 9. VDD Over−Voltage Protection Level ($V_{DD-OVP}$) vs. Temperature**

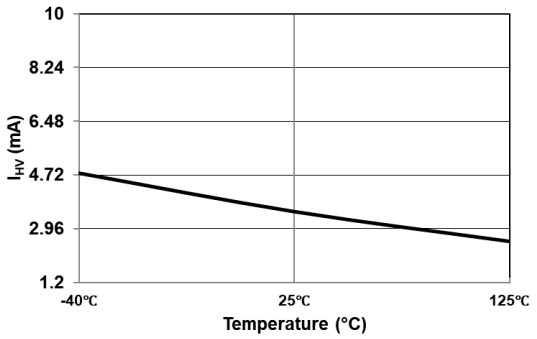



**Figure 10. Supply Current drawn from HV Pin ($I_{HV}$) vs. Temperature**

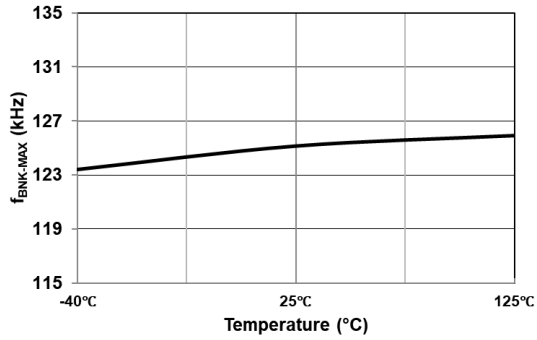



**Figure 11. Maximum Blanking Frequency ($f_{BNK-MAX}$) vs. Temperature**

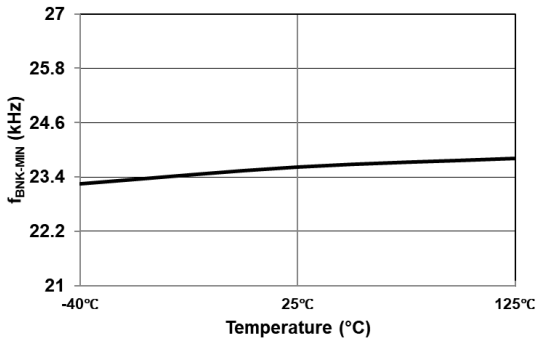



**Figure 12. Minimum Blanking Frequency ($f_{BNK-MIN}$) vs. Temperature**

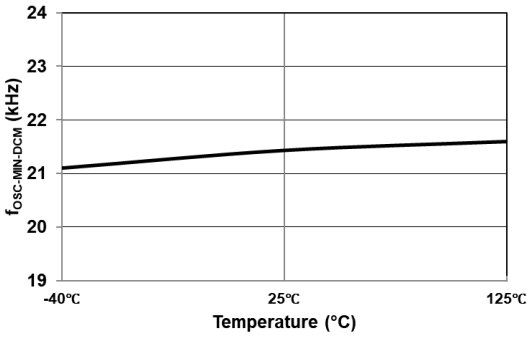



**Figure 13. Minimum Frequency for DCM ($f_{OSC-MIN-DCM}$) vs. Temperature**

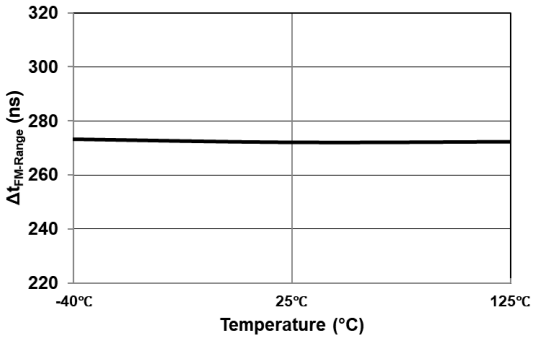



**Figure 14. Forced Frequency Modulation Range ($\Delta t_{FM-Range}$) vs. Temperature**

DISCONTINUED DESIGN
NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT
REPRESENTATIVE FOR

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

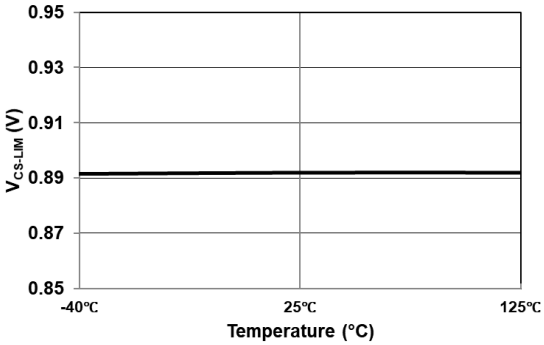



**Figure 15. Current Limit Threshold Voltage ($V_{CS-LIM}$) vs. Temperature**

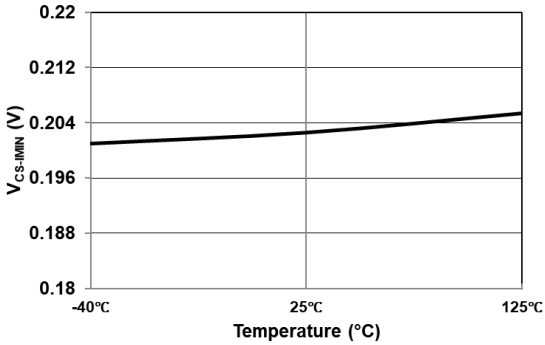



**Figure 16. Current Sense Threshold Voltage ($V_{CS-IMIN}$) vs. Temperature**

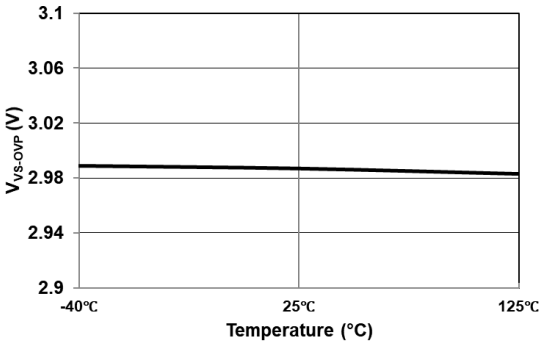



**Figure 17. Output Over−Voltage Protection with VS Sampling Voltage ($V_{VS-OVP}$) vs. Temperature**

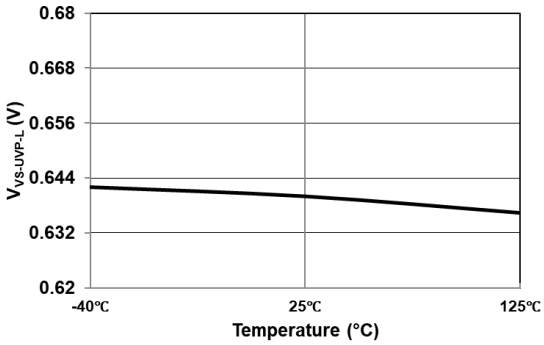



**Figure 18. Output Under−Voltage Protection with VS Sampling Voltage ($V_{VS-UVP-L}$) vs. Temperature**

DISCONTINUED DESIGN
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR ON SEMI
REPRESENTATIVE FOR ALTERNATIVES

## OPERATION PRINCIPLE

FAN6080HMX is an offline PWM controller which operates in a quasi−resonant (QR) mode and significantly enhances system efficiency and power density. The maximum operating blanking frequency is optimized to minimize the components temperature while maximizing system efficiency. It offers constant output voltage (CV) regulation through opto−coupler feedback circuitry.

Line voltage compensation gain can be programmed using an external resistor to minimize the effect of line voltage variation on output current regulation due to turn−off delay of the gate drive circuit. Minimum peak current ($I_{MIN}$), which controls the burst mode entry/exit and improves light load efficiency, is also optimized to make a balance between the standby power consumption and audible noise.

### Valley Switching

Quasi−resonant (QR) switching is a method to reduce MOSFET switching losses especially in high line. In order to perform QR turn−on of the Primary MOSFET, the valley of the resonance occurring between transformer magnetizing inductance ($L_m$) and MOSFET effective output capacitance ($C_{oss.eff}$) must be detected. Typically, during the turn−off time, there can be several valleys as the load reduces as shown in Figure 19. In order to limit the maximum switching frequency, a blanking window is introduced. To limit the minimum switching frequency, the maximum allowable time or Time−out window is fixed. These two windows allow the flyback converter to operate in a narrow user−configurable frequency range. Figure 20 shows these two windows in a switching cycle. In FAN6080HMX, the time−out window ($f_{OSC−MIN−DCM}$) is the same as the minimum frequency for CRM ($f_{OSC−MIN−CRM}$), which is 21.5 kHz.

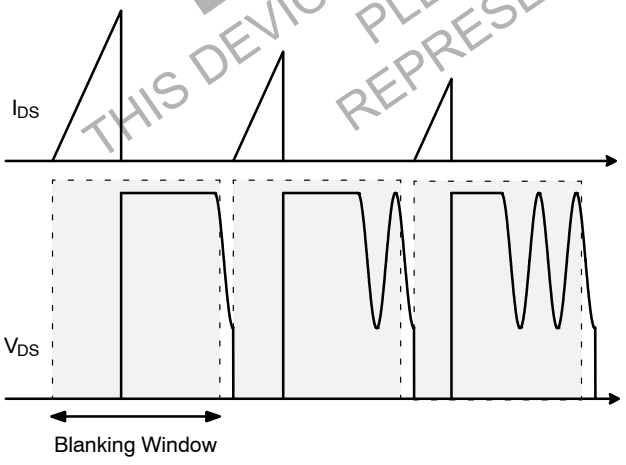



**Figure 19. Valleys Formed by Resonant Ringing Increase in Number as Load Decreases**

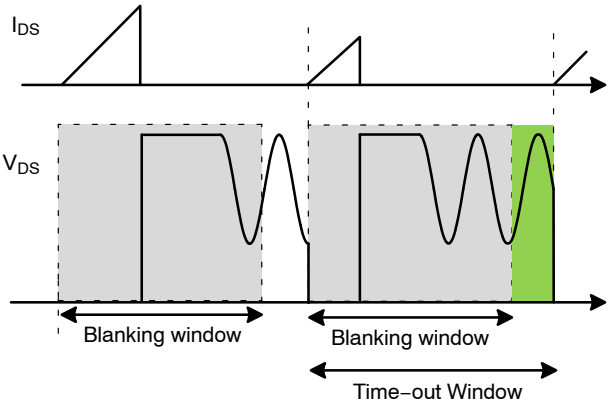



**Figure 20. Blanking Window and Time−out Window Limit the Frequency Range**

### Valley Detection

In FAN6080HMX, valley detection is done by detecting the downward zero−crossing of the VS pin. The VS pin is connected to the transformer auxiliary winding through a resistor divider configured with $R_{VSH}$ and $R_{VSL}$.

The effective resistance, $R_{VS}$ ($R_{VSH}$//$R_{VSL}$) will form an RC filter with pin capacitance, $C_{VS}$ and delay the detection by $T_{RC}$. Furthermore, there will be a logic propagation delay from VS zero−crossing detection (VS−ZCrD) to IC Gate turn on and a MOSFET gate drive propagation delay from GATE pin to MOSFET turn−on. We can assume the sum of these propagation delays to be $t_{ZCD−to−PWM}$. Typical values of these parameters are $T_{RC}$ (30 − 50 ns) and $t_{ZCD−to−PWM}$ (100 − 150 ns). As soon as blanking time, $t_{BNK}$ expires, and VS−ZCrD has occurred, the turn−on decision is made and the IC gate can turn on. For any system, if Equation 1 holds true, and the turn−on decision is made at VS−ZCrD, perfect valley switching occurs.

$$T_{RC} + t_{ZCD-to-PWM} = \frac{T_{resonance}}{4} \quad \text{(eq. 1)}$$

However, if $T_{resonance}$ / 4 is larger than $T_{RC}$ + $t_{ZCD−to−PWM}$, the switching occurs away from the valley causing higher losses. The time period of resonant ringing depends on $L_m$ and $C_{oss.eff}$. Typically, $T_{resonance}$ lies between 1 μs and 1.5 μs depending on the system parameters. Hence, the switching may occur at a point different from the valley depending on the system.

### Forced Frequency Modulation (FFM)

In order to maintain good EMI performance for low and high lines, forced frequency modulation is provided by modulating the turn−on instant of the next switching cycle near the valley point.

DISCONTINUED
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR onsemi
REPRESENTATIVE FOR INFORMATION

### Line Voltage Detection

The FAN6080HMX indirectly senses the line voltage through the VS pin while the MOSFET is turned on. During MOSFET turn−on period, the auxiliary winding voltage, $V_{AUX}$, is proportional to the input bulk capacitor voltage, $V_{BLK}$, due to the transformer coupling between the primary and auxiliary windings. During the MOSFET conduction time, the line voltage detector can detect the line voltage using Equation 2.

$$I_{VS} = \frac{V_{BLK}}{R_{VSH}} \cdot \frac{N_A}{N_P} \quad \text{(eq. 2)}$$

### Modulated Blanking Frequency

The FAN6080HMX is an adaptive hybrid QR PWM controller that adaptively changes its control method according to the load condition (valley switching with fixed blanking frequency at heavy and light load and valley switching with modulated blanking frequency at medium load) to maximize the efficiency. Also, low line blanking frequency curve is separated from high line blanking frequency curve to reduce conduction loss at low line and switching loss at high line.

In case of high line, the blanking frequency $f_{BNK}$ (= 1 / $t_{BNK}$) for valley detection is fixed by $f_{BNK-MAX}$ (125 kHz) at heavy load condition above $V_{FB}$ = 2.4 V, where $t_{BNK}$ is the blanking time (= the blanking window period). For medium load condition between $V_{FB}$ = 2.0 V and $V_{FB}$ = 2.4 V, $f_{BNK}$ is modulated as a function of $V_{FB}$ corresponding to load. $f_{BNK}$ decreases in order to reduce the switching loss, as load decreases. For light load condition below $V_{FB}$ = 2.0 V, $f_{BNK}$ is fixed by $f_{BNK-MIN}$ (24 kHz). In case of low line, $f_{BNK}$ is fixed by $f_{BNK-MAX}$ at heavy load condition above $V_{FB}$ = 2.0 V. For medium load condition between $V_{FB}$ = 1.6 V and $V_{FB}$ = 2.0 V, $f_{BNK}$ is modulated as a function of $V_{FB}$ corresponding to load. For light load condition below $V_{FB}$ = 1.6 V, $f_{BNK}$ is fixed by $f_{BNK-MIN}$.

High line blanking frequency curve is enabled when $I_{VS}$ becomes higher than $I_{VS-HL}$ (typ. 1.440 mA), while low line blanking frequency curve is enabled. Low line blanking frequency curve is enabled when $I_{VS}$ becomes less than $I_{VS-LH}$ (typ. 1.350 mA), while high line blanking frequency curve is enabled. High line voltage judgement level, $V_{HL.BNK}$, corresponding to $I_{VS-HL}$ and low line voltage judgement level, $V_{LL.BNK}$, corresponding to $I_{VS-LH}$ are determined as

$$V_{HL.BNK} = I_{VS-HL} \cdot \frac{R_{VSH}}{N_A / N_P} \quad \text{(eq. 3)}$$

$$V_{LL.BNK} = I_{VS-LH} \cdot \frac{R_{VSH}}{N_A / N_P} \quad \text{(eq. 4)}$$

where it is recommended to set $V_{HL.BNK}$ lower than 215 $V_{AC}$ for a high line blanking frequency curve at 230 $V_{AC}$ and $V_{LL.BNK}$ higher than 130 $V_{AC}$ for a low line blanking frequency curve at 115 $V_{AC}$.

From Equations 3 and 4, $R_{VSH}$ can be determined considering tolerances of $I_{VS-HL}$ and $I_{VS-LH}$ as

$$\frac{N_A}{N_P} \cdot \frac{130\ V_{AC}}{I_{VS-LH.MIN}} < R_{VSH} < \frac{N_A}{N_P} \cdot \frac{215\ V_{AC}}{I_{VS-HL.MAX}} \quad \text{(eq. 5)}$$

where $I_{VS-LH.MIN}$ is 1.208 mA and $I_{VS-HL.MAX}$ is 1.590 mA.

### CV/CC Operation Mode

Figure 21 shows the simplified CV PWM control circuit of FAN6080HMX. In constant voltage (CV) regulation, the output voltage is sensed via a voltage divider and compared with the internal reference of shunt−regulator to generate a compensation signal. The compensation signal is transferred to the primary side through an opto−coupler and fed to FB pin. The FB signal is level shifted, and scaled down by an internal attenuator AV to generate the COMV signal. The COMV signal is then applied to the PWM comparator to determine the PWM duty cycle, as shown in Figure 21.

In constant current (CC) regulation, the output current estimator calculates the output current using the transformer primary side current and the rectifier diode conduction time which is sensed on the VS pin. By comparing the estimated output current with an internal reference signal, COMI signal is generated, which determines the PWM duty cycle, as shown in Figure 21.

Two internal comparators are used to compare the COMV and COMI signals with sawtooth waveform ($V_{SAW}$) in order to determine the PWM duty cycle. As shown in Figure 21, the outputs of the two comparators are combined with an OR gate to determine the MOSFET turn−off instant. The lower between the COMV and COMI signals determines the PWM duty cycle. In CV mode, COMV determines the PWM duty cycle while COMI signal is saturated to high level. Whereas, in CC mode, COMI determines the PWM duty cycle while COMV signal is saturated to high level.

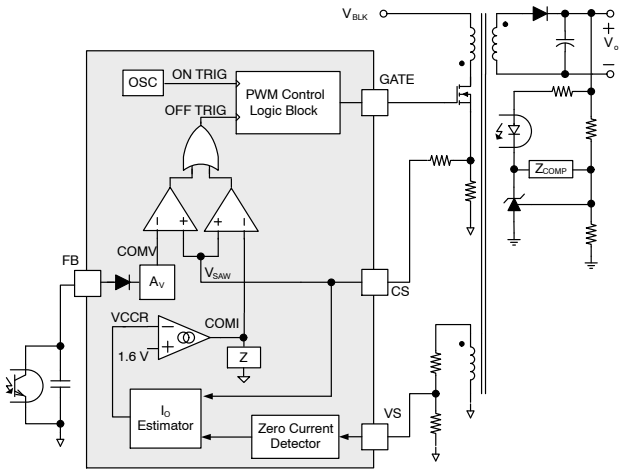



**Figure 21. Simplified PWM Control Circuit**

DISCONTINUED
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR onsemi
REPRESENTATIVE FOR INFORMATION

### Leading−Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn−on voltage spike is induced across the sense resistor. To avoid premature termination of the switching pulse due to the voltage spike, a 300 ns leading−edge blanking time ($t_{LEB}$) is built in. External RC filtering can therefore be omitted. During this blanking period, the current−limit comparator is disabled and it cannot switch off the gate driver.

### CCM Prevention

Time−out window sets the frequency to $f_{OSC-MIN-DCM}$ as explained in "Valley Switching" section. However, if the secondary side current does not reduce to zero within Time out window, FAN6080HMX does not initiate turn−on. When the secondary current reaches zero, the transformer winding voltage begins to drop sharply, and hence, the VS pin voltage drops as well. When VS pin voltage drops enough, FAN6080HMX turns on the primary MOSFET ensuring Boundary Conduction Mode (BCM) operating. Thus, FAN6080HMX does not allow the converter to enter CCM operation. During CCM prevention, FAN6080HMX can reduce the frequency down to $f_{OSC-MIN-CRM}$.

### HV Startup and Brown−In

An internal JFET provides a high voltage current source. To improve reliability and surge immunity, it is typical to use a $R_{HV}$ resistor between the HV pin and the bulk capacitor voltage.

During startup, the internal startup circuit is enabled and the bulk capacitor voltage supplies the current $I_{HV}$ to charge the hold−up capacitor, $C_{VDD}$, through $R_{HV}$. When $V_{DD}$ reaches $V_{DD-ON}$, the internal startup circuit is disabled and the sampling circuit is turned on to sample the bulk capacitor voltage. When this bulk capacitor voltage is higher than the internal brown−in reference, PWM switching starts. The brown−in voltage is trimmed at 92 V with 360 kΩ of $R_{HV}$. If line voltage is lower than the brown−in voltage, FAN6080HMX goes in auto−restart mode.

Once switching starts, the internal HV startup circuit is disabled. Once the HV startup circuit is disabled, the energy stored in $C_{VDD}$ supplies the IC operating current until the transformer auxiliary winding voltage reaches the nominal value. Therefore, $C_{VDD}$ should be properly designed to prevent $V_{DD}$ from dropping below $V_{DD-OFF}$ threshold (typically 6 V) before the auxiliary winding builds up enough voltage to supply $V_{DD}$. During startup the IC current is limited to $I_{DD-ST}$.

### Burst Mode Operation

FAN6080HMX features burst mode operation with a trimmable burst mode entry load condition using minimum peak current ($I_{MIN}$) control, which enables light load efficiency to be optimized for a given application. The $I_{MIN}$ can be selected by trim options to select minimum $V_{CS-IMIN}$ threshold level for burst mode entry.

Figure 22 illustrates the operation of the burst mode feature in FAN6080HMX. When $V_{FB}$ drops below $V_{FB-Burst-L}$, the PWM output shuts off, and the output voltage drops at a rate which is dependent on the load current level. This causes the feedback voltage to rise. Once $V_{FB}$ exceeds $V_{FB-Burst-H}$, FAN6080HMX resumes switching. The feedback voltage then falls and peak current reduces. Once the FB voltage drops below the corresponding $I_{MIN}$, the peak current, during each switching cycle, is fixed to $I_{MIN}$ regardless of FB voltage. Thus, more power is delivered to the load than required, and once FB voltage decreases lower than $V_{FB-Burst-L}$, switching stops. In this manner, the burst mode operation alternately enables and disables switching of the MOSFET to reduce the switching losses at light load condition.

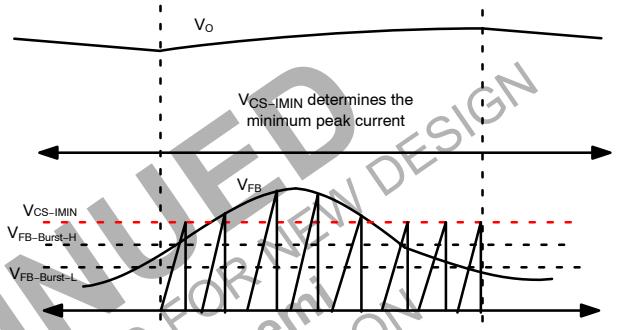



**Figure 22. Burst−Mode Operation with IMIN**

The current consumption of FAN6080HMX is reduced to $I_{DD-Burst}$ to minimize power consumption if FB voltage stays lower than $V_{FB-Burst-L}$ for more than $t_{IDD-Burst}$ (100 μs). Once feedback voltage is more than $V_{FB-Burst-H}$, IC resumes switching with normal operating current, $I_{DD-OP}$.

### Protections

When the Auto−restart mode protection is triggered, switching is terminated, and the MOSFET remains off, causing $V_{DD}$ to drop because of IC operating current $I_{DD-OP}$ (VDD−OVP, AOCP and TSD), as shown in Figure 23. When $V_{DD}$ drops to the $V_{DD}$ turn−off voltage, $V_{DD-OFF}$, the protection is reset, and the supply current drawn from HV pin begins to charge the $V_{DD}$ hold−up capacitor. When $V_{DD}$ reaches the turn−on voltage, $V_{DD-ON}$, FAN6080HMX resumes normal operation. In this manner, the auto−restart alternately enables and disables the switching of the MOSFET until the abnormal condition is eliminated.

When 3 and 6 cycles Auto−Restart mode protection is triggered at low and high lines respectively, for the case of VS−OVP or VS−UVP, the switching stops to avoid switching losses while 3 (or 6) cycles of AR are repeated, as shown in Figure 24. The multi−cycles AR operation is implemented to reduce input power consumption during output short condition.

There is no Latch mode protection in FAN6080HMX.

DISCONTINUED
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR onsemi
REPRESENTATIVE FOR INFORMATION

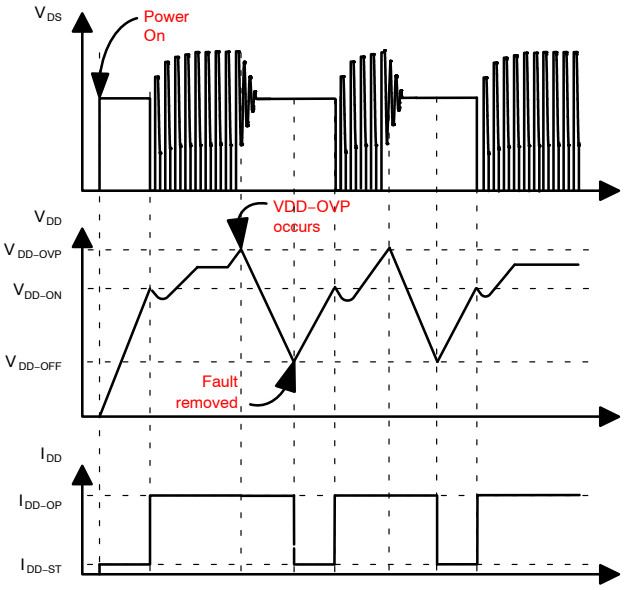



**Figure 23. Auto−restart Mode Operation (e.g. VDD−OVP)**

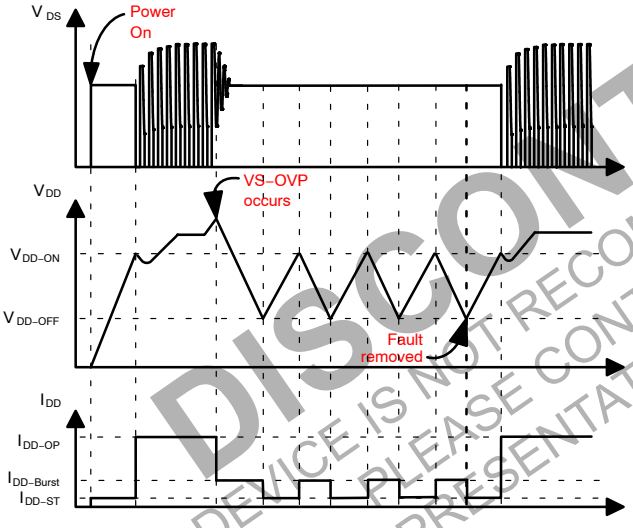



**Figure 24. 3 Cycle Auto−restart Mode Operation (e.g. VS−OVP)**

### Programming Constant Current (CC) Level

The constant current (CC) level can be programmed by the current sense resistor ($R_{CS}$) selection. FAN6080HMX estimates the output current of the converter using primary side peak current information and secondary rectifier conduction time. The CC level can be programmed by setting the current sensing resistor as

$$R_{CS} = \frac{1}{2} \cdot \frac{N_P}{N_S} \cdot \frac{1}{I_{O-CC}} \cdot \frac{V_{REF-CC}}{A_{PK}} \quad \text{(eq. 6)}$$

$V_{REF-CC}$ (1.6 V) is the inverting input of the error amplifier of the current regulator, $A_{PK}$ (3.3) is peak gain, and $I_{O-CC}$ is the desired CC level.

### Line Voltage Compensation

The output current estimation is also affected by the turn−off delay of the MOSFET. The actual MOSFET turn−off time is delayed due to the MOSFET gate charge and gate driver capability, resulting in peak current detection error as

$$\Delta I_{DS}{}^{PK} = \frac{V_{BLK}}{L_m} \cdot t_{OFF.DLY} \quad \text{(eq. 7)}$$

where $L_m$ is the transformer primary side magnetizing inductance. Since the output current error is proportional to the line voltage, the FAN6080HMX incorporates line voltage compensation to improve output current estimation accuracy. The line compensation gain is programmed by using CS pin series resistor, $R_{CS.COMP}$ depending on the MOSFET turn−off delay, $t_{OFF.DLY}$ as shown in Equations 8~10. $I_{COMP}$ creates a voltage drop, $V_{OFFSET}$, across $R_{CS.COMP}$. This line compensation offset is proportional to the DC link capacitor voltage, $V_{BLK}$ and turn−off delay, $t_{OFF.DLY}$.

$$I_{COMP} = V_{BLK} \frac{N_A}{N_P} \frac{1}{R_{VSH}} \cdot 0.04167 \quad \text{(eq. 8)}$$

$$\Delta V_{CS} = \left[ I_{ds}^{PK} - \left( \frac{V_{BLK}}{L_m} \right) \cdot (t_{ON} - t_{OFF.DLY}) \right] \cdot R_{CS} \quad \text{(eq. 9)}$$

$$R_{CS.COMP} = \frac{\Delta V_{CS}}{I_{COMP}} \quad \text{(eq. 10)}$$

where $R_{VSH}$ is given by Equation (5).

### VDD Over−Voltage−Protection (VDD−OVP)

VDD over−voltage protection prevents IC damage from over−voltage stress. It operates in the Auto−restart mode. When the $V_{DD}$ voltage exceeds $V_{DD-OVP}$ for the debounce time, $t_{D-VDDOVP}$ due to abnormal condition, the protection is triggered. This protection is typically caused by an open circuit of secondary side feedback network.

### Brown−Out Protection

Brown−out protection is operated in Auto−restart mode. When the current on VS pin is smaller than $I_{VS-Brown-Out}$ for longer than $t_{D-Brown-Out}$, the brown−out protection is triggered. The input bulk capacitor voltage to trigger brown−out protection is given as

$$V_{BLK.BO} = 450\,\mu \cdot \frac{R_{VSH}}{N_A / N_P} \quad \text{(eq. 11)}$$

where $R_{VSH}$ is given by Equation 5.

### IC Internal Over−Temperature−Protection (OTP)

The internal temperature−sensing circuit disables the PWM output if the junction temperature exceeds 140°C ($T_{OTP}$), and the FAN6080HMX enters Auto−restart mode protection.

DISCONTINUED
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR onsemi REPRESENTATIVE FOR INFORMATION

### VS Over−Voltage−Protect (VS−OVP)

VS over−voltage protection prevents damage caused by output over−voltage condition. It is operated in Auto−restart mode. When abnormal system conditions occur, which cause VS sampling voltage to exceed $V_{VS-OVP}$ for more than 3 consecutive switching cycles ($N_{VS-OVP}$), PWM pulses are disabled, and FAN6080HMX enters Auto−restart protection. VS over−voltage conditions are usually caused by open circuit of the secondary side feedback network or a fault condition in the VS pin voltage divider resistors. The desired VS−OVP is calculated as follows

$$V_{O-OVP} = \frac{N_S}{N_A} \cdot \left(1 + \frac{R_{VSH}}{R_{VSL}}\right) \cdot V_{VS-OVP} \quad \text{(eq. 12)}$$

where $V_{O-OVP}$ is the output over−voltage protection level.

### VS Under−Voltage−Protection (VS−UVP)

In the event of an output short, output voltage will drop and the primary peak current will increase. To prevent operation for a long time in this condition, FAN6080HMX incorporates under−voltage protection. The output voltage is indirectly sensed through VS pin. When VS sampling voltage is less than $V_{VS-UVP-L}$ longer than debounce cycles $N_{VS-UVP}$, VS−UVP is triggered and the FAN6080HMX enters the Auto−restart Mode.

To avoid VS−UVP triggering during the startup sequence, a startup blanking time, $t_{VS-UVP-BLANK}$, is included for system power−on. For VS pin voltage divider design, $R_{VSH}$ is calculated using Equation 5 for a certain high/low line voltage judgement level. Then, $R_{VSL}$ is designed in order to have both VS−OVP and VS−UVP level within the desired range using Equations 12 and 13.

$$V_{O-UVP} = \frac{N_S}{N_A} \cdot \left(1 + \frac{R_{VSH}}{R_{VSL}}\right) \cdot V_{VS-UVP-L} \quad \text{(eq. 13)}$$

where $V_{O-UVP}$ is the output under−voltage protection level.

### Pulse−by−Pulse Current Limit

During startup or overload condition, the feedback loop is saturated, and is unable to control the primary peak current. To limit the current during such conditions, FAN6080HMX has pulse−by−pulse current limit protection which forces the GATE to turn off when the CS pin voltage reaches the current limit threshold, $V_{CS-LIM}$.

### CS Short Protection

To prevent any inductance saturation or thermal failure due to a short circuit on the CS pin, a CS short protection feature is implemented in FAN6080HMX, as illustrated in Figure 25. In every switching cycle, the voltage on the CS pin ($V_{CS}$) is compared against a reference voltage, $V_{CS.Short}$ = 0.1 V. If $V_{CS}$ voltage is less than $V_{CS.Short}$ after a $t_{BNK.CS.Short}$ time period, CS short protection will be triggered, and turn off the GATE immediately. The CS short protection is operating pulse−by−pulse manner.

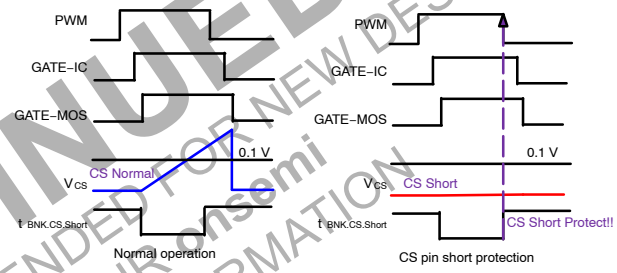



**Figure 25. CS−Short Protection Operation**

### Abnormal Over Current Protection (AOCP)

The AOCP protection triggers when a shoot−through current occurs which means primary and secondary MOSFETs turn on simultaneously. This protection is set at 1.6 V. When the PWM goes high, a leading edge blanking time ($t_{LEB}$) starts blanking this protection. Once the counter expires, the $V_{CS}$ is measured and compared to the reference voltage 1.6 V. If $V_{CS}$ is greater than 1.6 V, FAN6080HMX will shut off, and stop switching. It is a one switching cycle protection, and after it gets triggered the system enters the Auto−restart mode.

DISCONTINUED
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR onsemi
REPRESENTATIVE FOR INFORMATION

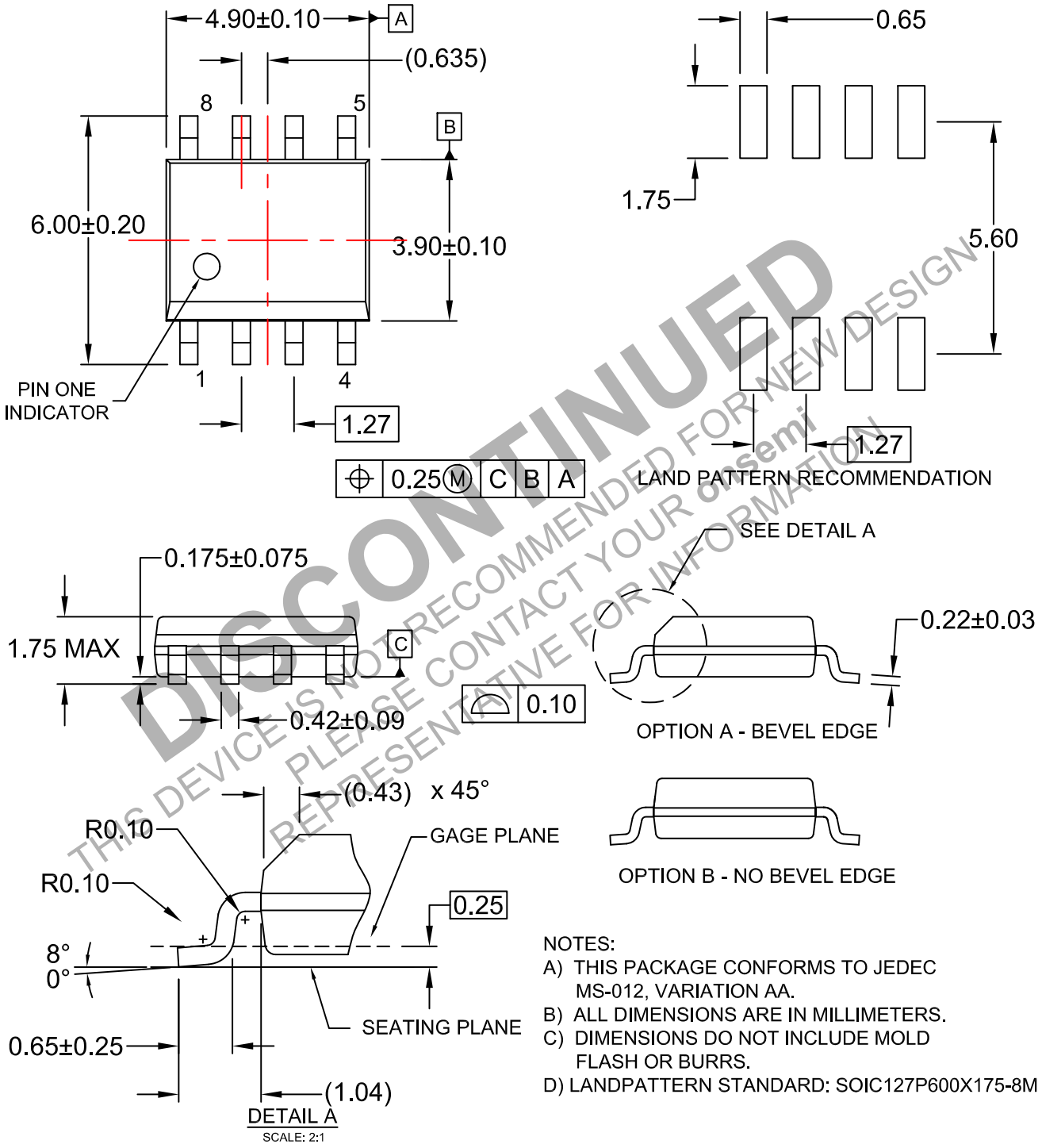
## ORDERING INFORMATION

| Device | Operating Temperature Range | Package | Shipping† |
|---|---|---|---|
| FAN6080HMX | −40°C to + 125°C | 8−Lead, Small Outline Package (SOIC), JEDEC MS−012, .150−Inch Narrow Body (Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## PACKAGE DIMENSIONS

**SOIC8**
CASE 751EB
ISSUE A




NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

DISCONTINUED
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR onsemi
REPRESENTATIVE FOR INFORMATION

DISCONTINUED
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR onsemi
REPRESENTATIVE FOR INFORMATION

MWSAVER is registered trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT**:
**Email Requests to:** orderlit@onsemi.com

**ON Semiconductor Website:** www.onsemi.com

**TECHNICAL SUPPORT**
**North American Technical Support:**
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

ENTEGRECİ

Bu belge www.entegreci.com üzerinden sunulmaktadır.

# Elektronik komponent tedarikinde Entegreci

Entegreci, Eskişehir merkezli, Türkiye geneline satış yapan bir elektronik komponent mağazasıdır. Entegreler (IC), mikrodenetleyiciler, transistörler, diyotlar, pasif elemanlar, konnektörler, modüller ve geliştirme kartları tek adetten seri üretim adetlerine kadar satılır. Ürün sayfalarında güncel stok durumunu, fiyatı ve datasheet bağlantısını bulabilirsiniz.

### Parça koduyla arama

Üretici parça numarasını yazın; stok ve fiyatı hemen görün.

**www.entegreci.com**

### Ürün kategorileri

Entegreden kapasitöre tüm elektronik komponent kategorileri.

**Kategorilere göz atın**

### Üreticiler

Aradığınız üreticinin ürünlerini tek sayfada inceleyin.

**Üreticileri görün**

### Toplu alım ve teklif

Listede olmayan ya da yüksek adetli parçalar için teklif isteyin.

**Teklif isteyin**

**www.entegreci.com** | **destek@entegreci.com** | **0850 305 90 34**

Entegreci is an online electronic components store based in Türkiye. Search by manufacturer part number to see stock, prices and datasheets for integrated circuits, microcontrollers, transistors, passive components and connectors, or request a quote for parts that are not listed.

Bu sayfa Entegreci tarafından eklenmiştir. Belgenin önceki sayfaları asıl yayıncısına aittir ve içeriği değiştirilmemiştir; en güncel sürüm için belgenin yayıncısına başvurun.