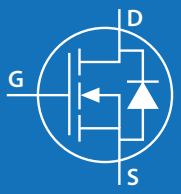
EPC2044 – Enhancement Mode Power Transistor

V_{DS}, 100 V
$R_{DS(on)}$, 10.5 mΩ
I_D, 9.4 A



EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Revised December 11, 2023

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Application Notes:

- Easy-to-use and reliable gate, Gate Drive ON = 5–5.25 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

Questions: Ask a GaN Expert

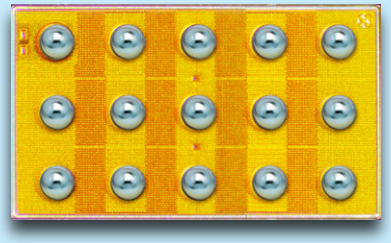
Maximum Ratings			
PARAMETER		**VALUE**	**UNIT**
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	120	
I_D	Continuous (T_A = 25°C)	9.4	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	89	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics			
PARAMETER		**TYP**	**UNIT**
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.3	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	4.1	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	72	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 0.2 mA	100			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 80 V		0.03	0.17	mA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.01	0.17	
	Gate-to-Source Forward Leakage#	V_{GS} = 5 V, T_J = 125°C		0.07	3.4	
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.03	0.33	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 3 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 10 A		7	10.5	mΩ
V_{SD}	Source-Drain Forward Voltage#	I_S = 0.5 A, V_{GS} = 0 V		2.0		V

Defined by design. Not subject to production test.



Die Size: 2.15 x 1.25 mm

EPC2044 eGaN® FETs are supplied only in passivated die form with copper pillars.

Applications

- 48 V servers
- Lidar/pulsed power
- Isolated power supplies
- Point of load converters
- Class-D audio
- LED lighting
- Low inductance
- Motor drive

Benefits

- Higher switching frequency – lower switching losses and lower drive power
- Higher Efficiency – lower conduction and switching losses, zero reverse recovery losses
- Ultra small footprint – higher power density

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC2044

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V		503	664	pF
C_{RSS}	Reverse Transfer Capacitance			1.8		
C_{OSS}	Output Capacitance			196	294	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{DS} = 0 to 50 V, V_{GS} = 0 V		247		
$C_{OSS(TR)}$	Effective Output Capacitance, Energy Related (Note 3)			318		
R_G	Gate Resistance			0.5		Ω
Q_G	Total Gate Charge	V_{DS} = 50 V, V_{GS} = 5 V, I_D = 10 A		4.3	5.5	nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 50 V, I_D = 10 A		1.3		
Q_{GD}	Gate-to-Drain Charge			0.5		
$Q_{G(TH)}$	Gate Charge at Threshold			1.0		
Q_{OSS}	Output Charge	V_{DS} = 50 V, V_{GS} = 0 V		15	23	
Q_{RR}	Source-Drain Recovery Charge			0		

All measurements were done with substrate connected to source.
Defined by design. Not subject to production test.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25 °C

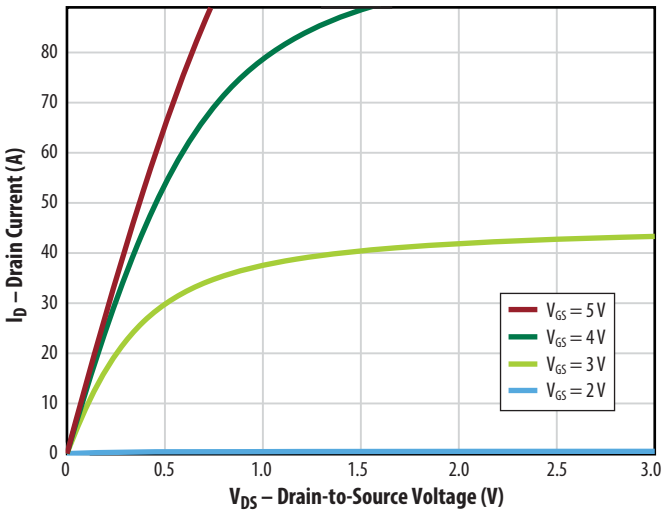


Figure 2: Typical Transfer Characteristics

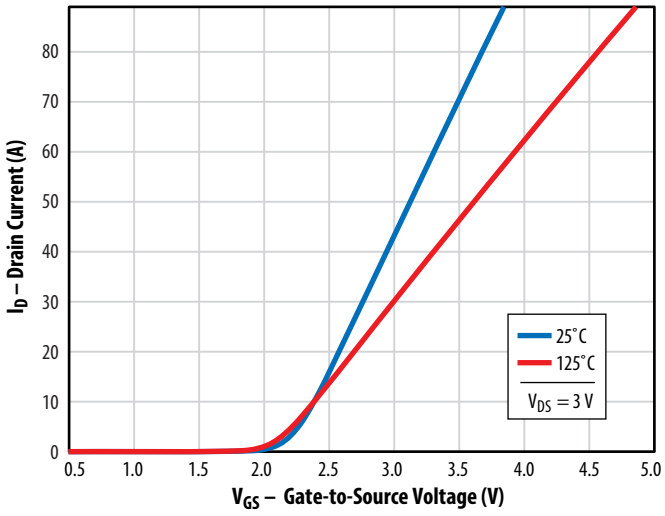


Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

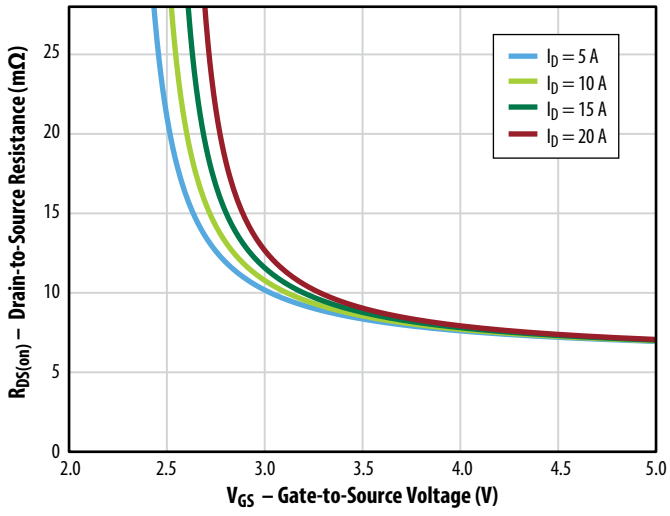


Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

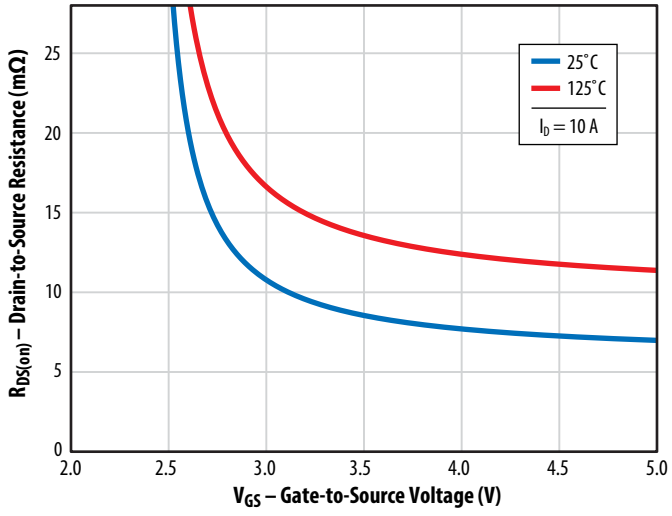


Figure 5a: Typical Capacitance (Linear Scale)

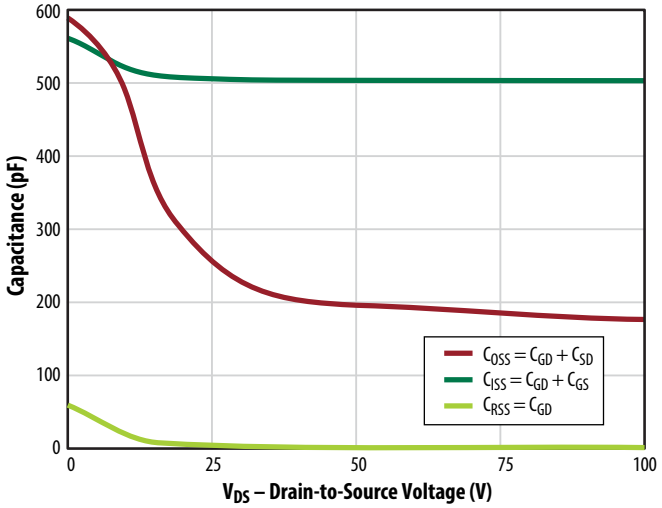


Figure 5b: Typical Capacitance (Log Scale)

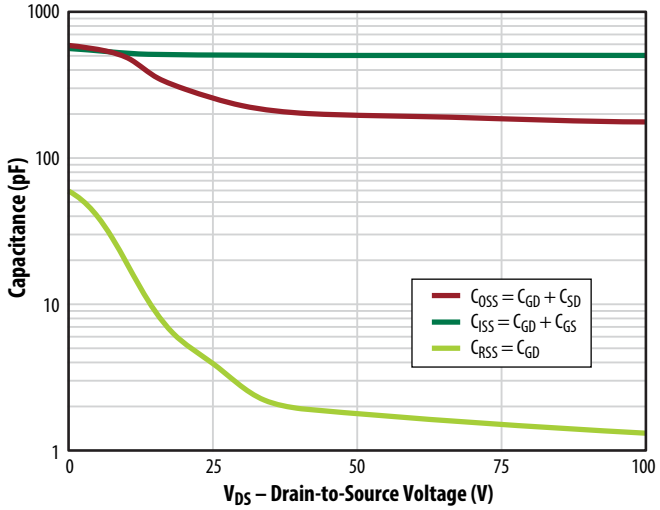


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

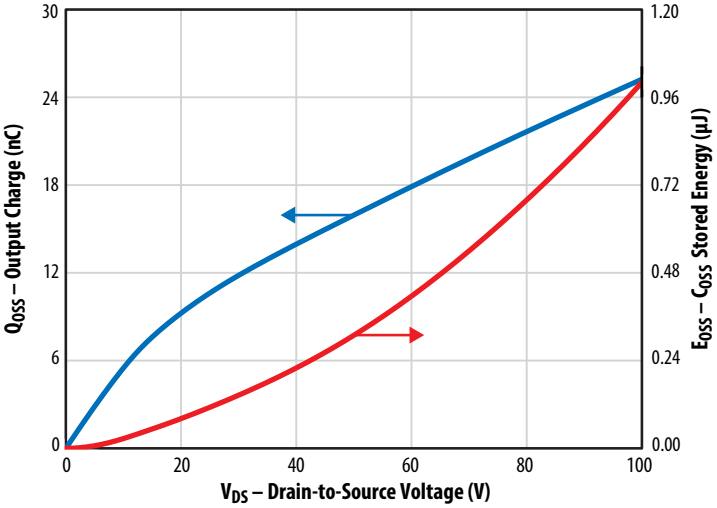


Figure 7: Typical Gate Charge

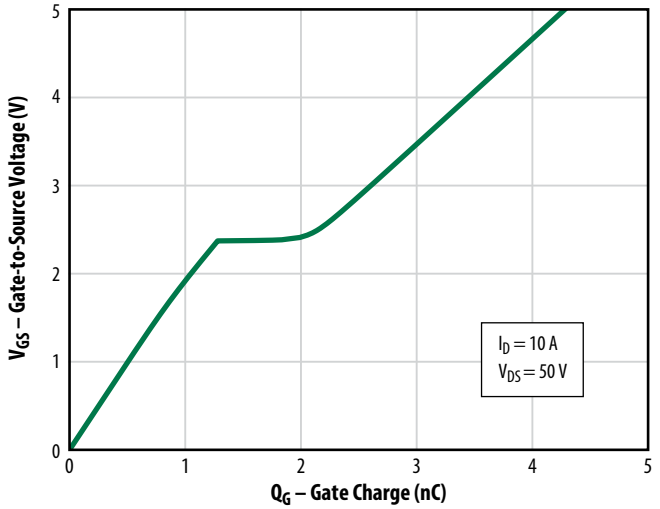


Figure 8: Typical Reverse Drain-Source Characteristics

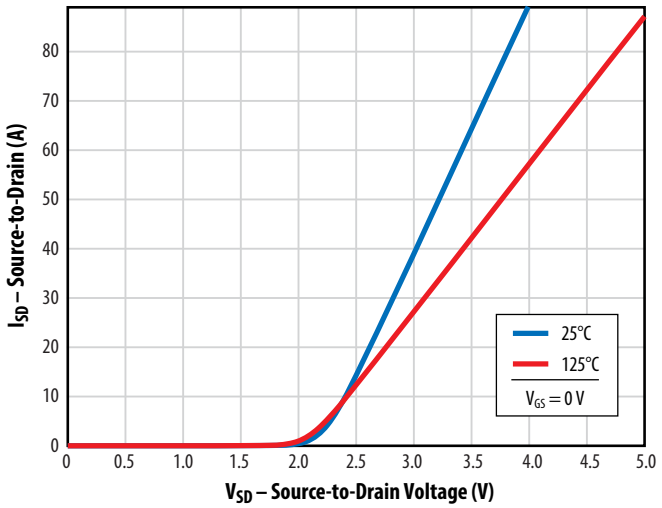
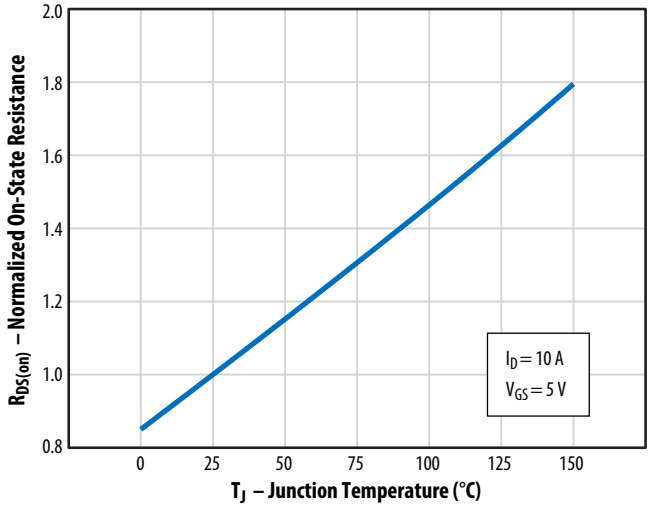


Figure 9: Typical Normalized On-State Resistance vs. Temp.



Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

Figure 10: Typical Normalized Threshold Voltage vs. Temp.

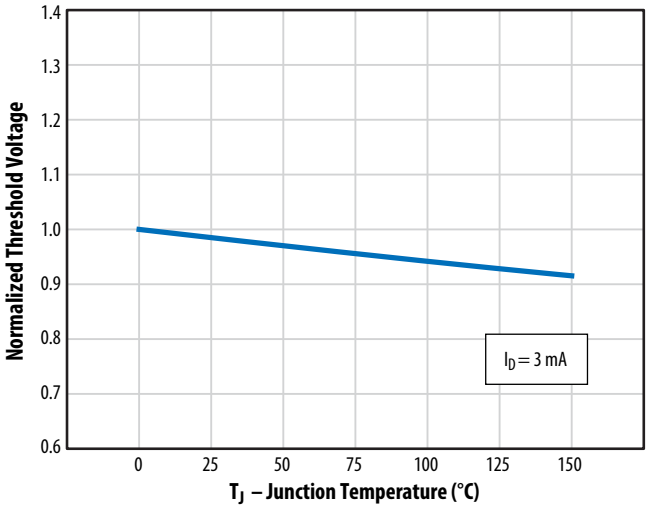


Figure 11: Typical Transient Thermal Response Curves

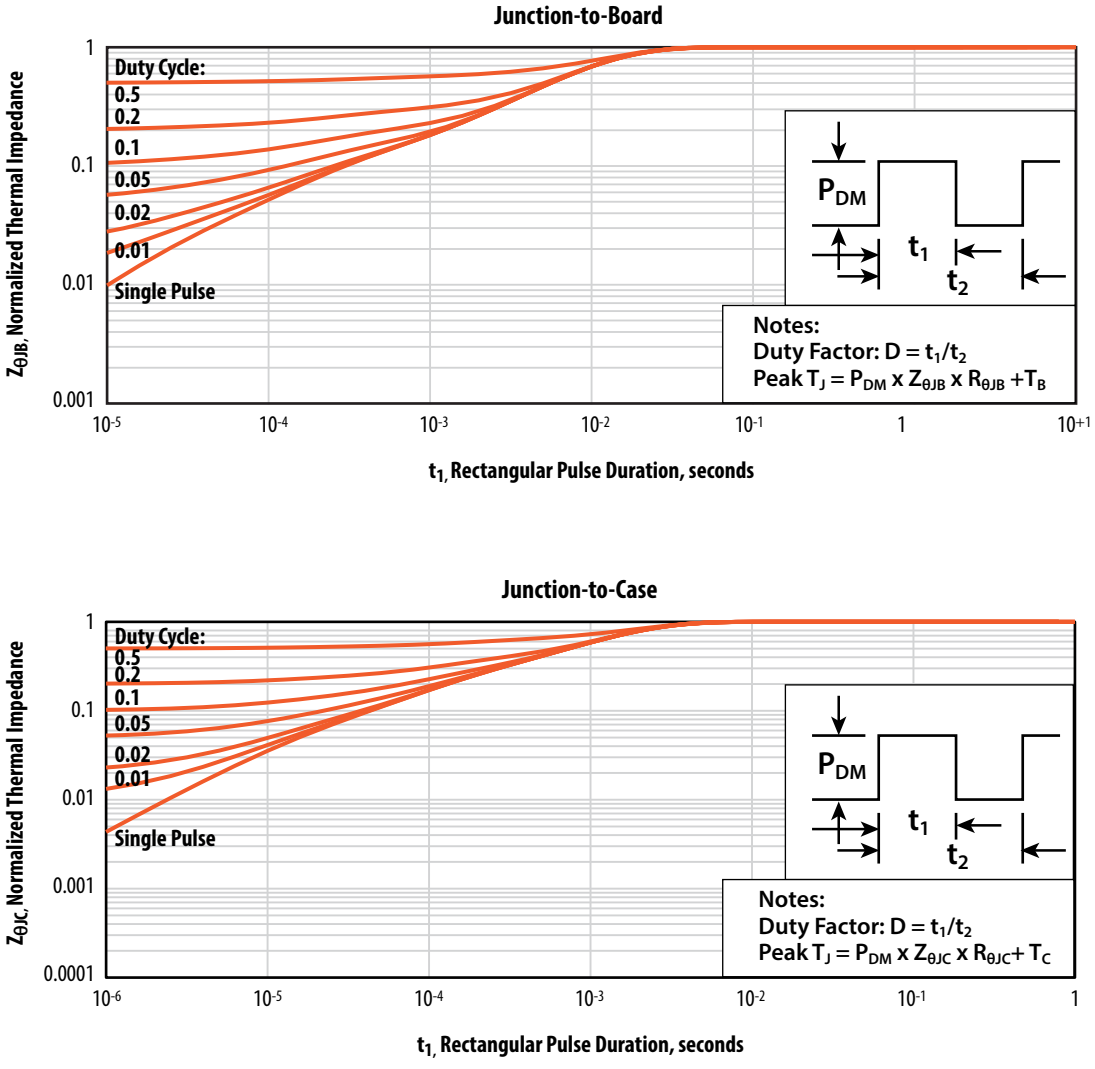
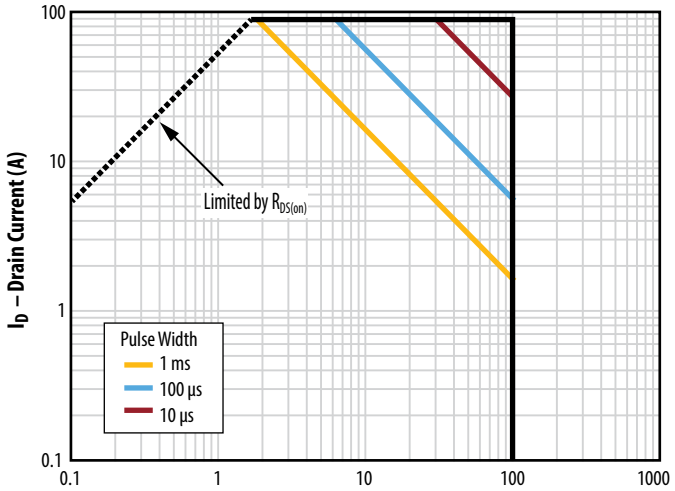


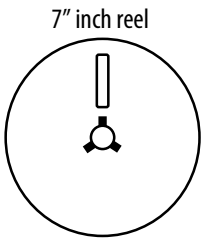
Figure 12: Safe Operating Area

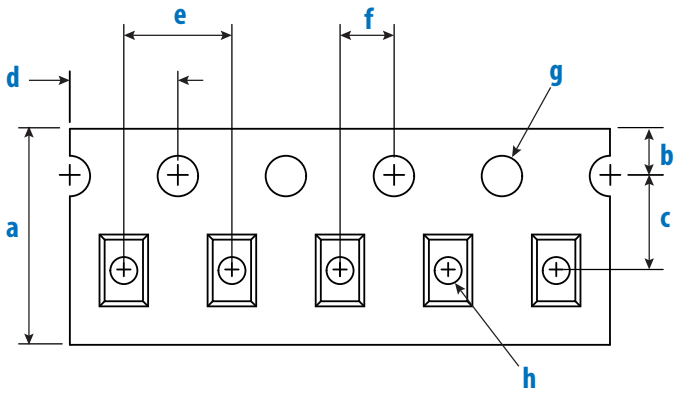


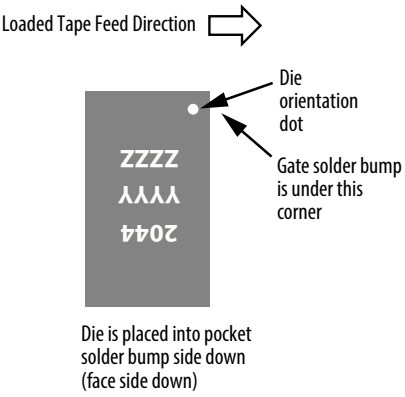
T_J = Max Rated, T_C = +25°C, Single Pulse

TAPE AND REEL CONFIGURATION

4 mm pitch, 8 mm wide tape on 7" reel





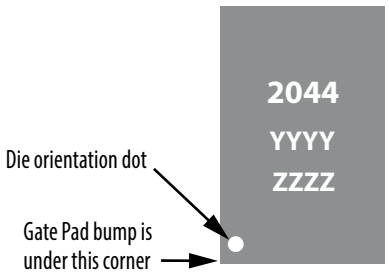


EPC2044 (Note 1)	Dimension (mm) Target	MIN	MAX
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (Note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

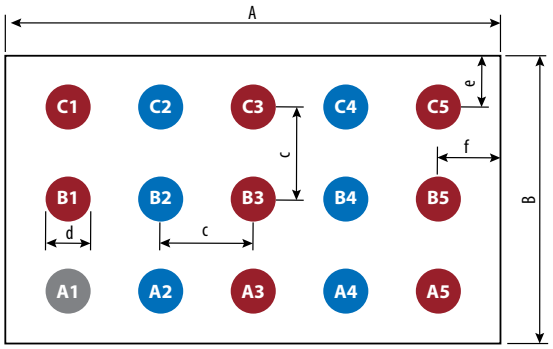
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2044	2044	YYYY	ZZZZ

DIE OUTLINE

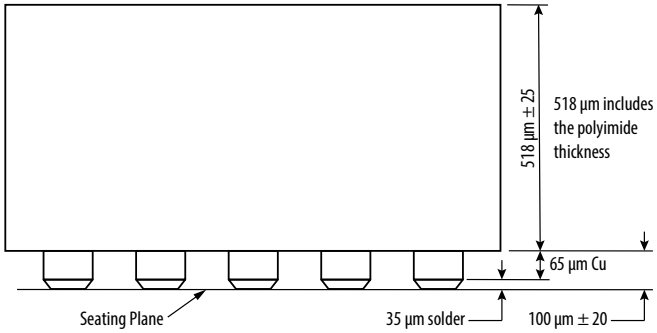
Solder Bar View



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	2120	2150	2180
B	1220	1250	1280
c		400	
d	180	200	220
e	209	225	
f	259	275	

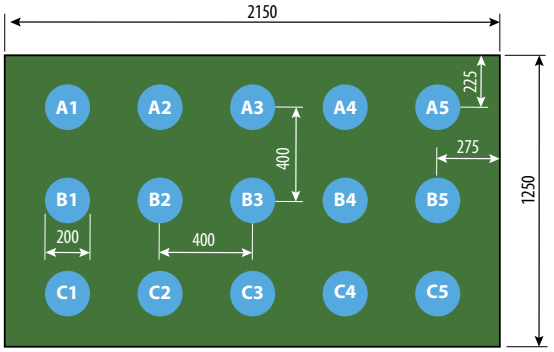
Pad A1 is Gate;
Pads B1, C1, A3, B3, C3, A5, B5, C5 are Source;
Pads A2, B2, C2, A4, B4, C4 are Drain.

Side View



RECOMMENDED LAND PATTERN

(measurements in µm)



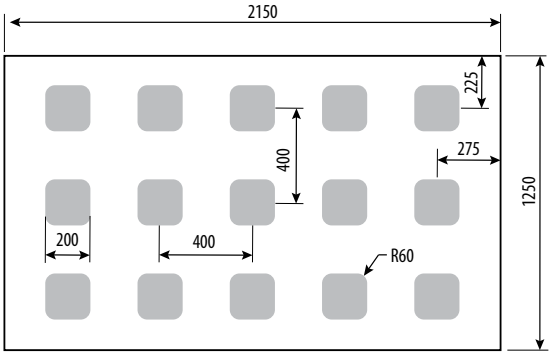
The land pattern is solder mask defined.

Pad A1 is Gate;
Pads B1, C1, A3, B3, C3, A5, B5, C5 are Source;
Pads A2, B2, C2, A4, B4, C4 are Drain.

Solder mask
(for solder mask defined pads)

RECOMMENDED STENCIL DRAWING

(units in µm)



Recommended stencil should be 4 mil (100 µm) thick, must be laser cut , opening per drawing.
The corner has a radius of R60.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Note: Cu pillar dies are not intended for mounting on a PCB, they are intended for use in a package. Terms of die usage: The die represented by this data sheet are intended for initial evaluation for integration to buyer defined package. EPC does not guarantee reliability in the buyer specific package. To ensure reliability, the die may need redesign to be optimized to buyers specific package. NRE may apply.

Solder mask defined pads are recommended for best reliability.

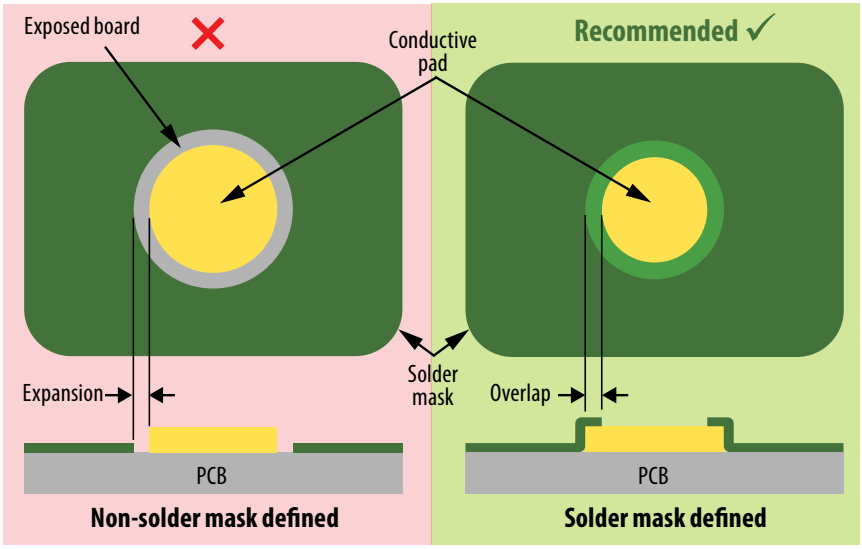


Figure 13: Solder mask defined versus non-solder mask defined pad

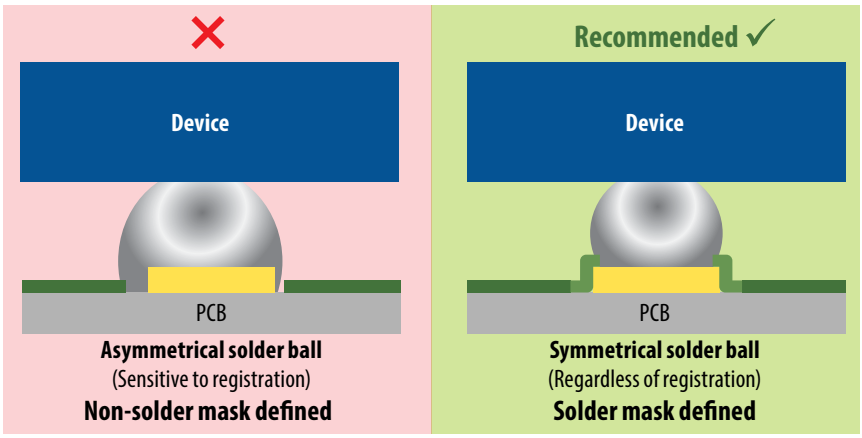


Figure 14: Effect of solder mask design on the solder ball symmetry

- Assembly resources – https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf
- Library of Altium footprints for production FETs and ICs – https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip (for preliminary device Altium footprints, contact EPC)

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