# 1-A Output, High-PSRR, Low-Noise Low-Dropout Linear Regulator

## Features

- Input Voltage Range: 2.2 V to 6.5 V
- Output Voltage Options:
  - Fixed Output: 1.2 V, 1.8 V, 3.3 V, and 5 V
  - Adjustable Output: 0.8 V to 6 V
- ±2% Accuracy over Line Regulation, Load Regulation, and Operating Temperature Range
- 1-A Maximum Output Current
- Low Dropout Voltage: 500 mV Maximum at 1 A
- High PSRR:
  - 80 dB at 1 kHz
  - 50 dB at 1 MHz
- 4.5-$\mu V_{RMS}$ Output Voltage Noise (100 Hz to 100 kHz)
- Excellent Transient Response
- Stable with a 4.7-µF or Larger Ceramic Output Capacitor
- Over-Current Protection and Over-Temperature Protection
- Package: DFN3X3-8

## Applications

- Communication: CPU, ASIC, FPGA, CPLD, DSP
- High-Performance Analog: ADC, DAC, LVDS, VCO
- Noise-Sensitive Imaging: CMOS Sensors, Video ASICs

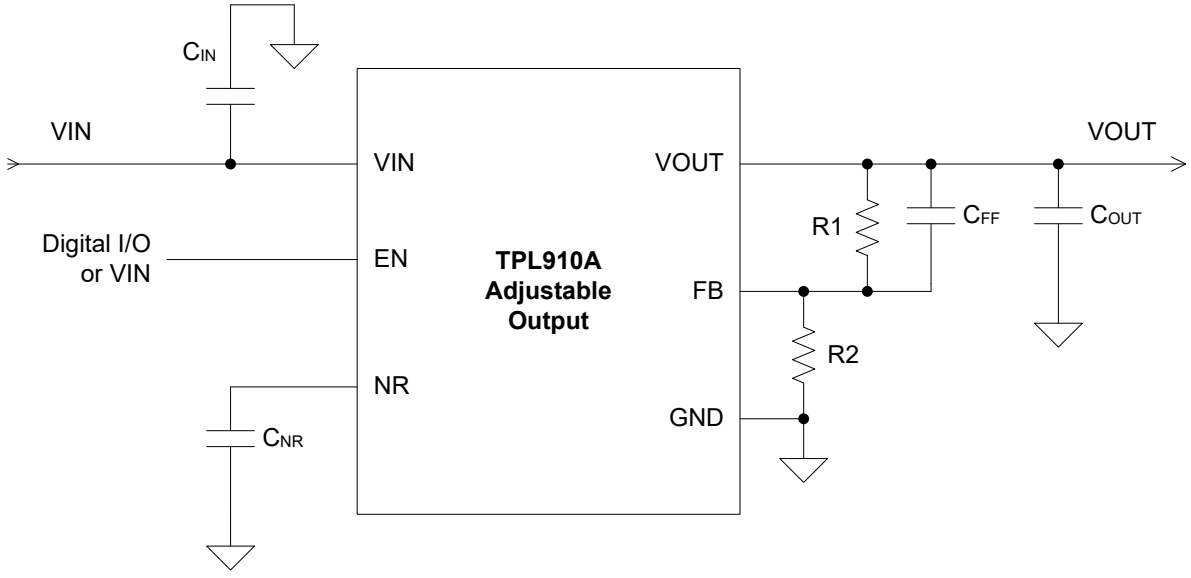
## Description

The TPL910A is a series of 1-A high-current, 4.5-$\mu V_{RMS}$ low-noise, high-PSRR, and high-accuracy linear regulators with only 500-mV maximum ultra-low dropout voltage at 1-A load current. The TPL910A series supports both fixed output voltage ranging from 1.2 V to 5 V and adjustable output voltage ranging from 0.8 V to 6 V with an external resistor divider.

Ultra-low noise, high PSRR, and high output current capability make the TPL910A series the ideal power supply for noise-sensitive applications, such as high-speed communication facilities, and high-definition imaging equipment. Accurate output voltage tolerance, excellent transient response, and adjustable soft-start control ensure the TPL910A series optimal power supply for large-scale processors or digital loads, such as ASIC, FPGA, CPLD, and DSP.

The TPL910A series provides a small DFN3X3-8 package with guaranteed operating temperature ranging from –40°C to +125°C.

## Typical Application Circuit



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## Product Family Table

| Order Number | Output Voltage (V) | Package |
|---|---|---|
| TPL910ADJA-DF6R | Adjustable | DFN3X3-8 |

## Revision History

| Date | Revision | Notes |
|---|---|---|
| 2020-12-31 | Rev.Pre.0 | Preliminary version |
| 2021-08-31 | Rev.A.0 | Initial release |
| 2023-09-15 | Rev.A.1 | 1. Updated Output Accuracy<br>2. Added Typical Value of Dropout Voltage |
| 2024-11-30 | Rev.A.2 | 1. Updated to a new datasheet format<br>2. Updated the format of Package Outline Dimensions |

## Pin Configuration and Functions

TPL910A
DFN3X3-8 Package
Top View

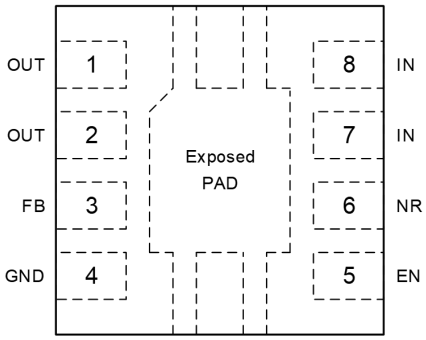



**Table 1. Pin Functions: TPL910A**

| Pin | | I/O | Description |
|---|---|---|---|
| No. | Name | | |
| 5 | EN | I | Regulator enable pin. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to IN directly. The EN pin must not be left floating. |
| 3 | FB | I | Output voltage feedback pin. Connect to an external resistor divider to adjust the output voltage. A 10-nF feed-forward capacitor from FB to OUT (as close as possible to FB pin) is recommended to maximize regulator AC performance. |
| 4 | GND | – | Ground reference pin. Connect the GND pin to the PCB ground plane directly. |
| 7, 8 | IN | I | Input voltage pin. Suggest connecting a 10-μF or larger ceramic capacitor from IN to ground (as close as possible to the IN pin) to reduce the jitter from the previous-stage power supply. |
| 6 | NR/SS | I | Noise-reduction and soft-start pin. A 10-nF or larger capacitor from NR/SS to GND (as close as possible to NR/SS pin) is recommended to maximize AC performance. |
| 1, 2 | OUT | O | Regulated output voltage pin. A 4.7-μF or larger ceramic capacitor from OUT to ground (as close as possible to OUT pin) is required to ensure regulator stability. |
| – | Exposed Pad | – | Exposed PAD must be connected to a large-area ground plane to maximize the thermal performance. |

# Specifications

## Absolute Maximum Ratings

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| IN, EN | | –0.3 | 7 | V |
| OUT | | –0.3 | $V_{IN}$ + 0.3 | V |
| FB, NR | | –0.3 | 3.6 | V |
| $T_J$ | Junction Temperature Range | –40 | 150 | °C |
| $T_{STG}$ | Storage Temperature Range | –65 | 150 | °C |
| $T_L$ | Lead Temperature (Soldering 10 sec) | | 260 | °C |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) All voltage values are with respect to GND.

## ESD, Electrostatic Discharge Protection

| Symbol | Parameter | Condition | Minimum Level | Unit |
|---|---|---|---|---|
| HBM | Human Body Model ESD | ANSI/ESDA/JEDEC JS-001 (1) | ±4 | kV |
| CDM | Charged Device Model ESD | ANSI/ESDA/JEDEC JS-002 (2) | ±1.5 | kV |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## Recommended Operating Conditions

| Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| IN | Input Voltage | 2.2 | | 6.5 | V |
| EN | Enable Voltage | 0 | | 6.5 | V |
| OUT | Output Voltage | 0.8 | | 6 | V |
| OUT | Output Current | 0 | | 1 | A |
| $C_{OUT}$ | Output Capacitor | 4.7 | | | μF |
| $C_{FF}$ | Feed-forward Capacitor | | 10 | | nF |
| $C_{NR}$ | NR Capacitor | | 10 | | nF |
| $T_J$ | Junction Temperature Range | –40 | | 125 | °C |

## Thermal Information

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| DFN3×3-8 | 69.3 | 8.16 | °C/W |

## Electrical Characteristics

All test conditions: $T_J$ = –40°C to +125°C (typical value at $T_J$ = +25°C), $V_{IN}$ = $V_{OUT\ (NOM)}$ + 0.5 V or 2.2 V, whichever is greater; $V_{EN}$ = 2.2 V, $I_{OUT}$ = 1 mA, $C_{IN}$ = 4.7 µF, $C_{OUT}$ = 4.7 µF, $C_{NR}$ = 10 nF, $C_{FF}$ = open, unless otherwise noted.

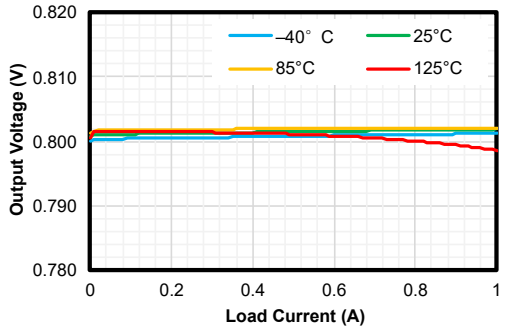
| Parameter | | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply Input Voltage and Current** | | | | | | |
| $V_{IN}$ | Supply Voltage Range (1) | | 2.2 | | 6.5 | V |
| UVLO | Input Supply UVLO | $V_{IN}$ rising, $R_L$= 1 kΩ | | | 2.1 | V |
| | Hysteresis | | | 70 | | mV |
| $I_{GND}$ | GND Pin Current | $V_{IN}$ = 6.5 V, $I_{OUT}$ = 1 mA | | 130 | 190 | µA |
| | | $V_{IN}$ = 6.5 V, $I_{OUT}$ = 1 A | | 5.4 | 8 | mA |
| $I_{SD}$ | Shutdown Current | $V_{IN}$ = 6.5 V, $V_{EN}$ = 0 V | | 2.2 | 10 | µA |
| **Device Enable** | | | | | | |
| $V_{IH(EN)}$ | EN High-level Input Voltage | Device enable | 1.2 | | 6.5 | V |
| $V_{IL(EN)}$ | EN Low-level Input Voltage | Device disable | 0 | | 0.4 | V |
| $I_{EN}$ | EN Leakage Current | $V_{IN}$ = 6.5 V, $V_{EN}$ = 0 V to 6.5 V | | 0.1 | 1 | µA |
| **Regulated Output Voltage and Current** | | | | | | |
| $V_{FB}$ | Feedback Voltage (2) | | | 0.8 | | V |
| $I_{FB}$ | FB Pin Leakage Current (2) | $V_{IN}$ = 6.5 V, stress $V_{FB}$ = 0.8 V | | 0.1 | 1 | µA |
| $V_{NR/SS}$ | NR/SS Pin Voltage | | | 0.8 | | V |
| $I_{NR/SS}$ | NR/SS Pin Charging Current | $V_{IN}$ = 6.5 V, $V_{NR}$ = GND | | 6.2 | 9 | µA |
| $V_{OUT}$ | Output Accuracy (3) | $V_{IN}$ = $V_{OUT\ (NOM)}$ + 0.5 V or 2.2 V to 6.5 V, $V_{OUT}$ = 0.8 V to 6 V, $I_{OUT}$ = 100 mA to 1 A | –2% | | 2% | |
| $\Delta V_{OUT}$ | Line Regulation | $V_{IN}$ = $V_{OUT\ (NOM)}$ + 0.5 V or 2.2 V to 6.5 V, $I_{OUT}$ = 100 mA | | 0.03 | | mV/V |
| | Load Regulation | $I_{OUT}$ = 100 mA to 1 A | | 2 | | mV/A |
| **Regulated Output Voltage and Current** | | | | | | |
| VDO | Dropout Voltage (4) | $V_{IN}$ = $V_{OUT\ (NOM)}$ + 0.5 V or 2.2 V to 6.5 V, $I_{OUT}$ = 500 mA, $V_{FB}$ = GND or $V_{SNS}$ = GND | | 75 | 250 | mV |
| | | $V_{IN}$ = $V_{OUT\ (NOM)}$ + 0.5 V or 2.2 V to 6.5 V, $I_{OUT}$ = 750 mA, $V_{FB}$ = GND or $V_{SNS}$ = GND | | 105 | 350 | mV |
| | | $V_{IN}$ = $V_{OUT\ (NOM)}$ + 0.5 V or 2.2 V to 6.5 V, $I_{OUT}$ = 1 A, $V_{FB}$ = GND or $V_{SNS}$ = GND | | 150 | 500 | mV |
| $I_{LIM}$ | Output Current Limit | $V_{OUT}$ is forced at 0.9 × $V_{OUT\ (NOM)}$, $V_{IN}$ ≥ 3.3 V | 1.1. | 1.6 | | A |

| Parameter | | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{SC}$ | Short Circuit to Ground Current Limit | $V_{OUT}$ is forced to ground, $T_A$ = 25°C | | | 0.6 | | A |
| $t_{STR}$ | Start-up Time | $V_{OUT\ (NOM)}$ = 3.3 V, $V_{OUT}$ = 0% to 90% × $V_{OUT\ (NOM)}$, $R_L$ = 3.3 kΩ, $C_{OUT}$ = 10 µF, $C_{NR}$ = 470 nF | | | 80 | | ms |
| **PSRR and Noise** | | | | | | | |
| PSRR | Power Supply Ripple Rejection | $V_{IN}$ = 4.3 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 1 A, $C_{OUT}$ = 4.7µF, $C_{NR}$ = 470 nF, $C_{FF}$ = 470 nF | f = 1 kHz | | 80 | | dB |
| | | | f = 10 kHz | | 65 | | dB |
| | | | f = 100 kHz | | 54 | | dB |
| | | | f = 1 MHz | | 45 | | dB |
| $V_N$ | Output Noise Voltage | BW = 100 Hz to 100 kHz, $V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 1 A, $C_{OUT}$ = 4.7 µF, $C_{NR}$ = 470 nF, $C_{FF}$ = 470 nF | | | 4.5 | | $\mu V_{RMS}$ |
| **Temperature Range** | | | | | | | |
| $T_{SD}$ | Thermal Shutdown Threshold | Temperature increasing | | | 165 | | °C |
| | Hysteresis | | | | 20 | | °C |

(1) Minimum $V_{IN}$ = $V_{OUT\ (NOM)}$ + $V_{DO}$ or 2.2 V, whichever is greater.
(2) For adjustable output voltage version only.
(3) Resistor tolerance is not included. Output accuracy is not tested at this condition: $V_{OUT}$ = 0.8 V, 4.5 V ≤ $V_{IN}$ ≤ 5.5 V, and 750 mA ≤ $I_{OUT}$ ≤ 1 A, because the power dissipation is out of package limitation.
(4) Dropout voltage is the minimum input-to-output voltage differential needed to maintain regulation at a specified output current and measure for $V_{OUT\ (NOM)}$ ≥ 2.2 V. In dropout mode, the output voltage will be equal to $V_{IN}$ – $V_{DO}$.

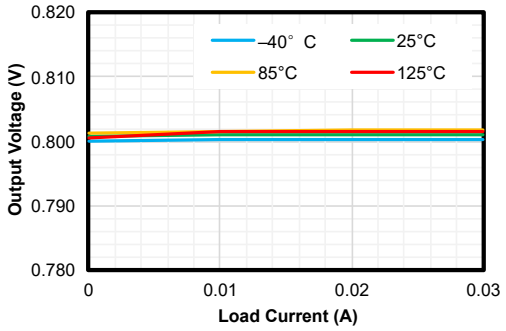
## Typical Performance Characteristics

All test conditions: $T_J$ = –40°C to +125°C (typical value at $T_J$ = +25°C), $V_{IN}$ = $V_{OUT\ (NOM)}$ + 0.5 V or 2.2 V, whichever is greater; $V_{EN}$ = 2.2 V, $I_{OUT}$ = 1 mA, $C_{IN}$ = 4.7 µF, $C_{OUT}$ = 4.7 µF, $C_{NR}$ = 10 nF, $C_{FF}$ = open, unless otherwise noted.



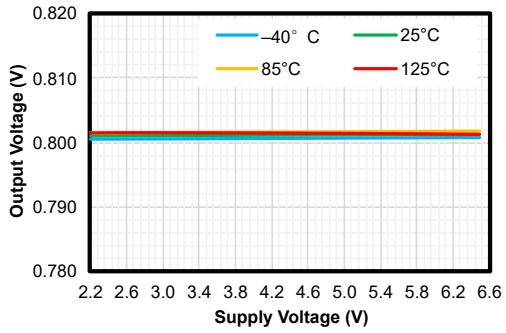

$V_{OUT}$ = 0.8 V

**Figure 1. Load Regulation**



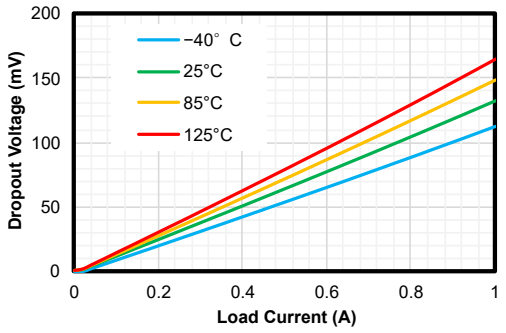

$V_{OUT}$ = 0.8 V

**Figure 2. Load Regulation at Light Load**



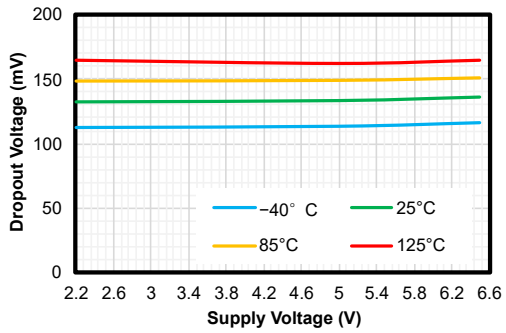

$V_{OUT}$ = 0.8 V, $I_{OUT}$ = 5 mA

**Figure 3. Line Regulation**



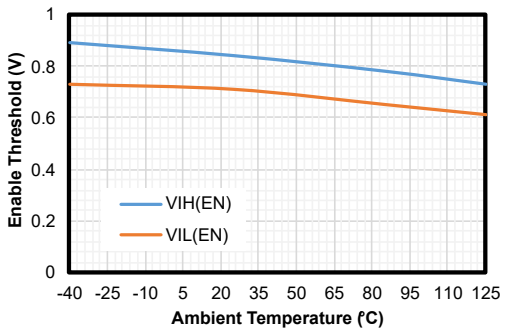

$V_{IN}$ = 2.2 V

**Figure 4. Dropout Voltage vs. Load Current**



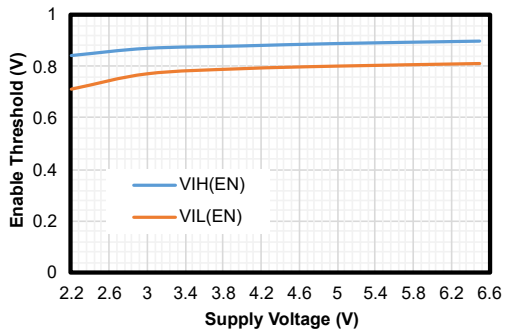

$I_{OUT}$ = 1 A

**Figure 5. Dropout Voltage vs. Supply Voltage**



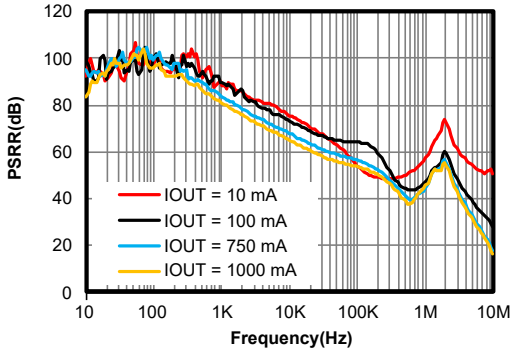

$V_{IN}$ = 2.2 V

**Figure 6. Enable Threshold vs. Temperature**



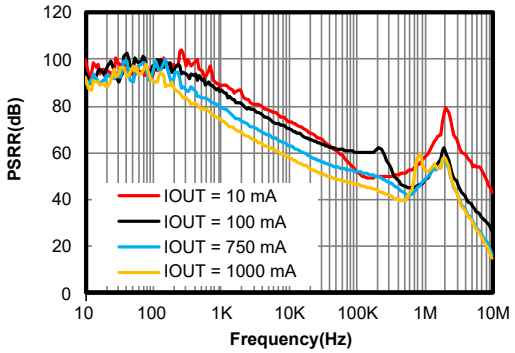

$T_A$ = 25°C

**Figure 7. Enable Threshold vs. Supply Voltage**



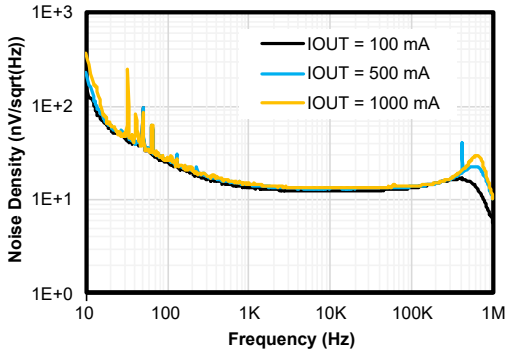

$V_{IN}$ = 4.3 V, $V_{OUT}$ = 3.3 V, $C_{OUT}$ = 10 µF, $C_{NR/SS}$ = 470 nF, $C_{FF}$ = 470 nF

**Figure 8. PSRR**



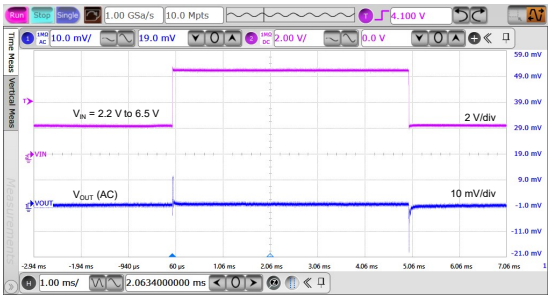

$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $C_{OUT}$ = 4.7 µF, $C_{NR/SS}$ = 470 nF, $C_{FF}$ = 470 nF

**Figure 9. PSRR**




$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $C_{OUT}$ = 4.7 µF, $C_{NR/SS}$ = 470 nF, $C_{FF}$ = 470 nF

**Figure 10. Noise**




$V_{IN}$ = 2.2 V to 6.5 V, $V_{OUT}$ = 0.8 V

**Figure 11. Line Transient**




$I_{OUT}$ = 1 mA to 1 A, $V_{OUT}$ = 0.8 V

**Figure 12. Load Transient**

# Detailed Description

## Overview

The TPL910A is a series of 1-A high-current, 4.5-$\mu V_{RMS}$ low-noise, high-PSRR, and high-accuracy linear regulators with only 500-mV maximum ultra-low dropout voltage at 1-A load current. The TPL910A series supports both fixed output voltage ranging from 1.2 V to 5 V and adjustable output voltage ranging from 0.8 V to 6 V with an external resistor divider.

Ultra-low noise, high PSRR, and high output current capability make the TPL910A series the ideal power supply for noise-sensitive applications, such as high-speed communication facilities, and high-definition imaging equipment. Accurate output voltage tolerance, excellent transient response, and adjustable soft-start control ensure the TPL910A series optimal power supply for large-scale processors or digital loads, such as ASIC, FPGA, CPLD, and DSP.

## Functional Block Diagram

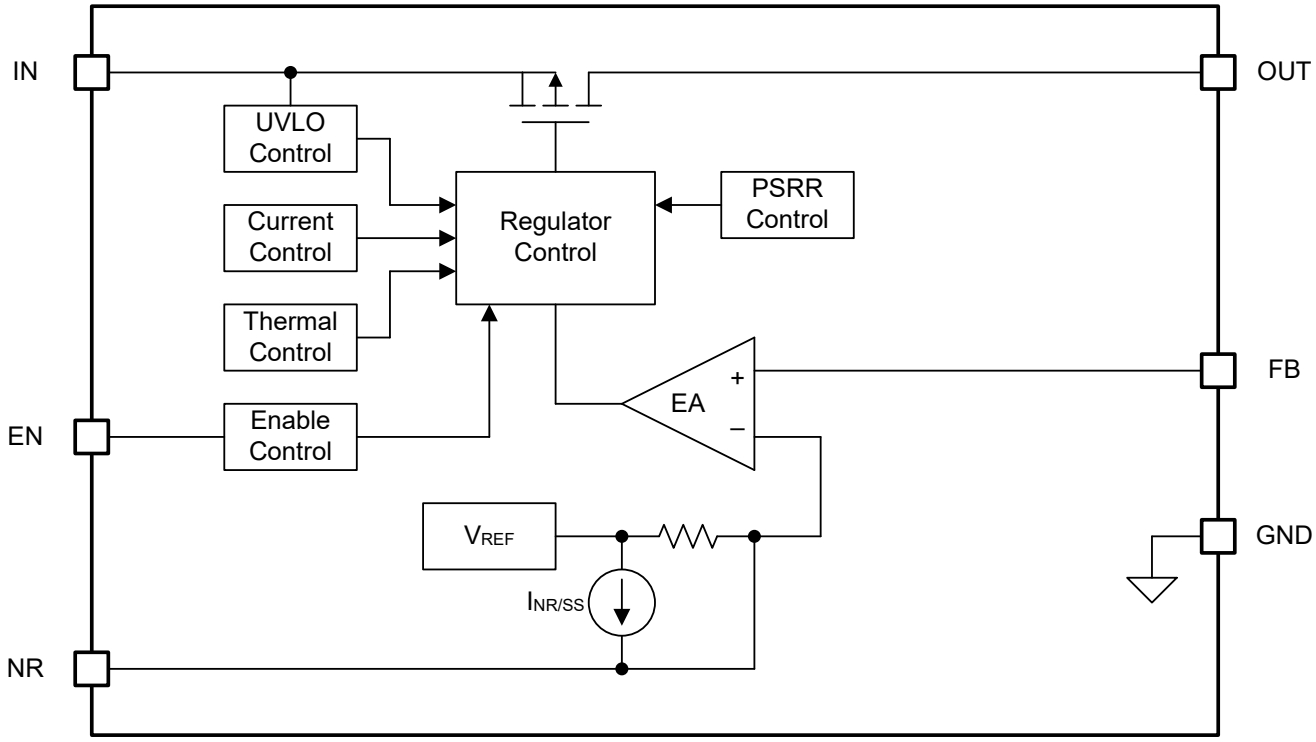



**Figure 13. Functional Block Diagram**

## Feature Description

#### Enable (EN)

The TPL910A series provides a device enable pin (EN) to enable or disable the device. Connect this pin to the GPIO of an external digital logic control circuit to control the device. When the $V_{EN}$ voltage falls below $V_{IL(EN)}$, the LDO device turns off, and when the $V_{EN}$ ramps above $V_{IH(EN)}$, the LDO device turns on.

### Under-Voltage Lockout (IN and UVLO)

The TPL910A series uses an under-voltage lockout circuit to keep the output shut off until the internal circuitry operates properly. Refer to the Electrical Characteristics table for UVLO threshold and hysteresis.

### Fixed Output Voltage (OUT)

The TPL910A series is available in fixed voltage versions of 1.2 V, 1.8 V, 3.3 V, and 5 V. When the input voltage is higher than $V_{OUT\ (NOM)}$ + $V_{DO}$ or 2.2V, whichever is greater, the OUT pin is regulated with a fixed voltage. When the input voltage falls below $V_{OUT\ (NOM)}$ + $V_{DO}$ and is greater than the UVLO threshold, the OUT pin tracks the input voltage, and the output voltage value equals to $V_{IN}$ − $V_{DO}$.

### Adjustable Output Voltage (OUT and FB)

The TPL910A series is also available in adjustable voltage versions of 0.8 V to 5 V. Using an external resistor divider, the output voltage of the TPL910A series is determined by the value of the resistors R1 and R2 in Figure 15. Use Equation 1 to calculate the output voltage.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Where the feedback voltage $V_{FB}$ is 0.8 V.

Table 2 provides a list of recommended resistor combinations to achieve the common output voltage values.

**Table 2. External Resistor Combinations**

| Target Output Voltage (V) | External Resistors Divider | | Calculated Output Voltage (V) |
|---|---|---|---|
| | R1 (kΩ) | R2 (kΩ) | |
| 0.80 | 0 | 10 | 0.800 |
| 0.85 | 0.62 | 10 | 0.850 |
| 0.90 | 1.24 | 10 | 0.899 |
| 0.95 | 1.87 | 10 | 0.950 |
| 1.00 | 2.49 | 10 | 0.999 |
| 1.20 | 4.99 | 10 | 1.199 |
| 1.50 | 8.75 | 10 | 1.500 |
| 1.80 | 12.5 | 10 | 1.800 |
| 2.50 | 21.3 | 10 | 2.504 |
| 2.80 | 25 | 10 | 2.800 |
| 3.00 | 27.5 | 10 | 3.000 |
| 3.30 | 31.3 | 10 | 3.304 |
| 3.60 | 35 | 10 | 3.600 |
| 4.50 | 46.3 | 10 | 4.504 |
| 5.00 | 52.5 | 10 | 5.000 |

### Programmable Soft Start

The TPL910A series integrates a programmable soft-start function to control the output voltage ramp-up slew rate and start-up time. By selecting the external capacitor at the NR/SS pin, the output start-up time can be calculated with Equation 2.

$$t_{Start-up} = 1.25 \times \left( \frac{V_{NR/SS} \times C_{NR/SS}}{I_{NR/SS}} \right) \quad (2)$$

Where, the typical value of $V_{NR/SS}$ is 0.8 V, the typical value of $I_{NR/SS}$ is 6.2 μA, and $C_{NR/SS}$ is the external capacitor at the NR/SS pin.

### Over-Current Protection

The TPL910A series integrates an internal current limit that helps to protect the regulator during fault conditions.

- When the output voltage is pulled down below the regulated voltage, over-current protection starts to work and limits the output current to $I_{LIM}$.
- When the output voltage is pulled down below the short-to-ground threshold (about 140 mV), or shorted to the ground directly, short-to-ground protection starts to work and limits the output current to $I_{SC}$.
- During startup, the output current is limited to $I_{SC}$ before the output voltage ramps higher than the short-to-ground threshold.

Under the over-current conditions, the internal junction temperature ramps up quickly. When the junction temperature is high enough, it will cause over-temperature protection.

### Over-Temperature Protection

The over-temperature protection starts to work when the junction temperature exceeds the thermal shutdown (TSD) threshold, which turns off the regulator immediately. When the device cools down and the junction temperature falls below the thermal shutdown threshold minus thermal shutdown hysteresis, the regulator turns on again.

The junction temperature range should be limited according to the Recommended Operating Conditions table, continuously operating above the junction temperature range will reduce the device lifetime.

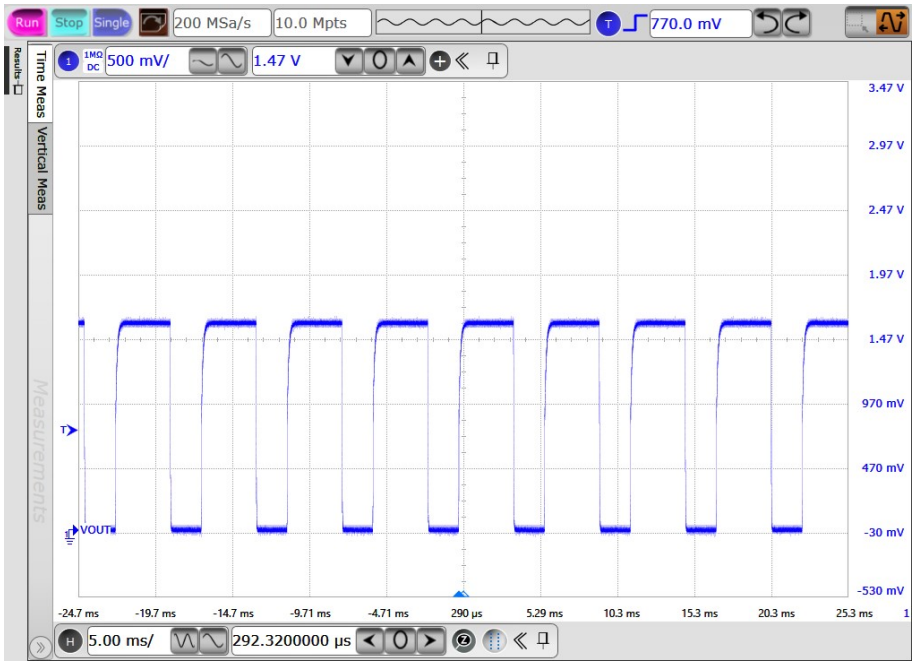



**Figure 14. Over-Temperature Protection**

# Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## Application Information

The TPL910A is a series of 1-A high-current, 4.5-$\mu V_{RMS}$ low-noise, high-PSRR, and high-accuracy linear regulators with only 500-mV maximum ultra-low dropout voltage. The following application schematic shows a typical usage of the TPL910A series.

## Typical Application

Figure 15 shows the typical application schematic.

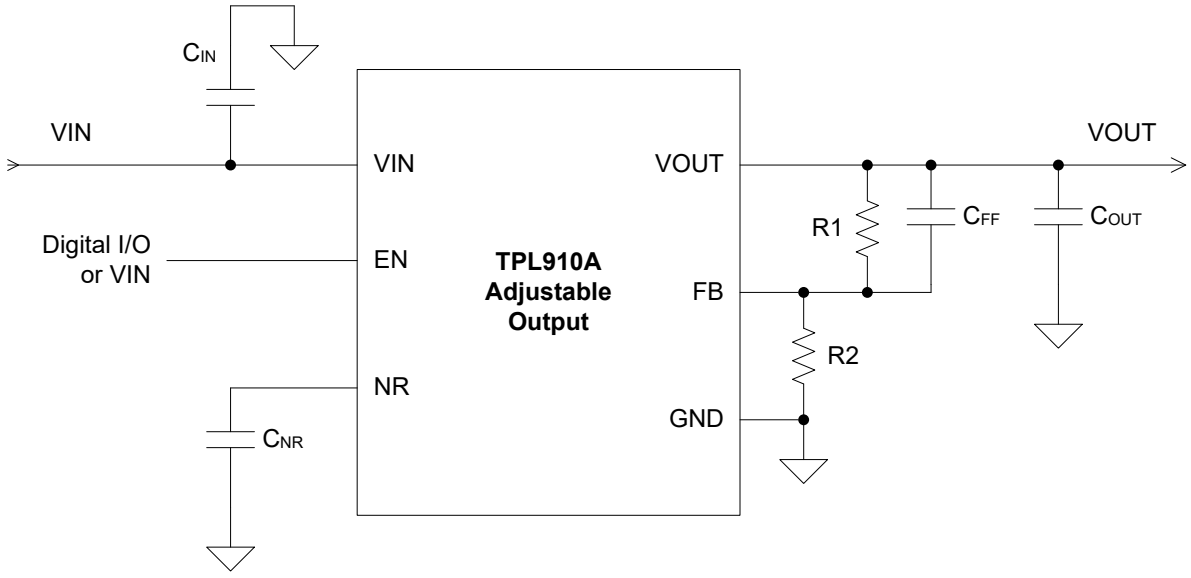



**Figure 15. Typical Application Circuit**

### Input Capacitor and Output Capacitor

The TPL910A series is designed to be stable with low equivalent series resistance (ESR) ceramic capacitors at the input, output, and noise-reduction pin (NR/SS). It is recommended to use ceramic capacitors with X7R-, X5R-, and COG-rated dielectric materials to get good capacitive stability across temperatures.

3PEAK recommends adding a 10 µF or greater capacitor with a 0.1 µF bypass capacitor in parallel at the IN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

To ensure loop stability, the TPL910A series requires a minimum 4.7 µF low ESR output capacitor. 3PEAK recommends selecting an X7R-type 10-µF ceramic capacitor with low ESR over temperature.

Both input and output capacitors must be placed as close to the device pins as possible.

**Power Dissipation**

During normal operation, the LDO junction temperature should meet the requirement in the Recommended Operating Conditions table. Use the below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 3

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (3)$$

The junction temperature can be estimated using Equation 4. $\theta_{JA}$ is the junction-to-ambient thermal resistance.

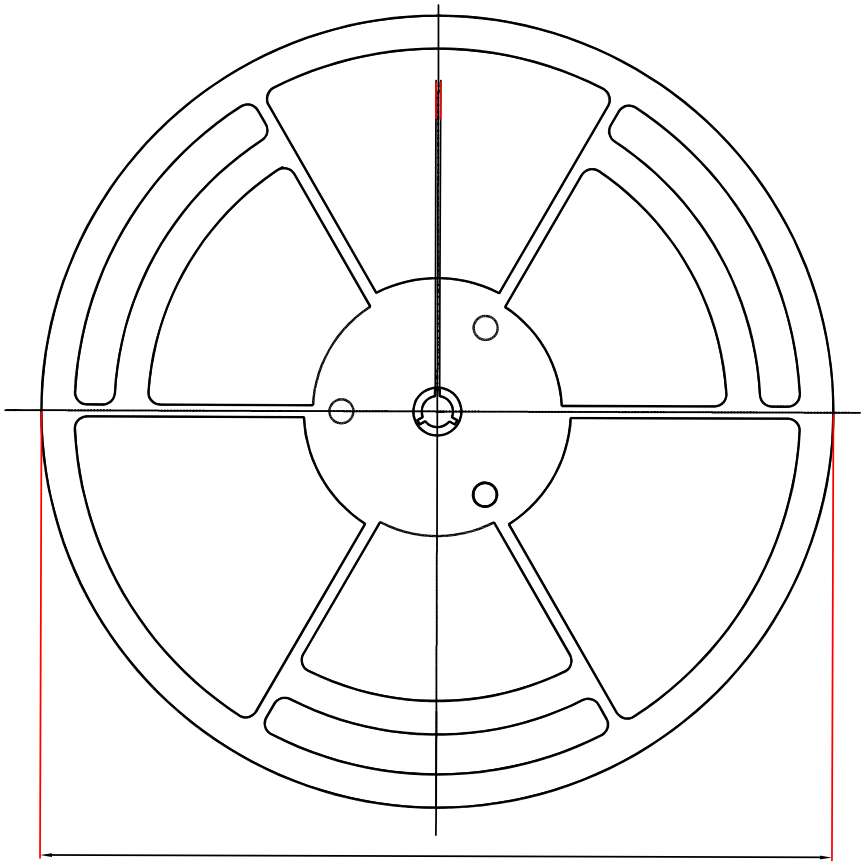
$$T_J = T_A + P_D \times \theta_{JA} \quad (4)$$

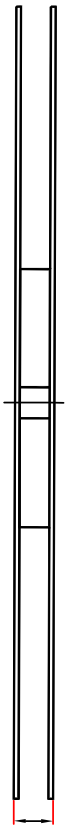
# Layout

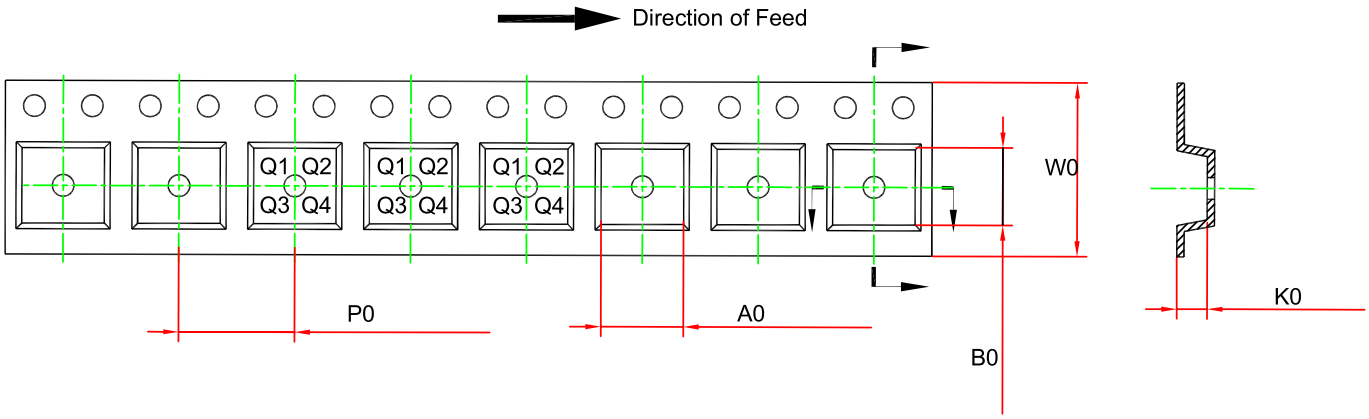
## Layout Guideline

- Both input and output capacitors must be placed as close to the device pins as possible, and vias between capacitors and device power pins must be avoided.
- It is recommended to bypass the input pin to ground with a 0.1-μF bypass capacitor. The loop area formed by the bypass capacitor connection, the IN pin, and the GND pin of the system must be as small as possible.
- It is recommended to use wide and thick copper to minimize I×R drop and heat dissipation.

## Tape and Reel Information



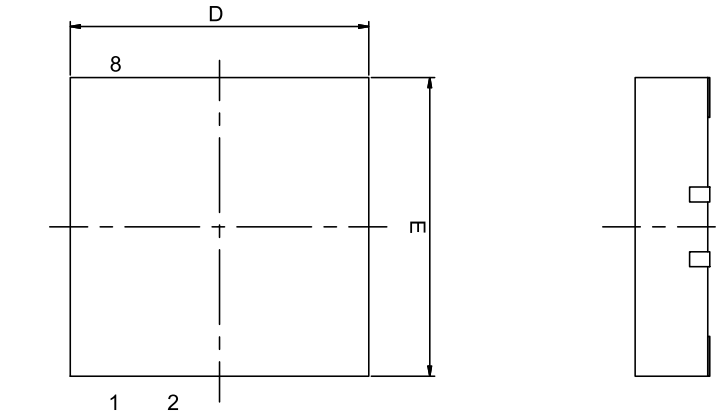



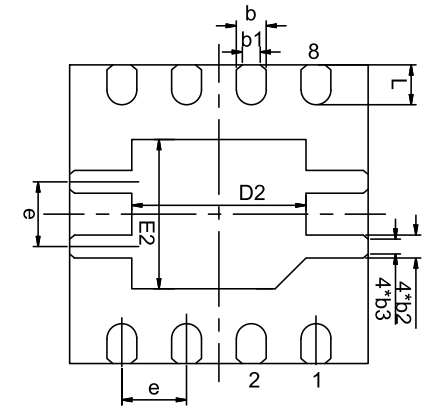

| Order Number | Package | D1 (mm) | W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | W0 (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|
| TPL910ADJA-DF6R | DFN3X3-8 | 330.0 | 17.6 | 3.4 | 3.4 | 1.1 | 8.0 | 12.0 | Q2 |

## Package Outline Dimensions

### DFN3X3-8

Package Outline Dimensions DF6(DFN3X3-8-C)




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| b | 0.250 | 0.350 | 0.010 | 0.014 |
| b1 | 0.180 REF | | 0.007 REF | |
| b2 | 0.180 | 0.280 | 0.007 | 0.011 |
| b3 | 0.150 REF | | 0.006 REF | |
| A3 | 0.150 | 0.250 | 0.006 | 0.010 |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| D2 | 1.650 | 1.850 | 0.065 | 0.073 |
| E | 2.900 | 3.100 | 0.114 | 0.122 |
| E2 | 1.400 | 1.600 | 0.055 | 0.063 |
| e | 0.650 BSC | | 0.026 BSC | |
| L | 0.350 | 0.450 | 0.014 | 0.018 |

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

## Order Information

| Order Number | Operating Temperature Range | Package | Marking Information | MSL | Transport Media, Quantity | Eco Plan |
|---|---|---|---|---|---|---|
| TPL910ADJA-DF6R | –40°C to +125°C | DFN3X3-8 | L910A | MSL3 | Tape and Reel, 4,000 | Green |

**Green**: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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