Bi-Directional Current and Power Monitor

Features

- Senses Bus Voltages From 0 V to 36 V
- High-Side or Low-Side Sensing
- Reports Current, Voltage, and Power
- High Accuracy
- Configurable Averaging Options
- 16 Programmable Addresses
- Operates from 2.7-V to 5.5-V Power Supply
- MSOP10 Package

Applications

- Power Management
- Servers
- Telecom Equipment
- Computing
- Test Equipment

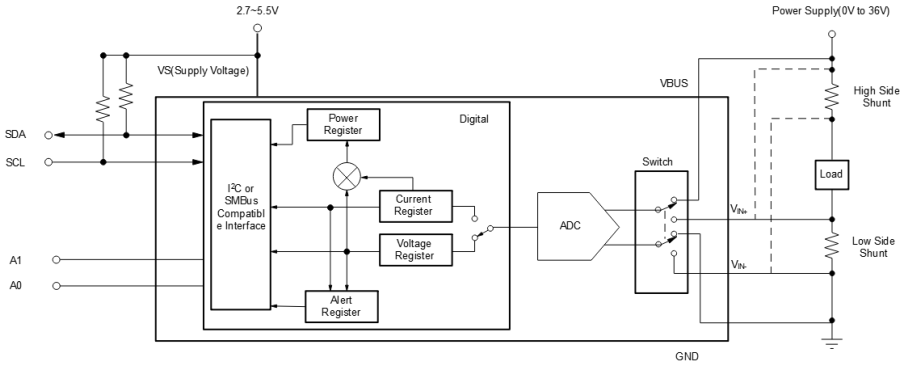
Description

The TPA620 is a current and power monitor, with I^2C or SMBUS-compatible interface. The device monitors both a shunt voltage drop and bus supply voltage.

The TPA620 common mode input voltage can vary from 0 V to 36 V.

The TPA620 features up to 16 programmable addresses on the I^2C-compatible interface.

Functional Block Diagram



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Revision History

Date	Revision	Notes
2020-6-10	Rev.A.1	Initial version.
2021-5-25	Rev.A.2	Updated diagram.
2021-11-10	Rev.A.3	Updated I^2C address table, added a note of configuration register.
2021-11-16	Rev.A.4	Corrected typo of package name.
2022-12-15	Rev.A.5	Updated block diagram.
2022-12-30	Rev.A.6	Corrected typo of the power unit from mA to μA.
2023-1-10	Rev.A.7	Updated application information.
2024-12-02	Rev.A.8	Updated to a new datasheet format. Added the Tape and Reel Information. Updated the Package Outline Dimensions.

Pin Configuration and Functions

TPA620
MSOP10 Package
Top View

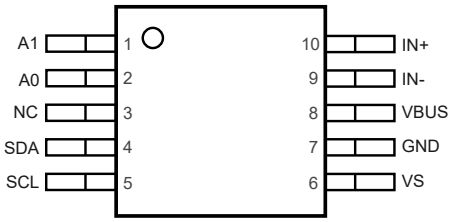


Table 1. Pin Functions: TPA620

Pin No.	Pin Name	I/O	Description
2	A0	Digital input	Address pin. Connect to GND, SCL, SDA, or VS.
1	A1	Digital input	Address pin. Connect to GND, SCL, SDA, or VS.
3	NC	NA	NC
7	GND	Analog	Ground.
10	IN+	Analog input	Connect to the supply side of the shunt resistor.
9	IN–	Analog input	Connect to the load side of the shunt resistor.
5	SCL	Digital input	Serial bus clock line, open-drain input.
4	SDA	Digital I/O	Serial bus data line, open-drain input/output.
8	VBUS	Analog input	Bus voltage input.
6	V_S	Analog	Power supply, 2.7 V to 5.5 V.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Typ	Max	Unit
V_S	Supply Voltage			6	V
Analog Inputs, IN+, IN–	Differential (V_{IN+} – V_{IN-}) (2)	–40		40	V
	Common-Mode (V_{IN+} + V_{IN-}) / 2	–0.3		40	V
V_{VBUS}		–0.3		40	V
V_{SDA}		GND – 0.3		6	V
V_{SCL}		GND – 0.3		V_{VS} + 0.3	V
I_{IN}	Input Current into any Pin			5	mA
I_{OUT}	Open-Drain Digital Output Current			10	mA
T_J	Junction Temperature			150	℃
T_{STG}	Storage Temperature Range	−65		150	℃

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) IN+ and IN– may have a differential voltage between –40 V and 40 V. However, the voltage at these pins must not exceed the range –0.3 V to 40 V.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
MSOP10	171	42.9	°C/W

Electrical Characteristics

All test conditions: TA = 25°C, VVS = 3.3 V, V_{IN+} = 12 V, V_{SHUNT} = (V_{IN+} – $V_{IN–}$) = 32 mV, V_{VBUS} = 12 V, PGA = /1, and BRNG (1) = 1, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Input						
Shunt Voltage Input Range		PGA = /1	–40		40	mV
		PGA = /2	–80		80	mV
		PGA = /4	–160		160	mV
		PGA = /8	–320		320	mV
Bus Voltage Input Range (1)		BRNG = 1	0		32	V
		BRNG = 0	0		16	
CMRR	Common-Mode Rejection	0 V ≤ VIN+ ≤ 36 V	110			dB
VOS Shunt Offset Voltage, RTI (2)		PGA=/1		±2.5	±50	μV
		PGA=/2				
		PGA=/4		±2.5	±75	μV
		PGA=/8				
Shunt Offset Voltage, RTI (2) vs Temperature		–40°C ≤ T_A ≤ 125°C		0.15		μV/°C
Shunt Offset Voltage, RTI (2) vs Power Supply		2.7 V ≤ VS ≤ 5.5 V		5		μV/V
VOS Bus Offset Voltage, RTI (2)				±1.25	±30	mV
Bus Offset Voltage, RTI (2) vs Temperature		–40°C ≤ T_A ≤ 125°C		30		μV/°C
Bus Offset Voltage, RTI (2) vs Power				2		mV/V
IB Input bias Current				10		μA
VBUS Input Impedance				325		kΩ
Input Leakage (3)		(IN+ pin) + (IN– pin), Power-down mode		1		μA
DC Accuracy						
ADC Native Resolution				12		Bits
1 LSB Step Size		Shunt voltage		10		μV
		Bus voltage		4		mV
Shunt Voltage Gain Error				0.02%	0.40%	
Shunt Voltage Gain Error Vs Temperature		–40°C ≤ T_A ≤ 125°C		50		ppm/°C
Bus Voltage Gain Error				0.02%	0.40%	
Bus Voltage Gain Error Vs Temperature		–40°C ≤ T_A ≤ 125°C		50		ppm/°C
t_{CT}	ADC Conversion Time	12 bit		542		μs

Parameter		Conditions	Min	Typ	Max	Unit
		11 bit		269		µs
		10 bit		134		µs
		9 bit		66		µs
SMBus Timeout (4)				28		ms
Input Capacitance				3		
Leakage Input Current		$0\ V \le V_{SCL} \le V_{VS}$		0.1		µA
		$0\ V \le V_{SDA} \le V_{VS}$				
		$0\ V \le V_{Alert} \le V_{VS}$				
		$0\ V \le V_{A0} \le V_{VS}$				
		$0\ V \le V_{A1} \le V_{VS}$				
V_{IH}	High-Level Input Voltage		$0.7\times V_{VS}$			V
V_{IL}	Low-Level Input Voltage				$0.3\times V_{VS}$	V
V_{OL}	Low-Level Output Voltage, SDA, Alert	I_{OL} = 3 mA	0		0.4	V
Hysteresis				150		mV
Operating Supply Range			2.7		5.5	V
I_Q	Quiescent Current			1100		µA
	Quiescent Current, Power-Down (shutdown) Mode			8		µA
V_{POR}	Power-on Reset Threshold			2.2		V

(1) This parameter only expresses the full-scale range of the ADC scaling.
(2) RTI = Referred-to-input.
(3) Input leakage is positive (current flowing into the pin) for the conditions shown at the top of this table. Negative leakage currents can occur under different input conditions.
(4) SMBus timeout in the TPA620 resets the interface any time SCL is low for more than 28 ms.

Typical Performance Characteristics

All test conditions are: T_A = 25°C, V_{VS} = 3.3 V, V_{IN+} = 12 V, V_{SHUNT} = (V_{IN+} – V_{IN-}) = 32 mV, V_{VBUS} = 12 V, PGA = /1, and BRNG [(1)] = 1 unless otherwise noted.

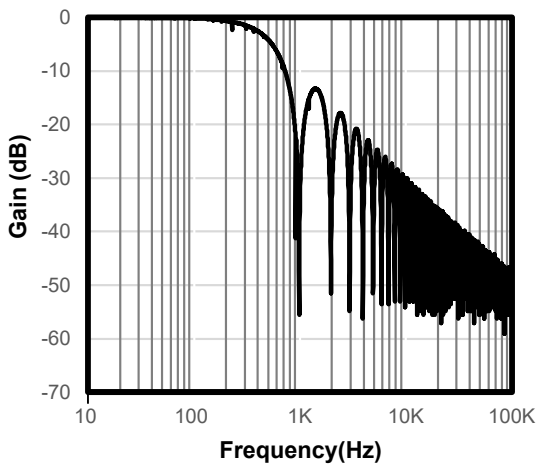


Figure 1.

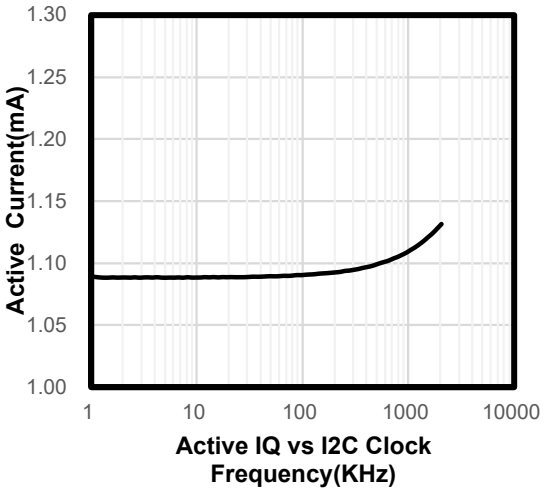


Figure 2.

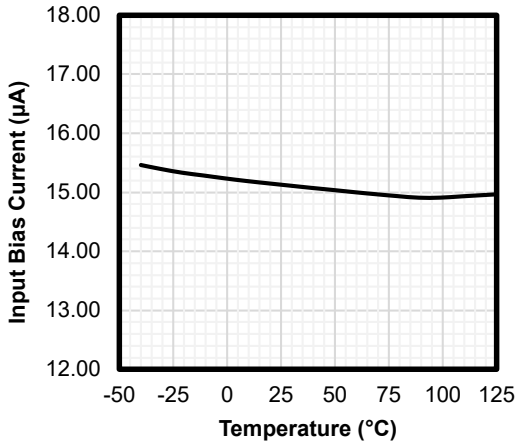


Figure 3.

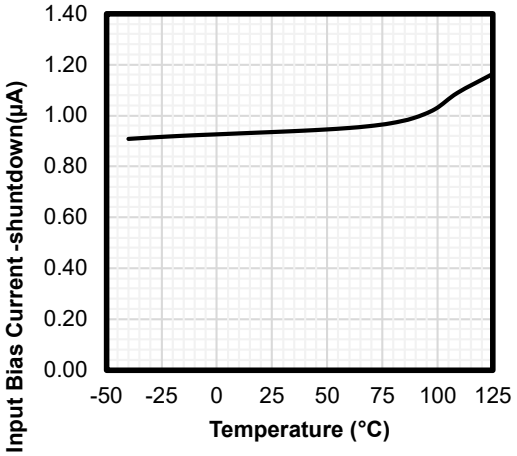


Figure 4.

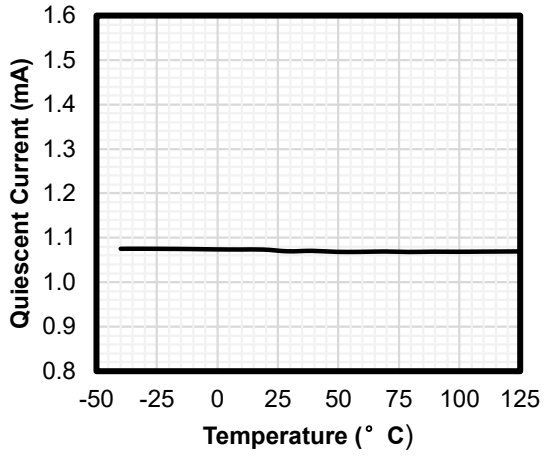


Figure 5.

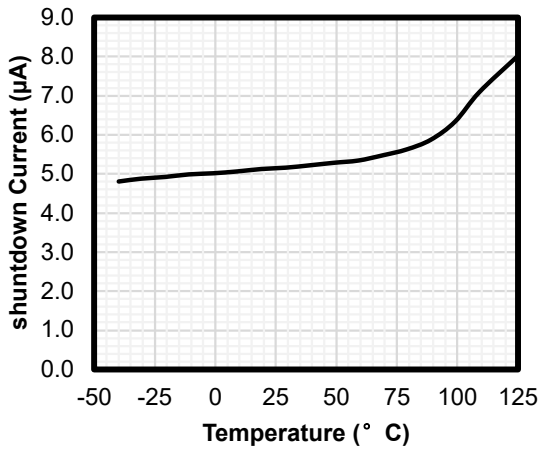


Figure 6.

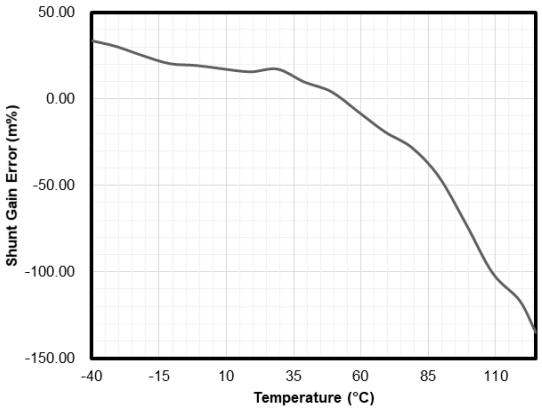


Figure 7.

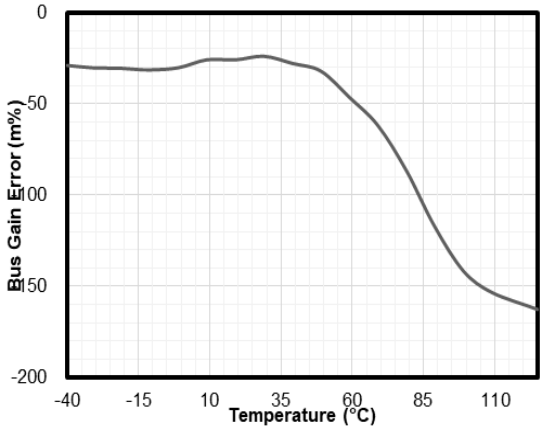


Figure 8.

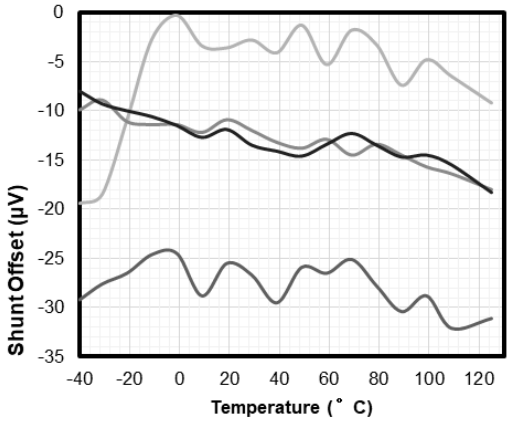


Figure 9.

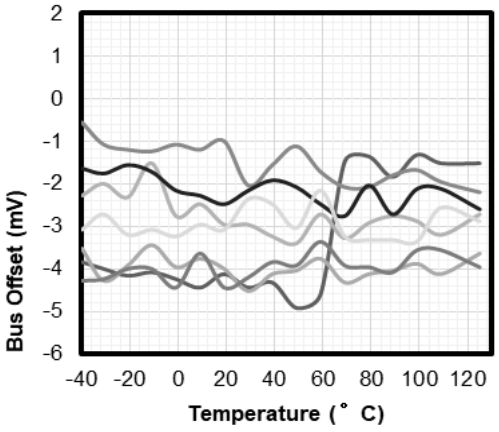


Figure 10.

Detailed Description

Overview

The TPA620 is a digital current sense amplifier with an I²C- and SMBus-compatible interface. It performs two measurements on the power-supply bus: The differential shunt voltage created by load current flowing through a shunt resistor is measured at the IN+ and IN– pins. The power supply bus voltage is measured at the VBUS pin.

Serial Bus Interface

TPA620 has two I²C address pins, A0 and A1. 16 addresses are available by connecting A0 and A1 to different logic levels. At the beginning of I²C communication, the states of A0 and A1 are sampled by the chip to set the I²C address. Following is the address table:

Table 2. I²C Address Table

A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	VS	1000001
GND	SDA	1000010
GND	SCL	1000011
VS	GND	1000100
VS	VS	1000101
VS	SDA	1000110
VS	SCL	1000111
SDA	GND	1001000
SDA	VS	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	VS	1001101
SCL	SDA	1001110
SCL	SCL	1001111

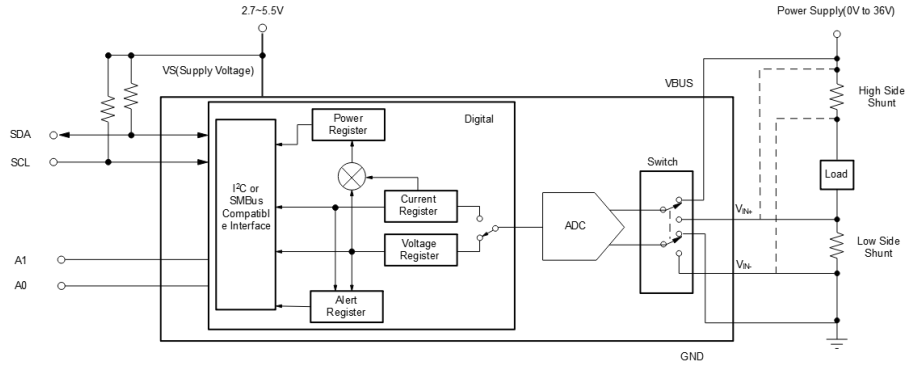
Register Maps

Table 3. Register Map

Pointer Address	Register Name	Function	Power On Reset		Type(1)
Hex			Binary	Hex	
00	Configuration	All-register reset, settings for bus voltage range, PGA gain, ADC resolution/ averaging.	00111001 10011111	399F	R/W
01	Shunt voltage	Shunt voltage measurement data.	Shunt voltage	—	R
02	Bus voltage	Bus voltage measurement data.	Bus voltage	—	R
03	Power (2)	Power measurement data.	00000000 00000000	0000	R
04	Current (2)	Contains the value of the current flowing through the shunt resistor.	00000000 00000000	0000	R
05	Calibration	Sets full-scale range and LSB of current and power measurements. Overall system calibration.	00000000 00000000	0000	R/W

(1) Values based on a statistical analysis of a one-time sample of devices. Minimum and maximum values are not ensured and not production tested. Condition: A0 = A1 = 0.
(2) Type: R = Read only, R/W = Read/Write.
(3) The Power register and Current register default to 0 because the Calibration register defaults to 0, yielding a zero current value until the Calibration register is programmed.

Functional Block Diagram



Feature Description

All TPA620 registers 16-bit registers are two 8-bit bytes through the I2C- or SMBUS-compatible interface.

Configuration Register (address = 00h) [reset = 399Fh]

Table 4. Configuration Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST	—	BRNG	PG1	PG0	BADC4	BADC3	BADC2	BADC1	SADC4	SADC3	SADC2	SADC1	MODE3	MODE2	MODE1
R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

(1) R/W = Read/Write; R = Read only; -n = value after reset.
(2) When an ADC measurement process is running, writing to this register will interrupt the current process and restart ADC measurement with the latest register configuration.

RST:	**Reset Bit**
Bit 15	Setting this bit to 1 generates a system reset that is the same as power-on reset. Resets all registers to default values;
	this bit self-clears.
BRNG:	**Bus Voltage Range**
Bit 13	0 = 16-V FSR
	1 = 32-V FSR (default value)
PG:	**PGA (Shunt Voltage Only)**
Bits 11, 12	Sets PGA gain and range. Note that the PGA defaults to /8 (320-mV range). Table 3 shows the gain and range for the various product gain settings.

Table 5. Bit Settings [12:11] (1)

PG1	PG0	GAIN	RANGE
0	0	1	±40 mV
0	1	/2	±80 mV
1	0	/4	±160 mV
1	1	/8	±320 mV

(1) Shaded values are default.

BADC:	BADC Bus ADC Resolution/Averaging
Bits 7–10:	These bits adjust the Bus ADC resolution (9-, 10-, 11-, or 12-bit) or set the number of samples used when averaging results for the Bus Voltage Register (02h).
SADC:	**SADC Shunt ADC Resolution/Averaging**
Bits 3–6	These bits adjust the Shunt ADC resolution (9-, 10-, 11-, or 12-bit) or set the number of samples used when averaging results for the Shunt Voltage Register (01h).
	BADC (Bus) and SADC (Shunt) ADC resolution/averaging, and conversion time settings are shown in Table 4.

Table 6. ADC Settings (SADC [6:3], BADC [10:7])(1)

ADC4	ADC3	ADC2	ADC1	Mode/Samples	Conversion Time
0	X (2)	0	0	9-bit	66 μs
0	X (2)	0	1	10-bit	134 μs
0	X (2)	1	0	11-bit	269 μs
0	X (2)	1	1	12-bit	542 μs
1	0	0	0	12-bit	542 μs
1	0	0	1	2	1.08 mS
1	0	1	0	4	2.17 mS
1	0	1	1	8	4.34 mS
1	1	0	0	16	8.67 mS
1	1	0	1	32	17.3 mS
1	1	1	0	64	34.7 mS
1	1	1	1	128	69.4 mS

(1) Shaded values are default.
(2) X = Don't care.

MODE	Operating Mode
Bits 0-2	Selects continuous, triggered, or power-down mode of operation. These bits default to continuous shunt and bus measurement mode. The mode settings are shown in Table 5.

Table 7. Mode Settings [2:0] (1)

MODE3	MODE2	MODE1	MODE
0	0	0	Power-down
0	0	1	Shunt voltage, triggered
0	1	0	Bus voltage, triggered
0	1	1	Shunt and bus, triggered
1	0	0	ADC off (disabled)
1	0	1	Shunt voltage, continuous
1	1	0	Bus voltage, continuous
1	1	1	Shunt and bus, continuous

(1) Shaded values are default.

Data Output Registers

Shunt Voltage Register (address = 01h)

The Shunt Voltage register stores the current shunt voltage reading, V_{SHUNT}. Shunt Voltage register bits are shifted according to the PGA setting selected in the Configuration register (00h). When multiple sign bits are present, they are all the same value. Negative numbers are represented in 2's complement format. Generate the 2's complement of a negative number by complementing the absolute value binary number and adding 1. Extend the sign, denoting a negative number by setting the MSB = 1. Extend the sign to any additional sign bits to form the 16-bit word.

At PGA = /8, full-scale range = ±320 mV (decimal = 32000). For V_{SHUNT}= +320 mV, Value = 7D00h; For V_{SHUNT} = –320 mV, Value =8300h; and LSB = 10 μV.

Table 8. Shunt Voltage Register at PGA = /8

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN	SD14_8	SD13_8	SD12_8	SD11_8	SD10_8	SD9_8	SD8_8	SD7_8	SD6_8	SD5_8	SD4_8	SD3_8	SD2_8	SD1_8	SD0_8

At PGA = /4, full-scale range = ±160 mV (decimal = 16000). For V_{SHUNT} = +160 mV, Value = 3E80h; For V_{SHUNT} = –160 mV, Value = C180h; and LSB = 10 μV

Table 9. Shunt Voltage Register at PGA = /4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN	SIGN	SD13_4	SD12_4	SD11_4	SD10_4	SD9_4	SD8_4	SD7_4	SD6_4	SD5_4	SD4_4	SD3_4	SD2_4	SD1_4	SD0_4

At PGA = /2, full-scale range = ±80 mV (decimal = 8000). For V_{SHUNT} = +80 mV, Value = 1F40h; For V_{SHUNT} = –80 mV, Value = E0C0h; and LSB = 10 μV.

Table 10. Shunt Voltage Register at PGA = /2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN	SIGN	SIGN	SD12_2	SD11_2	SD10_2	SD9_2	SD8_2	SD7_2	SD6_2	SD5_2	SD4_2	SD3_2	SD2_2	SD1_2	SD0_2

At PGA = /1, full-scale range = ±40 mV (decimal = 4000). For V_{SHUNT}= +40 mV, Value = 0FA0h; For V_{SHUNT} = –40 mV, Value = F060h; and LSB = 10 μV.

Table 11. Shunt Voltage Register at PGA = /1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN	SIGN	SIGN	SIGN	SD11_1	SD10_1	SD9_1	SD8_1	SD7_1	SD6_1	SD5_1	SD4_1	SD3_1	SD2_1	SD1_1	SD0_1

Shunt Voltage Register Format (1)

V_{SHUNT}Reading (mV)	Decimal Value	PGA = /8 (D15:D0)	PGA = /4 (D15:D0)	PGA = /2 (D15:D0)	PGA = /1 (D15:D0)
320.02	32002	0111 1101 0000 0000	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
320.01	32001	0111 1101 0000 0000	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
320.00	32000	0111 1101 0000 0000	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
319.99	31999	0111 1100 1111 1111	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
319.98	31998	0111 1100 1111 1110	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
⋮	⋮	⋮	⋮	⋮	⋮
160.02	16002	0011 1110 1000 0010	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
160.01	16001	0011 1110 1000 0001	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
160.00	16000	0011 1110 1000 0000	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
159.99	15999	0011 1110 0111 1111	0011 1110 0111 1111	0001 1111 0100 0000	0000 1111 1010 0000

V_{SHUNT}Reading (mV)	Decimal Value	PGA = /8 (D15:D0)	PGA = /4 (D15:D0)	PGA = /2 (D15:D0)	PGA = /1 (D15:D0)
159.98	15998	0011 1110 0111 1110	0011 1110 0111 1110	0001 1111 0100 0000	0000 1111 1010 0000
⋮	⋮	⋮	⋮	⋮	⋮
80.02	8002	0001 1111 0100 0010	0001 1111 0100 0010	0001 1111 0100 0000	0000 1111 1010 0000
80.01	8001	0001 1111 0100 0001	0001 1111 0100 0001	0001 1111 0100 0000	0000 1111 1010 0000
80.00	8000	0001 1111 0100 0000	0001 1111 0100 0000	0001 1111 0100 0000	0000 1111 1010 0000
79.99	7999	0001 1111 0011 1111	0001 1111 0011 1111	0001 1111 0011 1111	0000 1111 1010 0000
79.98	7998	0001 1111 0011 1110	0001 1111 0011 1110	0001 1111 0011 1110	0000 1111 1010 0000
⋮	⋮	⋮	⋮	⋮	⋮
40.02	4002	0000 1111 1010 0010	0000 1111 1010 0010	0000 1111 1010 0010	0000 1111 1010 0000
40.01	4001	0000 1111 1010 0001	0000 1111 1010 0001	0000 1111 1010 0001	0000 1111 1010 0000
40.00	4000	0000 1111 1010 0000	0000 1111 1010 0000	0000 1111 1010 0000	0000 1111 1010 0000
39.99	3999	0000 1111 1001 1111	0000 1111 1001 1111	0000 1111 1001 1111	0000 1111 1001 1111
39.98	3998	0000 1111 1001 1110	0000 1111 1001 1110	0000 1111 1001 1110	0000 1111 1001 1110
⋮	⋮	⋮	⋮	⋮	⋮
0.02	2	0000 0000 0000 0010	0000 0000 0000 0010	0000 0000 0000 0010	0000 0000 0000 0010
0.01	1	0000 0000 0000 0001	0000 0000 0000 0001	0000 0000 0000 0001	0000 0000 0000 0001
0	0	0000 0000 0000 0000	0000 0000 0000 0000	0000 0000 0000 0000	0000 0000 0000 0000
–0.01	–1	1111 1111 1111 1111	1111 1111 1111 1111	1111 1111 1111 1111	1111 1111 1111 1111
–0.02	–2	1111 1111 1111 1110	1111 1111 1111 1110	1111 1111 1111 1110	1111 1111 1111 1110
⋮	⋮	⋮	⋮	⋮	⋮
–39.98	–3998	1111 0000 0110 0010	1111 0000 0110 0010	1111 0000 0110 0010	1111 0000 0110 0010
–39.99	–3999	1111 0000 0110 0001	1111 0000 0110 0001	1111 0000 0110 0001	1111 0000 0110 0001

V_{SHUNT}Reading (mV)	Decimal Value	PGA = /8 (D15:D0)	PGA = /4 (D15:D0)	PGA = /2 (D15:D0)	PGA = /1 (D15:D0)
–40.00	–4000	1111 0000 0110 0000	1111 0000 0110 0000	1111 0000 0110 0000	1111 0000 0110 0000
–40.01	–4001	1111 0000 0101 1111	1111 0000 0101 1111	1111 0000 0101 1111	1111 0000 0110 0000
–40.02	–4002	1111 0000 0101 1110	1111 0000 0101 1110	1111 0000 0101 1110	1111 0000 0110 0000
⋮	⋮	⋮	⋮	⋮	⋮
–79.98	–7998	1110 0000 1100 0010	1110 0000 1100 0010	1110 0000 1100 0010	1111 0000 0110 0000
–79.99	–7999	1110 0000 1100 0001	1110 0000 1100 0001	1110 0000 1100 0001	1111 0000 0110 0000
–80.00	–8000	1110 0000 1100 0000	1110 0000 1100 0000	1110 0000 1100 0000	1111 0000 0110 0000
–80.01	–8001	1110 0000 1011 1111	1110 0000 1011 1111	1110 0000 1100 0000	1111 0000 0110 0000
–80.02	–8002	1110 0000 1011 1110	1110 0000 1011 1110	1110 0000 1100 0000	1111 0000 0110 0000
⋮	⋮	⋮	⋮	⋮	⋮
–159.98	–15998	1100 0001 1000 0010	1100 0001 1000 0010	1110 0000 1100 0000	1111 0000 0110 0000
–159.99	–15999	1100 0001 1000 0001	1100 0001 1000 0001	1110 0000 1100 0000	1111 0000 0110 0000
–160.00	–16000	1100 0001 1000 0000	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–160.01	–16001	1100 0001 0111 1111	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–160.02	–16002	1100 0001 0111 1110	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
⋮	⋮	⋮	⋮	⋮	⋮
–319.98	–31998	1000 0011 0000 0010	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–319.99	–31999	1000 0011 0000 0001	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–320.00	–32000	1000 0011 0000 0000	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–320.01	–32001	1000 0011 0000 0000	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–320.02	–32002	1000 0011 0000 0000	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000

(1) Out-of-range values are shown in gray shading.

Bus Voltage Register (address = 02h)

The Bus Voltage register stores the most recent bus voltage reading, VBUS.

At full-scale range = 32 V (decimal = 8000, hex = 1F40), and LSB = 4 mV.

Table 12. Bus Voltage Register (BRNG = 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BD12	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	—	CNVR	OVF

At full-scale range = 16 V (decimal = 4000, hex = 0FA0), and LSB = 4 mV.

Table 13. Bus Voltage Register (BRNG = 0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	—	CNVR	OVF

CNVR:	**Conversion Ready**
Bit 1	Although the data from the last conversion can be read at any time, the TPA620 Conversion Ready bit (CNVR) indicates when data from a conversion is available in the data output registers. The CNVR bit is set after all conversions, averaging, and multiplications are complete. CNVR will clear under the following conditions: 1. Writing a new mode into the Operating Mode bits in the Configuration Register (except for Power-Down or Disable). 2. Reading the Bus Voltage Register.
OVF:	**Math Overflow Flag**
Bit 0	The Math Overflow Flag (OVF) is set when the Power or Current calculations are out of range. It indicates that current and power data may be meaningless.

Power Register (address = 03h) [reset = 00h]

Full-scale range and LSB are set by the Calibration register. The Power register records power in watts by multiplying the values of the current with the value of the bus voltage.

Table 14. Power Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

(1) LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

Current Register (address = 04h) [reset =00h]

Full-scale range and LSB depend on the value entered in the Calibration register. Negative values are stored in 2's complement format.

Table 15. Current Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSIGN	CD14	CD13	CD12	CD11	CD10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

(1) LEGEND: R/W = Read/Write; R = Read only; -n = value after reset.

Calibration Register

The value of the Current register is calculated by multiplying the value in the Shunt Voltage register with the value in the calibration register.

Calibration Register (address = 05h) [reset = 00h]

Current and power calibrations are set by bits FS15 to FS1 of the Calibration register. Note that bit FS0 is not used in the calculation. This register sets the current that corresponds to a full-scale drop across the shunt. Full- scale range and the LSB of the current and power measurement depend on the value entered in this register. This register is suitable for use in overall system calibration. Note that the 0 POR values are all default.

Table 16. Calibration Register (1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FS15	FS14	FS13	FS12	FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

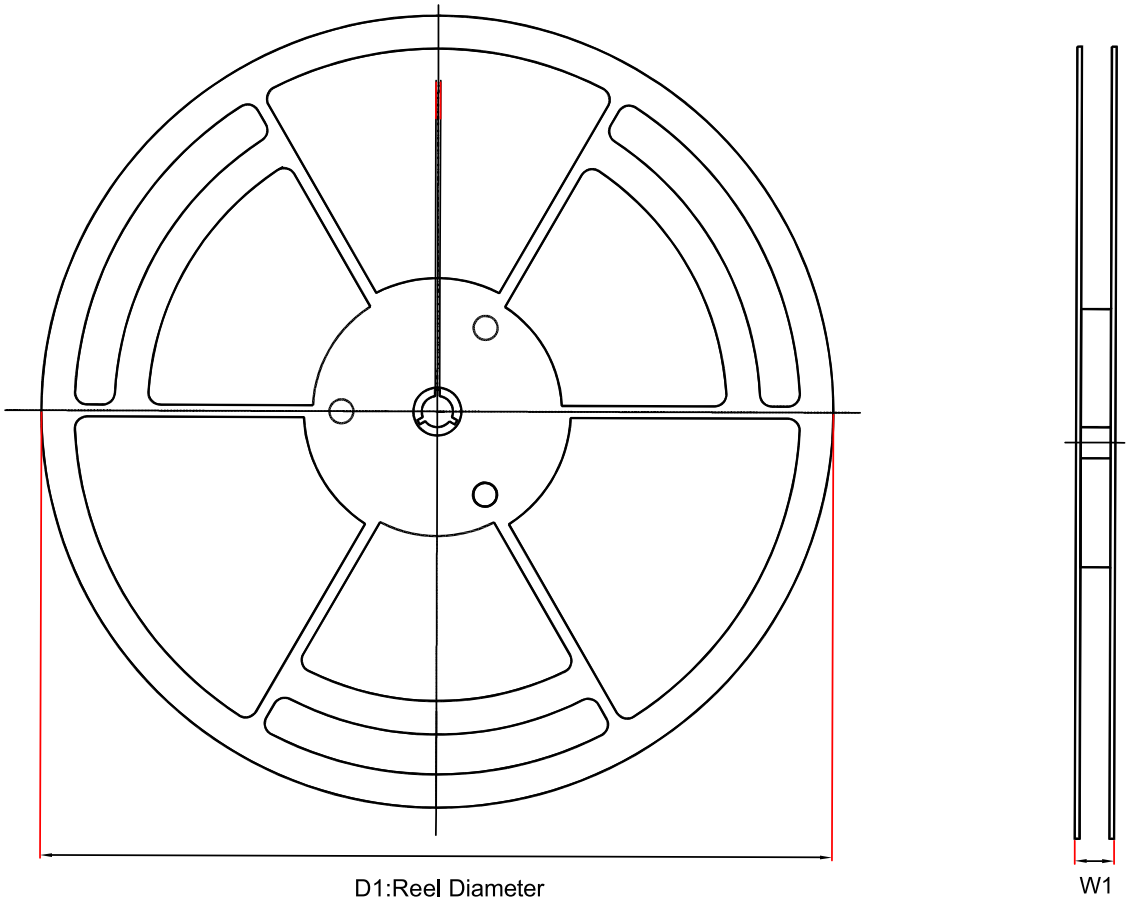
(1) FS0 is a void bit and will always be 0. It is not possible to write a 1 to FS0. CALIBRATION is the value stored in FS15 : FS1.

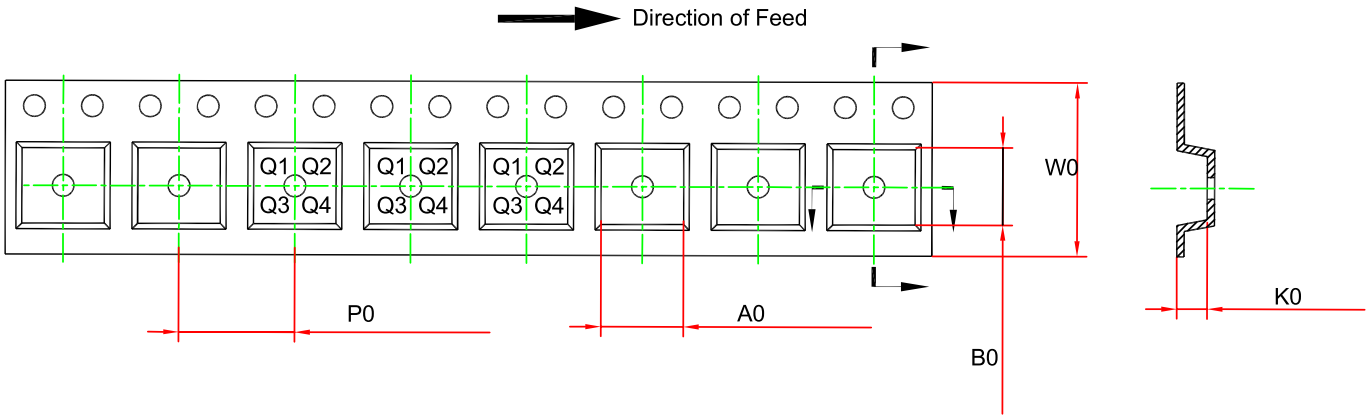
The device could not accept stop command immediately after a start operation. If customer wants to reset I2C communication, 9 clocks could be sent to the device after a start operation, to make sure the device quite to default mode, and then wait for a new I2C start operation.

SMBUS alert function is supported respond to the SMBus Alert Response address (0001 100) when an alert occurs. But be aware when master is accessing the address if the device doesn't has alert, the device will still acknowledge to address but without following response.

I^2C Data hold time should be at least 10nS for a proper start function is recognized.

Tape and Reel Information



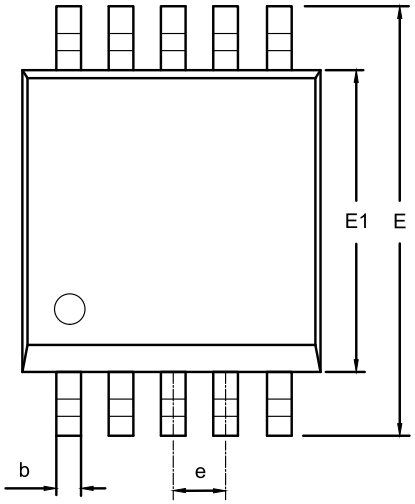


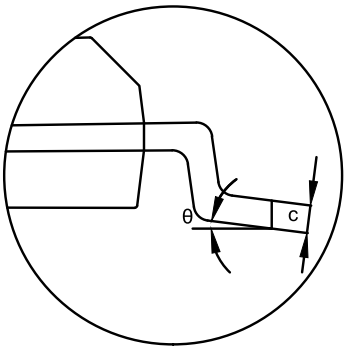
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPA620-VR-S	MSOP10	330	17.6	5.3	3.3	1.6	8	12	Q1

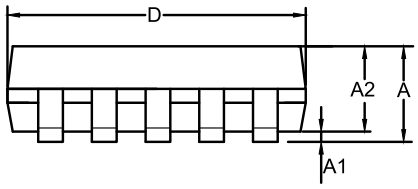
Package Outline Dimensions

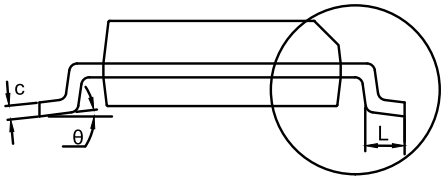
MSOP10

Package Outline Dimensions VS2(MSOP-10-A)









Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	1.100	0.031	0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	4.700	5.100	0.185	0.201
E1	2.900	3.100	0.114	0.122
e	0.500 BSC		0.020 BSC	
L	0.400	0.800	0.016	0.031
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPA620-VR-S	−40 to 125°C	MSOP10	TPA620	1	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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