800mA Very High PSRR Low-Dropout Linear Regulator

Description

LX8240 is a low-dropout regulator offering the highest Power Supply Rejection Ratio (PSRR), higher than 48 dB over all frequency up to 100kHz, and higher than 32 dB over all frequency up to 1MHz for LDO devices supplying 800mA of output current. LX8240 also requires very low quiescent current. It has separate Bias and Input supply rails to improve efficiency and minimize power dissipation. The V_{BIAS} input includes a voltage compliance range from 2.7V to 5.5V, and the V_{IN} supply range is 1.2V to 4.2V. The output voltage is programmed by an external resistor divider utilizing the 0.5V reference feedback (FB) pin allowing output voltages as low as 1V.

LX8240 is an ideal selection for battery-powered systems where the low quiescent current cannot be compromised. It is also guaranteed to be the stable even with only a 1µF ceramic capacitor.

To protect the device the LX8240 aso includes internal thermal shutdown, and overcurrent limit features.

Features

- High PSRR, higher than 48 dB over all frequency up to 100kHz
- High PSRR, higher than 32 dB over all frequency up to 1MHz
- +/-2% Accuracy over Temp, Supply and Load
- Adjustable Output (0.5V reference)
- Over Current Limit
- Thermal Protection

Applications

- Low Power Mobile Devices
- Portable Devices
- Post Processing for a Switching Regulator

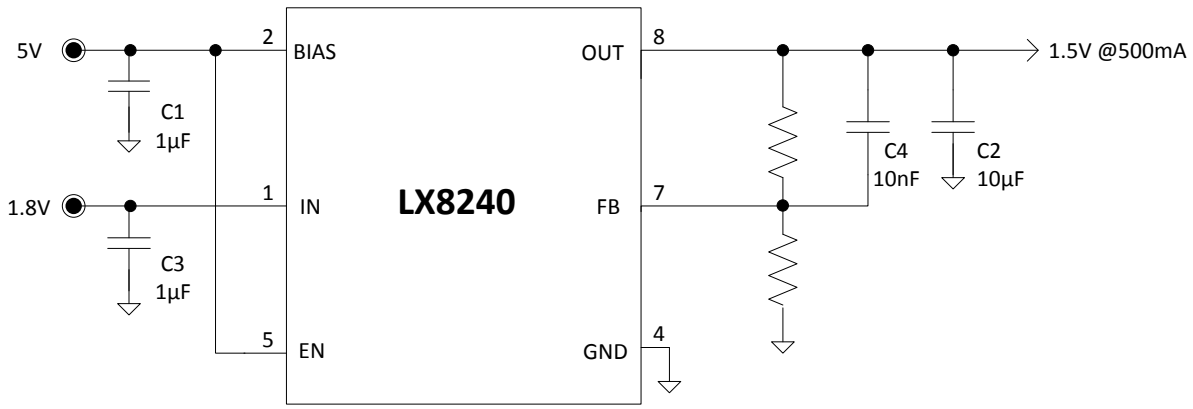

Figure 1 · **Typical Application of LX8240**

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Pin Configuration and Pinout

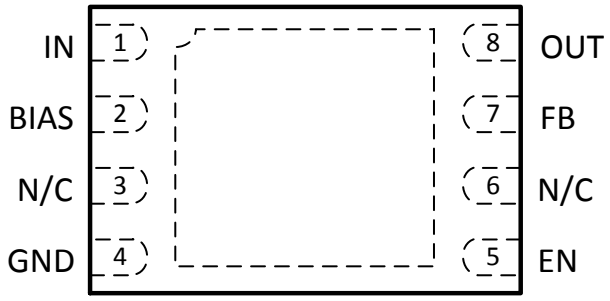


Figure 2 · **Pinout WDFN 3mm x 2mm 8L Top View**

Marking: Line 1 8240
Line 2 Date / Lot Code
Line 3 * MSC (*Pin 1 identifier)

Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type
-40°C to 85°C	RoHS Compliant, Pb-free	WDFN 3mm x 2mm 8L	LX8240ILD	Bulk / Tube
			LX8240ILD-TR	Tape and Reel

Pin Description

Pin Number	Pin Designator	Description
1	IN	Power Source Input. Bypass IN to GND with a 1µF or greater capacitor.
2	BIAS	Bias Voltage. Bypass to GND with a 1µF capacitor or greater.
3, 6	NC	No Connect.
4	GND	Ground.
5	EN	Enable Input. Drive EN high to turn on, drive EN low to turn it off. For automatic startup, connect EN to Bias.
7	FB	Feedback Input. Connect a resistive voltage divider from OUT to FB to set the output voltage. OUT feedback threshold is 0.5V.
8	OUT	Regulator Output. OUT is the output of the linear regulator. Bypass OUT to GND with a 1µF or greater capacitor.

Block Diagram

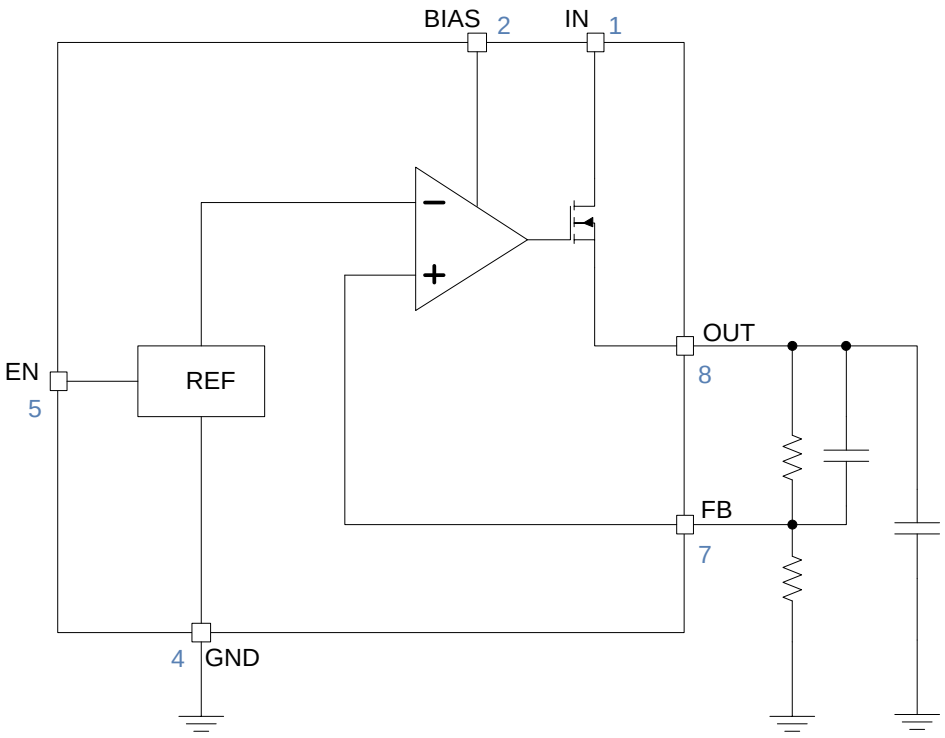


Figure 3 · **Simplified Block Diagram of LX8240**

Absolute Maximum Ratings

Parameter		Min	Max	Units
IN to GND		-0.3	7	V
BIAS to GND		-0.3	< V_{EN}	
EN, FB to GND		-0.3	7	V
OUT to GND		-0.3	7	V
Junction Temperature		-40	150	°C
Storage Temperature		-65	150	°C
Peak Solder Reflow Temperature (40 seconds)			260 (+0,-5)	°C
ESD Rating	HBM		5000	V
	CDM		2000	V

Note: Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage, or negatively impact long-term operating reliability

Operating Ratings

	Min	Max	Units
IN	1.2	4.2	V
BIAS	2.7	5.5	V
Output Voltage	1	4	V
Output Current	0	800	mA
Ambient Temperature	-40	85	°C

Note: Performance is generally guaranteed over this range as further detailed below under Electrical Characteristics.

Thermal Properties

Thermal Resistance	Typ	Units
θ_{JA}	55	°C/W
θ_{JC}	12	°C/W

Note: The θ_{JX} numbers assume no forced airflow. Junction Temperature is calculated using $T_J = T_A + (PD \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

Electrical Characteristics

Note: The following specifications apply over the operating ambient temperature of -40°C ≤ T_A ≤ 85°C except where otherwise noted with the following test conditions: V_{IN} = 1.8V,V_{BIAS} = 5.0V, V_{OUT} = 1.5V, C1 = C3 = 1µF and C2 = 10µF at T_A = 25°C.

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
V_{BIAS}	Bias Voltage Range	$V_{BIAS} > V_{IN}$ + 1.3V	2.7		5.5	V
V_{IN}	Input Voltage Range	$V_{IN} < V_{BIAS}$ - 1.3V, $V_{IN} < V_{OUT}$ + 0.9V @ I_{OUT} = 800mA	1.2		4.2	V
		$V_{IN} < V_{BIAS}$ - 1.3V, $V_{IN} < V_{OUT}$ + (0.727 / I_{OUT})V @ V_{OUT} = 1.5V, (Note 3)	1.2		4.2	V
I_{BIAS}	Bias Current	I_{OUT} = 10µA, V_{OUT} = 1.5V			200	µA
I_{IN}	Input Current	I_{OUT} = 0µA, V_{OUT} = 1.5V			20	µA
I_{FB}	FB Biasing Current	V_{FB} = 0.5V, T_A = 25°C	-0.5		0.5	µA
		V_{FB} = 0.5V, T_A = 85°C (Note 1)		0		µA
V_{REF}	FB Reference Voltage	I_{OUT} = 1mA to 800mA	0.49	0.5	0.51	V
		-40°C ≤ T_A ≤ 85°C	0.49	0.5	0.51	
V_{DO}	Dropout Voltage	V_{BIAS} = 4.75V, V_{OUT} = 1.5V, I_{OUT} = 800mA, V_{IN} = sweep, (Note 2)			200	mV
V_{OUT}	Output Voltage		1		4	V

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
	V_{BIAS} Line Regulation	I_{OUT} = 100mA, V_{IN} = 1.8V, V_{OUT} = 1.5V, V_{BIAS} = 3.1V to 5.5V $\frac{V_{OUT}(V_{BIAS}=5.5V)-V_{OUT}(V_{BIAS}=3.1V)}{V_{OUT}(V_{BIAS}=5V)\times(5.5V-3.1V)}\times 100\%$		0.07	0.4	%/V
	V_{IN} Line Regulation	I_{OUT} = 1mA, V_{BIAS} = 5V, V_{OUT} = 1.5V, V_{IN} = 1.7V to 4.2V $\frac{V_{OUT}(V_{IN}=4.2V)-V_{OUT}(V_{IN}=1.7V)}{V_{OUT}(V_{IN}=1.8V)\times(4.2V-1.7V)}\times 100\%$		0.002	0.02	%/V
	Load Regulation	I_{OUT} = 1mA to 800mA		0.0005		%/mA
PSRR	V_{BIAS} PSRR	V_{IN} > V_{OUT} + 0.2V, C2 = 10µF, V_{BIAS}(AC) = 100mV, f = 1kHz, I_{LOAD} = 100mA, (Note 1)		55		dB
		V_{IN} > V_{OUT} + 0.2V, C2 = 10µF, V_{BIAS}(AC) = 100mV, f = 1MHz, I_{LOAD} = 100mA (Note 1)		33		
PSRR	V_{IN} PSRR	V_{BIAS} > V_{OUT} + 1.3V, C2 = 10µF, V_{IN}(AC) = 100mV, f = 1kHz, I_{LOAD} = 100mA, (Note 1)		59		dB
		V_{BIAS} > V_{OUT} + 1.3V, C2 = 10µF, V_{IN}(AC) = 100mV, f = 1MHz, I_{LOAD} =100mA (Note 1)		33		
I_{CL}	Output Current Limit		850			mA
I_Q	Quiescent Ground Current	EN = GND		0.1	2	µA
		1.3V < EN ≤ V_{BIAS}, I_{LOAD} = 500mA		150	200	µA
	V_{OUT} Undershoot Over Step Load Transient	Load step from 20mA to 450mA with rising time of 100ns (Note 1)		33		mV
	V_{OUT} Overshoot Over Step Load Transient	Load step from 450mA to 20mA with falling time of 600ns (Note 1)		23		mV
	EN Input High Voltage		1.3			V
	EN Input Low Voltage				0.4	V
	EN Input Bias Current	V_{EN} = 1.2V	-1		1	µA
$T_{THERMAL}$	Thermal Protection Threshold	Rising (Note 1)		155		°C
		Falling (Note 1)		125		°C

Note: 1. Guaranteed by Design

Note: 2. Dropout is defined as V_{IN} - V_{OUT_LDO} when V_{OUT_LDO} is 98% of the value of V_{OUT_LDO} for V_{IN} = V_{OUT}(V_{IN} = 1.8V, V_{BIAS} = 5V, I_{OUT} = 800mA)

Note: 3. 0.727 is the maximum allowed power before thermal shutdown.

Typical Performance Curves -- (V_{OUT} = 1.5V)

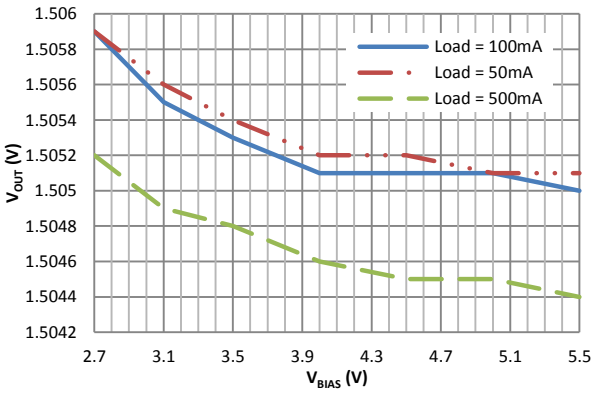


Figure 4 · **V_{BIAS} Line Regulation, V_{IN} = 1.8V**

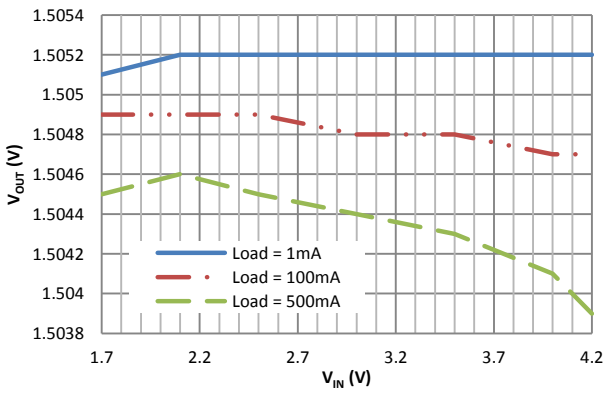


Figure 5 · **V_{IN} Line Regulation, V_{BIAS} = 5V**

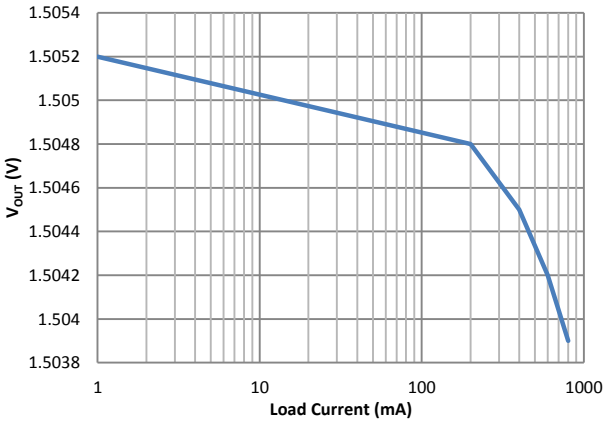


Figure 6 · **Load Regulation, V_{IN} = 1.8V, V_{BIAS} = 5V**

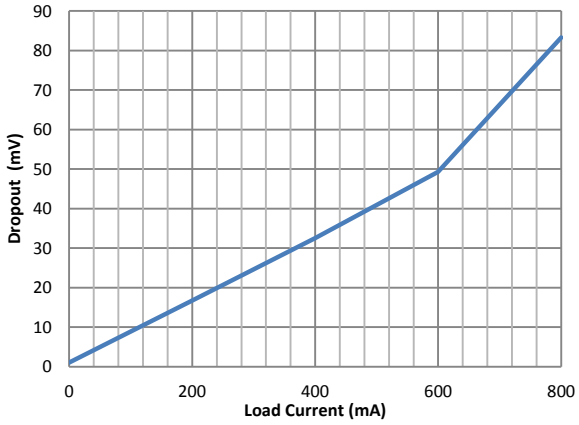


Figure 7 · **Voltage Dropout, V_{IN} = 1.8V, V_{BIAS} = 4.75V**

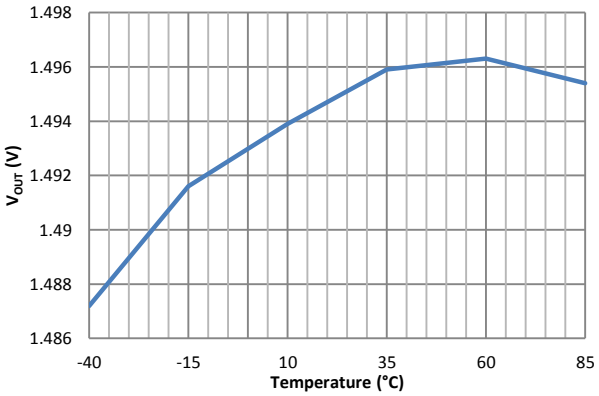


Figure 8 · **Output Voltage vs. Temperature**

V_{IN} = 1.8V, V_{BIAS} = 4.75V, I_{Load} = 300mA

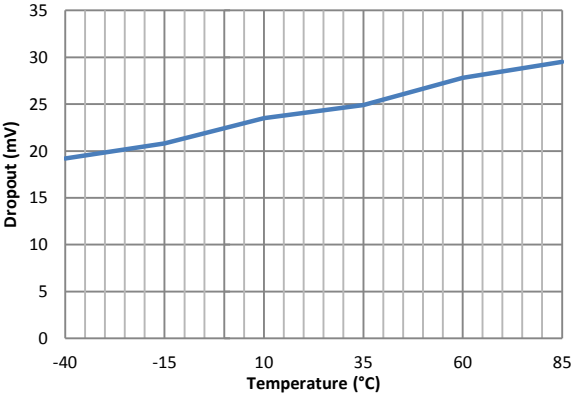


Figure 9 · **Voltage Dropout vs. Temperature**

V_{IN} = 1.8V, V_{BIAS} = 4.75V, I_{Load} = 300mA

Typical Performance Curves -- (V_{OUT} = 1.5V)

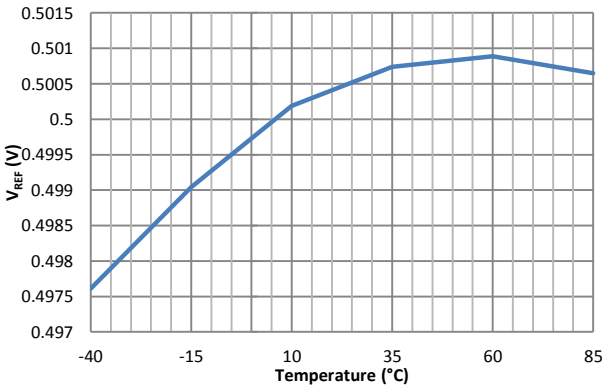


Figure 10 · **Reference Voltage vs. Temperature**

V_{IN} = 1.8V, V_{BIAS} = 4.75V, I_{Load} = 300mA

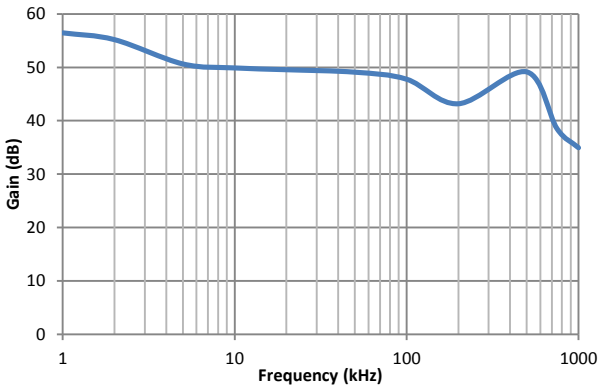


Figure 11 · **V_{BIAS} to V_{OUT} PSRR**

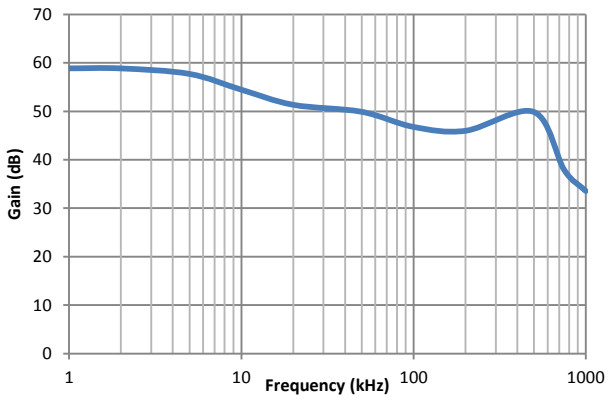


Figure 12 · **V_{IN} to V_{OUT} PSRR**

Typical Performance Curves -- (Start Up & Shut Down, V_{OUT} = 1.5V)

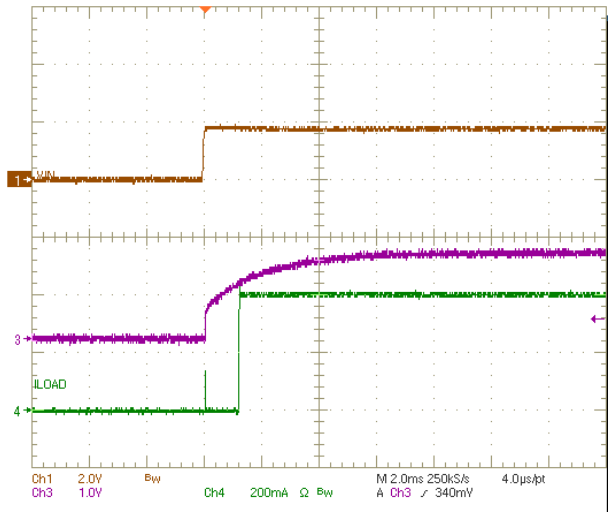


Figure 13 · **Power Up with 400mA Load Current**

V_{IN} = 1.8V, V_{BIAS} = 5V

CH1: V_{IN}, CH3: V_{OUT}, CH4: Load Current

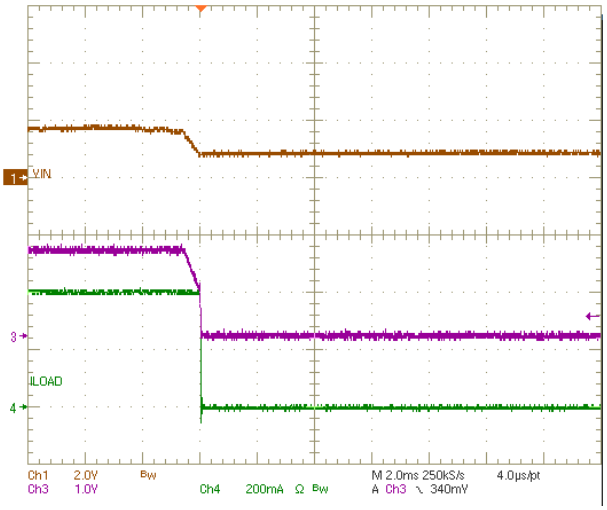


Figure 14 · **Power Down with 400mA Load Current**

V_{IN} = 1.8V, V_{BIAS} = 5V

CH1: V_{IN}, CH3: V_{OUT}, CH4: Load Current

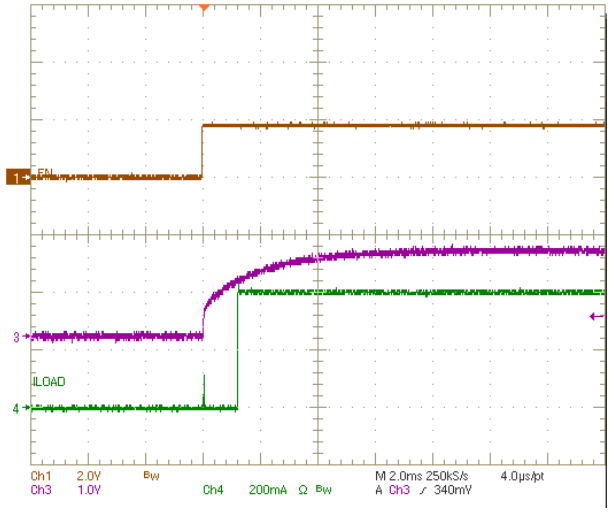


Figure 15 · **Enable Up with 400mA Load Current**

V_{IN} = 1.8V, V_{BIAS} = 5V

CH1: V_{IN}, CH3: V_{OUT}, CH4: Load Current

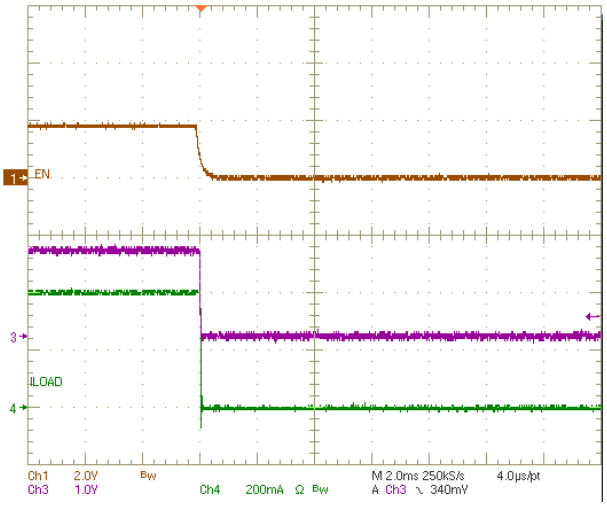


Figure 16 · **Enable Down with 400mA Load Current**

V_{IN} = 1.8V, V_{BIAS} = 5V

CH1: V_{IN}, CH3: V_{OUT}, CH4: Load Current

Typical Performance Curves -- (Step Response & Over Current Limit)

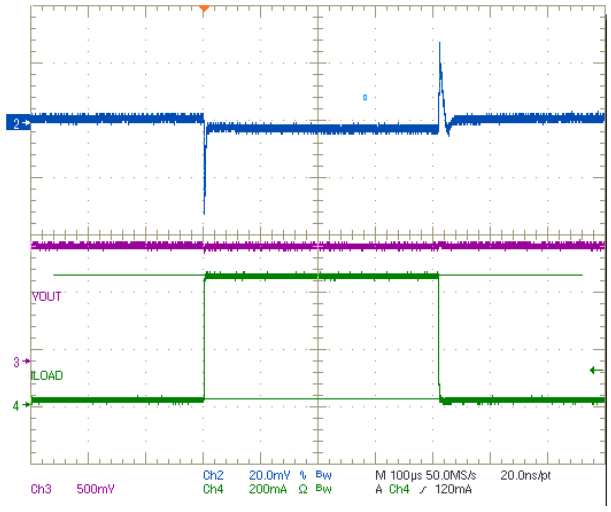


Figure 17 · **Dynamic Response, I_{Load} = 20mA to 450mA**

V_{IN} = 1.2V, V_{BIAS} = 2.7V, V_{OUT} = 1V
CH2: V_{OUT} AC, CH3: V_{OUT} DC,
CH4: Load Current

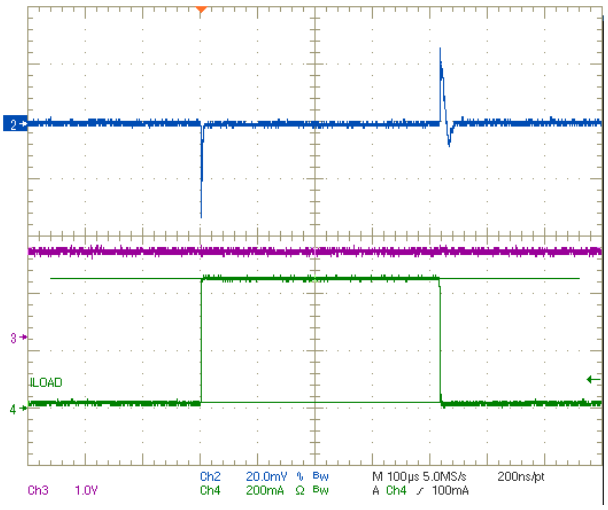


Figure 18 · **Dynamic Response, I_{Load} = 20mA to 450mA**

V_{IN} = 1.8V, V_{BIAS} = 5V, V_{OUT} = 1.5V
CH2: V_{OUT} AC, CH3: V_{OUT} DC,
CH4: Load Current

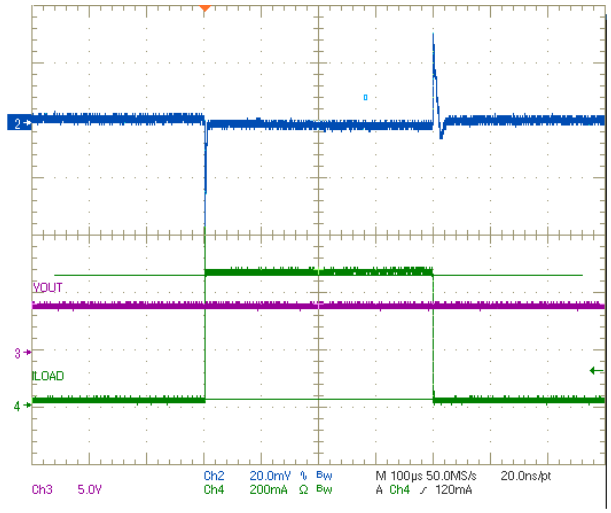


Figure 19 · **Dynamic Response, I_{Load} = 20mA to 450mA**

V_{IN} = 4.2V, V_{BIAS} = 5.5V, V_{OUT} = 4V
CH2: V_{OUT} AC, CH3: V_{OUT} DC,
CH4: Load Current

Theory of Operation / Application Information

BIAS pin operation

The IC uses a BIAS pin to allow low R_{DSON}. V_{BIAS} needs to be higher than V_{IN} by 1.3V to provide circuit headroom since there is no internal charge pump. The V_{BIAS} all insures the high V_{IN} – to - V_{OUT} PSRR, and the low noise performance is achieved with this topology at lower cost.

Adaptive PSRR compensation

LX8240 has internal adaptive feedforward control. A typical feedforward design depends on the zero from the external feedforward capacitance, C4 in Figure 20. In LX8240, the internal adaptive feedforward control circuit has an automatic pole compensator to allow different frequency inputs to experience a different zero frequency. This is equivalent to pole-zero pair in the control loop. This method allows LX8240 to maintain high gain over a very wide frequency range. Furthermore, it helps LX8240 sustain PSRR higher than 32dB over the entire frequency range up to 1MHz.

Setting the output Voltage

A typical LX8240 application circuit is shown in Figure 19. External component selection is driven by the load requirement. The LX8240 develops a 0.5V reference voltage between the feedback pin and the ground. The output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 0.5 \times \left(1 + \frac{R1}{R2}\right)$$

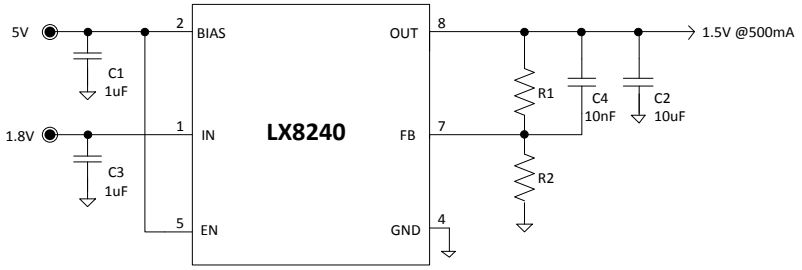
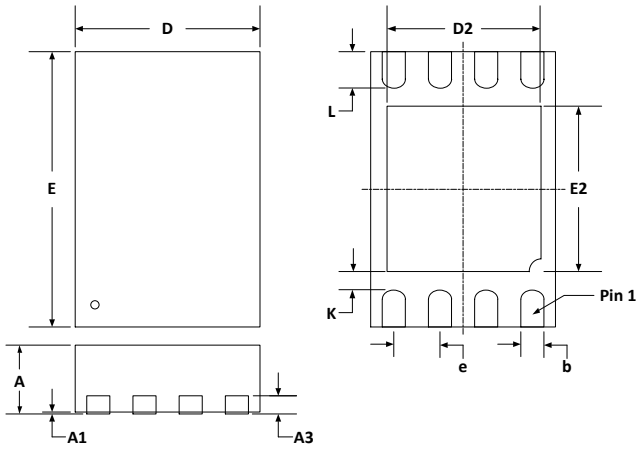


Figure 20 · **Typical Application**

PACKAGE OUTLINE DIMENSIONS



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.70	0.80	0.028	0.032
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008	
D	2.00 BSC		0.079 BSC	
D2	1.50	1.75	0.059	0.030
b	0.18	0.30	0.007	0.012
E	3.00 BSC		0.118 BSC	
E2	1.65	1.90	0.065	0.075
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.002
K	0.20		0.008	

Figure 21 · **LD 8-Pin WDFN Package Dimensions**

Note: 1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm (.006”) on any side. Lead dimension shall not include solder coverage.

Note: 2. Dimensions are in mm, inches are for reference only.

LAND PATTERN RECOMMENDATION

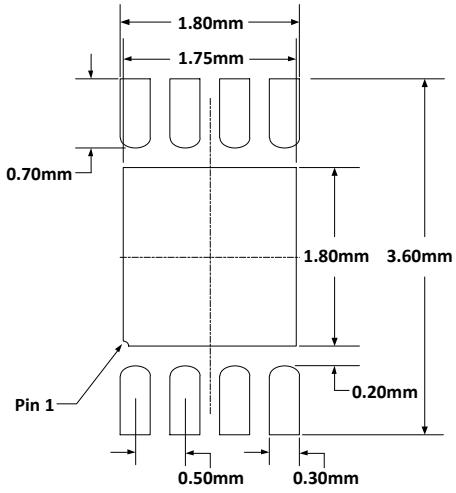


Figure 22 · **LD 8-Pin WDFN Package Land Pattern**

Disclaimer:
This PCB land pattern recommendation is based on information available to Microsemi by its suppliers. The actual land pattern to be used could be different depending on the materials and processes used in the PCB assembly, end user must account for this in their final layout. Microsemi makes no warranty or representation of performance based on this recommended land pattern.

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Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1(949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

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LX8240-3/1.0

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