115V N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV_{DSS}	BV_{DSS}@ $T_{J\ Max}$	$R_{DS(ON)}$ Max	I_D Max T_A = +25°C
115V	120V	65mΩ @ V_{GS} = 10V	4.3A
		70mΩ @ V_{GS} = 4.5V	4.5A

Features and Benefits

- 0.6mm Profile – Ideal for Low Profile Applications
- PCB Footprint of 4mm^2
- Low On-Resistance
- 100% Unclamped Inductive Switching (UIS) Test in Production – Ensures More Reliable and Robust End Application
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Description

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

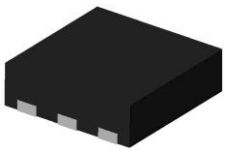
Mechanical Data

- Case: U-DFN2020-6
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.0065 grams (Approximate)

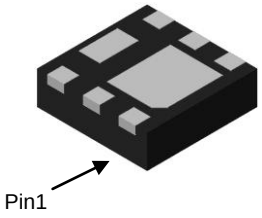
Applications

- DC-DC Primary Switch
- Load Switch

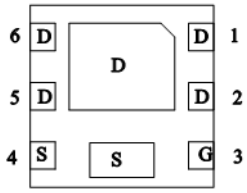
U-DFN2020-6 (Type F)



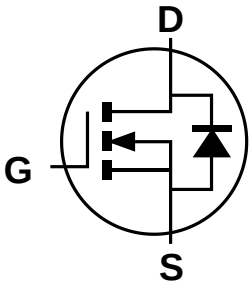
Top View



Bottom View



Pin Out
Bottom View



Equivalent Circuit

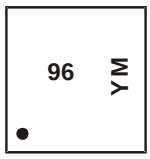
Ordering Information (Note 4)

Part Number	Case	Quantity Per Reel
DMT12H065LFDF-7	U-DFN2020-6 (Type F)	3,000
DMT12H065LFDF-13	U-DFN2020-6 (Type F)	10,000

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

U-DFN2020-6 (Type F)



96 = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: G = 2019)
M = Month (ex: 9 = September)

Date Code Key

Year	2019	2020	2021	2022	2023	2024	2025	2026	2027
Code	G	H	I	J	K	L	M	N	O

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

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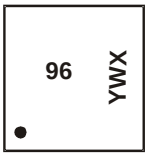
Marking Information (continued)

U-DFN2020-6 (Type F)



96 = Product Type Marking Code
YWX = Date Code Marking
Y = Year (ex: 9 = 2019)
W = Week (ex: a = week 27; z represents week 52 and 53)
X = Internal Code (ex: U = Monday)

Date Code Key

Year	2019	2020	2021	2022	2023	2024	2025	2026	2027
Code	9	0	1	2	3	4	5	6	7

Week	1-26	27-52	53
Code	A-Z	a-z	z

Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Code	T	U	V	W	X	Y	Z

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	115	V
Gate-Source Voltage		V_{GSS}	±12	V
Continuous Drain Current, V_{GS} = 10V (Note 6)	T_A = +25°C T_A = +70°C	I_D	4.3 3.4	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)		I_{DM}	25	A
Maximum Body Diode Continuous Current (Note 6)		I_S	6	A
Pulsed Body Diode Continuous Current (10µs Pulse, Duty Cycle = 1%)		I_{SM}	25	A
Avalanche Current, L = 0.3mH		I_{AS}	4	A
Avalanche Energy, L = 0.3mH		E_{AS}	2.4	mJ

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T_A = +25°C	P_D	1.0	W
	T_A = +70°C		0.6	
Thermal Resistance, Junction to Ambient (Note 5)		$R_{\theta JA}$	124	°C/W
Total Power Dissipation (Note 6)	T_A = +25°C	P_D	1.8	W
	T_A = +70°C		1.2	
Thermal Resistance, Junction to Ambient (Note 6)		$R_{\theta JA}$	69	°C/W
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	13	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

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Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	115	—	—	V	V_{GS} = 0V, I_D = 10mA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	V_{DS} = 92V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±9.6V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	0.6	—	2.2	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	43	65	mΩ	V_{GS} = 10V, I_D = 3A
		—	54	70		V_{GS} = 4.5V, I_D = 3A
		—	58	150		V_{GS} = 3.8V, I_D = 1.0A
		—	75	350		V_{GS} = 3V, I_D = 0.5A
Diode Forward Voltage	V_{SD}	—	0.8	1.3	V	V_{GS} = 0V, I_S = 2.4A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	252	—	pF	V_{DS} = 50V, V_{GS} = 0V, f = 1MHz
Output Capacitance	C_{oss}	—	80	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	3	—	pF	
Gate Resistance	R_g	—	6.9	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge	Q_g	—	5.5	—	nC	V_{DS} = 50V, I_D = 4.5A, V_{GS} = 10V
Gate-Source Charge	Q_{gs}	—	0.4	—	nC	
Gate-Drain Charge	Q_{gd}	—	1.7	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	2.1	—	ns	V_{DS} = 50V, R_L = 11Ω, V_{GS} = 10V, R_{GEN} = 3Ω
Turn-On Rise Time	t_R	—	2	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	10	—	ns	
Turn-Off Fall Time	t_F	—	3.6	—	ns	
Reverse Recovery Time	t_{RR}	—	101	—	ns	I_F = 4.5A, di/dt = 300A/μs
Reverse Recovery Charge	Q_{RR}	—	212	—	nC	

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

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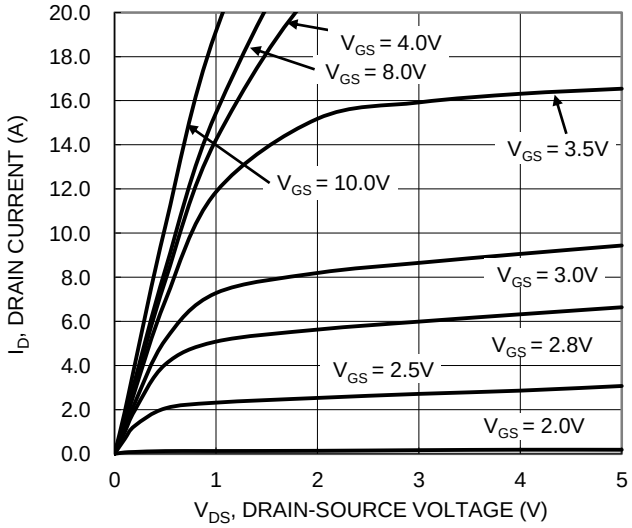

Figure 1. Typical Output Characteristic

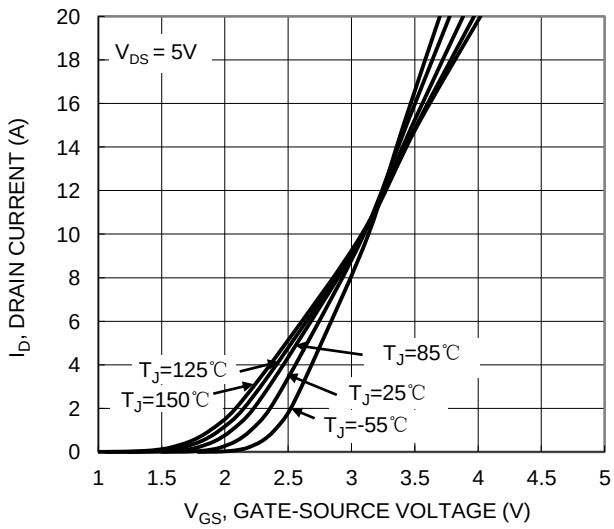

Figure 2. Typical Transfer Characteristic

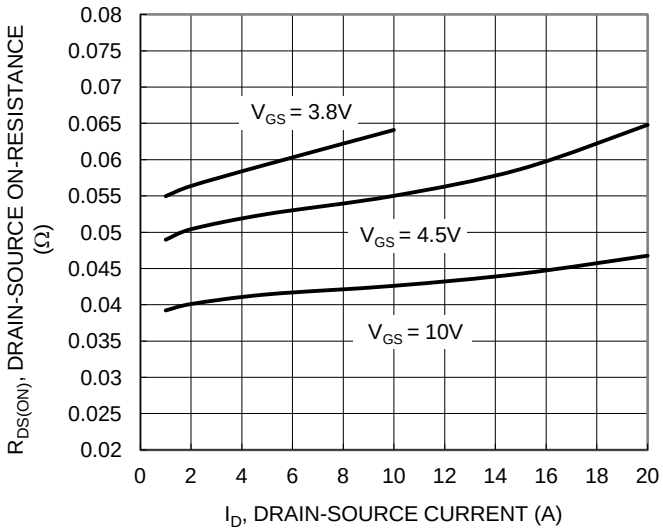

Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

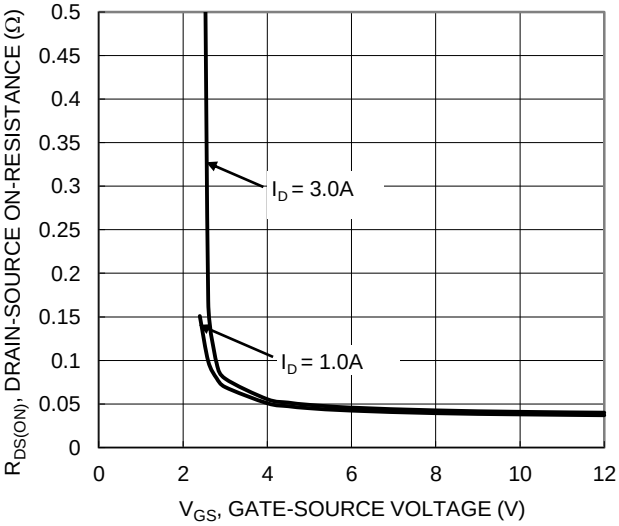

Figure 4. Typical Transfer Characteristic

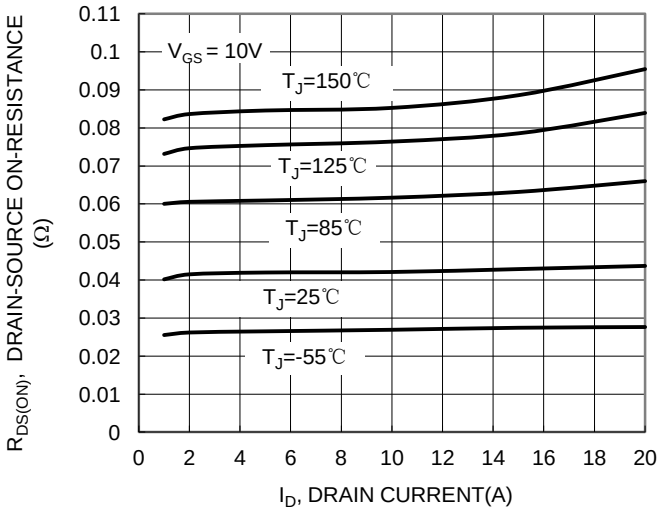

Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

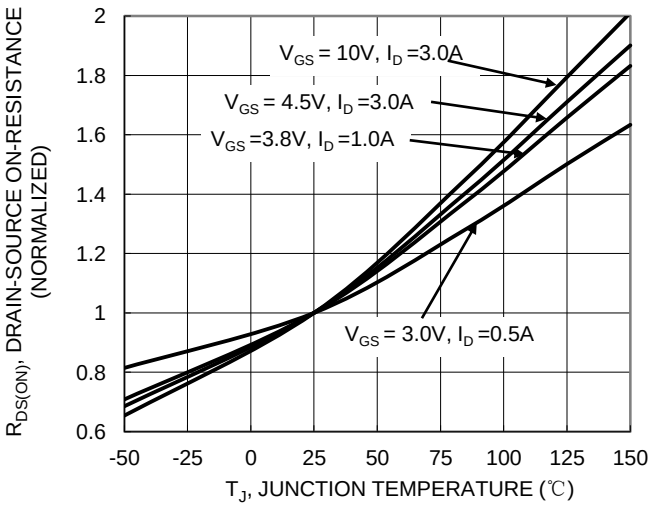

Figure 6. On-Resistance Variation with Junction Temperature

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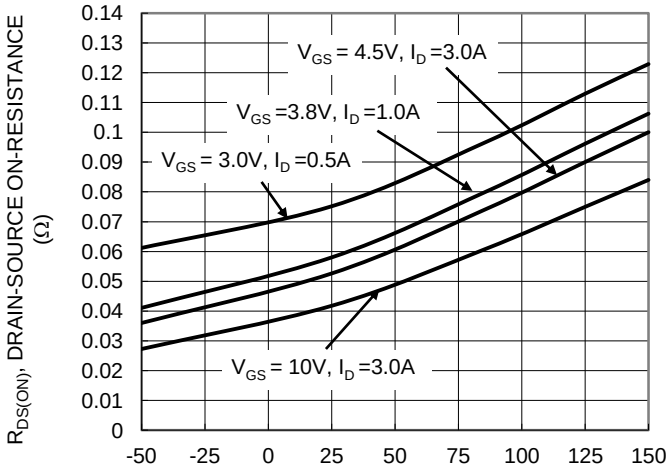

Figure 7. On-Resistance Variation with Junction Temperature

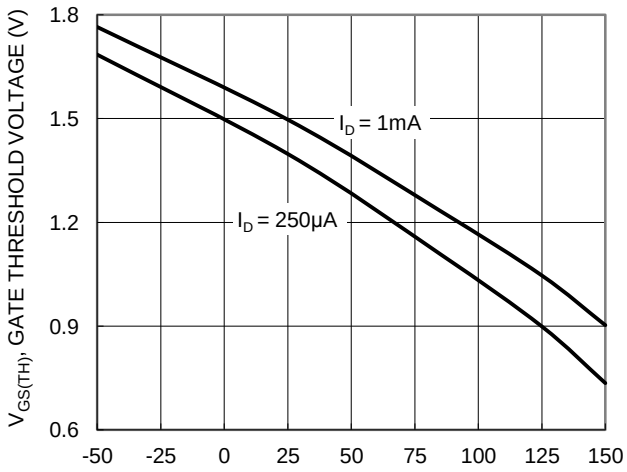

Figure 8. Gate Threshold Variation vs. Junction Temperature

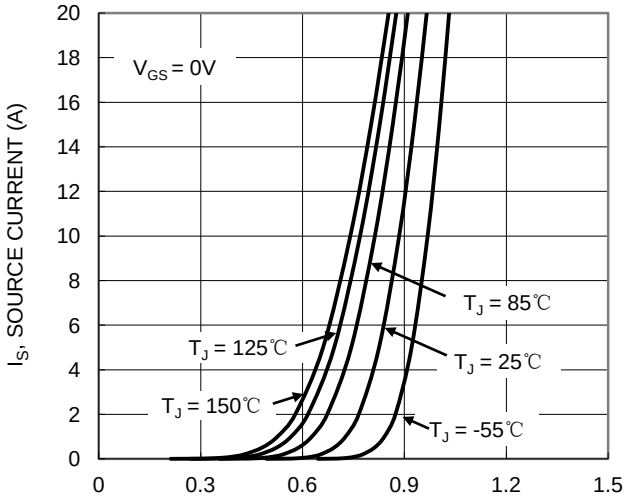

Figure 9. Diode Forward Voltage vs. Current

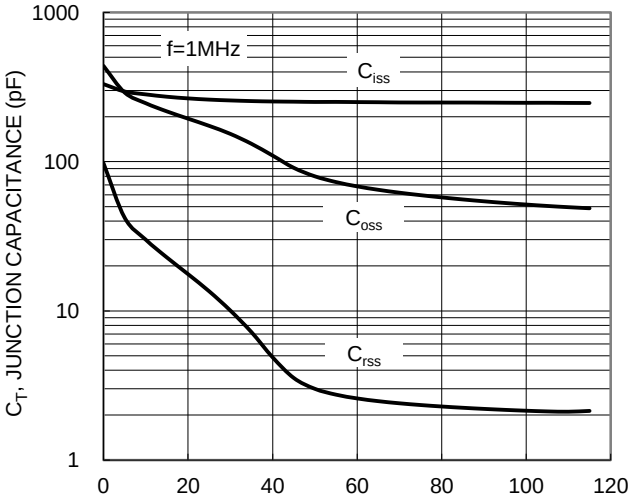

Figure 10. Typical Junction Capacitance

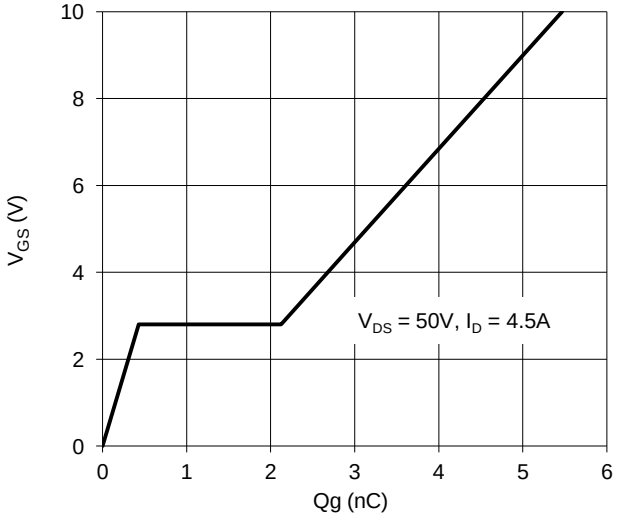

Figure 11. Gate Charge

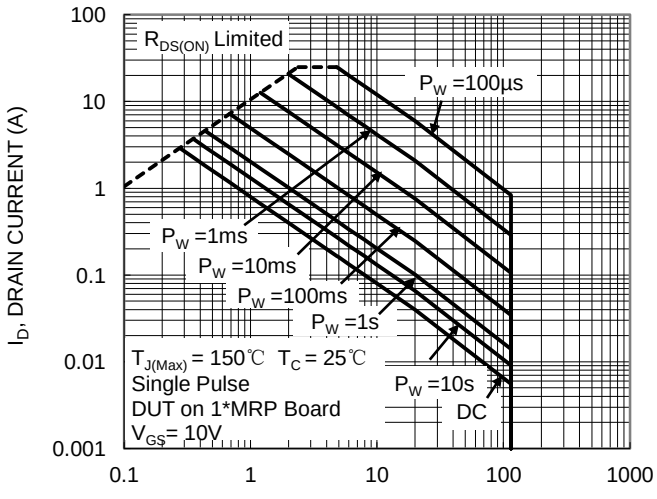

Figure 12. SOA, Safe Operation Area

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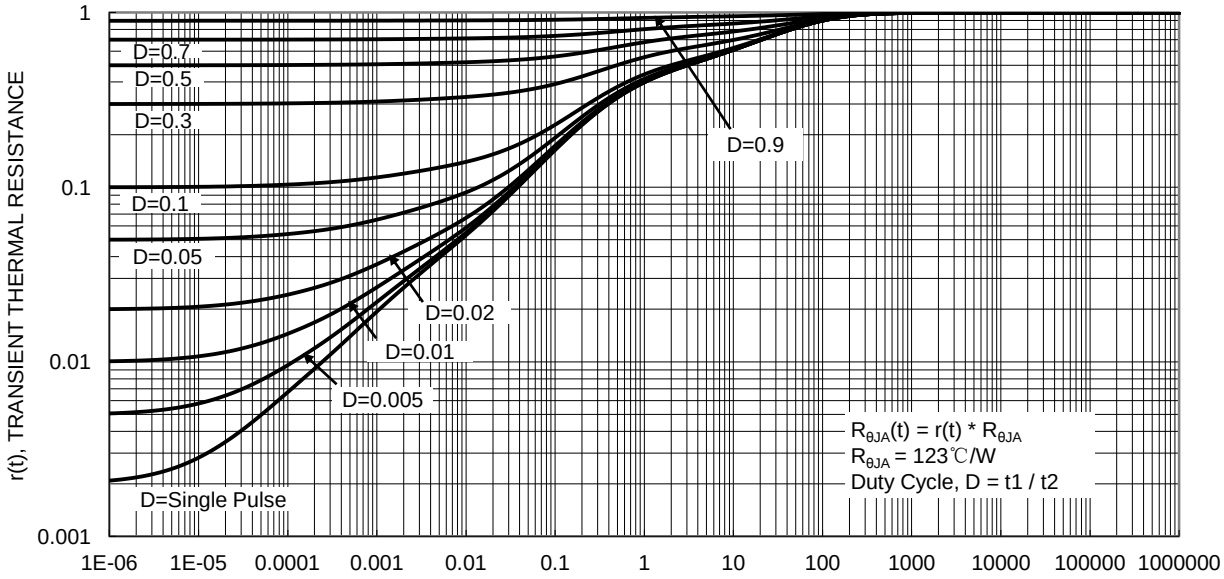

Figure 13. Transient Thermal Resistance

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Package Outline Dimensions

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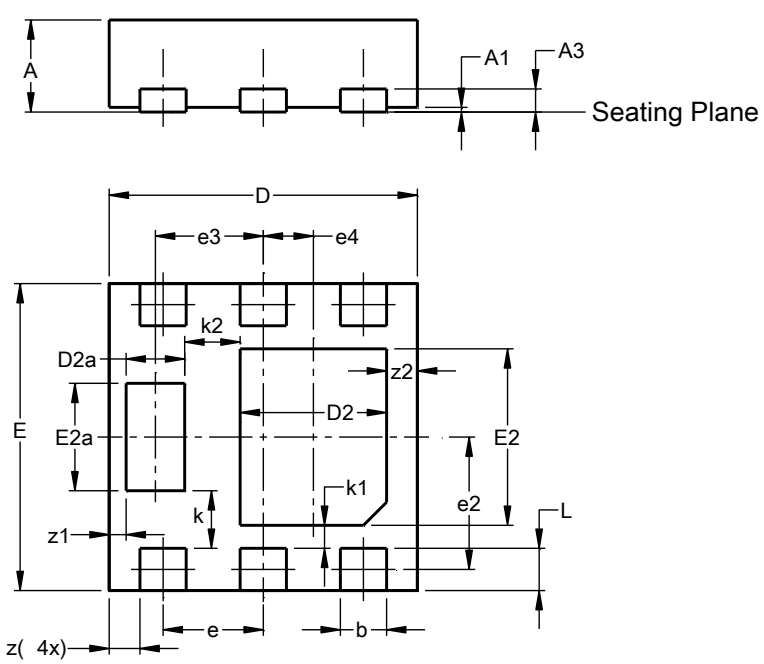
U-DFN2020-6 (Type F)

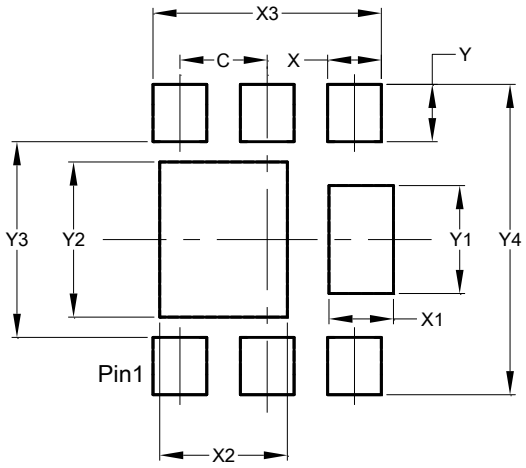


U-DFN2020-6 (Type F)			
Dim	**Min**	**Max**	**Typ**
A	0.57	0.63	0.60
A1	0.00	0.05	0.03
A3	-	-	0.15
b	0.25	0.35	0.30
D	1.95	2.05	2.00
D2	0.85	1.05	0.95
D2a	0.33	0.43	0.38
E	1.95	2.05	2.00
E2	1.05	1.25	1.15
E2a	0.65	0.75	0.70
e	0.65 BSC		
e2	0.863 BSC		
e3	0.70 BSC		
e4	0.325 BSC		
k	0.37 BSC		
k1	0.15 BSC		
k2	0.36 BSC		
L	0.225	0.325	0.275
z	0.20 BSC		
z1	0.110 BSC		
z2	0.20 BSC		
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2020-6 (Type F)



Dimensions	Value (in mm)
C	0.650
X	0.400
X1	0.480
X2	0.950
X3	1.700
Y	0.425
Y1	0.800
Y2	1.150
Y3	1.450
Y4	2.300

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