# CSD18535KTT 60V N-Channel NexFET™ Power MOSFET

## 1 Features

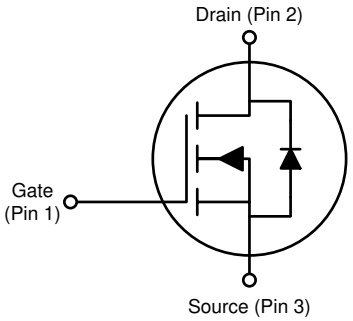
- Ultralow $Q_g$ and $Q_{gd}$
- Low thermal resistance
- Avalanche rated
- Pb-free terminal plating
- RoHS compliant
- Halogen free
- $D^2PAK$ plastic package

## 2 Applications

- Secondary side synchronous rectifier
- Motor control

## Description

This 60V, 1.6mΩ, $D^2PAK$ (TO-263) NexFET™ power MOSFET is designed to minimize losses in power conversion applications.




### Product Summary

| $T_A$ = 25°C | | TYPICAL VALUE | | UNIT |
|---|---|---|---|---|
| $V_{DS}$ | Drain-to-Source Voltage | 60 | | V |
| $Q_g$ | Gate Charge Total (10V) | 63 | | nC |
| $Q_{gd}$ | Gate Charge Gate-to-Drain | 10.4 | | nC |
| $R_{DS(on)}$ | Drain-to-Source On-Resistance | $V_{GS}$ = 4.5V | 2.3 | mΩ |
| | | $V_{GS}$ = 10V | 1.6 | mΩ |
| $V_{GS(th)}$ | Threshold Voltage | 1.9 | | V |

### Ordering Information (1)

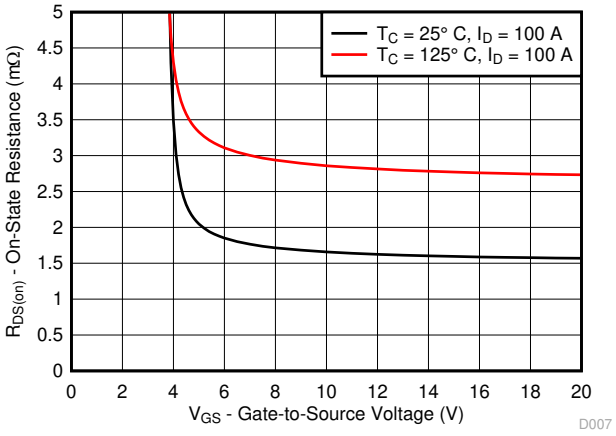
| DEVICE | QTY | MEDIA | PACKAGE | SHIP |
|---|---|---|---|---|
| CSD18535KTT | 500 | 13-Inch Reel | $D^2PAK$ Plastic Package | Tape & Reel |
| CSD18535KTTT | 50 | | | |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

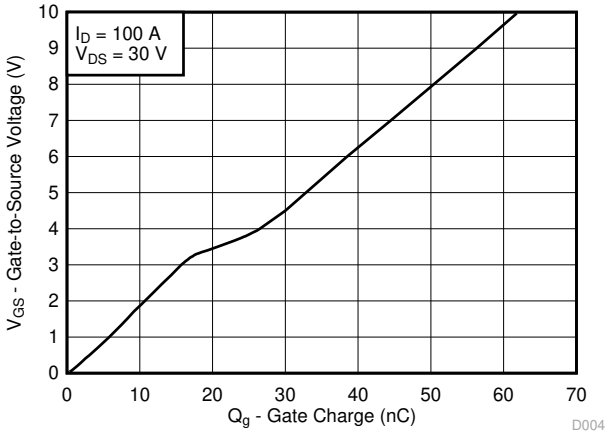
### Absolute Maximum Ratings

| $T_A$ = 25°C | | VALUE | UNIT |
|---|---|---|---|
| $V_{DS}$ | Drain-to-Source Voltage | 60 | V |
| $V_{GS}$ | Gate-to-Source Voltage | ±20 | V |
| $I_D$ | Continuous Drain Current (Package limited) | 200 | A |
| | Continuous Drain Current (Silicon limited), $T_C$ = 25°C | 279 | A |
| | Continuous Drain Current (Silicon limited), $T_C$ = 100°C | 197 | A |
| $I_{DM}$ | Pulsed Drain Current (1) | 400 | A |
| $P_D$ | Power Dissipation | 300 | W |
| $T_J$, $T_{stg}$ | Operating Junction and Storage Temperature | –55 to 175 | °C |
| $E_{AS}$ | Avalanche Energy, Single Pulse $I_D$ = 111A, L = 0.1mH, $R_G$ = 25Ω | 616 | mJ |

(1) Max $R_{\theta JC}$ = 0.5°C/W, pulse duration ≤100µs, duty cycle ≤1%




**$R_{DS(on)}$ vs $V_{GS}$**




**Gate Charge**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

# Table of Contents

**1 Features**....1
**2 Applications**....1
**3 Specifications**....3
3.1 Electrical Characteristics....3
3.2 Thermal Information....3
3.3 Typical MOSFET Characteristics....4
**4 Device and Documentation Support**....7
4.1 Third-Party Products Disclaimer....7
4.2 Receiving Notification of Documentation Updates....7
4.3 Support Resources....7
4.4 Trademarks....7
4.5 Electrostatic Discharge Caution....7
4.6 Glossary....7
**5 Revision History**....7
**6 Mechanical, Packaging, and Orderable Information**....8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# 3 Specifications

## 3.1 Electrical Characteristics

($T_A$ = 25°C unless otherwise stated)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **STATIC CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain-to-source voltage | $V_{GS}$ = 0V, $I_D$ = 250µA | 60 | | | V |
| $I_{DSS}$ | Drain-to-source leakage current | $V_{GS}$ = 0V, $V_{DS}$ = 48V | | | 1 | µA |
| $I_{GSS}$ | Gate-to-source leakage current | $V_{DS}$ = 0V, $V_{GS}$ = 20V | | | 100 | nA |
| $V_{GS(th)}$ | Gate-to-source threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA | 1.4 | 1.9 | 2.4 | V |
| $R_{DS(on)}$ | Drain-to-source on-resistance | $V_{GS}$ = 4.5V, $I_D$ = 100A | | 2.3 | 2.9 | mΩ |
| | | $V_{GS}$ = 10V, $I_D$ = 100A | | 1.6 | 2.0 | mΩ |
| $g_{fs}$ | Transconductance | $V_{DS}$ = 6V, $I_D$ = 100A | | 263 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input capacitance | $V_{GS}$ = 0V, $V_{DS}$ = 30V, $f$ = 1 MHz | | 5090 | 6620 | pF |
| $C_{oss}$ | Output capacitance | | | 890 | 1150 | pF |
| $C_{rss}$ | Reverse transfer capacitance | | | 24 | 31 | pF |
| $R_G$ | Series gate resistance | | | 0.8 | 1.6 | Ω |
| $Q_g$ | Gate charge total (10V) | $V_{DS}$ = 30V, $I_D$ = 100A | | 63 | 81 | nC |
| $Q_{gd}$ | Gate charge gate-to-drain | | | 10.4 | | nC |
| $Q_{gs}$ | Gate charge gate-to-source | | | 15.7 | | nC |
| $Q_{g(th)}$ | Gate charge at $V_{th}$ | | | 9.4 | | nC |
| $Q_{oss}$ | Output charge | $V_{DS}$ = 30V, $V_{GS}$ = 0V | | 140 | | nC |
| $t_{d(on)}$ | Turn on delay time | $V_{DS}$ = 30V, $V_{GS}$ = 10V, $I_{DS}$ = 100A, $R_G$ = 0Ω | | 9 | | ns |
| $t_r$ | Rise time | | | 3 | | ns |
| $t_{d(off)}$ | Turn off delay time | | | 19 | | ns |
| $t_f$ | Fall time | | | 3 | | ns |
| **DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Diode forward voltage | $I_{SD}$ = 100A, $V_{GS}$ = 0V | | 0.9 | 1.0 | V |
| $Q_{rr}$ | Reverse recovery charge | $V_{DS}$= 30V, $I_F$ = 100A, di/dt = 300A/µs | | 214 | | nC |
| $t_{rr}$ | Reverse recovery time | | | 63 | | ns |

## 3.2 Thermal Information

($T_A$ = 25°C unless otherwise stated)

| THERMAL METRIC | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-case thermal resistance | | | 0.5 | °C/W |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | | | 62 | °C/W |

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## 3.3 Typical MOSFET Characteristics

($T_A$ = 25°C unless otherwise stated)

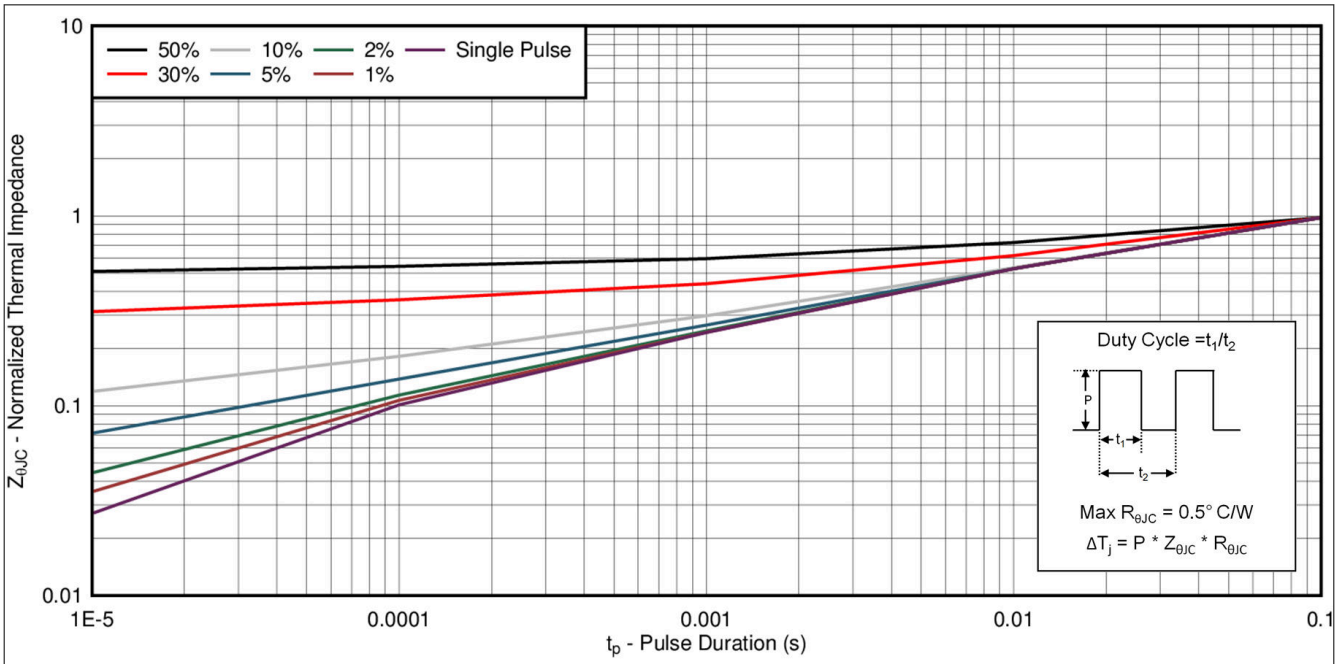



**Figure 3-1. Transient Thermal Impedance**

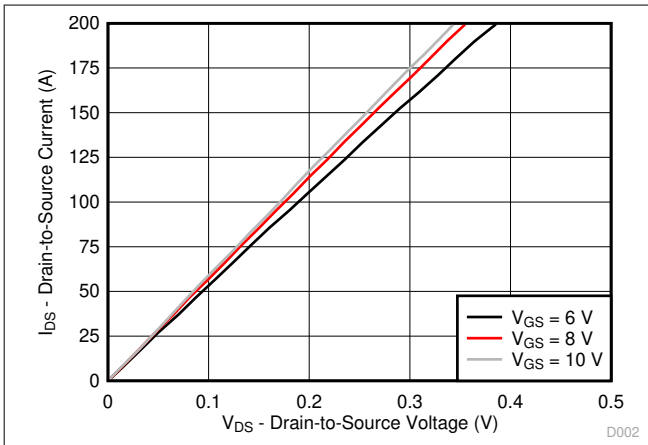
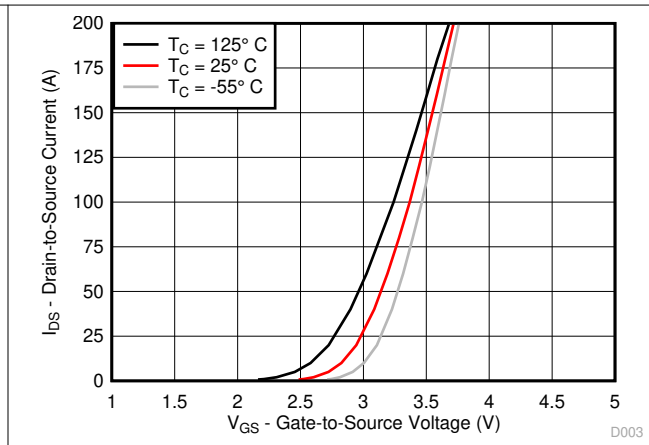



**Figure 3-2. Saturation Characteristics**




VDS = 5V

**Figure 3-3. Transfer Characteristics**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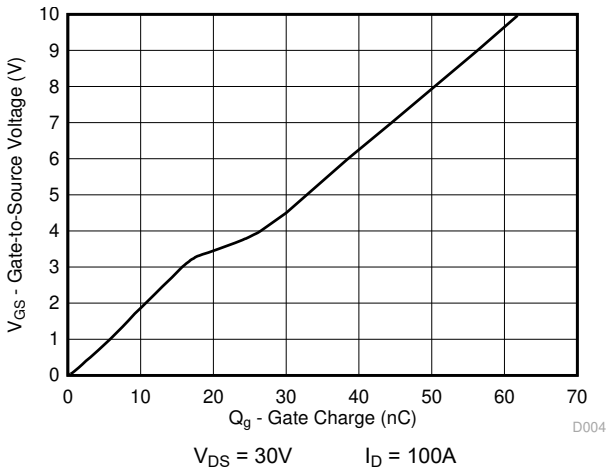



**Figure 3-4. Gate Charge**

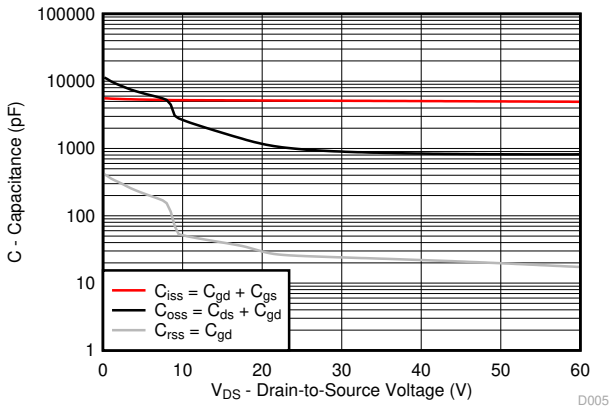



**Figure 3-5. Capacitance**

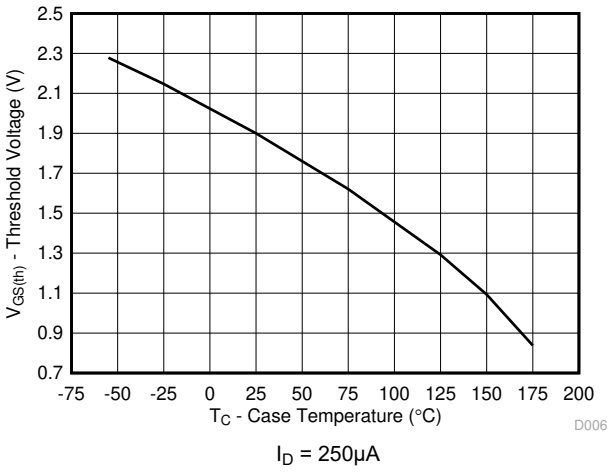



**Figure 3-6. Threshold Voltage vs Temperature**

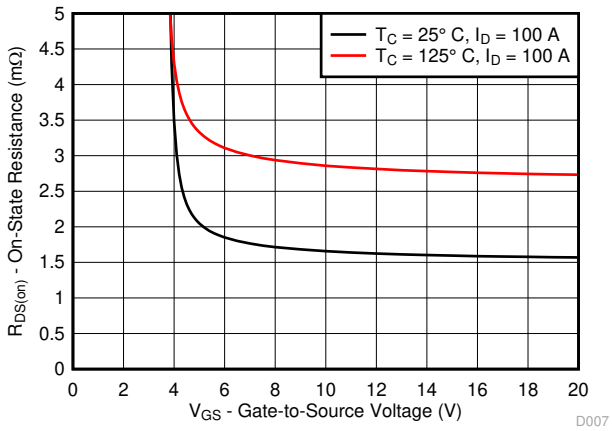



**Figure 3-7. On-State Resistance vs Gate-to-Source Voltage**

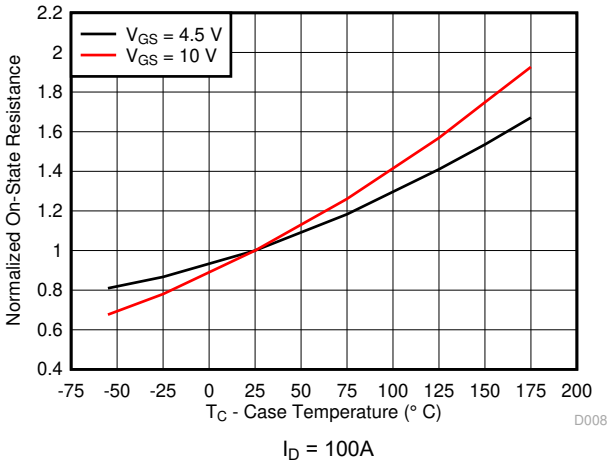



**Figure 3-8. Normalized On-State Resistance vs Temperature**

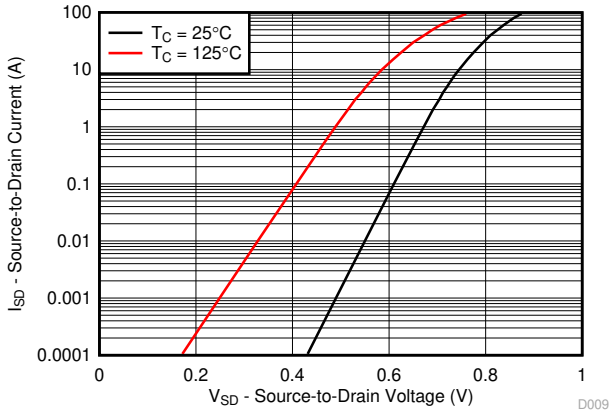
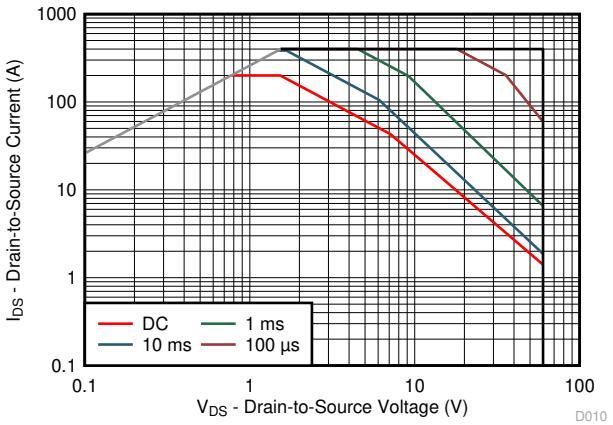



**Figure 3-9. Typical Diode Forward Voltage**




Single Pulse, Max $R_{\theta JC}$ = 0.5°C/W

**Figure 3-10. Maximum Safe Operating Area**

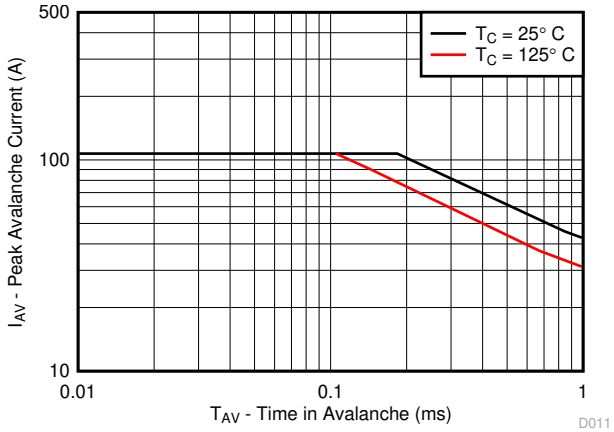



**Figure 3-11. Single Pulse Unclamped Inductive Switching**

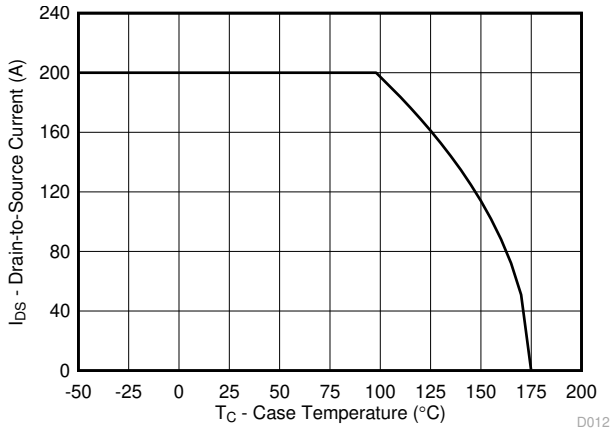



**Figure 3-12. Maximum Drain Current vs Temperature**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# 4 Device and Documentation Support

## 4.1 Third-Party Products Disclaimer

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To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 4.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 4.4 Trademarks

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TI E2E™ is a trademark of Texas Instruments.
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## 4.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 4.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 5 Revision History

| Changes from Revision * (March 2016) to Revision A (June 2025) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document | 1 |

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## 6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| CSD18535KTT | Active | Production | DDPAK/ TO-263 (KTT) \| 2 | 500 \| LARGE T&R | ROHS Exempt | SN | Level-2-260C-1 YEAR | -55 to 175 | CSD18535KTT |
| CSD18535KTT.B | Active | Production | DDPAK/ TO-263 (KTT) \| 2 | 500 \| LARGE T&R | ROHS Exempt | SN | Level-2-260C-1 YEAR | -55 to 175 | CSD18535KTT |
| CSD18535KTTT | Active | Production | DDPAK/ TO-263 (KTT) \| 2 | 50 \| SMALL T&R | ROHS Exempt | SN | Level-2-260C-1 YEAR | -55 to 175 | CSD18535KTT |
| CSD18535KTTT.B | Active | Production | DDPAK/ TO-263 (KTT) \| 2 | 50 \| SMALL T&R | ROHS Exempt | SN | Level-2-260C-1 YEAR | -55 to 175 | CSD18535KTT |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

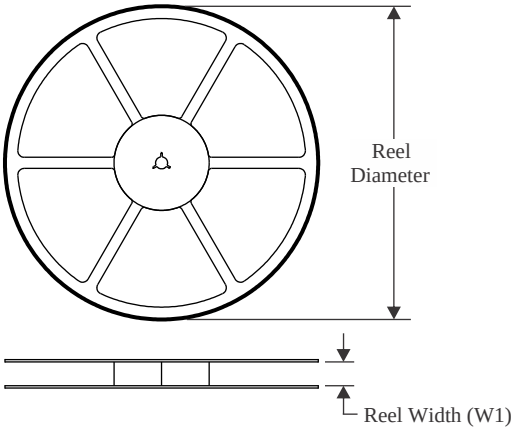
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

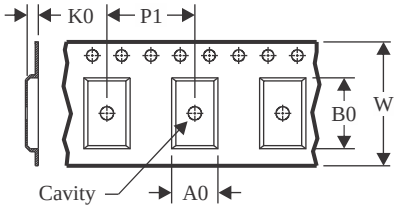
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

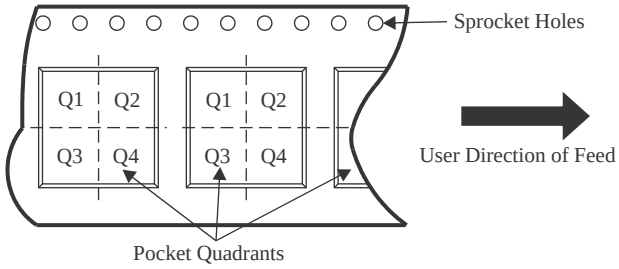



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

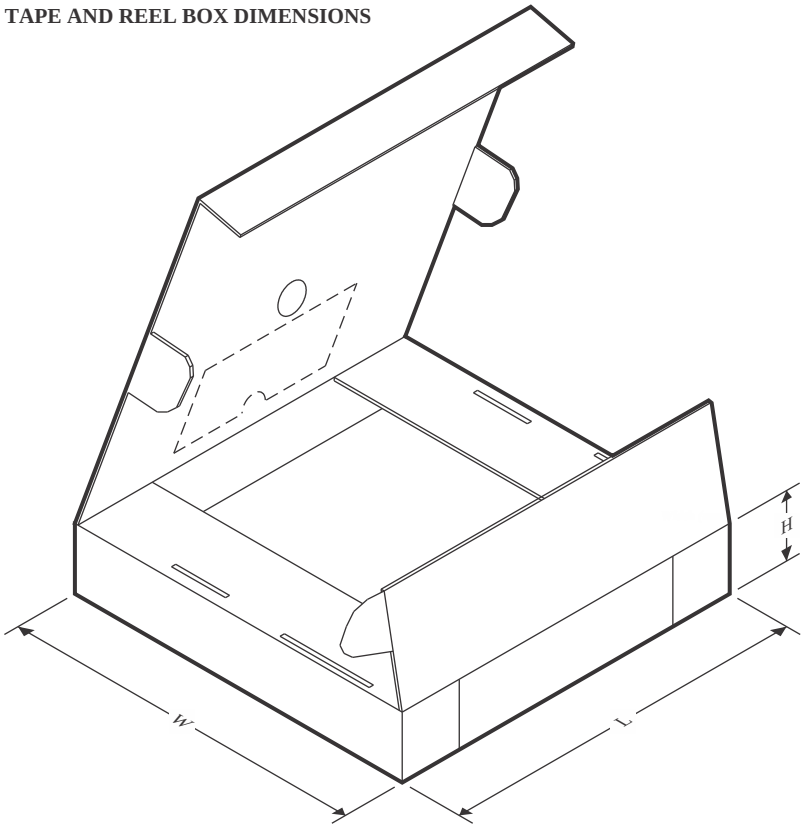
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CSD18535KTT | DDPAK/ TO-263 | KTT | 2 | 500 | 330.0 | 24.4 | 10.8 | 16.3 | 5.11 | 16.0 | 24.0 | Q2 |
| CSD18535KTTT | DDPAK/ TO-263 | KTT | 2 | 50 | 330.0 | 24.4 | 10.8 | 16.3 | 5.11 | 16.0 | 24.0 | Q2 |

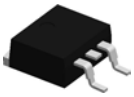
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CSD18535KTT | DDPAK/TO-263 | KTT | 2 | 500 | 340.0 | 340.0 | 38.0 |
| CSD18535KTTT | DDPAK/TO-263 | KTT | 2 | 50 | 340.0 | 340.0 | 38.0 |

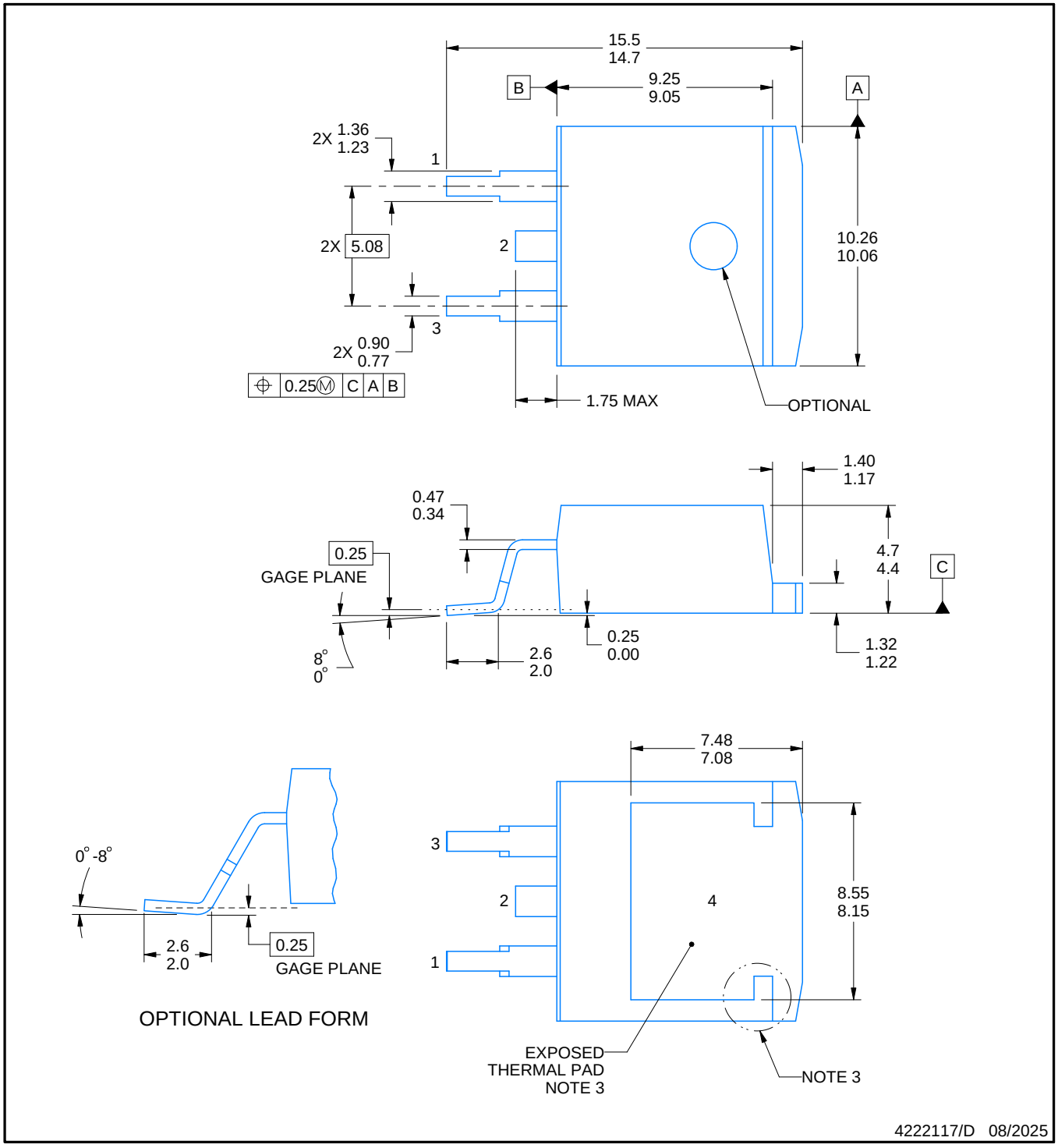
# KTT0002A



# PACKAGE OUTLINE

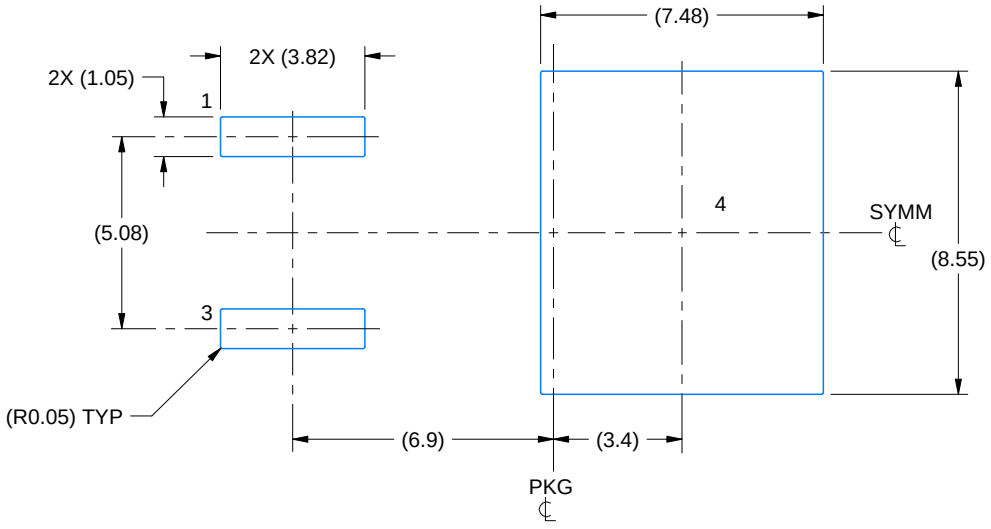
## TO-263 - 4.7 mm max height

TRANSISTOR OUTLINE

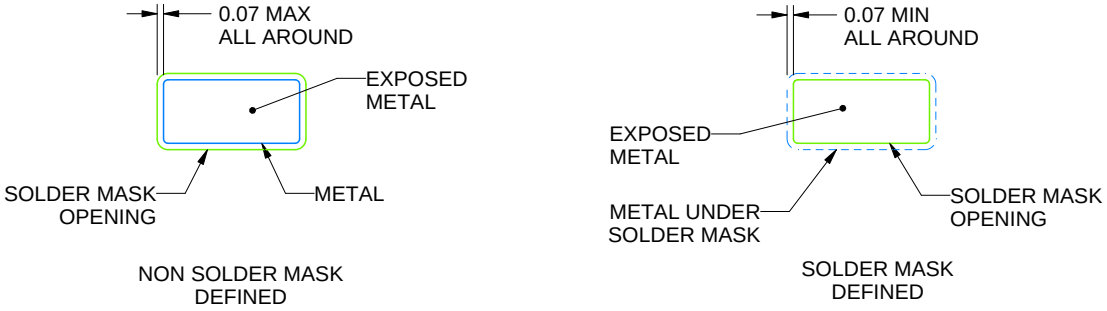



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Features may not exist and shape may vary per different assembly sites. Pin 2 and Pin 4 connected.
4. Reference JEDEC registration TO-263.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:5X

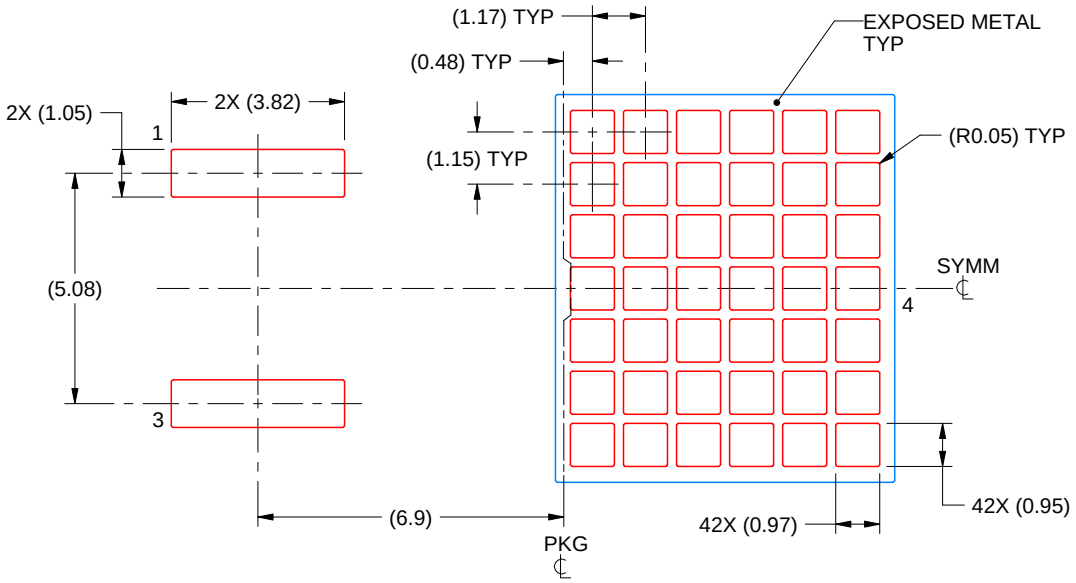



SOLDER MASK DETAILS

4222117/D 08/2025

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
60.5% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

4222117/D 08/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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# Elektronik komponent tedarikinde Entegreci

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Üretici parça numarasını yazın; stok ve fiyatı hemen görün.

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