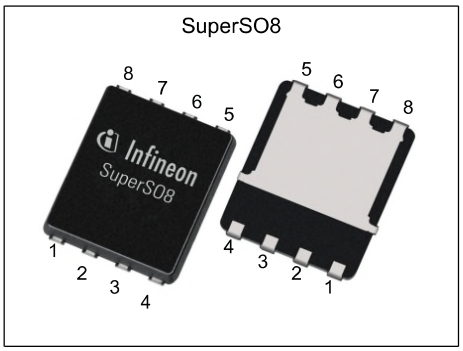
MOSFET

OptiMOS™ 5 Power-MOSFET, 30 V



Features

- Optimized for high performance buck converters
- Monolithically integrated Schottky-like diode
- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V
- 100% avalanche tested
- N-channel
- Qualified according to JEDEC[1)] for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

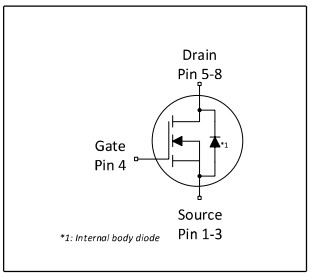


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	30	V
$R_{DS(on),max}$	2.3	mΩ
I_D	110	A
Q_{OSS}	13.5	nC
Q_G(0V..4.5V)	9.0	nC

Type / Ordering Code	Package	Marking	Related Links
BSC0502NSI	PG-TDSON-8	0502NSI	-

[1)] J-STD20 and JESD22

Table of Contents

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1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- - - - -	- - - - -	110 70 100 63 26	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=4.5 V, T_C=25 °C V_{GS}=4.5 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{thJA}=50 K/W[2]
Pulsed drain current[3]	$I_{D,pulse}$	-	-	440	A	T_C=25 °C
Avalanche current, single pulse[4]	I_{AS}	-	-	45	A	T_C=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	14	mJ	I_D=45 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	43 2.5	W	T_C=25 °C T_A=25 °C, R_{thJA}=50 K/W[2]
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	2.9	K/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	K/W	-
Device on PCB, 6 cm² cooling area[2]	R_{thJA}	-	-	50	K/W	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[3] See Diagram 3 for more detailed information
[4] See Diagram 13 for more detailed information

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	V_{GS}=0 V, I_D=10 mA
Breakdown voltage temperature coefficient	$dV_{(BR)DSS}/dT_j$	-	15	-	mV/K	I_D=10 mA, referenced to 25 °C
Gate threshold voltage	$V_{GS(th)}$	1.2	-	2.0	V	V_{DS}=V_{GS}, I_D=250 µA
Zero gate voltage drain current	I_{DSS}	- -	- 0.4	0.5 -	mA	V_{DS}=24 V, V_{GS}=0 V, T_j=25 °C V_{DS}=24 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	2.4 1.9	2.8 2.3	mΩ	V_{GS}=4.5 V, I_D=30 A V_{GS}=10 V, I_D=30 A
Gate resistance	R_G	-	1.4	2.3	Ω	-
Transconductance	g_{fs}	65	130	-	S	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=30 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1)]	C_{iss}	-	1200	1600	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Output capacitance[1)]	C_{oss}	-	420	570	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	44	-	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	3.6	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	3.8	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	19	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	2.6	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω

[1)] Defined by design. Not subject to production test.

Table 6 Gate charge characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	3.1	-	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	2.0	-	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate to drain charge	Q_{gd}	-	2.3	-	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Switching charge	Q_{sw}	-	3.4	-	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge total[2)]	Q_g	-	9.0	12	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate plateau voltage	$V_{plateau}$	-	2.5	-	V	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge total[2)]	Q_g	-	19	26	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	8.3	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V
Output charge[2)]	Q_{oss}	-	13.5	18	nC	V_{DD}=15 V, V_{GS}=0 V

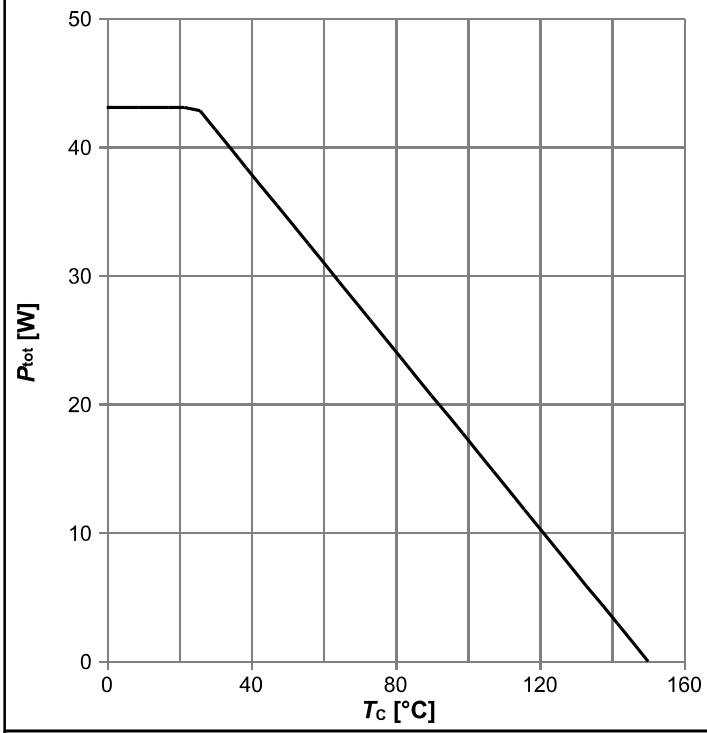
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	50	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	440	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.54	0.65	V	V_{GS}=0 V, I_F=5 A, T_j=25 °C
Reverse recovery charge	Q_{rr}	-	15	-	nC	V_R=15 V, I_F=I_S, di_F/dt=400 A/µs

[1)] See ″Gate charge waveforms″ for parameter definition
[2)] Defined by design. Not subject to production test.

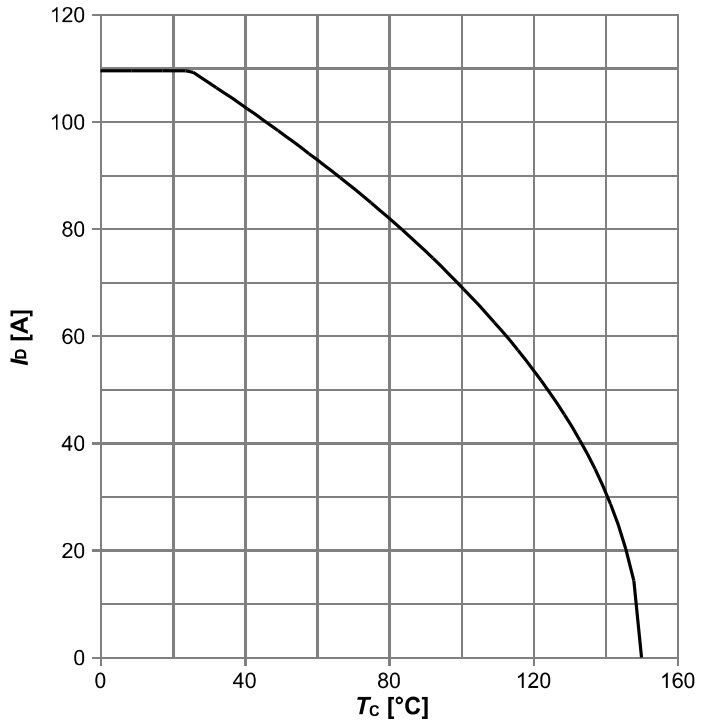
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



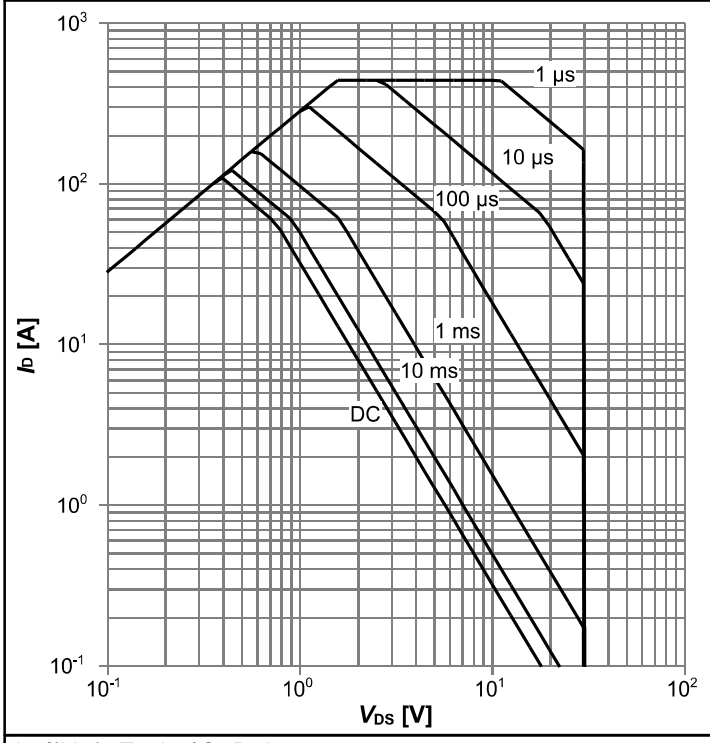
$P_{tot}=f(T_C)$

Diagram 2: Drain current



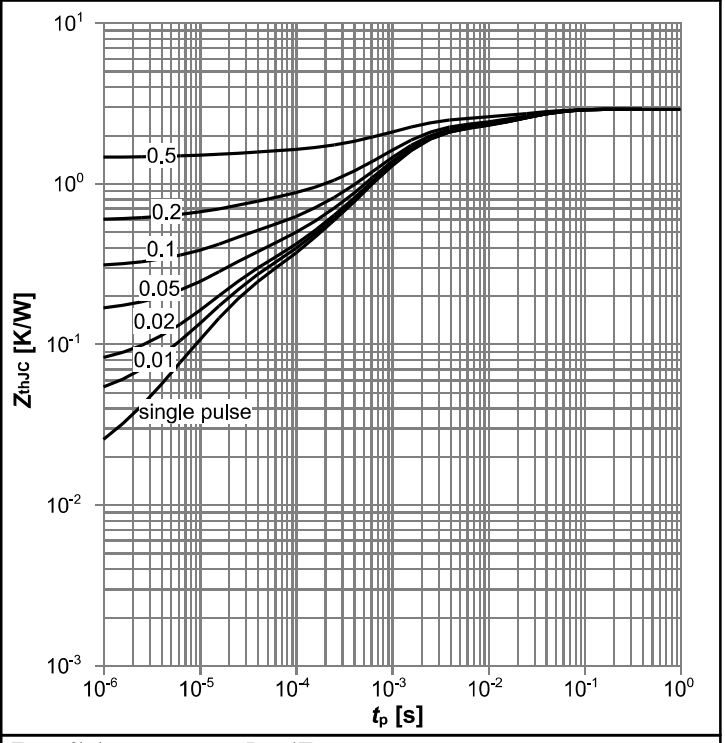
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



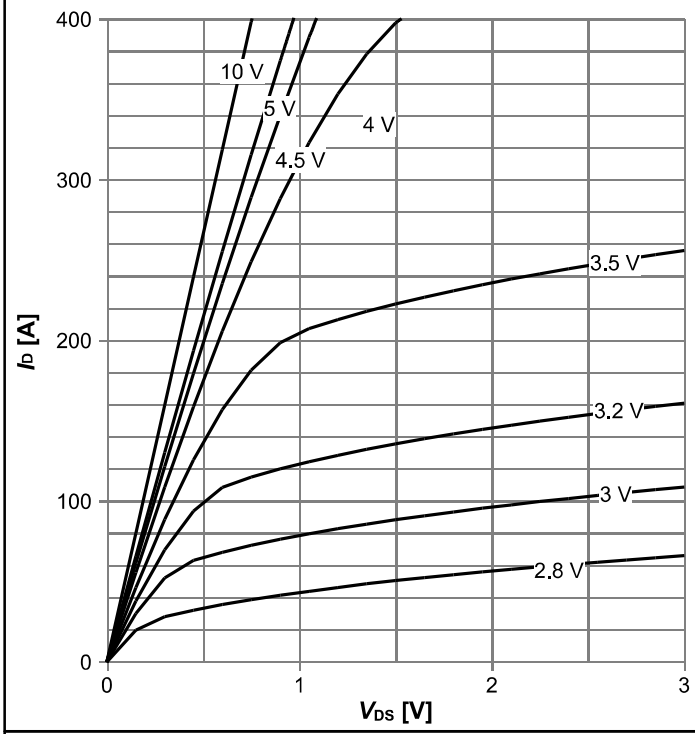
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance



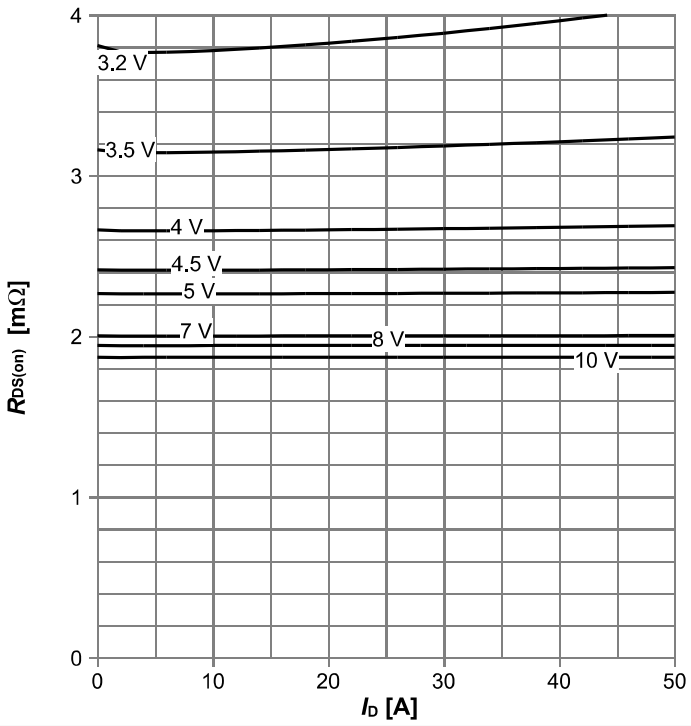
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



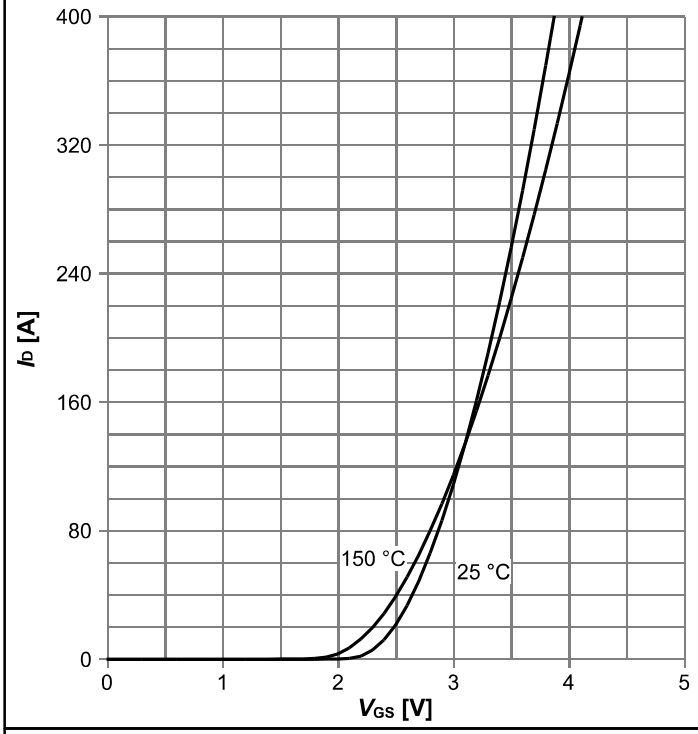
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



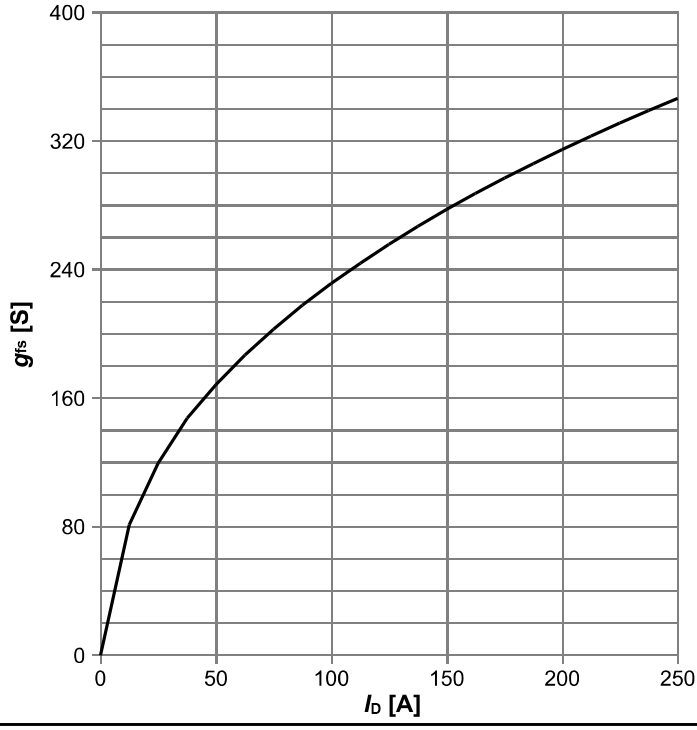
$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



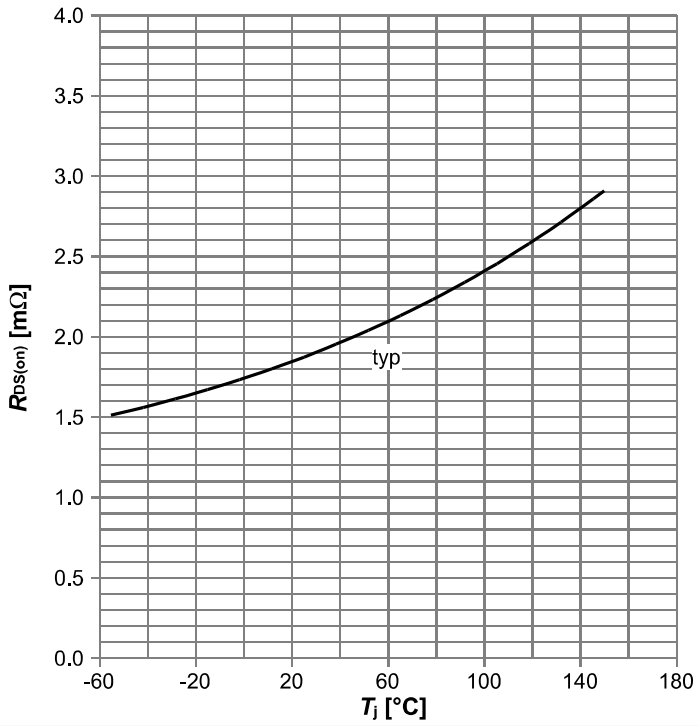
I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



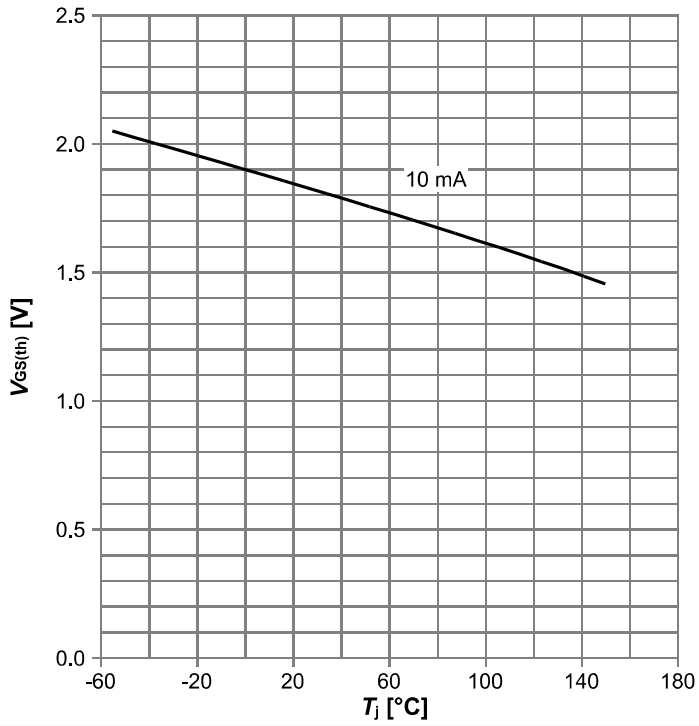
g_{fs}=f(I_D); T_j=25 °C

Diagram 9: Drain-source on-state resistance



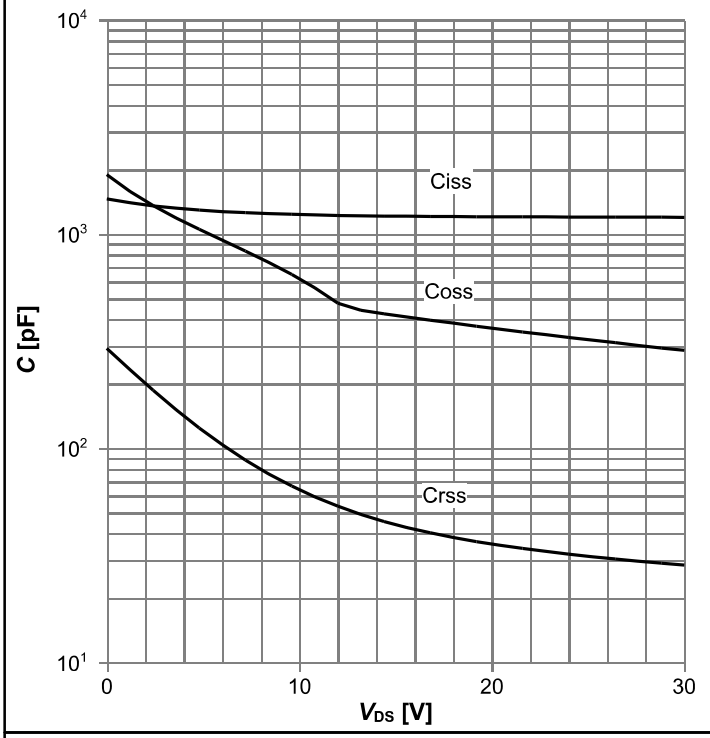
$R_{DS(on)}=f(T_j)$; I_D=30 A; V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



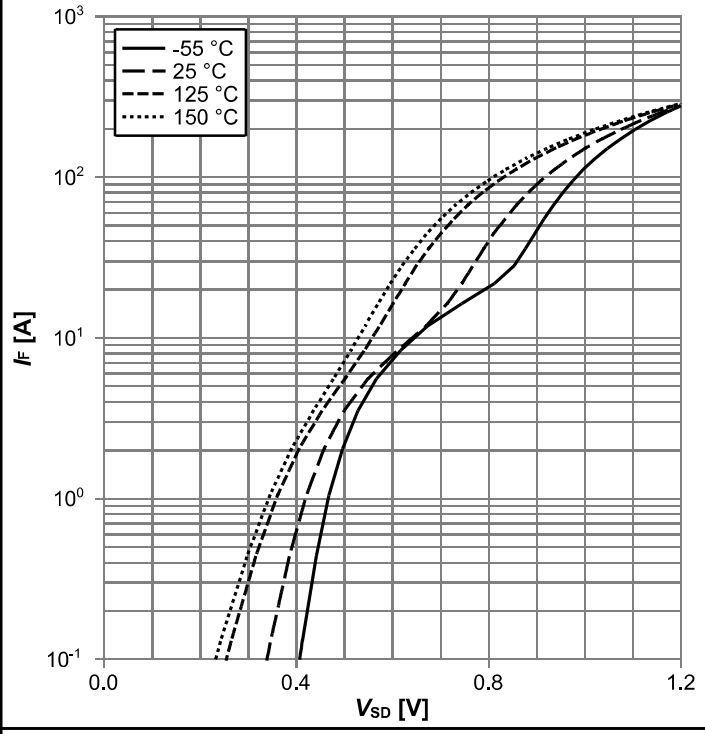
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$

Diagram 11: Typ. capacitances



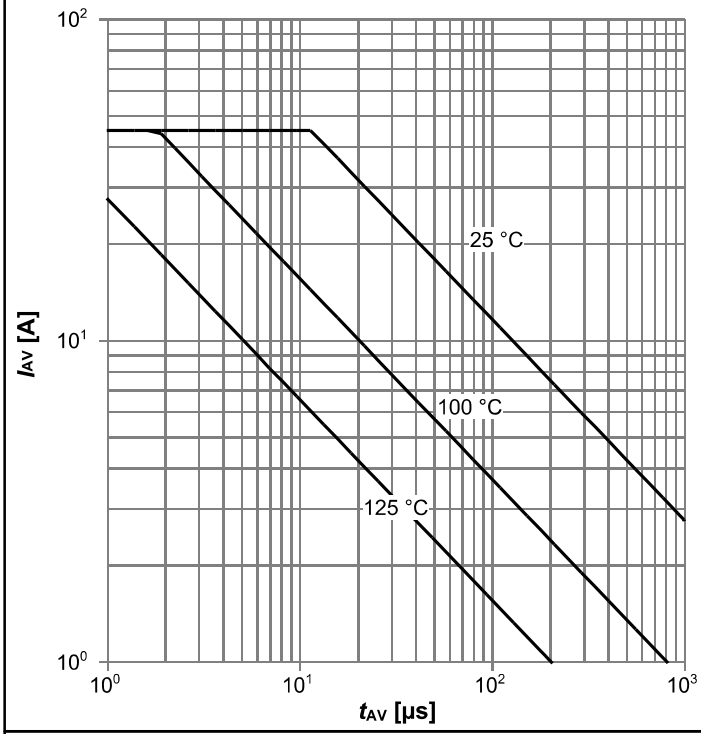
$C=f(V_{DS})$; V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



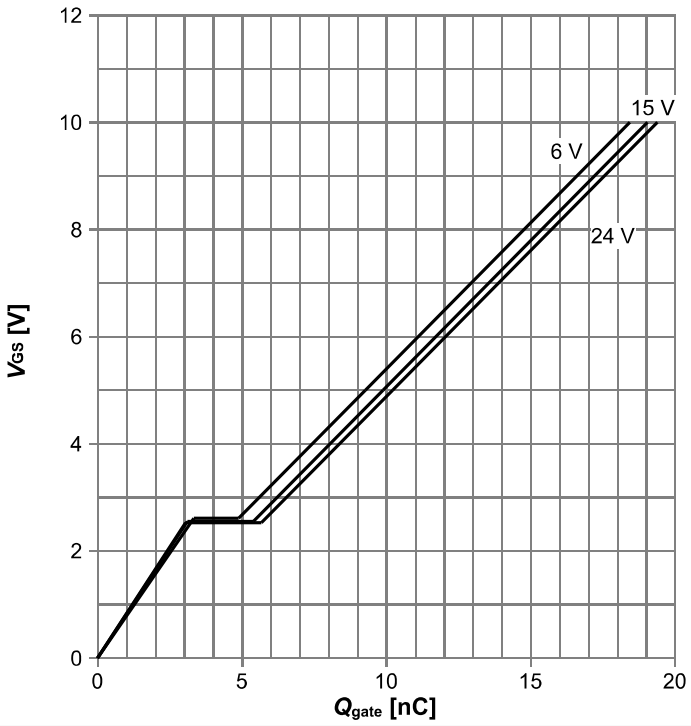
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



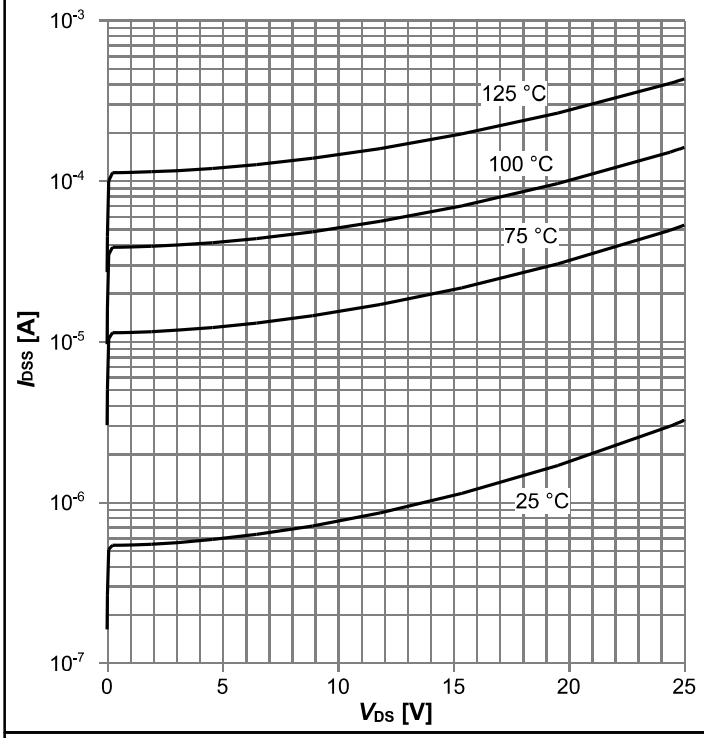
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



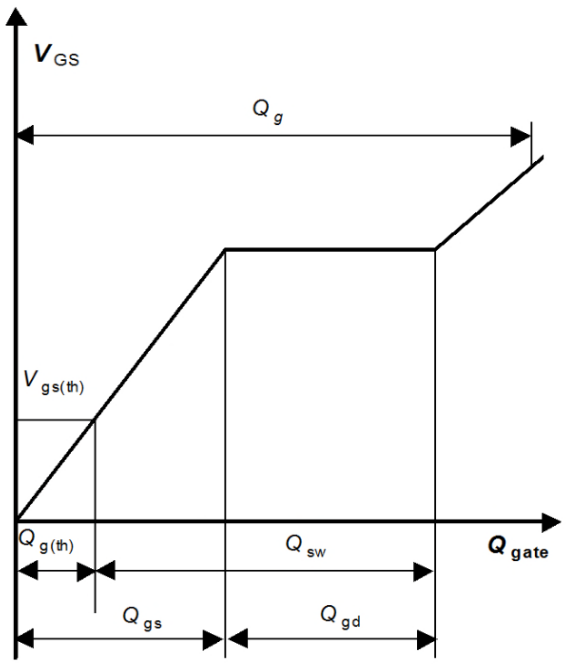
V_{GS}=f(Q_{gate}); I_D=30 A pulsed; parameter: V_{DD}

Diagram 15: Typ. drain-source leakage current

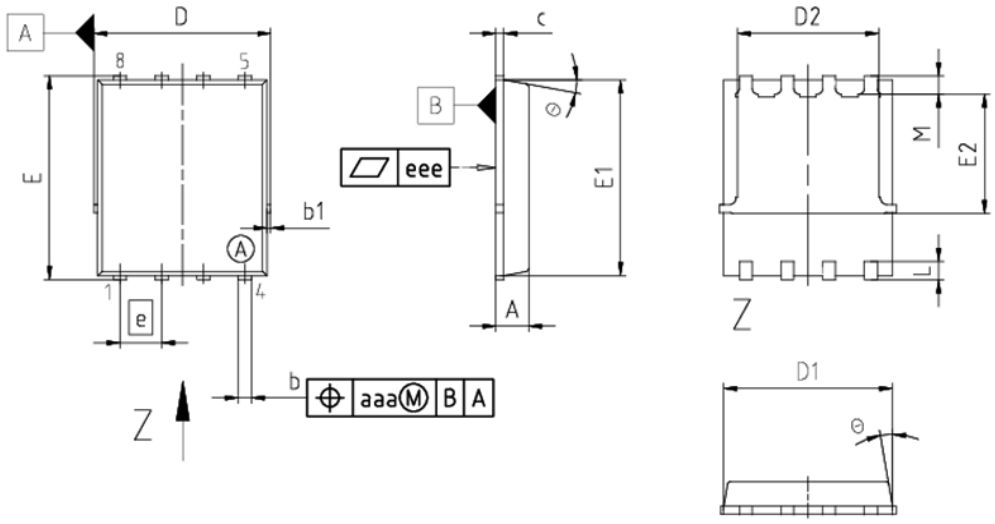


I_{DSS}=f(V_{DS}); V_{GS}=0 V; parameter: T_j

Diagram Gate charge waveforms



5 Package Outlines



DIM	MILLIMETERS	
	MIN	MAX
A	0.90	1.10
b	0.31	0.54
b1	0.02	0.22
c	0.15	0.35
D	5.15	5.49
D1	4.95	5.35
D2	3.70	4.40
E	5.95	6.35
E1	5.70	6.10
E2	3.40	3.80
e	1.27	
N	8	
L	0.45	0.71
M	0.45	0.75
Θ	8.5°	12°
aaa	0.25	
eee	0.08	

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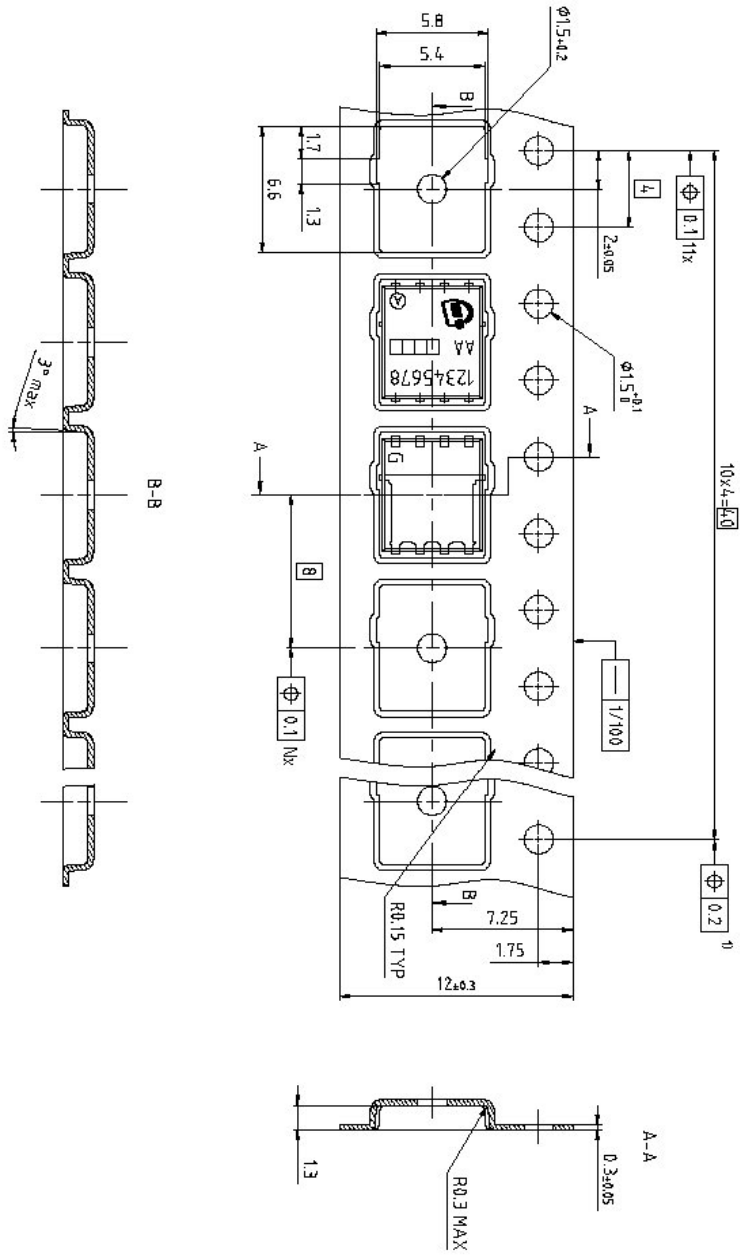
SCALE 0 2 0 2 4mm

EUROPEAN PROJECTION

ISSUE DATE
10-04-2013

REVISION
04

Figure 1 Outline PG-TDSON-8, dimensions in mm



Dimension in mm

Figure 2 Outline Tape (TDSON-8)

Revision History

BSC0502NSI

Revision: 2021-08-03, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2015-07-13	Release of final version
2.1	2021-08-03	Update current rating and footnotes

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