## Description

The AP3981D2 is a high-performance power switcher integrated with a primary-side regulation controller and an N-channel power MOSFET. It can be used for battery charger and adaptor applications. Accurate constant voltage (CV) and constant current (CC) can be achieved without an optocoupler and secondary control circuitry.

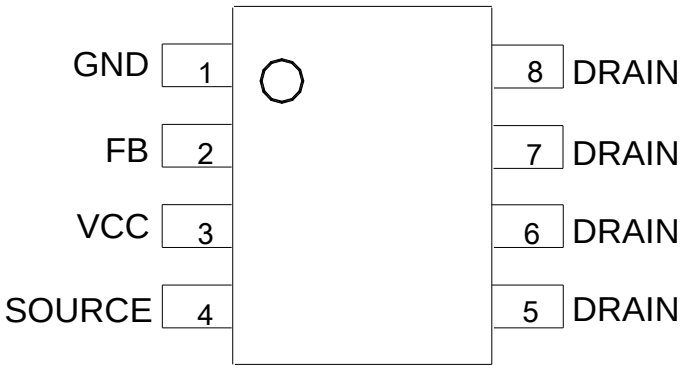
The AP3981D2 operates in pulse frequency modulation (PFM) mode and peak current amplitude modulation (AM) mode to form a fine-tune frequency curve within the whole power range. Therefore, AP3981D2 can achieve high-average efficiency and improve audible noise.

The AP3981D2 provides comprehensive protections without additional circuitry. It contains $V_{CC}$ overvoltage protection, output overvoltage protection, output undervoltage protection, output short-circuit protection, cycle-by-cycle current limit, open-loop protection, and internal OTP, etc.

The AP3981D2 is available in SO-8.

## Pin Assignments

**(Top View)**




**SO-8**

## Features

- Primary Side Control for Eliminating Optocoupler
- Built-In 650V Power MOSFET of AP3981D2
- 75mW No-Load Input Power
- Flyback Topology in DCM Operation
- External Adjustable Line Compensation for CC
- Fixed Internal Cable Compensation
- Multiple Segment AM/PFM Control Mode to Improve Audio Noise and Efficiency
- Frequency Jitter to Improve System EMI
- Capacitive Load Start-Up Capability
- Valley-On for the Higher Efficiency and Better EMI Behavior
- Multiple Protections:
  - Secondary-Side Overvoltage Protection (SOVP)
  - Secondary-Side Undervoltage Protection (SUVP)
  - Output Short-Circuit Protection (SCP)
  - Transformer Saturation Protection (TSP) via Primary Peak Current Limitation
  - Internal Overtemperature Protection (OTP)
- SO-8 Package
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

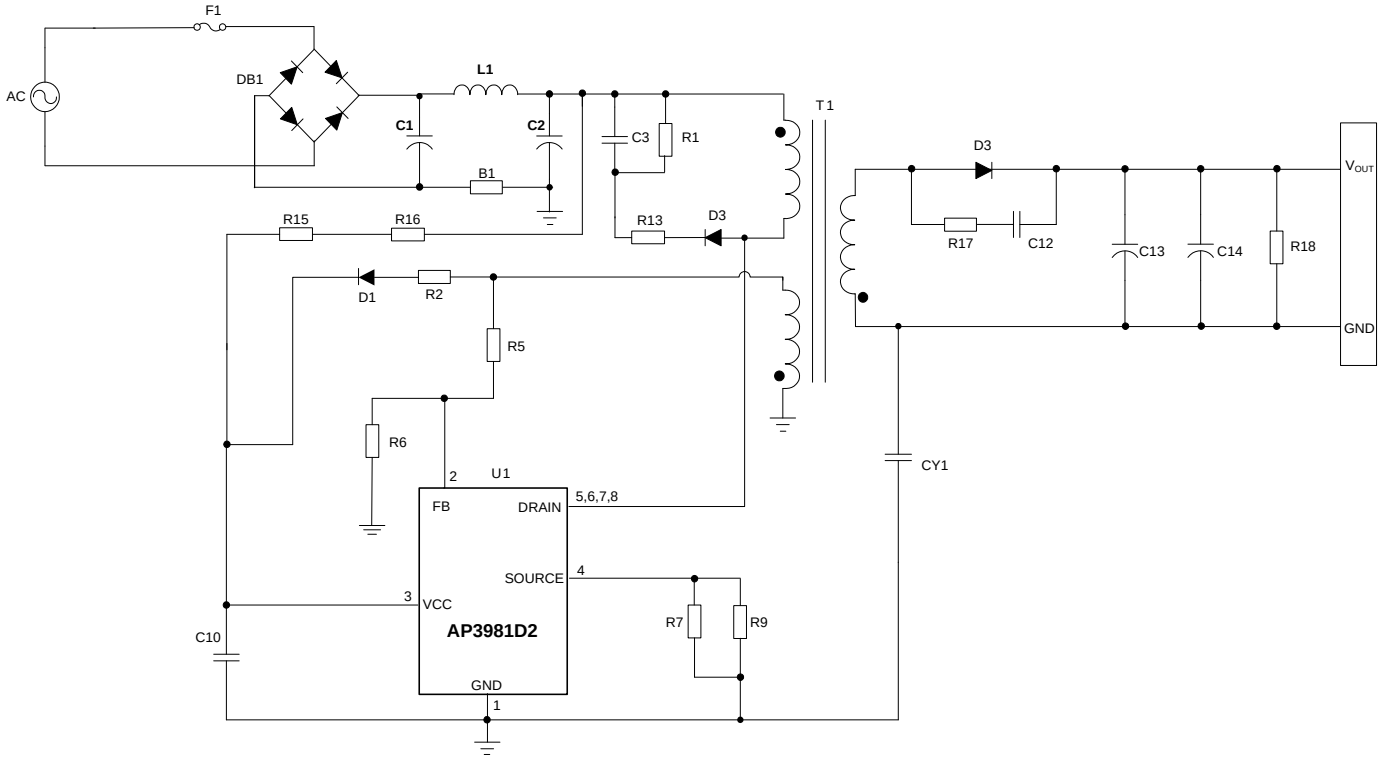
## Applications

- Routers
- Set-Top Box (STB) Power Supply
- Network Adaptors

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.


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## Typical Applications Circuit

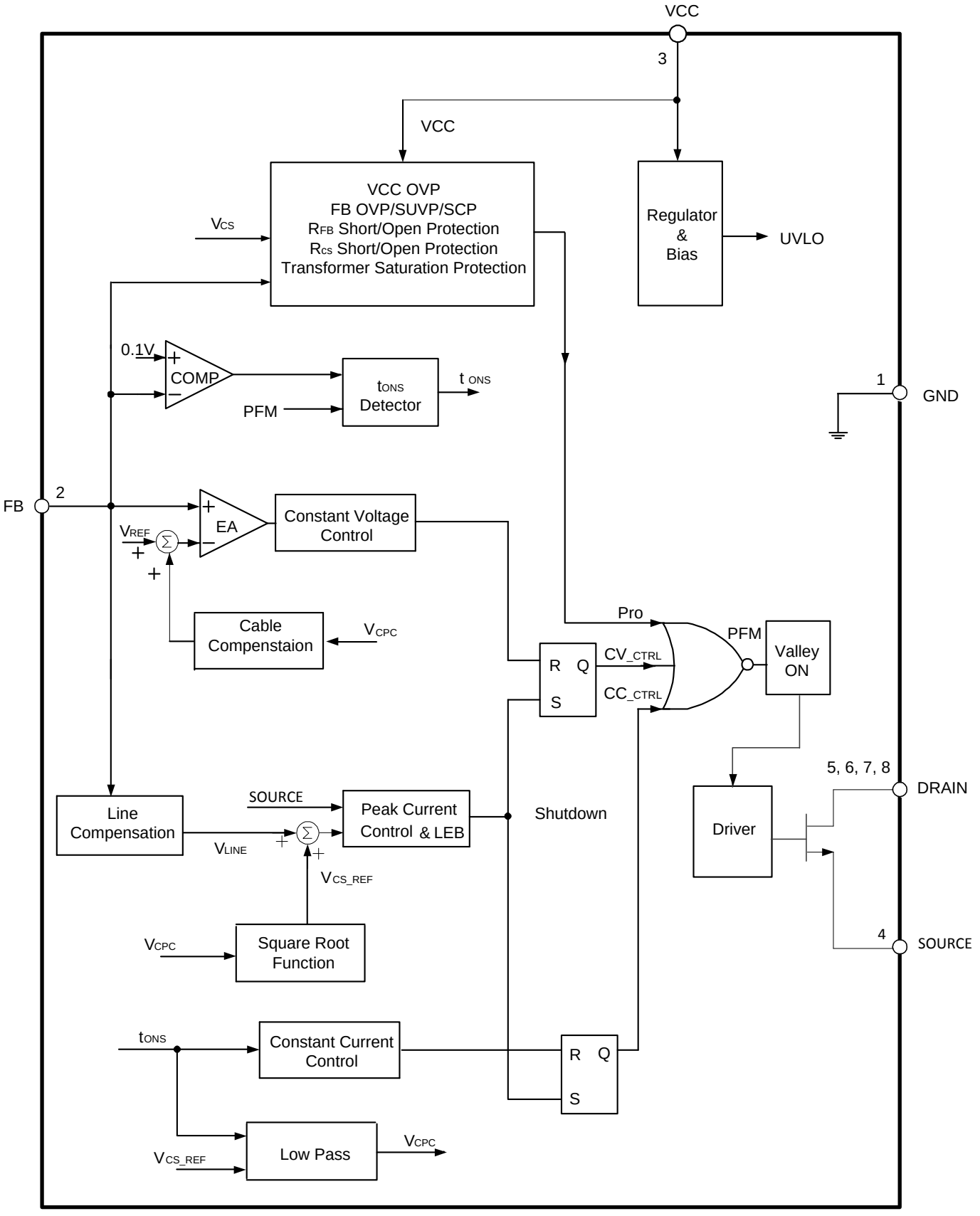



## Pin Descriptions

| Pin Number | Pin Name | Function |
|---|---|---|
| 1 | GND | IC ground |
| 2 | FB | Connect to the auxiliary winding through a divider network. Used as a multi-function pin to realize output voltage sample for CV control, tons detection for CC control, line voltage sense for line compensation, and FB-negative-protection detection. |
| 3 | VCC | IC power supply |
| 4 | SOURCE | SOURCE terminal of the integrated MOSFET |
| 5, 6,7,8 | DRAIN | DRAIN terminal of the integrated MOSFET |


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## Controller Functional Block Diagram





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## Absolute Maximum Ratings (Note 4)

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.3 to 35 | V |
| $V_{SOURCE}$ | SOURCE Input Voltage | -0.3 to 8 | V |
| $V_{FB}$ | FB Input Voltage | -0.3 to 8 | V |
| $V_{DS}$ | Drain-Source Voltage ($T_J$=+25°C) | 650 | V |
| $T_J$ | Operating Junction Temperature | -40 to +150 | °C |
| $T_{STG}$ | Storage Temperature | -65 to +150 | °C |
| $T_{LEAD}$ | Lead Temperature (Soldering, 10 sec) | +300 | °C |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Case) (Note 5) | 3 | °C/W |
| $\Theta_{JA}$ | Thermal Resistance (Junction to Ambient) (Note 5) | 65 | °C/W |
| — | ESD (Human Body Model) | 2000 | V |
| — | ESD (Charged Device Model) | 1000 | V |

Notes:
4. Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods may affect device reliability.
5. Test condition: Device mounted on FR-4 substrate PC board, 2oz copper, with 1in$^2$ cooling area.

## Recommended Operating Conditions

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 10 | 28 | V |
| $T_A$ | Ambient Temperature | -40 | +85 | °C |


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## Electrical Characteristics (@$T_A$ =+25°C, $V_{CC}$ = 15V, unless otherwise specified.)

| Symbol | Parameter | Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| **STARTUP AND UVLO SECTION** | | | | | | |
| $V_{TH_ST}$ | Startup Threshold | — | 14.5 | 16 | 17.5 | V |
| $V_{OPR(MIN)}$ | Minimum Operating Voltage | — | 6.1 | 6.8 | 7.5 | V |
| **STANDBY CURRENT SECTION** | | | | | | |
| $I_{ST}$ | Startup Current | $V_{CC}$=$V_{TH_ST}$-1V before Startup | — | 1 | 3 | μA |
| $I_{CC_OPR}$ | Minimum Operating Current | Static Current | 450 | 550 | 650 | μA |
| **CURRENT SENSE SECTION** | | | | | | |
| $V_{CS_H}$ | Peak Current Sense Threshold Voltage | 40% to 100% CC Load | 560 | 630 | 700 | mV |
| $V_{CS_L}$ | | No Load to 2% CC Load | 160 | 180 | 200 | mV |
| $R_{LINE}$ | Built-In Line Compensation Resistor | — | 45 | 55 | 65 | Ω |
| $t_{LEB}$ | Leading Edge Blanking | — | 370 | 470 | 570 | ns |
| **CONSTANT VOLTAGE SECTION** | | | | | | |
| $V_{FB}$ | Feedback Threshold Voltage | Closed Loop Test of $V_{OUT}$ | 2.35 | 2.4 | 2.45 | V |
| $Ratio_{SAMPLE_L}$ | Sample Ratio | No Load to 2% CC Load | 45 | 50 | 55 | % |
| $Ratio_{SAMPLE_H}$ | Sample Ratio | 40% to 100% CC Load | 75 | 80 | 85 | % |
| **CONSTANT CURRENT SECTION** | | | | | | |
| $t_{ONS}/t_{SW}$ | Below SUVP | Tested @ $V_{FB}$=1V | — | 0.75 | — | — |
| | Above SUVP | Tested @ $V_{FB}$=2V | — | 0.5 | — | — |
| **FREQUENCY JITTER** | | | | | | |
| $\Delta V_{CS}/V_{CS}$ | $V_{CS}$ Modulation | 10% Load to Full Load | 1.5 | 2 | 2.5 | % |
| **Cable Compensation** | | | | | | |
| $V_{CABLE}/V_{OUT}$ | Fixed Cable Compensation Ratio | — | — | 4 | — | % |
| **VALLEY-ON SECTION** | | | | | | |
| $t_{VAL-ON}$ | Valid Off Time of Valley-on | From the End of $t_{ONS}$ | 26 | 32 | 38 | μs |
| **DYNAMIC SECTION** | | | | | | |
| $t_{OFF(MAX)}$ | Maximum Off Time | — | 1.8 | 2 | 2.2 | ms |
| **PROTECTION FUNCTION SECTION** | | | | | | |
| $V_{FB(SOVP)}$ | Overvoltage Protection at FB Pin | — | 3.3 | 3.6 | 3.9 | V |
| $V_{FB(SUVP)}$ | Undervoltage Protection at FB Pin | — | 1.22 | 1.35 | 1.48 | V |
| $t_{DELAY(SUVP)}$ | Delay Time of SUVP | — | 116 | 128 | 140 | ms |
| $V_{FB(SCP)}$ | Output Short Protection at FB Pin | — | 680 | 750 | 820 | mV |
| $t_{DELAY(SCP)}$ | Delay Time of SCP | — | 58 | 64 | 70 | ms |
| $V_{CC(OVP)}$ | Overvoltage Protection at VCC Pin | — | 29.5 | 32 | 34.5 | V |
| $t_{ONP(MAX)}$ | Maximum Turn-on Time | — | 12 | 16 | 20 | μs |
| $V_{CS(MIN)}$ | Minimum Peak Current Sense Voltage at $t_{ONP}$=4μs | — | 120 | 150 | 180 | mV |
| $V_{CS(MAX)}$ | Maximum CS Voltage | — | 720 | 800 | 880 | mV |


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## Electrical Characteristics (continued) (@$T_A$ =+25°C, $V_{CC}$ = 15V, unless otherwise specified.)

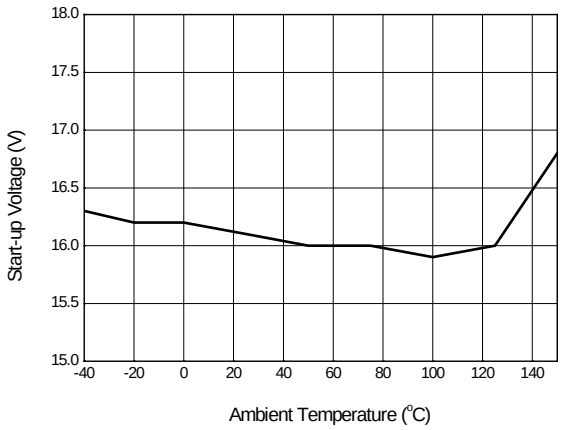
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **PROTECTION FUNCTION SECTION** | | | | | | |
| $V_{FB_NEG_L}$ | Low Threshold for FB Negative Voltage Protection | — | 11 | 14 | 17 | mV |
| $V_{FB_NEG_H}$ | High Threshold for FB Negative Voltage Protection | — | 27 | 36 | 45 | mV |
| $T_{OTP}$ | Shutdown Temperature | — | +130 | +145 | +160 | °C |
| $T_{HYS}$ | Temperature Hysteresis | — | +27 | +30 | +33 | °C |
| **POWER MOSFET SECTION** | | | | | | |
| $BV_{DSS}$ | Integrated MOSFET Drain-Source Break-Down Voltage (Note 6) | — | 650 | — | — | V |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | — | — | 1.7 | 2.5 | Ω |
| $I_D$ | Drain Current -Continuous | — | — | — | 4 | A |

Note: 6. The aging condition of drain-source voltage is 80% of $BV_{DSS}$.

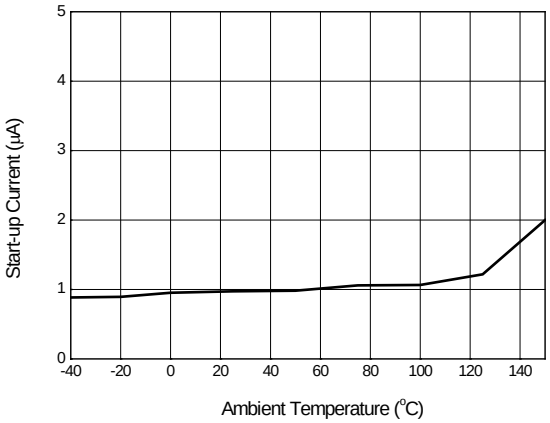

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## Performance Characteristics

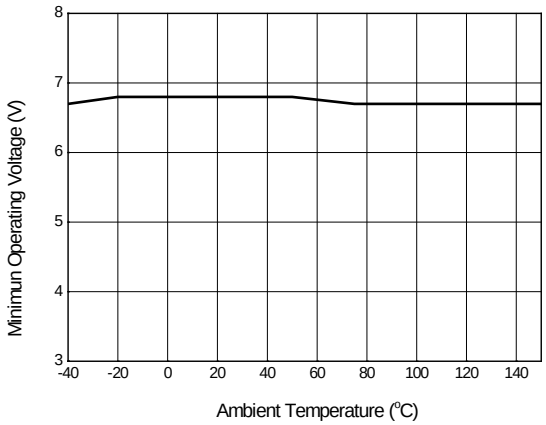
### Start-Up Voltage vs. Ambient Temperature



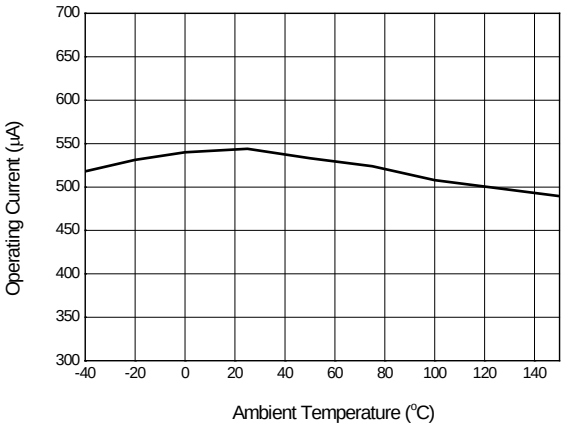

### Start-Up Current vs. Ambient Temperature



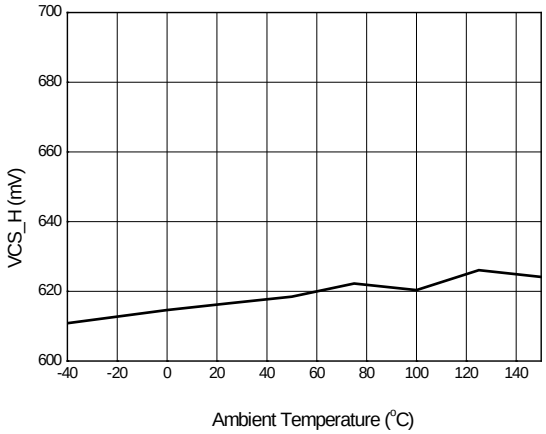

### Minimal Operating Voltage vs. Ambient Temperature



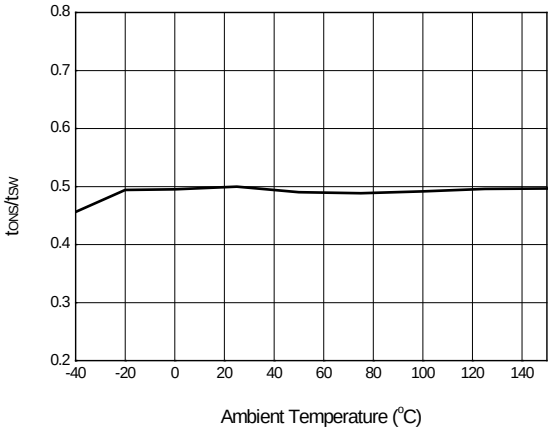

### Operating Current vs. Ambient Temperature




### $V_{CS_H}$ vs. Ambient Temperature




### $t_{ONS}/t_{SW}$ Above SUVP vs. Ambient Temperature

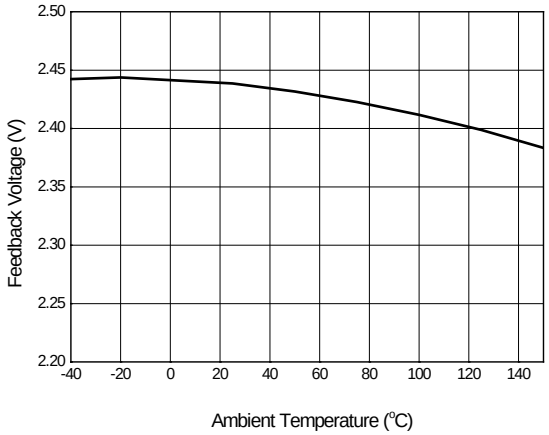




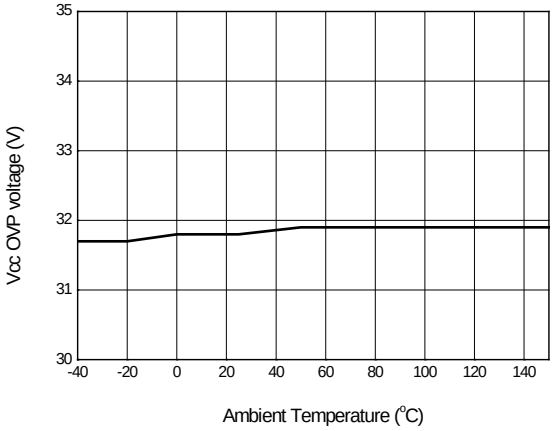
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## Performance Characteristics (continued)

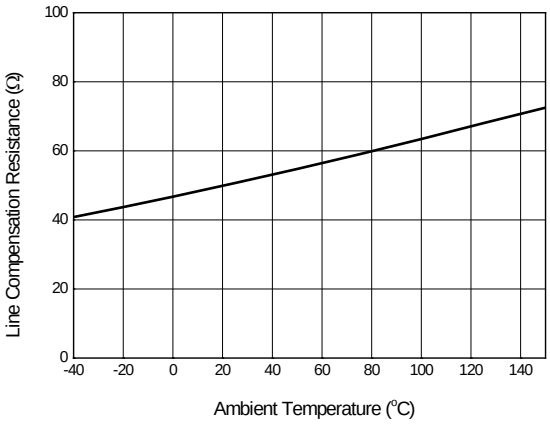
### Feedback Voltage vs. Ambient Temperature



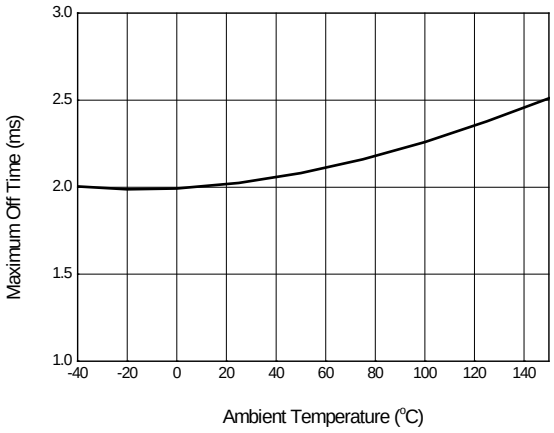

### $V_{CC}$ OVP Voltage vs. Ambient Temperature



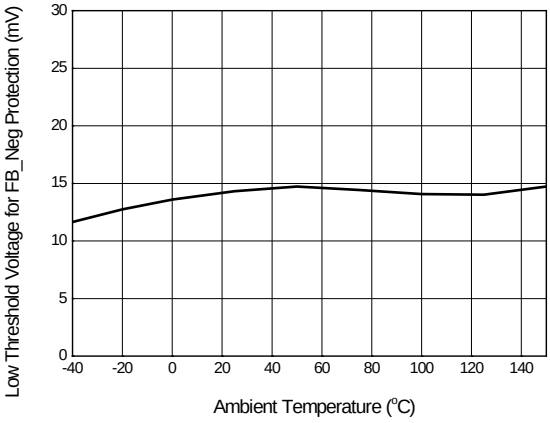

### Line Compensation Resistance vs. Ambient Temperature



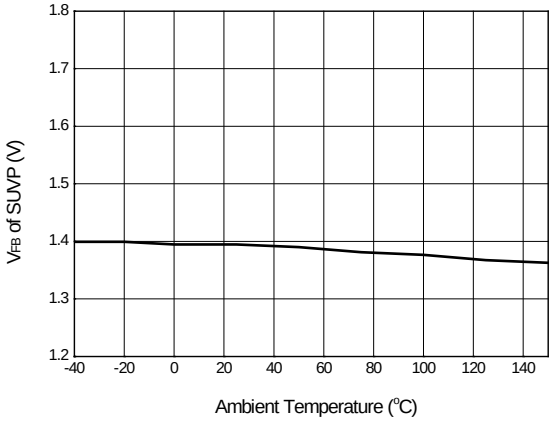

### Maximum Off Time vs. Ambient Temperature




### Low Threshold Voltage for FB_Negative Protection vs. Ambient Temperature




### Feedback Voltage of SUVP vs. Ambient Temperature





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## Operation Principle Description

### 1. The Conventional PSR Operating Waveforms

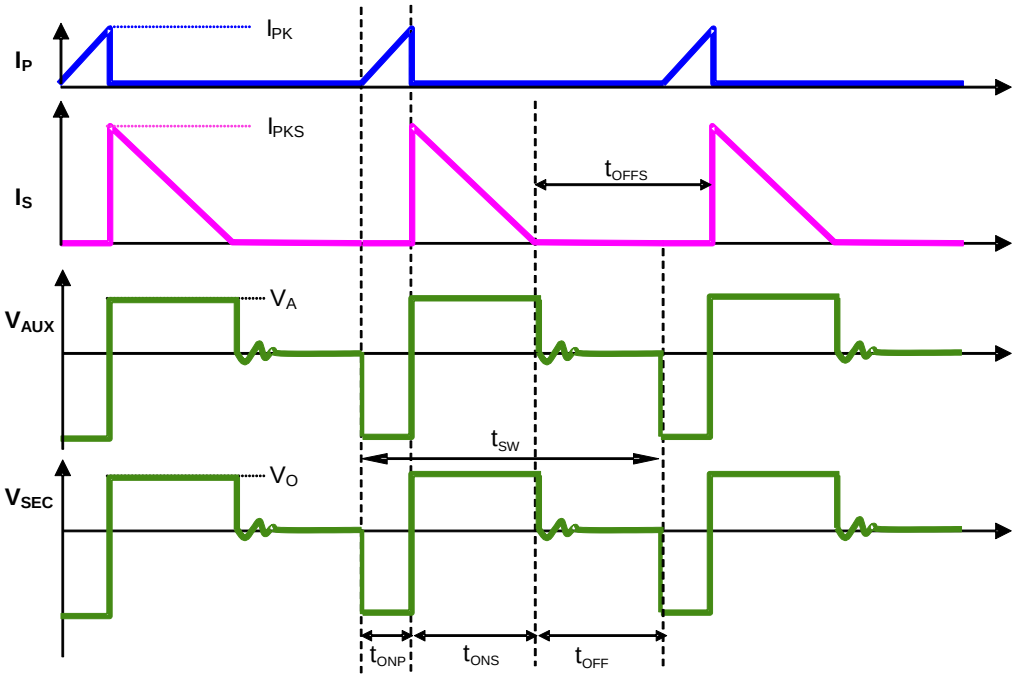



Figure 1: The Operation Waveform of Flyback PSR System

Figure 1 shows the typical waveforms which demonstrate the basic operating principle of AP3981D2 application. The parameters are defined as:

**$I_P$** — The primary side current
**$I_S$** — The secondary side current
**$I_{PK}$** — Peak value of primary side current
**$I_{PKS}$** — Peak value of secondary side current
**$V_{SEC}$** — The transient voltage at secondary winding
**$V_O$** — The output voltage
**$V_{AUX}$** — The transient voltage at auxiliary winding
**$V_A$** — The stable voltage at auxiliary winding when rectification diode is in conducting status, which equals the sum of voltage $V_{CC}$ and the forward voltage drop of auxiliary diode
**$t_{SW}$** — The period of switching frequency
**$t_{ONP}$** — The conduction time when primary side switch is “ON”
**$t_{ONS}$** — The conduction time when secondary side diode is “ON”
**$t_{OFF}$** — The dead time when neither primary side switch nor secondary side diode is “ON”
**$t_{OFFS}$** — The time when secondary side diode is “OFF”

For primary-side regulation, the primary current ip(t) is sensed by a current sense resistor $R_{CS}$ connected to PIN 4.The current rises up linearly at a rate of:

(1)

$$\frac{dip(t)}{dt} = \frac{V_{IN}(t)}{L_M}$$


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## Operation Principle Description (continued)

As shown in Figure 1, when the current ip(t) rises up to $I_{PK}$, the primary MOSFET turns off. The constant peak current is given by:

(2)

$$I_{PK} = \frac{V_{CS}}{R_{CS}}$$

Therefore, the energy stored in the magnetizing inductance $L_M$ each cycle is:

(3)

$$Eg = \frac{1}{2} \times L_M \cdot {I_{PK}}^2$$

So the power transferring from the input to the output is given by:

(4)

$$P = \frac{1}{2} \times L_M \times {I_{PK}}^2 \times f_{SW}$$

Where the $f_{SW}$ is the switching frequency. When the peak current $I_{PK}$ is constant, the output power depends on the switching frequency $f_{SW}$.

**2. Constant Voltage Operation**

The output voltage is proportional to the auxiliary winding voltage during $t_{ONS}$ period indicated by Equation 5, this auxiliary winding voltage is divided by resistors $R_{FB1}$ and $R_{FB2}$ (refer to Figure 5) before inputting to the FB PIN. As shown in Figure 2, AP3981D2 detects the FB voltage at the end of $t_{SAMPLE}$ during $t_{ONS}$ period, the detected voltage that reflects the output voltage is regulated to $V_{FB}$ of 2.4V with the help of the constant voltage control block in AP3981D2. For system design, adjust the ratio of $R_{FB1}$ and $R_{FB2}$ can get the target output voltage value.

(5)

$$V_{AUX} = \frac{N_{AUX}}{N_S} \times (Vo + Vd)$$

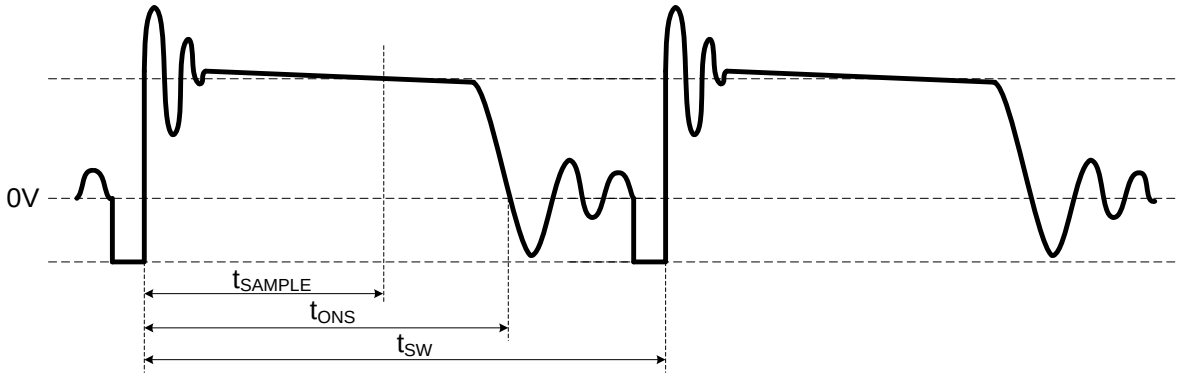



Figure 2: Auxiliary Voltage Waveform

**3. Constant Current Control**

In AP3981D2, Equation 6 shows the related parameters that determine the output current. To get a constant output current, the $V_{CS}$ and $t_{ONS}/t_{SW}$ is fixed in AP3981D2 during CC mode. Meanwhile, a reliable control logic is integrated within AP3981D2 to ensure the system swift smoothly between CC mode and CV mode.

(6)

$$Iout = \frac{1}{2} * \frac{Np}{Ns} * Ipk * \frac{t_{ONS}}{t_{SW}} = \frac{1}{2} * \frac{Np}{Ns} * \frac{Vcs}{Rcs} * \frac{t_{ONS}}{t_{SW}}$$

**4. Multiple Segment Peak Current**

In the original PFM PSR system, the switching frequency decreases with the decreasing output current, which will encounter audible noise issue when switching frequency decreases below 20kHz.


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## Operation Principle Description (cont.)

In order to avoid audible noise issue and a big drop in efficiency at light load, AP3981D2 uses a three-segment primary peak current control method at CV mode, the current sense threshold voltage is piecewise defined—as shown in Figure 3, the low threshold $V_{CS_L}$ is set under 2% CC load, the high threshold $V_{CS_H}$ is set above 40% CC load—within the range from 2% to 40%, the threshold $V_{CS_M}$ increases based on the load condition, and the $V_{CS_M}$ is carefully calculated inside AP3981D2 to make the system operate at a reasonable switching frequency, which rises above 20kHZ at a varying slope.

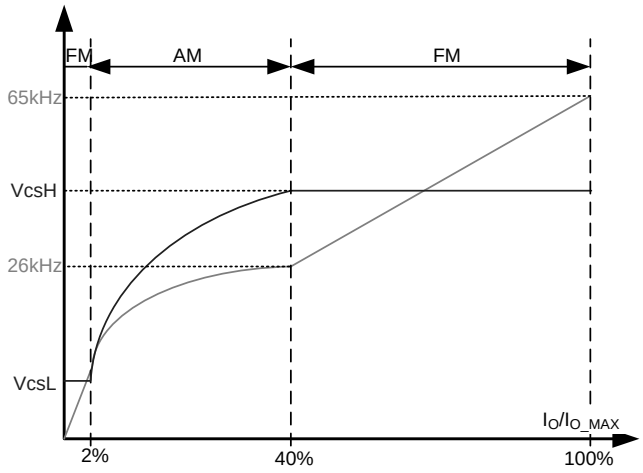



Figure 3. Segment Peak Current and Operating Frequency at CV Mode

**5. Sample Time**

As shown in Equation 5 and Figure 2, the detected auxiliary voltage reflects the output voltage. To be compatible with different system designs and avoid the turn-off ringing voltage influence on CV sampling, the $t_{SAMPLE}$ is designed to be proportional of $t_{ONS}$. On the other hand, to alleviate the Vd effect on the accuracy of Vout, the sample ratio of $t_{SAMPLE}$ to $t_{ONS}$ varies according to load condition. The $t_{SAMPLE}$ is usually 50% of $t_{ONS}$ for the below 2% CC load conditions and 80% of $t_{ONS}$ for the above 40% CC load conditions, within the range from 2% to 40% loading, the sample ratio rises linearly from 50% to 80%.

**6. Capacitive Load Start-Up Capability**

In order to achieve fast start-up for capacitive load startup applications, AP3981D2 induces a two-level CC point design during start-up time. The output voltage rises after power on, when the detected output voltage is lower than SUVP point, the $t_{ONS}/t_{SW}$ is set to be 0.75, which means output constant current is 1.5 times of normal output constant current. When the output voltage rises above SUVP point, the $t_{ONS}/t_{SW}$ is switched to the normal value of 0.5.

**7. Leading Edge Blanking**

When the power switch is turned on, a turn-on spike voltage will occur on the $V_{CS}$ sense resistor. To avoid false-termination of the switching pulse, a fixed 470ns leading-edge blanking time is built in. During this blanking period, the current sense comparator is disabled and the primary MOSFET cannot be turned off.

**8. Valley Turn-On**

When the off time ($t_{OFF}$) is shorter than $t_{VAL-ON}$, the AP3981D2 power system can work with valley turn-on. It can reduce the switching on power losses and achieve high overall efficiency. At the same time, because of valley turn-on the switching frequency has the random jitter feature, which will be of benefit to conductive EMI performance. The valley turn-on can also reduce the power switch turn on spike current and then achieve the better radiative EMI performance.


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## Operation Principle Description (cont.)

### 9. $V_{CS}$ Jitter

Even though the valley turn on function produces the random frequency jitter feature, an active frequency jitter function is added in the AP3981D2. The active frequency dithering is realized by applying variation on $V_{CS}$ reference ($V_{CS_REF}$). The $V_{CS_REF}$ is changed every 2 cycles and the period of variation is 12 cycles, which is shown as Figure 4. The variation between $V_{CS4}$ and $V_{CS1}$ is ±2% using the mean level as a reference.

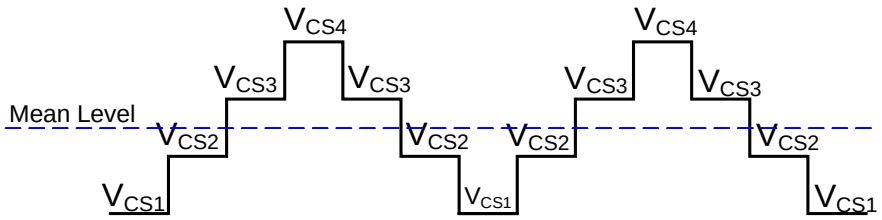



Figure 4: $V_{CS}$ Jitter

### 10. Adjustable Line Compensation

In real system, there exists a delay time, from the $V_{SOURCE}$ reach the inner $V_{CS}$ threshold to the actual switch turn off point. The delay time contains the propagation time of the inner comparator and the driver delay, and it does not change with line voltage. The delay time leads to different primary peak current under different line voltage, which results in different output current in CC mode.

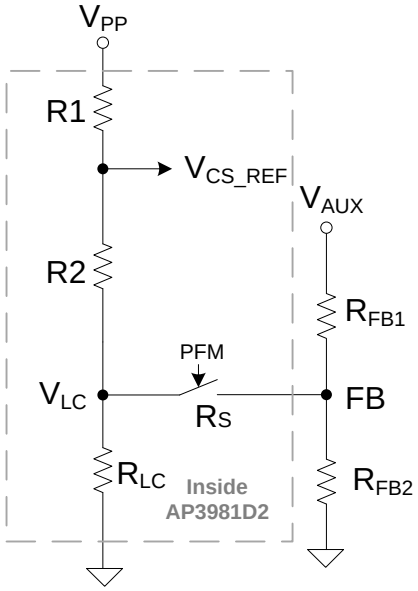



Figure 5: Line Compensation Control Circuit

In order to alleviate the difference under the universal input voltage, AP3981D2 integrated the line compensation control circuit shown as figure 5. During the primary on stage, an inner switcher $R_S$ switches on, the $R_{LC}$ is much smaller compared with $R_{FB2}$, so the $R_{FB2}$'s effect on line compensation can be neglected, the proportional line voltage is detected through $R_{FB1}$ and $R_{LC}$ and is added to the $V_{CS}$ threshold ($V_{CS_REF}$). The $V_{LC}$ can be derived from the Equation 7:

$$V_{LC} = \frac{\frac{R_{FB1}}{3*R2} * V_{PP} - V_{AUX}}{1 + \frac{R_{FB1}}{3*R2} + \frac{R_{FB1}}{R_{LC}}} \quad (7)$$


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## Operation Principle Description (cont.)

The final compensated $V_{CS}$ is:

$$V_{CS_REF} = \frac{1}{3} * V_{PP} + \frac{2}{3} * V_{LC} \quad (8)$$

In the above equations, $V_{PP}$ is 1.8V at CC mode, $R_{LC}$ is 55Ω, R2 is 60kΩ, R1 is two times of R2, $V_{AUX}$ is the value of the auxiliary winding voltage during primary-on period, which proportional to bus voltage. Based on the equation, it can be concluded that a smaller $R_{FB1}$ results in deeper line compensation. If the delay time, $t_{DELAY}$, is known—typically 150ns in AP3981D2, the $R_{FB1}$ can be calculated as a reference for the system design.

### 11. Protection

AP3981D2 provides versatile protections to prevent the system from damage under various fault conditions. Most protections trigger auto-recovery mode in which the system restarts as soon as the $V_{CC}$ drops to $V_{OPR(MIN)}$. When the fault conditions are removed, the system recovers to normal operation automatically.

#### $V_{CC}$ OVP

A $V_{CC}$ OVP threshold is set to protect the IC from damage. When the $V_{CC}$ OVP protection is triggered, the IC stops outputting drive signal immediately, and the system enters auto-recovery mode.

#### Output Overvoltage Protection (SOVP)

As previously described, the FB pin voltage during tons reflects the output voltage proportionally. This voltage can be used to realize SOVP. AP3981D2 sets a higher threshold, $V_{FB(OVP)}$, to shutdown the system if the sampled voltage reaches the threshold continuously for three switching cycles. The SOVP is then triggered, and the system enters auto-recovery mode.

#### Output Undervoltage Protection (SUVP)

Like SOVP, the AP3981D2 also integrated the SUVP protection. If the detected voltage on FB pin is lower than $V_{FB(SUVP)}$ for 128ms, the SOVP is triggered, and the system enters auto-recovery mode.

#### Output Short Protection (SCP)

A much lower threshold is set on FB pin to protect the system when output short condition occurs. If the detected FB voltage is lower than 0.78V for 64ms, the SCP is triggered, and the system enters auto-recovery mode.

#### Transformer Anti-Saturation Protection

Under some fault conditions or bad system design, the transformer may approach saturation, and the current increases dramatically. To avoid power device damage due to transformer saturation, AP3981D2 integrates a maximum $V_{CS}$ threshold $V_{CS(MAX)}$ to protect the system. If there are three consecutive pulses where $V_{CS}$ exceeds the threshold, the controller shuts down and enters auto-recovery mode.

#### Overtemperature Protection (OTP)

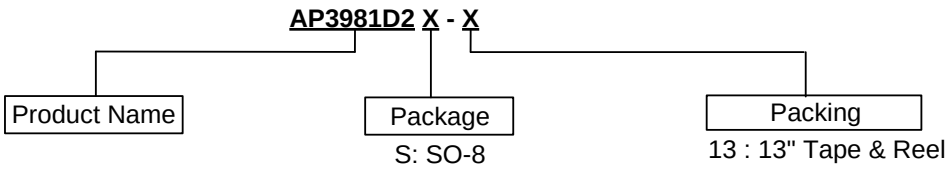
If the IC junction temperature exceeds the threshold of $T_{OTP}$, AP3981D2 shuts down immediately and enters auto-recovery mode. Note that even when the $V_{CC}$ reaches $V_{TH_ST}$, the IC does not output any drive pulse until the junction temperature falls at a hysteresis temperature of +30°C.

#### Brown-In/ Brown-Out Protection

AP3981D2 detects the bus voltage at each switching cycle through FB pin during $t_{ONP}$ period. When the $V_{CC}$ reaches $V_{TH_ST}$ after power on, AP3981D2 outputs one switching pulse to check if the detected bus voltage on FB pin is higher than $V_{FB_NEG_H}$. In this case, the system starts up normally; otherwise, AP3981D2 stops outputting following pulses. The $V_{CC}$ then drops below $V_{OPR(MIN)}$, and the system repeats the process described above until the detected FB voltage is higher than $V_{FB_NEG_H}$. When the power is off or there is a ditch in bus voltage, and if the detected voltage is lower than $V_{FB_NEG_L}$ for three consecutive switching cycles, the IC shuts down and enters auto-recovery mode. This function is very useful when the bulk capacitor is open or when the heavy load suddenly releases after power off.


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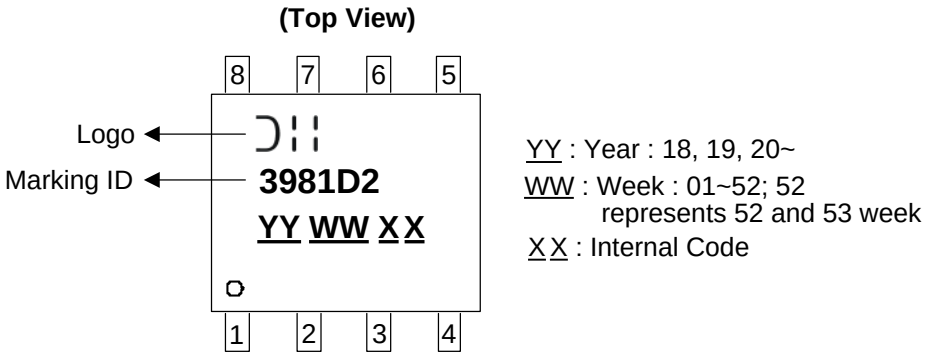
## Ordering Information




| Package | Part Number | Marking ID | 13'Tape and Reel | |
|---|---|---|---|---|
| | | | Quantity | Part Number Suffix |
| SO-8 | AP3981D2S-13 | 3981D2 | 4000/Tape and Reel | -13 |

## Marking Information

**SO-8**



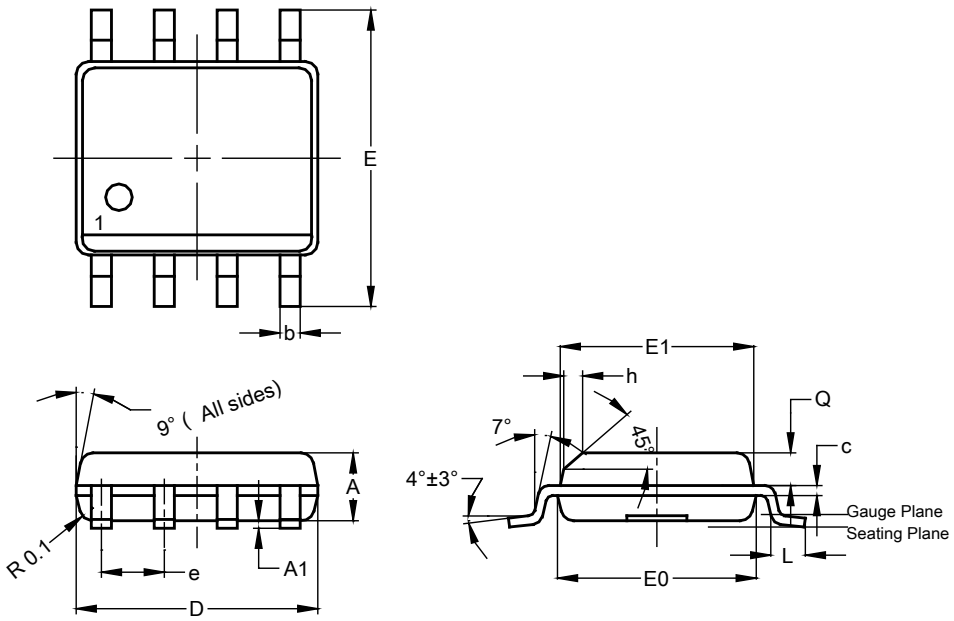


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## Package Outline Dimensions (All dimensions in mm (inch).)

Please see http://www.diodes.com/package-outlines.html for the latest version.

**SO-8**

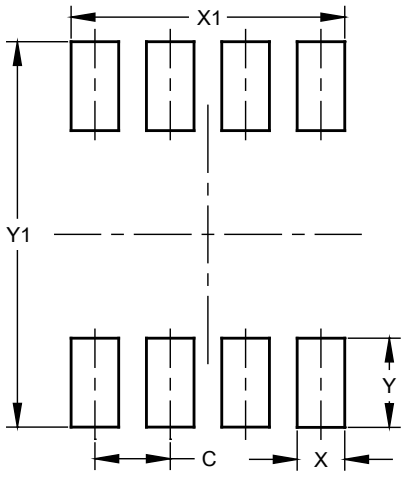



| SO-8 | | | |
|---|---|---|---|
| **Dim** | **Min** | **Max** | **Typ** |
| **A** | 1.40 | 1.50 | 1.45 |
| **A1** | 0.10 | 0.20 | 0.15 |
| **b** | 0.30 | 0.50 | 0.40 |
| **c** | 0.15 | 0.25 | 0.20 |
| **D** | 4.85 | 4.95 | 4.90 |
| **E** | 5.90 | 6.10 | 6.00 |
| **E1** | 3.80 | 3.90 | 3.85 |
| **E0** | 3.85 | 3.95 | 3.90 |
| **e** | — | — | 1.27 |
| **h** | — | — | 0.35 |
| **L** | 0.62 | 0.82 | 0.72 |
| **Q** | 0.60 | 0.70 | 0.65 |
| **All Dimensions in mm** | | | |

## Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

**SO-8**




| Dimensions | Value (in mm) |
|---|---|
| **C** | 1.27 |
| **X** | 0.802 |
| **X1** | 4.612 |
| **Y** | 1.505 |
| **Y1** | 6.50 |

**Note:** The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary depending on application. These dimensions may be modified based on user equipment capability or fabrication criteria. A more robust pattern may be desired for wave soldering and is calculated by adding 0.2 mm to the 'Z' dimension. For further information, please reference document IPC-7351A, Naming Convention for Standard SMT Land Patterns, and for International grid details, please see document IEC, Publication 97.

**Note:** For high voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.


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