ALPHA & OMEGA SEMICONDUCTOR

AON3414

30V N-Channel AlphaMOS

General Description

- Trench Power AlphaMOS (αMOS LV) technology
- Low $R_{DS(ON)}$
- High Current Capability
- RoHS and Halogen-Free Compliant

Applications

- System switch, inverter

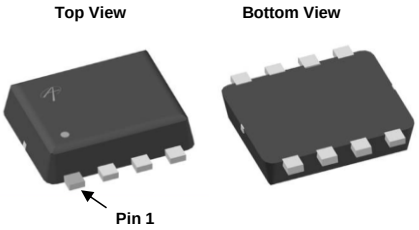
Product Summary

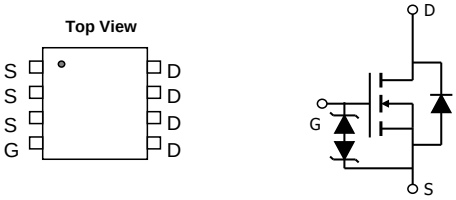
V_{DS}	30V
I_D (at V_{GS}=10V)	10.5A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 17mΩ
$R_{DS(ON)}$ (at V_{GS}=4.5V)	< 23mΩ
Typical ESD protection	**HBM Class 2**

100% Rg Tested

Green Product

DFN 3x3





Orderable Part Number	Package Type	Form	Minimum Order Quantity
AON3414	DFN 3x3	Tape & Reel	3000

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A=25°C	I_D	10.5	A
	T_A=70°C		8	
Pulsed Drain Current [C]		I_{DM}	42	
Power Dissipation [B]	T_A=25°C	P_D	3.1	W
	T_A=70°C		2	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	30	40	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		55	70	°C/W
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	20	25	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	ID=250µA, VGS=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±16V			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=$V_{GS,}$ I_D=250µA	1.2	1.8	2.4	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=9A		14	17	mΩ
		T_J=125°C		20.5	25	
		V_{GS}=4.5V, I_D=8A		18	23	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=9A		35		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.72	1	V
I_S	Maximum Body-Diode Continuous Current				4	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		690		pF
C_{oss}	Output Capacitance			105		pF
C_{rss}	Reverse Transfer Capacitance			80		pF
R_g	Gate resistance	f=1MHz	0.5	1.1	2.0	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=9A		15	25	nC
Q_g(4.5V)	Total Gate Charge			7.5	14	nC
Q_{gs}	Gate Source Charge			2.5		nC
Q_{gd}	Gate Drain Charge			3		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=1.67Ω, R_{GEN}=3Ω		5		ns
t_r	Turn-On Rise Time			3.5		ns
$t_{D(off)}$	Turn-Off DelayTime			19		ns
t_f	Turn-Off Fall Time			3.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=9A, dI/dt=500A/µs		7.5		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=9A, dI/dt=500A/µs		11.5		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using ≤ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initialT_J=25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

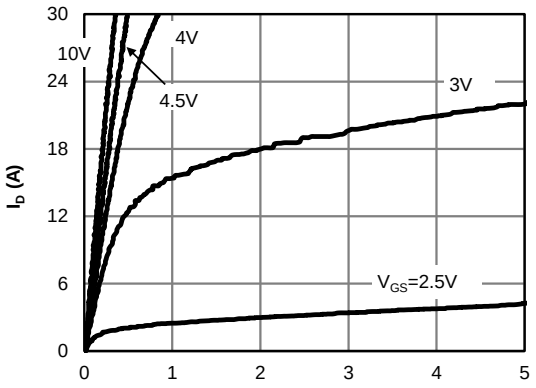


Figure 1: On-Region Characteristics (Note E)

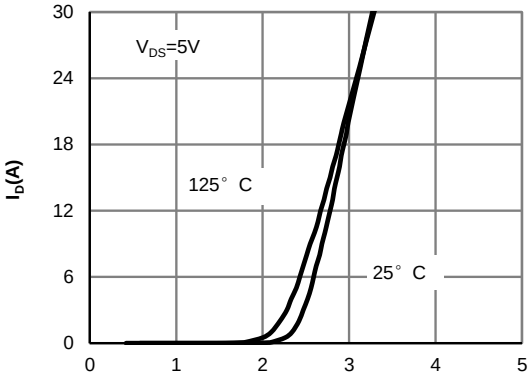


Figure 2: Transfer Characteristics (Note E)

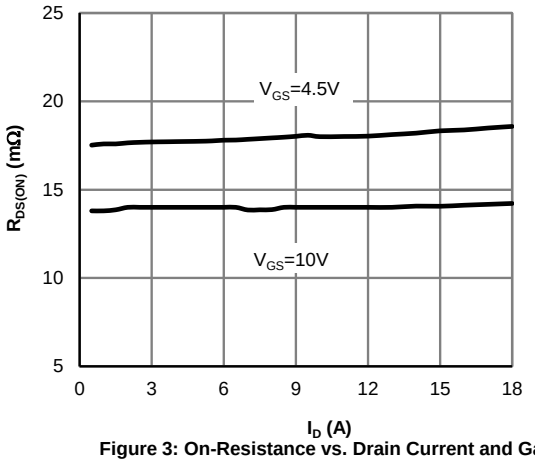


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

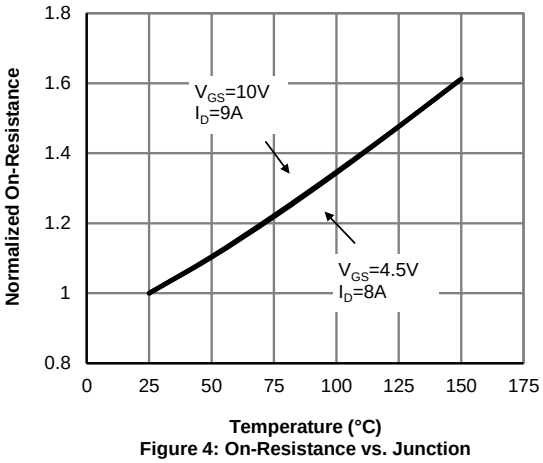


Figure 4: On-Resistance vs. Junction Temperature (Note E)

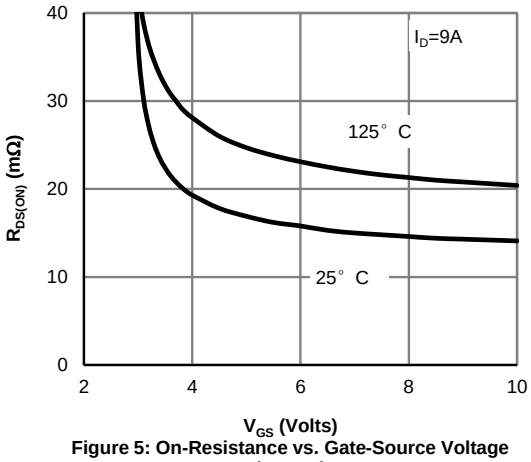


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

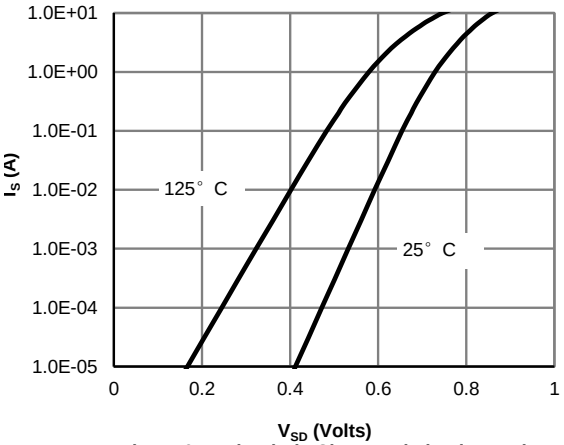


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

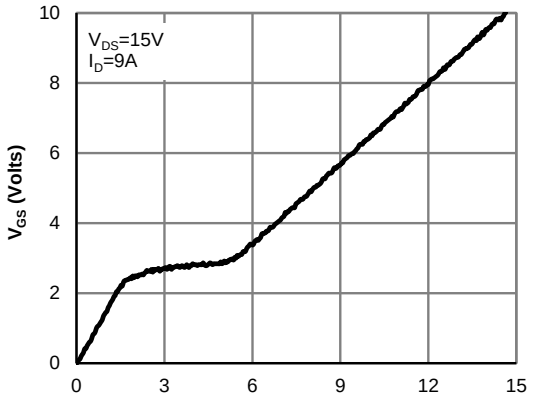


Figure 7: Gate-Charge Characteristics

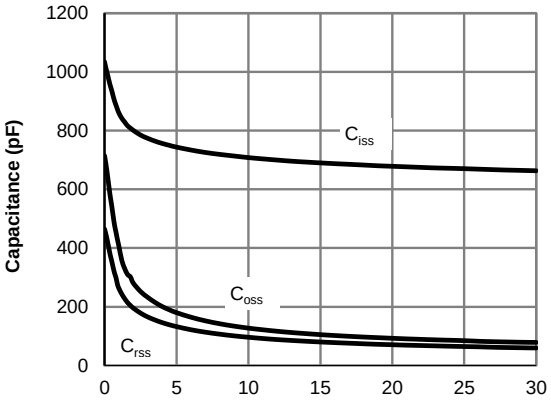
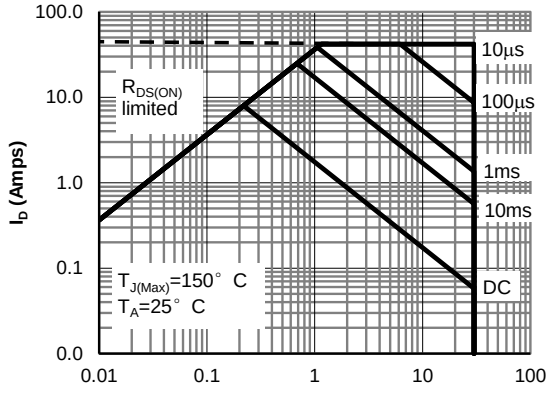


Figure 8: Capacitance Characteristics



V_{GS}> or equal to 4.5V

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

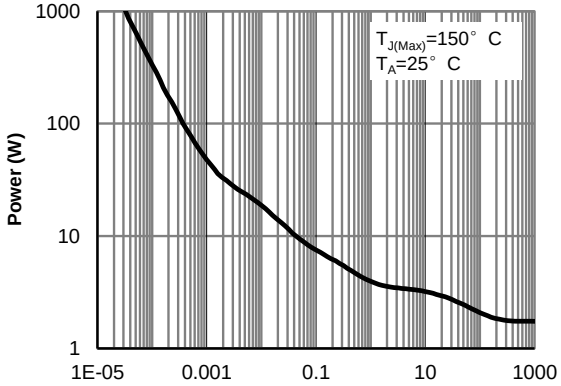


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

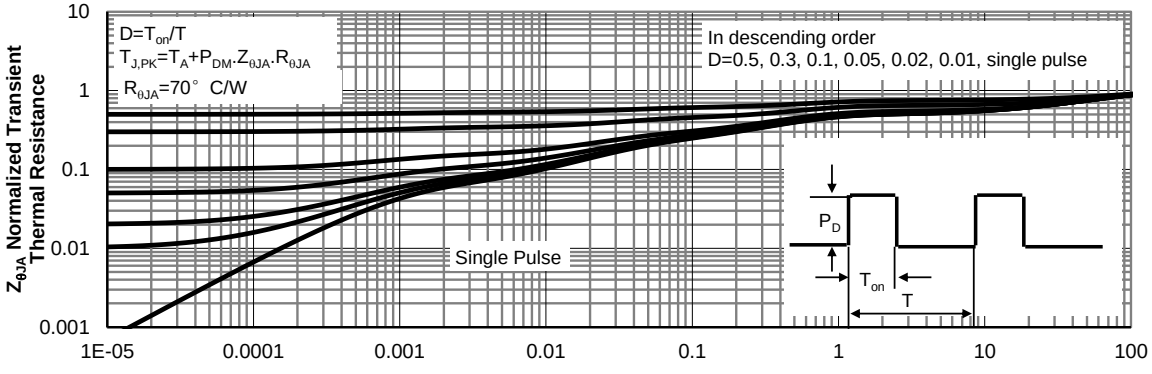
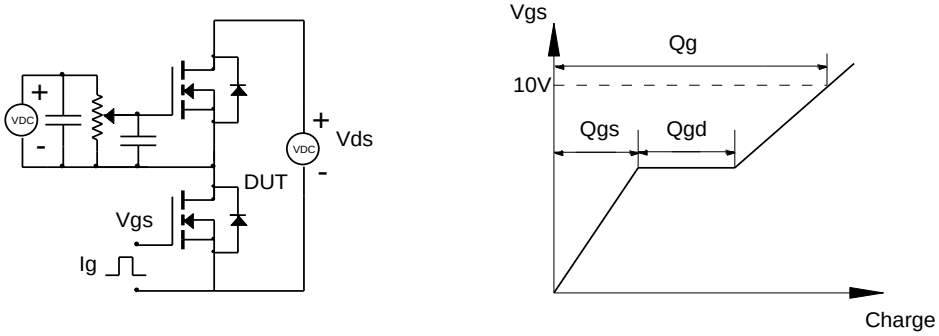
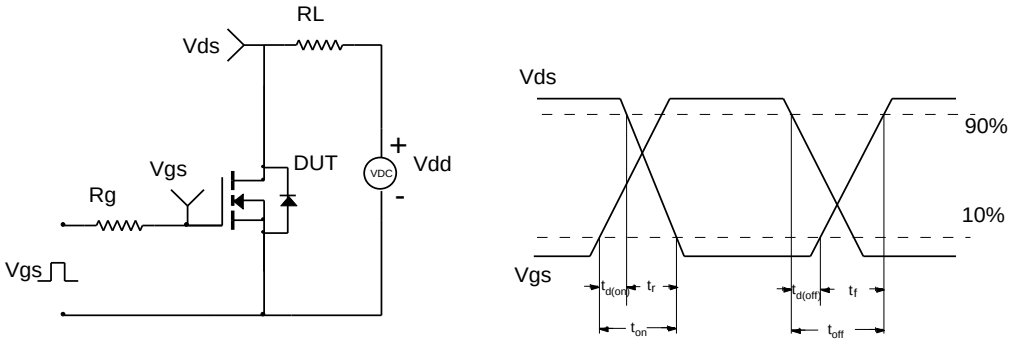


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

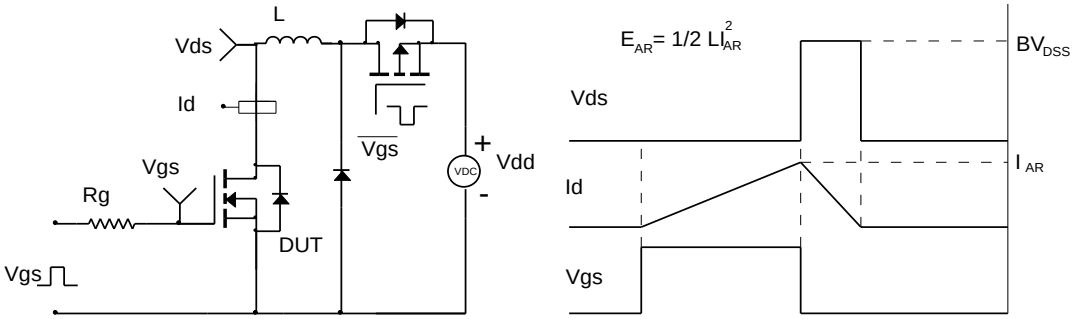
Gate Charge Test Circuit & Waveform



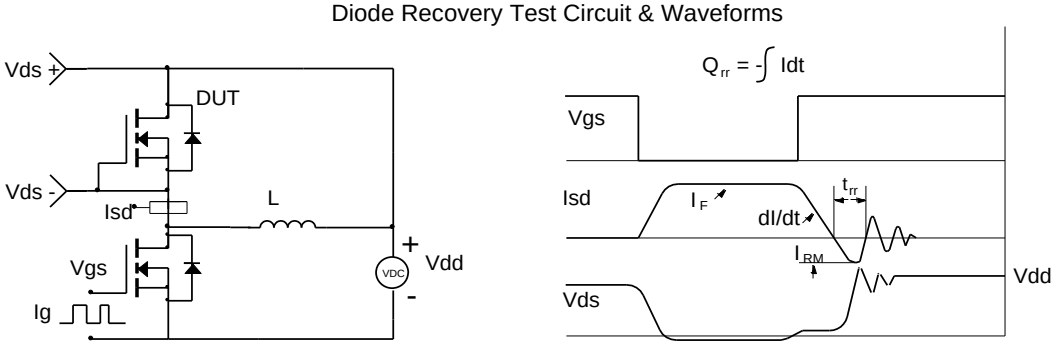
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



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