UMW FDD6676AS

30V N-Channel MOSFET

1.Features

- $V_{DS(V)}$=30V
- I_D=90A
- $R_{DS(ON)}$<5.7mΩ(V_{GS}=10V)
- $R_{DS(ON)}$<7.1mΩ(V_{GS}=4.5V)
- Low gate charge (46nC typical)
- High power and current handling capability

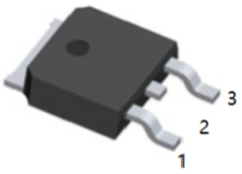
2.Applications

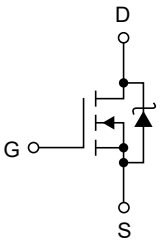
- DC/DC converter
- Low side notebook

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-252(DPAK)
top view





4.Absolute Maximum Ratings T_A= 25°C

Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DSS}	30	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current - Continuous	(Note 3)	I_D	90	A
-Pulsed	(Note 1a)		100	A
Power Dissipation for Single Operation	(Note 1)	P_D	70	W
	(Note 1a)		3.1	W
	(Note 1b)		1.3	W
Operating and Storage Junction Temperature Range		T_J, T_{STG}	-55 to 150	°C

5.Thermal Characteristics

Parameter		Symbol	Rating	Units
Thermal Resistance, Junction-to-Case	(Note 1)	$R_{\theta JC}$	1.8	°C/W
Thermal Resistance, Junction-to-Ambient	(Note 1a)	$R_{\theta JA}$	40	°C/W
Thermal Resistance, Junction-to-Ambient	(Note 1b)	$R_{\theta JA}$	96	°C/W

6.Electrical Characteristic (T_A=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Energy	W_{DSS}	Single Pulse,V_{DD}=15V, I_D=16A		108	250	mJ
Drain-Source Avalanche Current	I_{AR}				16	A
Drain–Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=1mA	30			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D=10mA Referenced to 25°C		31		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=24V, V_{GS}=0V			500	μA
Gate–Body Leakage	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=1mA	1	1.5	3	V
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I_D=10mA Referenced to 25°C		-3.6		mV/°C
Static Drain–Source On–Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=16A		4.7	5.7	mΩ
		V_{GS}=4.5V, I_D=15A		5.8	7.1	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V, I_D=16A		61		S
Input Capacitance	C_{iss}	V_{DS}=15V, V_{GS}=0V, f=1MHz		2500		pF
Output Capacitance	C_{oss}			710		pF
Reverse Transfer Capacitance	C_{rss}			270		pF
Gate Resistance	R_g	V_{GS}=0V, f=1MHz		1.6		Ω
Turn–On Delay Time	$t_{D(on)}$	V_{DD}=15V, I_D=1A V_{GS}=10V, R_{GEN}=6Ω		12	21	ns
Turn–On Rise Time	t_r			12	22	ns
Turn–Off Delay Time	$t_{D(off)}$			46	74	ns
Turn–Off Fall Time	t_f			28	44	ns
Turn–On Delay Time	$t_{D(on)}$	V_{DD}=15V, I_D=1A V_{GS}=4.5V, R_{GEN}=6Ω		20	32	ns
Turn–On Rise Time	t_r			24	38	ns
Turn–Off Delay Time	$t_{D(off)}$			35	56	ns
Turn–Off Fall Time	t_f			27	43	ns

Total Gate Charge, V_{GS}=10V	$Q_{g(TOT)}$	V_{DS}=15V,I_D=16A		46	64	nC
Total Gate Charge, V_{GS}=5V	Q_g			25	35	nC
Gate–Source Charge	Q_{gs}			7		nC
Gate–Drain Charge	Q_{gd}			9		nC
Maximum Continuous Drain–Source Diode Forward Current	I_S				3.5	A
Drain–Source Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=3.5A (Note 2)		0.4	0.7	V
Diode Reverse Recovery Time	t_{rr}	dIF/dt=300A/μs, I_F=16A		25		ns
Maximum Recovery Current	I_{RM}			1.9		A
Diode Reverse Recovery Charge	Q_{rr}			24		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.

$R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $R_{\theta JA}$=40°C/W when mounted on a 1in^2 pad of 2oz copper.



b) $R_{\theta JA}$= 96°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

3. Maximum current is calculated as: $\sqrt{\frac{P_D}{R_{DS(ON)}}}$

where P_D is maximum power dissipation at T_C=25°C and $R_{DS(ON)}$ is at $T_{J(max)}$ and V_{GS}=10V. Package current limitation is 21A.

7.1Typical characteristic

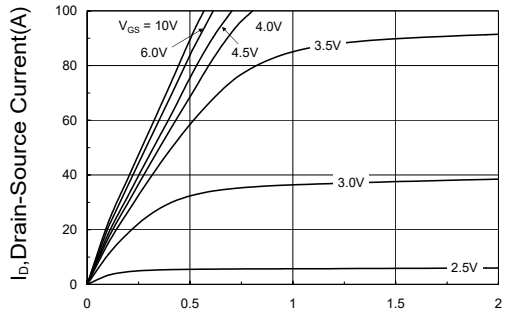


Figure 1: On-Region Characteristics

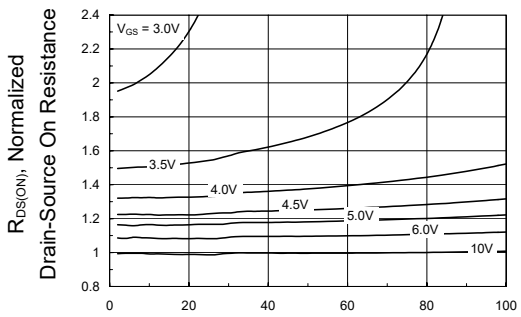


Figure 2: On-Resistance Variation with Drain Current and Gate Voltage

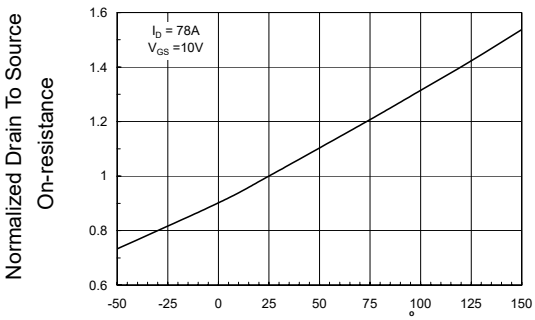


Figure 3: On-Resistance Variation with Temperature

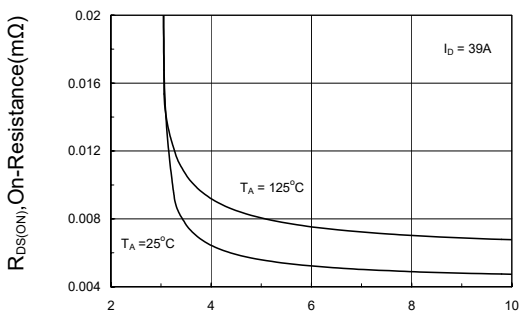


Figure 4: On-Resistance Variation with Gate-to-Source Voltage

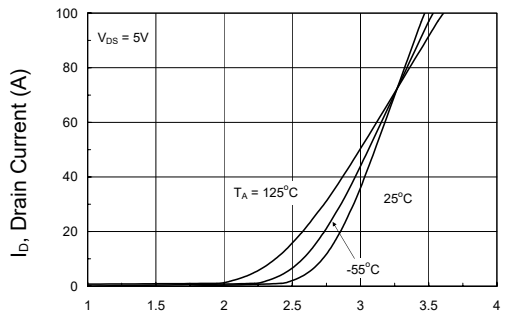


Figure 5: Transfer Characteristics

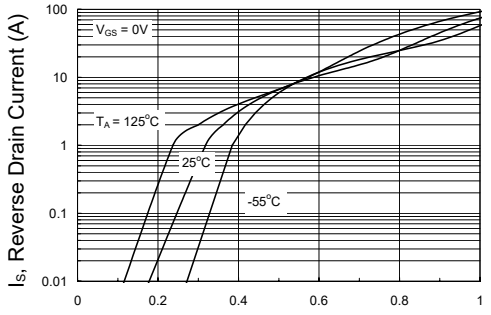


Figure 6: . Body Diode Forward Voltage Variation with Source Currentand Temperature

7.2Typical characteristic

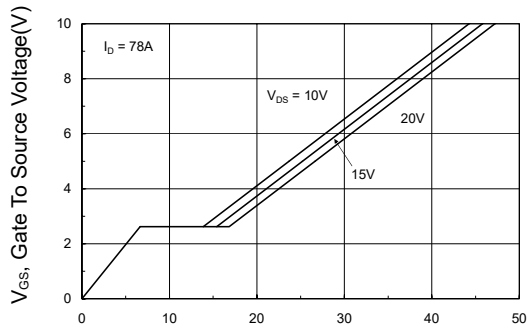


Figure 7: Gate Charge Characteristics

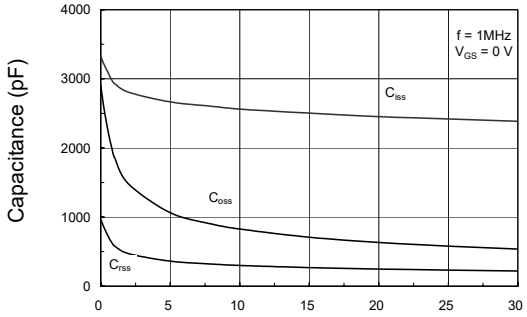


Figure 8: Capacitance Characteristics

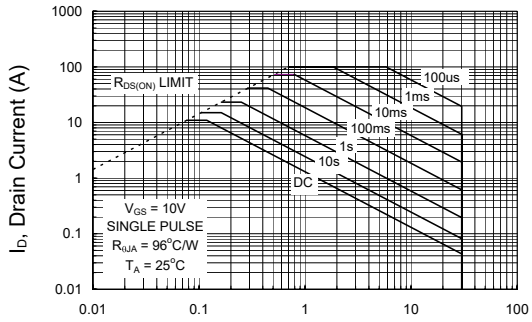


Figure 9: Maximum Safe Operating Area

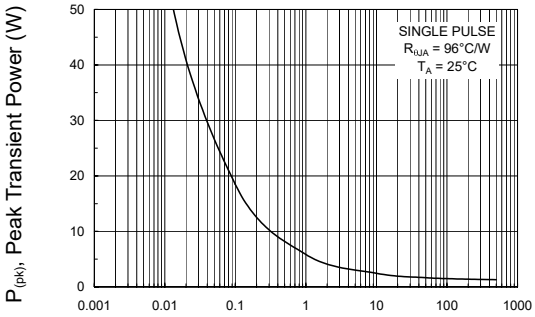


Figure 10: Single Pulse Maximum Power Dissipation

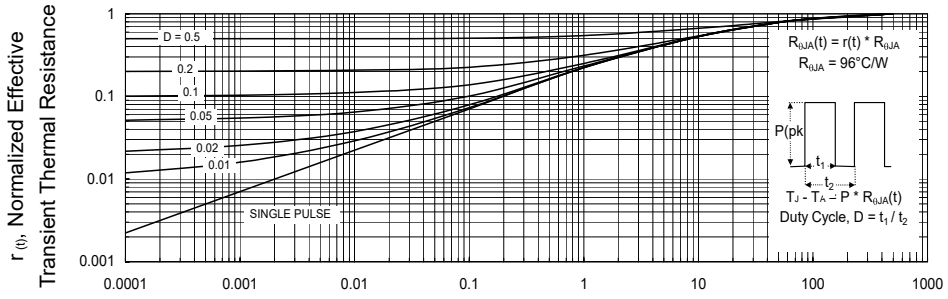
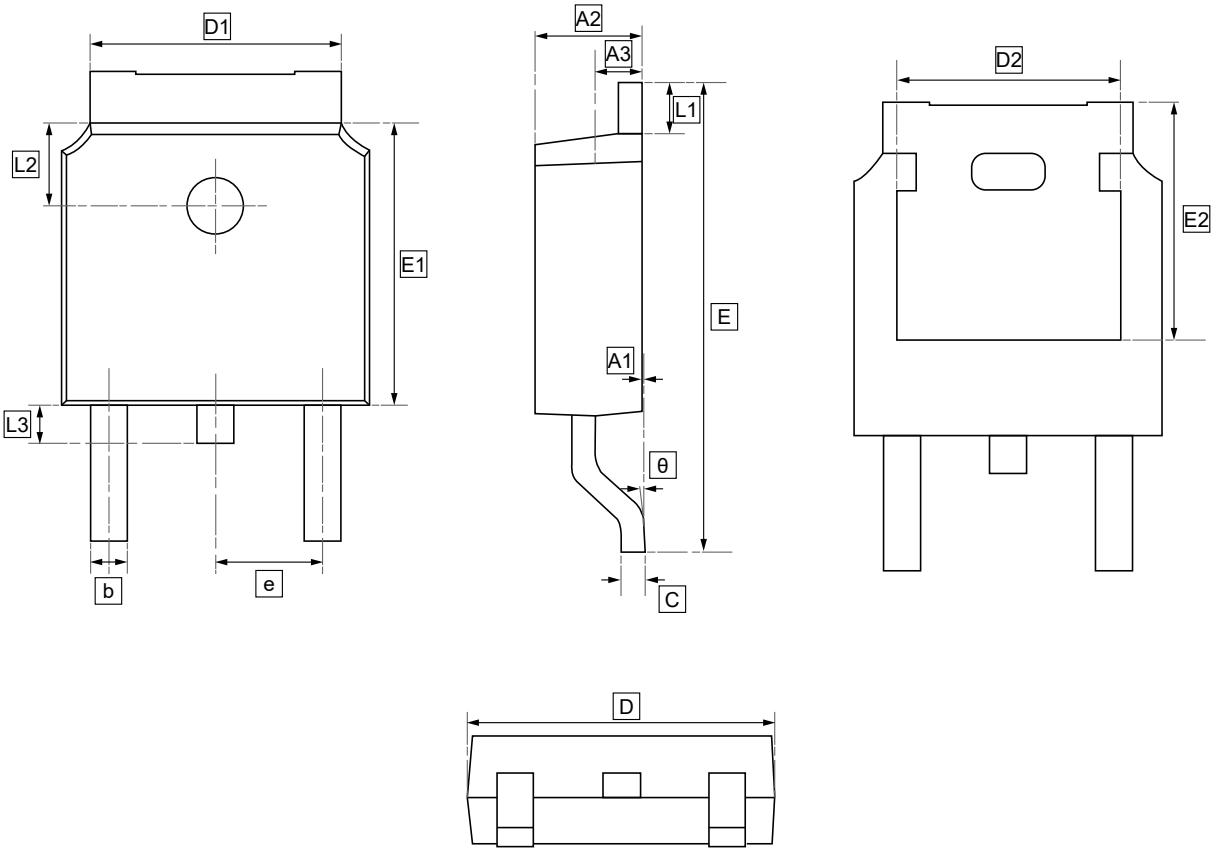


Figure 11: Transient Thermal Response Curve

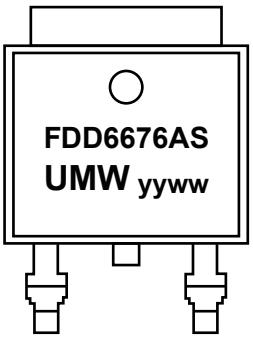
8.TO-252 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38	BSC	1.27	1.90	1.00	8.00

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDD6676AS	TO-252	2500	Tape and reel

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