UMW IRFB7440PBF

40V N-Channel MOSFET

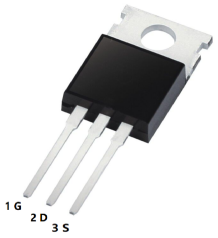
1.Features

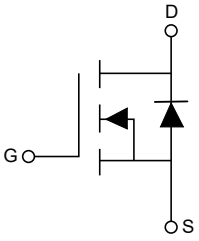
- $V_{DS(V)}$=40V
- I_D=120A
- $R_{DS(ON)}$<2.5mΩ(V_{GS}=10V)
- Enhanced body diode dV/dt and dI/dt Capability
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Lead-Free

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-220





4.Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
Continuous Drain Current, V_{GS}=10V(Silicon Limited)	T_C=25°C	I_D	172 ①	A
Continuous Drain Current, V_{GS}=10V (Silicon Limited)	T_C=100°C		122 ①	A
Continuous Drain Current, V_{GS}=10V (Wire Bond Limited)	T_C=25°C		120	A
Pulsed Drain Current ②		I_{DM}	772	A
Maximum Power Dissipation	T_C=25°C	P_D	143	W
Linear Derating Factor			0.95	W/°C
Gate-to-Source Voltage		V_{GS}	±20	V
Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C
Soldering Temperature, for 10 seconds (1.6mm from case)			300	°C
Mounting torque, 6-32 or M3 screw			10lbin (1.1Nm)	°C

Single Pulse Avalanche Energy ③	$E_{AS(Thermally\ limited)}$	161	mJ
Single Pulse Avalanche Energy ⑨	$E_{AS(Thermally\ limited)}$	387	mJ
Avalanche Current ②	I_{AR}	See Fig. 13, 14	A
Repetitive Avalanche Energy ②	E_{AR}	22a, 22b	mJ

5.Thermal resistance rating

Parameter	Symbol	Typ	Max	Units
unction-to-Case ⑧	$R_{\theta JC}$		1.05	°C/W
Case-to-Sink, Flat Greased Surface	$R_{\theta CS}$	0.5		°C/W
Junction-to-Ambient	$R_{\theta JA}$		62	°C/W

6.Electrical Characteristics @ T_J= 25°C (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=250μA, V_{GS}=0V	40			V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D=5mA,Reference to 25°C②		0.035		V/°C
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=100A ⑤		2	2.5	mΩ
		V_{GS}=6V, I_D=50A ⑤		3		mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=100μA	2.2	3	3.9	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=40V, V_{GS}=0V			1	μA
		V_{DS}=40V, V_{GS}=0V, T_J=125°C			150	μA
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS}=20V			100	nA
Gate-to-Source Reverse Leakage		V_{GS}=-20V			-100	nA
Internal Gate Resistance	R_g			2.6		Ω
Forward Transconductance	g_{FS}	V_{DS}=10V, I_D=100A	88			S
Total Gate Charge	Q_g	I_D=100A, V_{DS}=20V V_{GS}=10V ⑤		90	135	nC
Gate-to-Source Charge	Q_{gs}			23		nC
Gate-to-Drain ("Miller") Charge	Q_{gd}			32		nC
Total Gate Charge Sync.(Q_g-Q_{gd})	Q_{sync}			58		nC
Tum-On Delay Time	$t_{D(on)}$	V_{DD}=20V, I_D=30A R_G=2.7Ω, V_{GS}=10V ⑤		24		ns
Rise Time	t_r			68		ns
Turn-Off Delay Time	$t_{D(off)}$			115		ns
Fall Time	t_f			68		ns
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V f=1MHz		4730		pF
Output Capacitance	C_{oss}			680		pF
Reverse Transfer Capacitance	C_{rss}			460		pF
Effective Output Capacitance (Energy Related) ⑦	C_{oss}eff.(ER)	V_{GS}=0V, V_{DS}=0V to 32V ⑦		845		pF
Effective Output Capacitance (Time Related) ⑥	C_{oss}eff.(TR)	V_{GS}=0V, V_{DS}=0V to 32V ⑥		980		pF

Diode Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.			172	A
Pulsed Source Current (Body Diode) ②	I_{SM}				772	A
Diode Forward Voltage	V_{SD}	T_J=25°C,I_S=100,V_{GS}=0V ⑤		0.9	1.3	V
Peak Diode Recovery ④	dv/dt	T_J=175°C, I_S=100,V_{GS}=40V		6.8		V/ns
Reverse Recovery Time	t_{rr}	T_J=25°C, V_R=34V		24		ns
		T_J=125°C, I_F=100A		28		ns
Reverse Recovery Charge	Q_{rr}	T_J=25°C, di/dt=100A/μs ⑤		17		nC
		T_J=125°C		20		nC
Reverse Recovery Current	I_{RRM}	T_J=25°C		1.3		A

Notes:

① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 120A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.

② Repetitive rating; pulse width limited by max. junction temperature.

③ Limited by T_{Jmax}, starting T_J=25°C, L=0.032mH, R_G=50Ω, I_{AS}=100A, V_{GS}=10V.

④ I_{SD} ≤100A, di/dt ≤1330A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.

⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.

⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑧ R_θ is measured at T_J approximately 90°C.

⑨ Limited by T_{Jmax}, starting T_J=25°C, L=1mH, R_G=50Ω, I_{AS}=28A,V_{GS}=10V.

7.1Typical Characterisitics

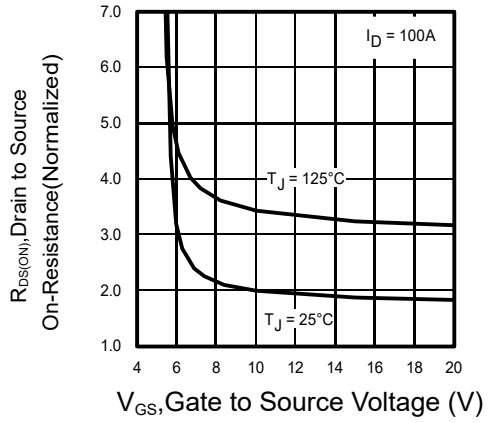


Figure 1: Typical On-Resistance vs. Gate Voltage

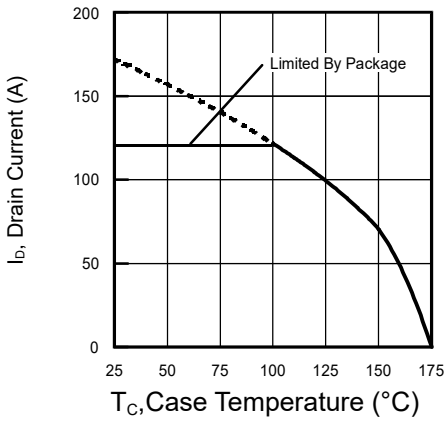


Figure 2: Maximum Drain Current vs. Case Temperature

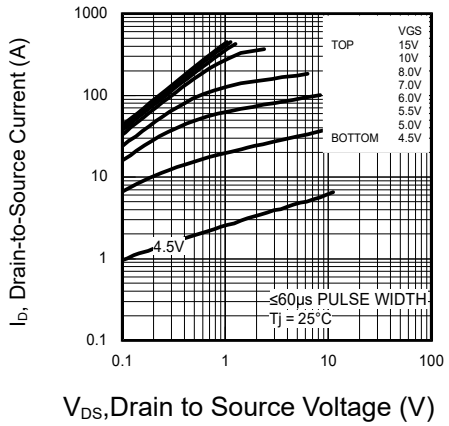


Figure 3: Typical Output Characteristics

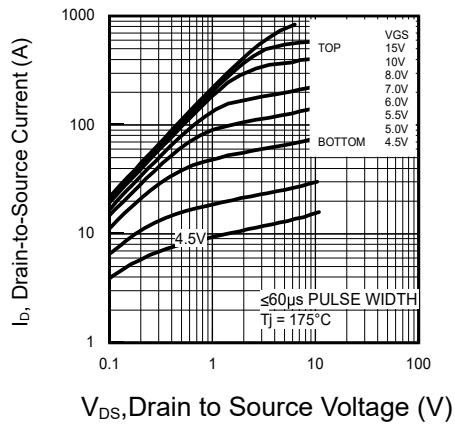


Figure 4: Typical Output Characteristics

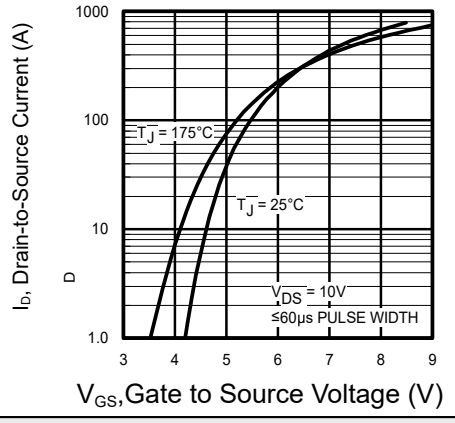


Figure 5: Typical Transfer Characteristics

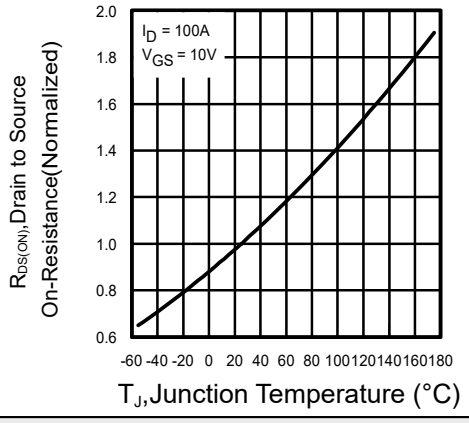
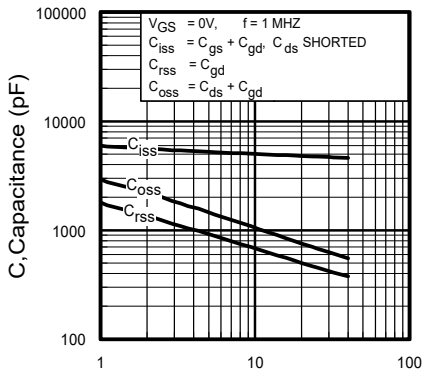


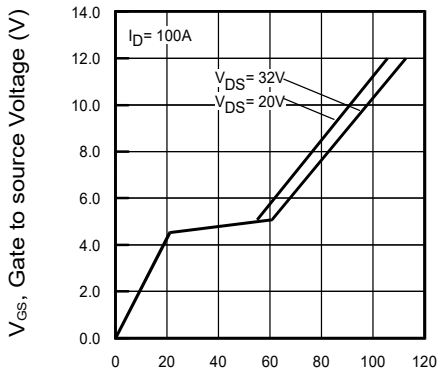
Figure 6: Normalized On-Resistance vs. Temperature

7.2Typical Characterisitics



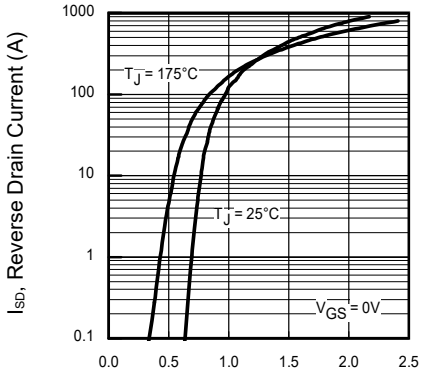
V_{DS},Drain to Source Voltage (V)

Figure 7: Typical Capacitance vs. Drain-to-Source Voltage



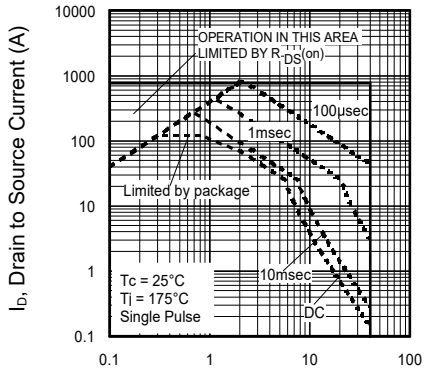
Q_G, Total Gate Charge (nC)

Figure 8: Typical Gate Charge vs. Gate-to-Source Voltage



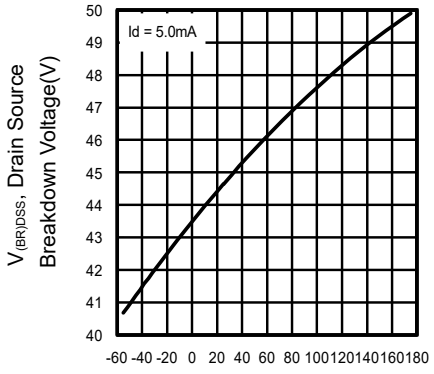
V_{SD},Source to Drain Voltage (V)

Figure 9: Typical Source-Drain Diode Forward Voltage



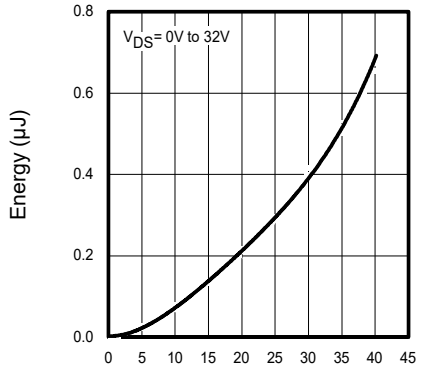
V_{DS},Drain to Source Voltage (V)

Figure 10: Maximum Safe Operating Area



T_J,Junction Temperature (°C)

Figure 11: Drain-to-Source Breakdown Voltage



V_{DS},Drain to Source Voltage (V)

Figure 12: Typical C_{OSS} Stored Energy

7.3Typical Characterisitics

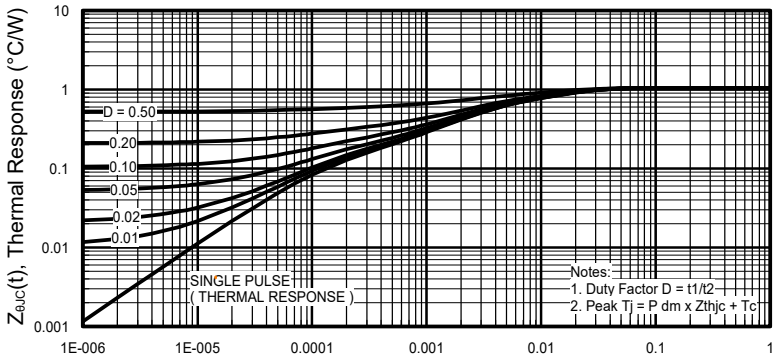


Figure 13: Maximum Effective Transient Thermal Impedance, Junction-to-Case

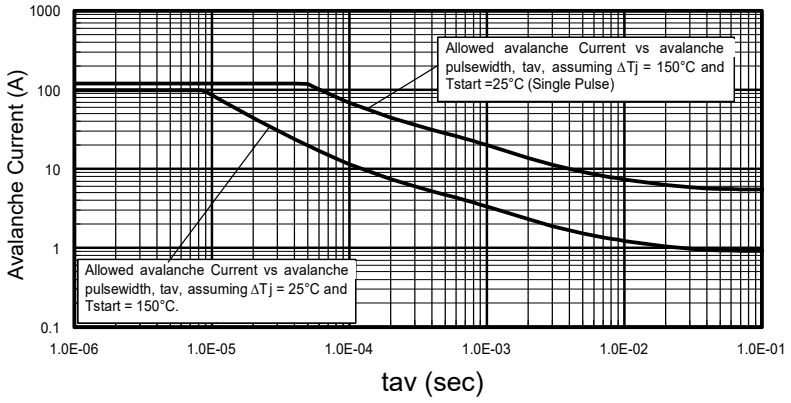


Figure 14: Typical Avalanche Current vs.Pulse width

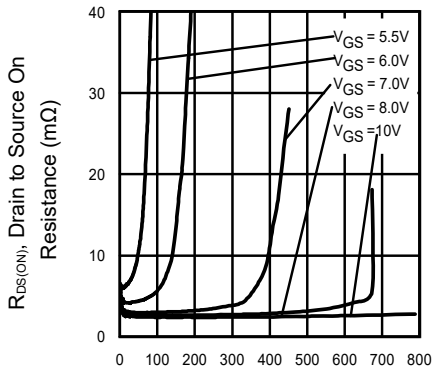


Figure 15: Typical On-Resistance vs. Drain Current

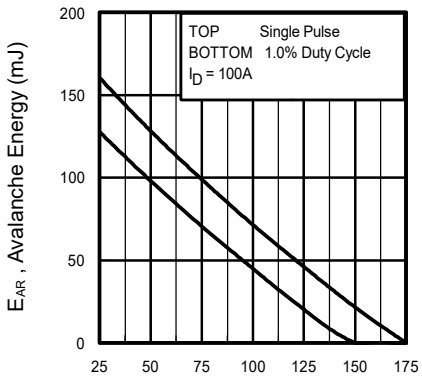


Figure 16: Maximum Avalanche Energy vs. Temperature

7.4Typical Characterisitics

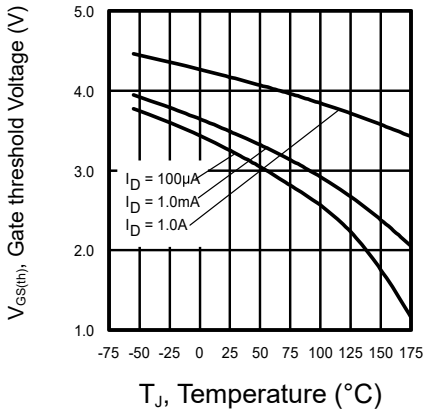


Figure 17: Threshold Voltage vs. Temperature

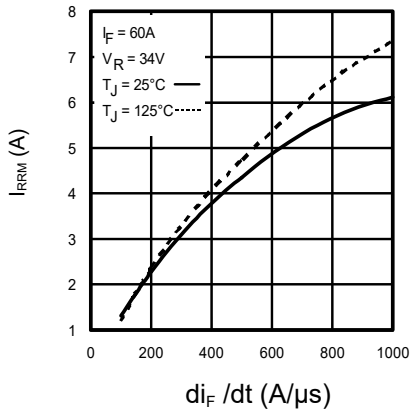


Figure 18: Typical Recovery Current vs. dif/dt

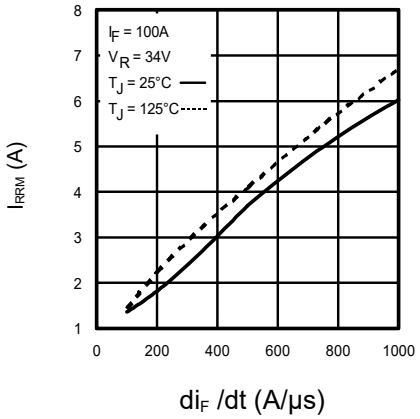


Figure 19: Typical Recovery Current vs. dif/dt

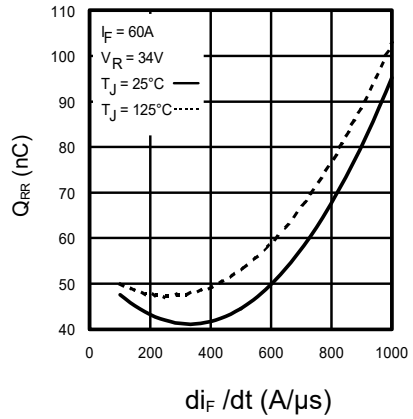


Figure 20: Typical Stored Charge vs. dif/dt

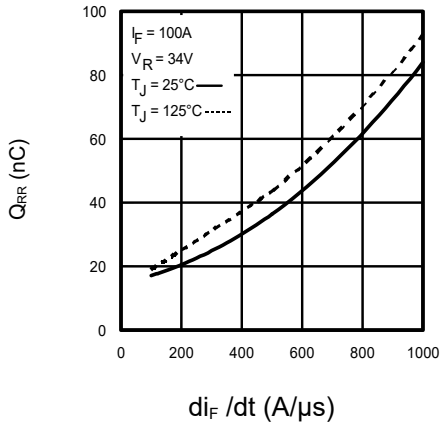


Figure 21: Typical Stored Charge vs. di_f/dt

Notes on Repetitive Avalanche Curves , Figures 13, 14

1.Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}.

This is validated for every part type.

2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.

3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.

4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.

5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).

6. I_{av} = Allowable avalanche current.

7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 13, 14).

t_{av} = Average time in avalanche.

D = Duty cycle in avalanche = t_{av} ·f

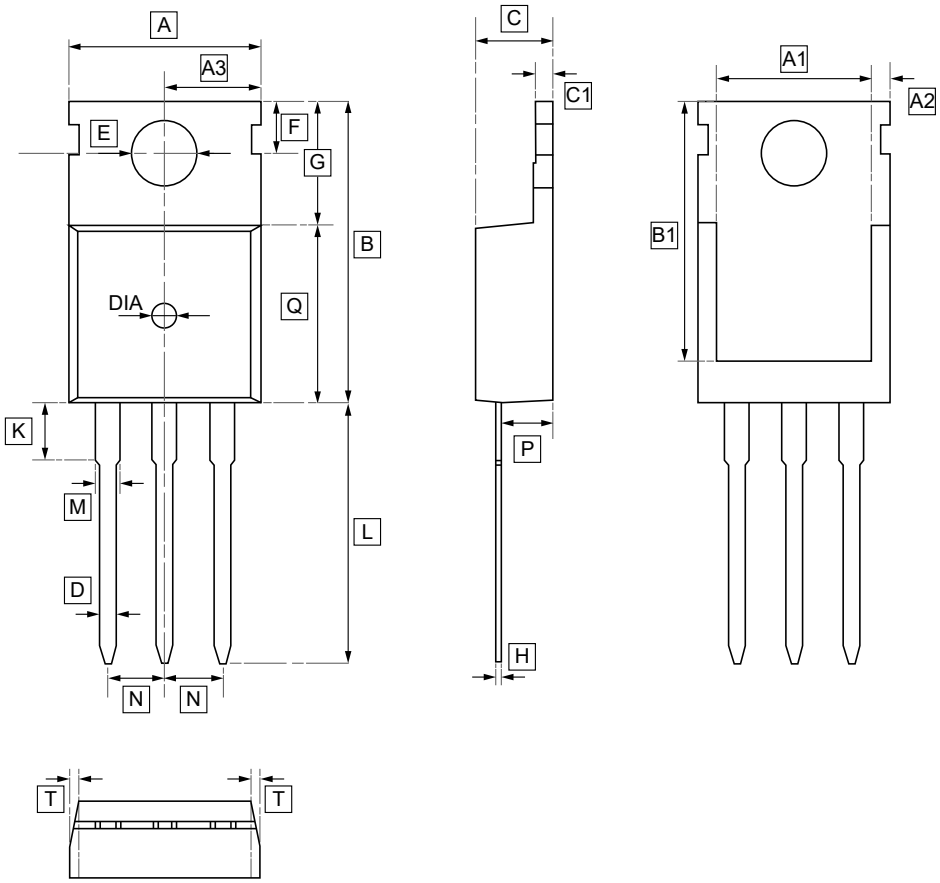
$Z_{thJC}(D, t_{av})$ = Transient thermal resistance

P_D (ave) = 1/2 (1.3·BV·I_{av}) = ΔT/ Z_{thJC}

I_{av} = 2ΔT/ [1.3·BV·Zth]

$E_{AS\ (AR)}$ = P_D (ave)·t_{av}

8.TO-220 Package Outline Dimensions

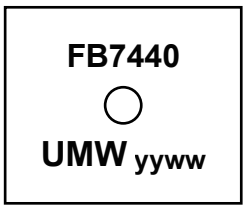


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	B	B1	C	C1	D	E	F	G
Min	9.7	8.44	1.05	4.8	15.4	12.9	4.28	1.1	0.6	3.4	2.65	5.2
Max	10.3	8.84	1.25	5.2	16.2	13.5	4.68	1.5	1.0	3.8	3.25	5.8

Symbol	H	K	L	L1	M	N	P	Q	T	DIA
Min	0.4	2.9	12.8	2.7	1.15	2.49	2.1	8.7	W:0.35	⊙1.5
Max	0.6	3.3	13.6	3.3	1.35	2.59	2.7	9.3		(deep 0.2)

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRFB7440PBF	TO-220	1000	Tube and box

10.Disclaimer

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