Enhancement Mode Field Effect Transistor

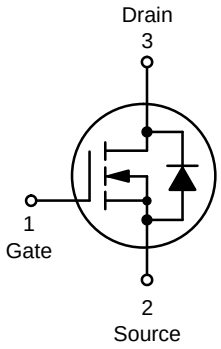
N-Channel

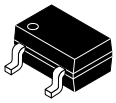
2N7002W

Features

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- These Devices are Pb-Free and are RoHS Compliant

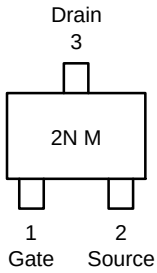
SIMPLIFIED SCHEMATIC





SC-70
CASE 419AB

MARKING DIAGRAM & PIN ASSIGNMENT



2N = Device Code
M = Date Code

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	60	V
Drain-Gate Voltage $R_{GS} \le 1.0$ MΩ	V_{DGR}	60	V
Gate-Source Voltage Continuous Pulsed	V_{GSS}	 ±20 ±40	V
Drain Current Continuous Continuous @ 100 °C Pulsed	I_D	 115 73 800	mA
Total Device Dissipation Derating above T_A = 25 °C	P_D	200 1.6	mW mW/°C
Junction and Storage Temperature Range	T_J, T_{STG}	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	625	°C/W

1. Device mounted on FR-4 PCB, 1 inch × 0.85 inch × 0.062 inch. Minimum land pad size.

ORDERING INFORMATION

Device	Package	Shipping†
2N7002W	SC-70 (Pb-Free)	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
OFF CHARACTERISTICS (Note 2)							
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 10 μA		60	78	–	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	T_C = 25 °C	–	0.001	1.0	μA
			T_C = 125 °C	–	7	500	
Gate-Body Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V		–	0.2	±10	nA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.0	1.76	2.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.05 A		–	1.6	7.5	Ω
		V_{GS} = 10 V, I_D = 0.5 A, @ T_J = 125 °C		–	2.53	13.5	
On-State Drain Current	$I_{D(ON)}$	V_{GS} = 10 V, V_{DS} = 7.5 V		0.5	1.43	–	A
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 0.2 A		80	356.5	–	mS
DYNAMIC CHARACTERISTICS							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz		–	37.8	50	pF
Output Capacitance	C_{OSS}			–	12.4	25	
Reverse Transfer Capacitance	C_{RSS}			–	6.5	7.0	
SWITCHING CHARACTERISTICS							
Turn-On Delay Time	$t_{D(ON)}$	V_{GEN} = 10 V, V_{DD} = 30 V, I_D = 0.2 A, R_L = 150 Ω, R_{GEN} = 25 Ω		–	5.85	20	ns
Turn-Off Delay Time	$t_{D(OFF)}$			–	12.5	20	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Short duration test pulse used to minimize self-heating effect.

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TYPICAL PERFORMANCE CHARACTERISTICS

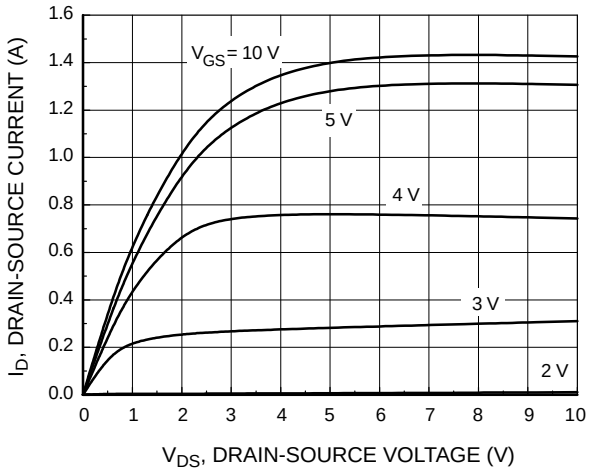


Figure 1. On-Region Characteristics

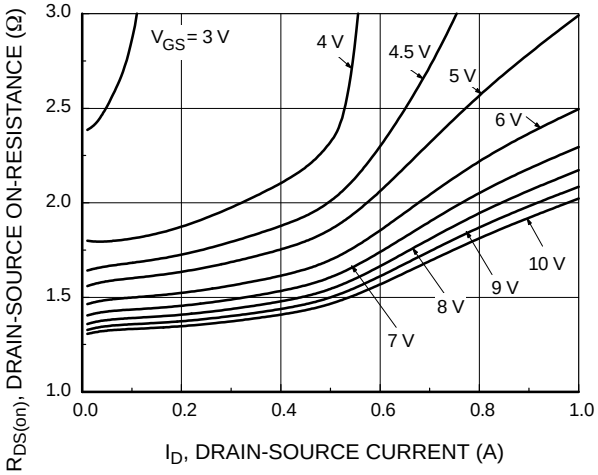


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

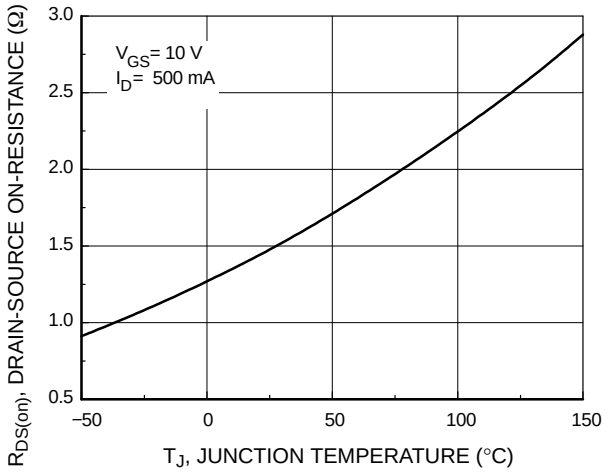


Figure 3. On-Resistance Variation with Temperature

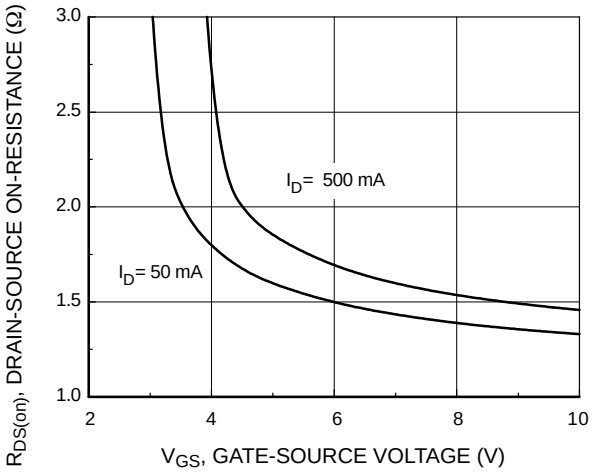


Figure 4. On-Resistance Variation with Gate-Source Voltage

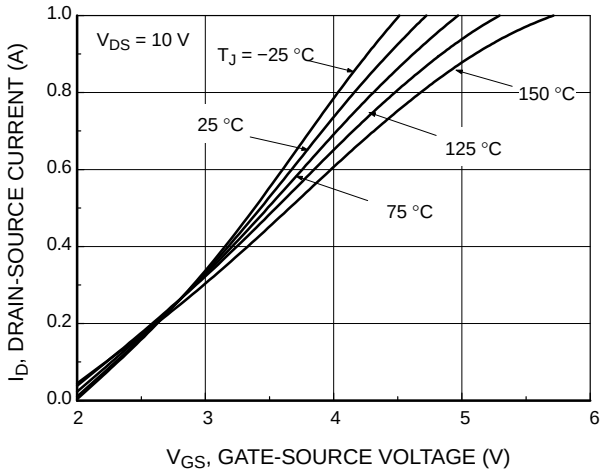


Figure 5. Transfer Characteristics

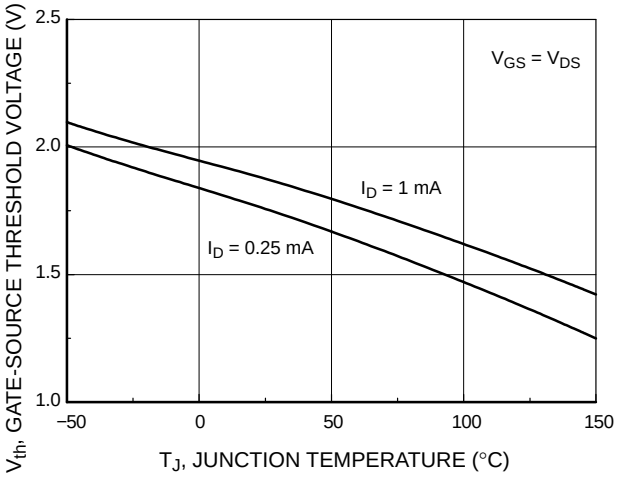


Figure 6. Gate Threshold Variation with Temperature

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TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

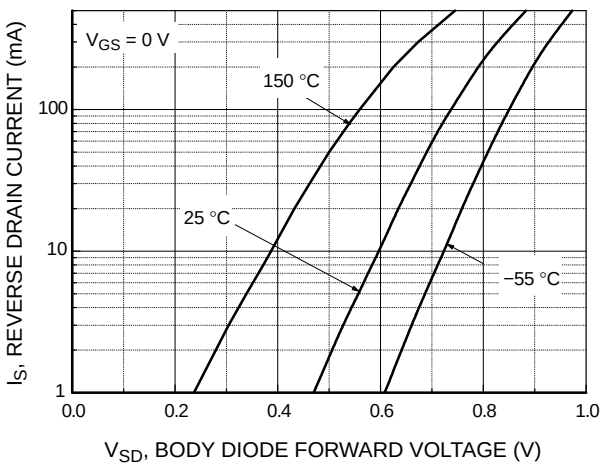


Figure 7. Reverse Drain Current Variation with Diode Forward Voltage and Temperature

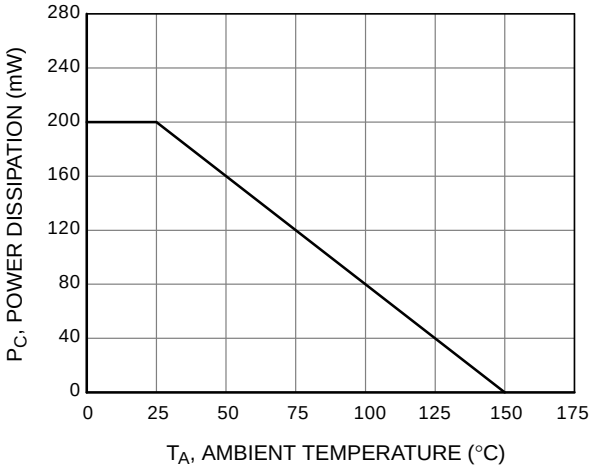


Figure 8. Power Derating

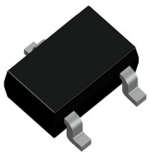
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REVISION HISTORY

Revision	Description of Changes	Date
5	Updated Absolute Maximum Ratings and Thermal Characteristics specifications.	11/4/2026

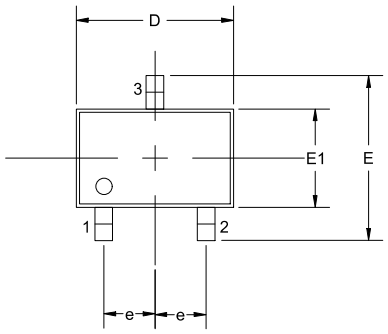
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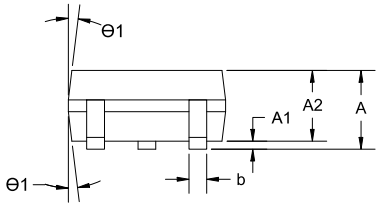


SC−70, 3 Lead, 1.25x2
CASE 419AB
ISSUE A

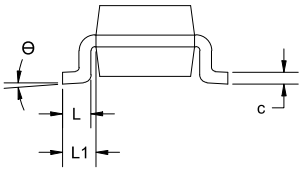
DATE 13 FEB 2023



TOP VIEW



SIDE VIEW

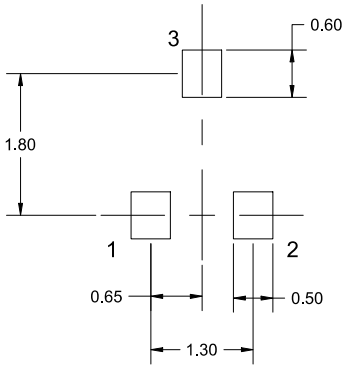


END VIEW

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES IN DEGREES.
2. COMPLIES WITH JEDEC MO-203

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80		1.10
A1	0.00		0.10
A2	0.80	0.90	1.00
b	0.15		0.30
c	0.08		0.22
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.26	0.36	0.46
L1	0.42 REF		
Θ	0°		8°
Θ1	4°		10°



SOLDERING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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