Data Sheet November 16, 2004 FN3158.5

4-Digit, LCD Display Driver

The ICM7211AM device is a non-multiplexed four-digit seven-segment CMOS LCD display decoder-driver.

This device is configured to drive conventional LCD displays by providing a complete RC oscillator, divider chain, backplane driver, and 28 segment outputs.

It also has a microprocessor compatible input configuration, which provides data input latches and Digit Address latches under control of high-speed Chip Select inputs. These devices simplify the task of implementing a cost-effective alphanumeric seven-segment display for microprocessor systems, without requiring extensive ROM or CPU time for decoding and display updating.

The ICM7211AM provides the “Code B” output code, i.e., 0-9, dash, E, H, L, P, blank, but will correctly decode true BCD to seven-segment decimal outputs.

Features

- Four Digit Non-Multiplexed 7 Segment LCD Display Outputs with Backplane Driver
- Complete Onboard RC Oscillator to Generate Backplane Frequency
- Backplane Input/Output Allows Simple Synchronization of Slave-Devices to a Master
- Provides Data and Digit Address Latches Controlled by Chip Select Inputs to Provide a Direct High Speed Processor Interface
- Decodes Binary to Code B (0-9, Dash, E, H, L, P, Blank)

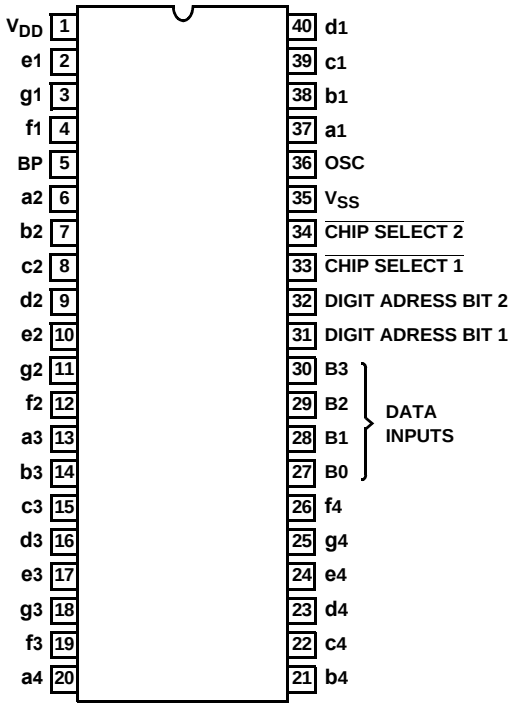
Ordering Information

PART NUMBER	DISPLAY TYPE	DISPLAY DECODING	INPUT INTERFACING	DISPLAY DRIVE TYPE	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ICM7211AMIPL	LCD	Code B	Microprocessor	Direct Drive	-40 to 85	40 Ld PDIP	E40.6

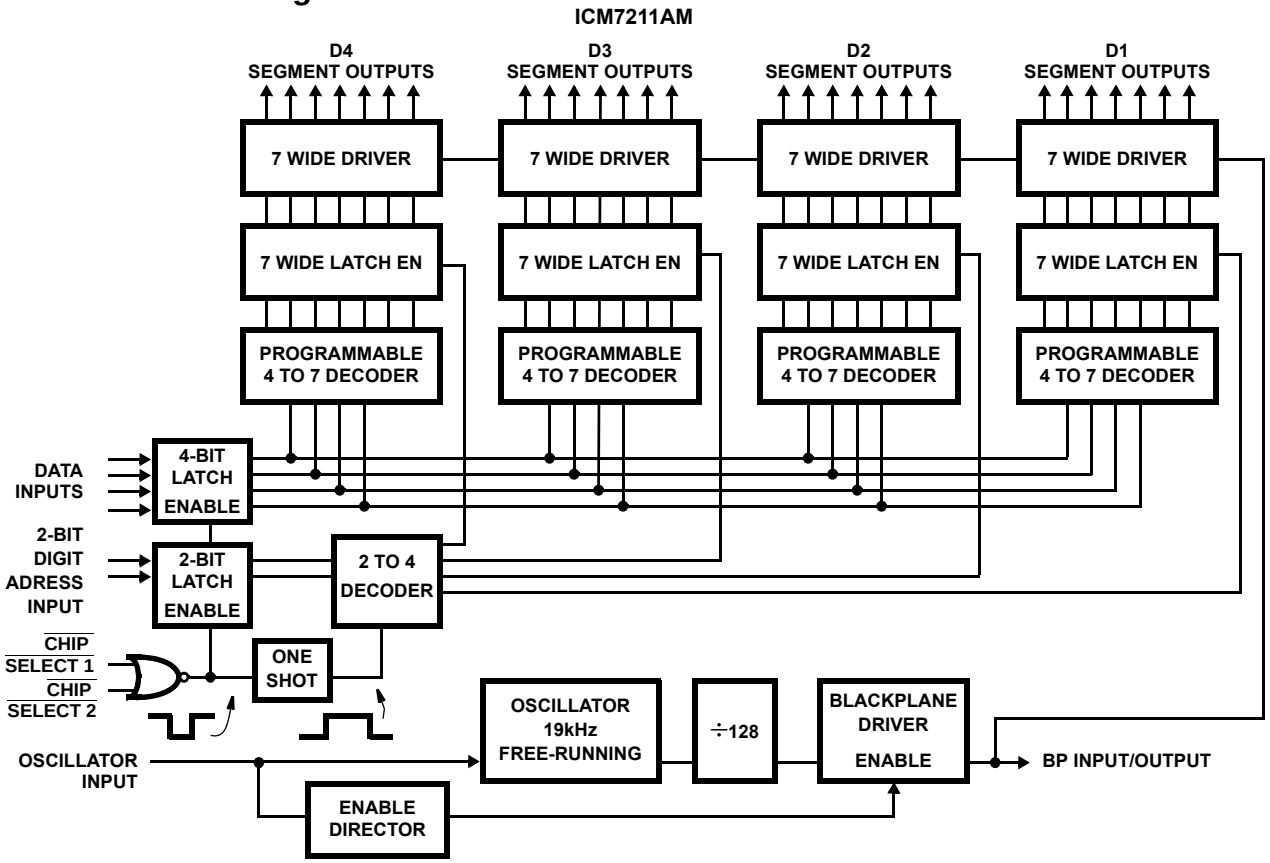
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Pinout

ICM7211AM (PDIP)
TOP VIEW



Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage (V_{DD} - V_{SS}) 6.5V
Input Voltage (Any Terminal) (Note 1) . . . V_{SS} - 0.3V to V_{DD}, + 0.3V

Operating Conditions

Temperature Range. . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
PDIP Package 60
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65×°C to 150°C
Maximum Lead Temperature (Soldering, 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7211AM be turned on first.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CHARACTERISTICS V_{DD} = 5V ±10%, T_A = 25°C, V_{SS} = 0V Unless Otherwise Specified					
Operating Supply Voltage Range (V_{DD} - V_{SS}), V_{SUPPLY}		3	5	6	V
Operating Current, I_{DD}	Test circuit, Display blank	-	10	50	µA
Oscillator Input Current, I_{OSCI}	Pin 36	-	±2	±10	µA
Segment Rise/Fall Time, t_r, t_f	C_L = 200pF	-	0.5	-	µs
Backplane Rise/Fall Time, t_r, t_f	C_L = 5000pF	-	1.5	-	µs
Oscillator Frequency, f_{OSC}	Pin 36 Floating	-	19	-	kHz
Backplane Frequency, f_{BP}	Pin 36 Floating	-	150	-	Hz
INPUT CHARACTERISTICS					
Logical "1" Input Voltage, V_{IH}		4	-	-	V
Logical "0" Input Voltage, V_{IL}		-	-	1	V
Input Leakage Current, I_{ILK}	Pins 27-34	-	±0.01	±1	µA
Input Capacitance, C_{IN}	Pins 27-34	-	5		pF
BP/Brightness Input Leakage, I_{BPLK}	Measured at Pin 5 with Pin 36 at V_{SS}	-	±0.01	±1	µA
BP/Brightness Input Capacitance, C_{BPI}	All Devices	-	200	-	pF
AC CHARACTERISTICS					
Chip Select Active Pulse Width, t_{WL}	Other Chip Select Either Held Active, or Both Driven Together	200	-	-	ns
Data Setup Time, t_{DS}		100	-	-	ns
Data Hold Time, t_{DH}		10	0	-	ns
Inter-Chip Select Time, t_{ICS}		2	-	-	µs

Input Definitions

In this table, V_{DD} and V_{SS} are considered to be normal operating input logic levels. Actual input low and high levels are specified under Operating Characteristics. For lowest power consumption, input signals should swing over the full supply.

INPUT	DIP TERMINAL	CONDITIONS	FUNCTION	
B0	27	V_{DD} = Logical One V_{SS} = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28	V_{DD} = Logical One V_{SS} = Logical Zero	Twos	
B2	29	V_{DD} = Logical One V_{SS} = Logical Zero	Fours	
B3	30	V_{DD} = Logical One V_{SS} = Logical Zero	Eights (Most Significant)	

Input Definitions In this table, V_{DD} and V_{SS} are considered to be normal operating input logic levels. Actual input low and high levels are specified under Operating Characteristics. For lowest power consumption, input signals should swing over the full supply. **(Continued)**

INPUT	DIP TERMINAL	CONDITIONS	FUNCTION
OSC	36	Floating or with External Capacitor to V_{DD}	Oscillator Input
		V_{SS}	Disables BP output devices, allowing segments to be synchronized to an external signal input at the BP terminal (Pin 5).

Interface Input Configuration

INPUT	DESCRIPTION	DIP TERMINAL	CONDITIONS	FUNCTION
DA1	Digit Address Bit 1 (LSB)	31	V_{DD} = Logical One V_{SS} = Logical Zero	DA1 and DA2 serve as a 2-bit Digit Address Input DA2, DA1 = 00 selects D4 DA2, DA1 = 01 selects D3 DA2, DA1 = 10 selects D2 DA2, DA1 = 11 selects D1
DA2	Digit Address Bit 2 (MSB)	32	V_{DD} = Logical One V_{SS} = Logical Zero	
$\overline{CS1}$	Chip Select 1	33	V_{DD} = Inactive V_{SS} = Active	When both $\overline{CS1}$ and $\overline{CS2}$ are taken low, the data at the Data and Digit Select code inputs are written into the input latches. On the rising edge of either Chip Select, the data is decoded and written into the output latches.
$\overline{CS2}$	Chip Select 2	34	V_{DD} = Inactive V_{SS} = Active	

Timing Diagram

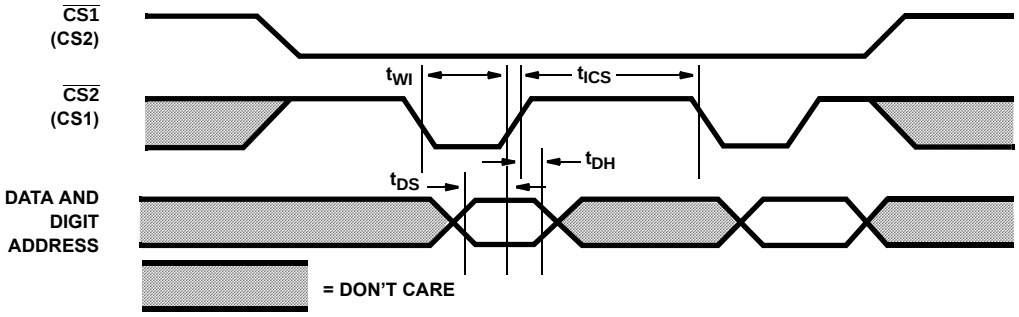


FIGURE 1. MICROPROCESSOR INTERFACE INPUT

Typical Performance Curves

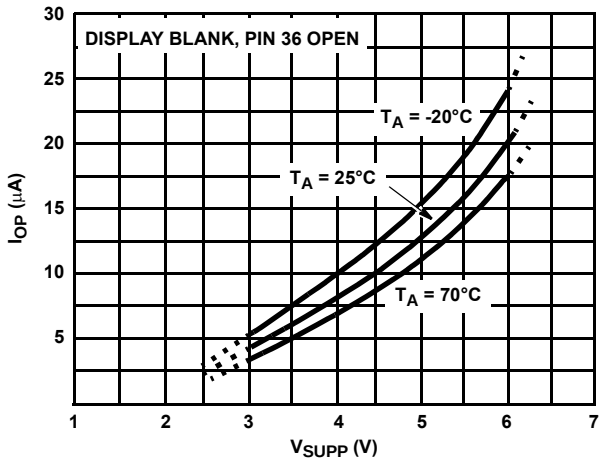


FIGURE 2. OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

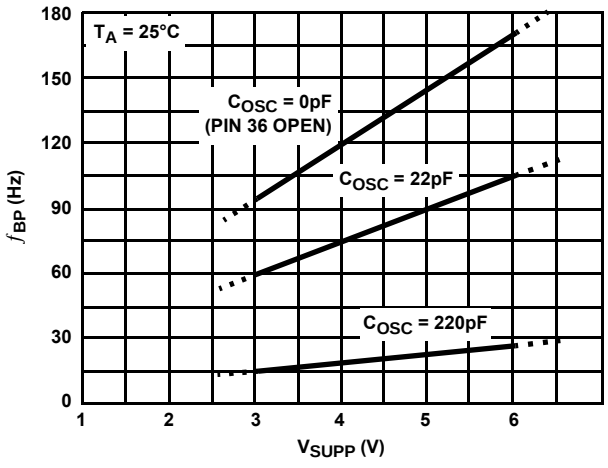


FIGURE 3. BACKPLANE FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

Description Of Operation

Device

The ICM7211AM provides outputs suitable for driving conventional four-digit, seven-segment LCD displays. These devices include 28 individual segment drivers, backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency.

The segment and backplane drivers each consist of a CMOS inverter, with the N-Channel and P-Channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any DC component, which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output devices can be disabled by connecting the OSCillator input (pin 36) to V_{SS}. This allows the 28 segment outputs to be synchronized directly to a signal input at the BP terminal (pin 5). In this manner, several slave devices may be cascaded to the backplane output of one master device, or the backplane may be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device represents a load of approximately 200pF (comparable to one additional segment). Thus the limitation of the number of devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits. A good rule of thumb to observe in order to minimize power consumption is to keep the backplane rise and fall times less than about 5μs. The backplane output driver should handle the backplane to a display of 16 one-half inch characters. It is recommended, if more than four devices are to be slaved together, the backplane signal be derived externally and all the ICM7211AM devices be slaved to it. This external signal should be capable of driving very large capacitive loads with short (1 - 2μs) rise and fall times. The maximum frequency for a backplane signal should be about 150Hz although this may be too fast for optimum display response at lower display temperatures, depending on the display type.

The onboard oscillator is designed to free run at approximately 19kHz at microampere current levels. The oscillator frequency is divided by 128 to provide the backplane frequency, which will be approximately 150Hz with the oscillator free-running; the oscillator frequency may be reduced by connecting an external capacitor between the OSCillator terminal and V_{DD}.

The oscillator may also be overdriven if desired, although care must be taken to ensure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a DC component to the display). This can be done by driving the OSCillator input between the positive supply and a level out of the range where the backplane disable is sensed (about one fifth of the supply voltage above V_{SS}).

Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

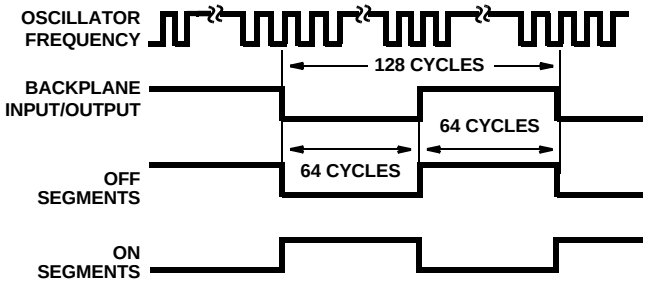


FIGURE 4. DISPLAY WAVEFORMS

Input Configurations and Output Codes

The ICM7211AM accepts a four-bit true binary (i.e., positive level = logical one) input at pins 27 thru 30, least significant bit at pin 27 ascending to the most significant bit at pin 30. It decodes the binary input into seven-segment alphanumeric “Code B” output, i.e., 0-9, dash, E, H, L, P, blank. These codes are shown explicitly in Table 1. It will correctly decode true BCD to a seven-segment decimal output.

TABLE 1. OUTPUT CODES

BINARY				CODE B ICM7211AM
B3	B2	B1	BO	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	-
1	0	1	1	E

TABLE 1. OUTPUT CODES (Continued)

BINARY				CODE B ICM7211AM
B3	B2	B1	BO	
1	1	0	0	H
1	1	0	1	L
1	1	1	0	P
1	1	1	1	BLANK

The ICM7211AM is intended to accept data from a data bus under processor control.

In these devices, the four data input bits and the two-bit digit address (DA1 pin 31, DA2 pin 32) are written into input buffer latches when both chip select inputs ($\overline{CS1}$ pin 33, $\overline{CS2}$ pin 34) are taken low. On the rising edge of either chip select input, the content of the data input latches is decoded and stored in the output latches of the digit selected by the contents of the digit address latches.

An address of 00 writes into D4, DA2 = 0, DA1 = 1 writes into D3, DA2 = 1, DA1 = 0 writes into D2, and 11 writes into D1. The timing relationships for inputting data are shown in Figure 1, and the chip select pulse widths and data setup and hold times are specified under Operating Characteristics.

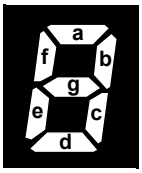


FIGURE 5. SEGMENT ASSIGNMENT

Test Circuit

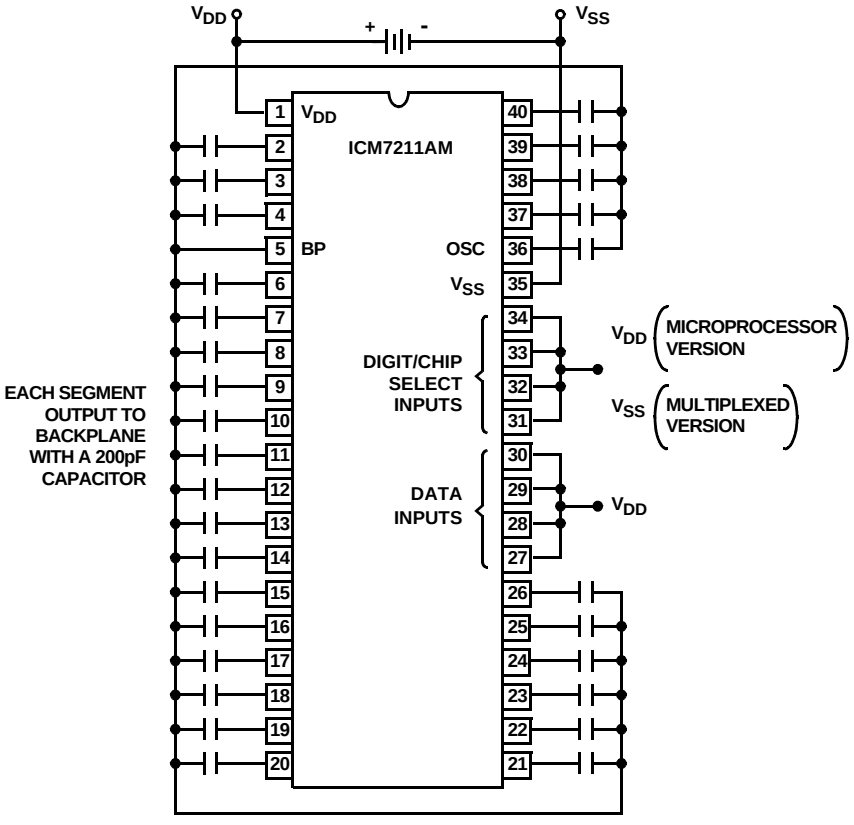


FIGURE 6.

Typical Application

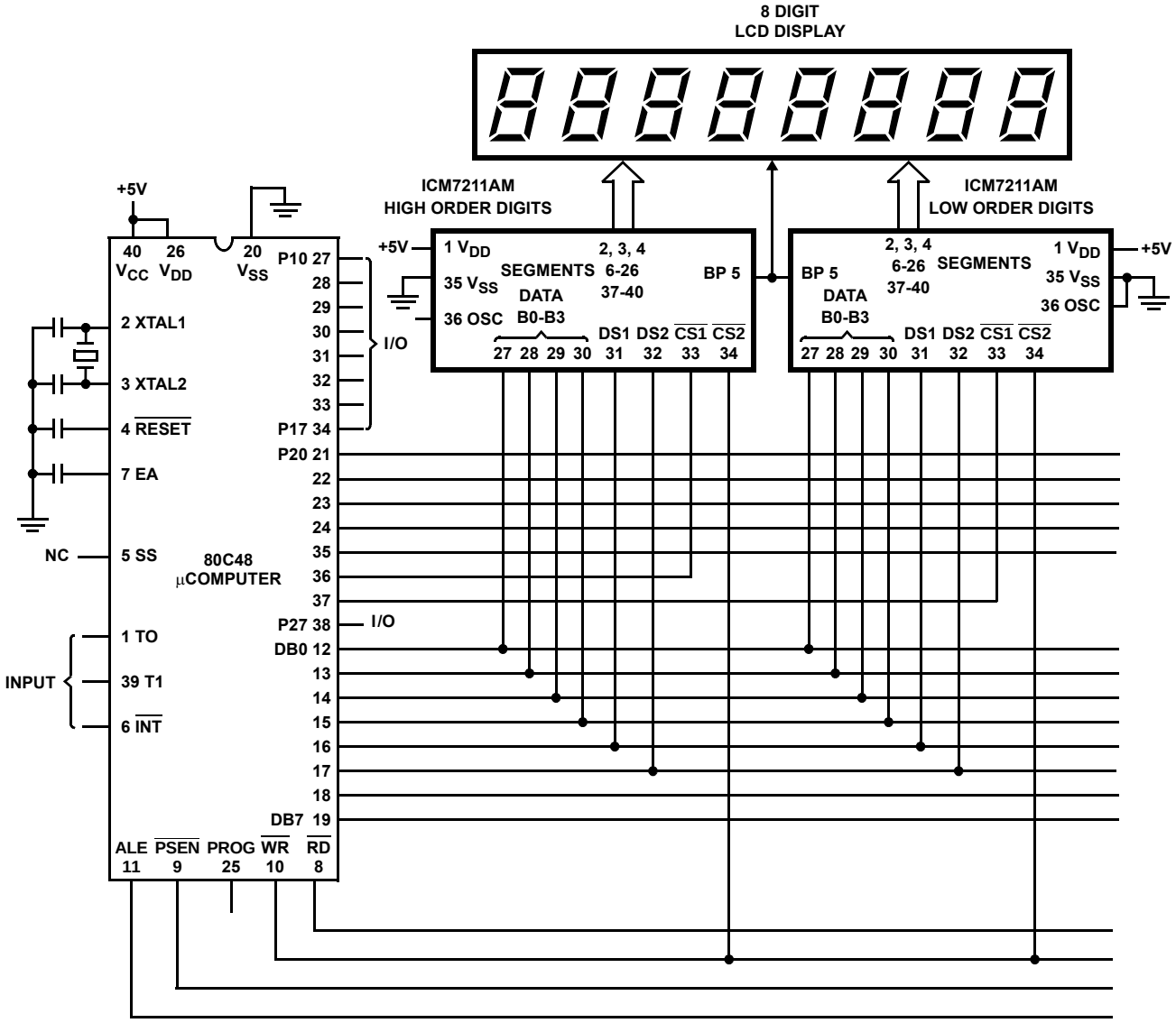


FIGURE 7. 80C48 MICROPROCESSOR INTERFACE

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