FAIRCHILD SEMICONDUCTOR™

October 1987
Revised April 2002

CD4024BC
7-Stage Ripple Carry Binary Counter

General Description

The CD4024BC is a 7-stage ripple-carry binary counter. Buffered outputs are externally available from stages 1 through 7. The counter is reset to its logical "0" stage by a logical "1" on the reset input. The counter is advanced one count on the negative transition of each clock pulse.

Features

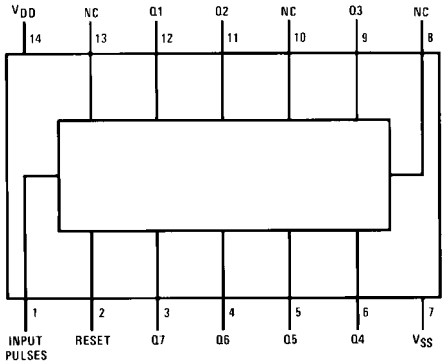
- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{DD} (typ.)
- Low power TTL compatibility: Fan out of 2 driving 74L or 1 driving 74LS
- High speed: 12 MHz (typ.)
  input pulse rate $V_{DD} - V_{SS} = 10V$
- Fully static operation

Ordering Code:

Order Number	Package Number	Package Description
CD4024BCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4024BCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Top View

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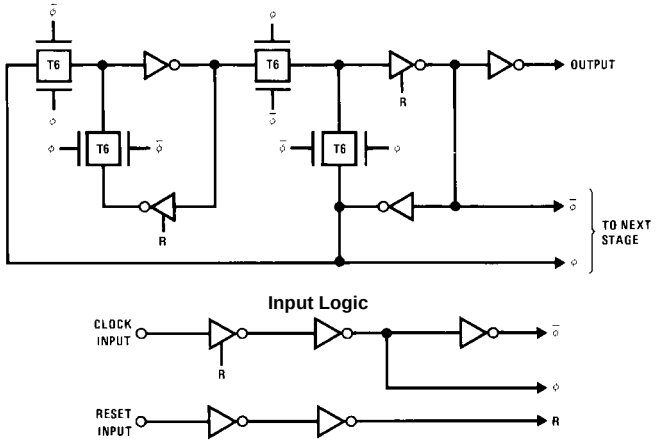
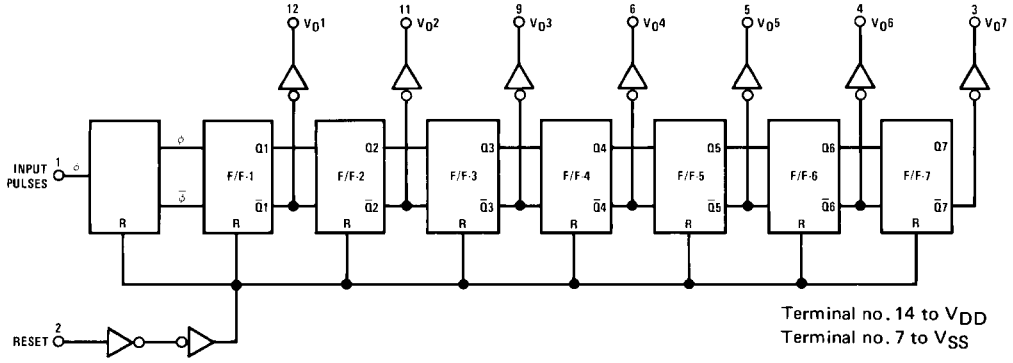
Logic Diagrams



Flip-flop logic (1 of 7 identical stages).

Block Diagram



Absolute Maximum Ratings (Note 1)

(Note 2)

DC Supply Voltage (V_{DD})	−0.5 to +18 V_{DC}
Input Voltage (V_{IN})	−0.5 to V_{DD} +0.5 V_{DC}
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature	
(Soldering, 10 seconds) (T_L)	260°C

Recommended Operating Conditions (Note 1)

DC Supply Voltage (V_{DD})	+3 to +15 V_{DC}
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	−55°C to +125°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.3	5		150	
		V_{DD} = 10V		10		0.5	10		300	µA
		V_{DD} = 15V		20		0.7	20		600	
V_{OL}	LOW Level Output Voltage	$\|I_O\|$<1 µA								
		V_{DD} = 5V		0.05		0	0.05		0.05	
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	
V_{OH}	HIGH Level Output Voltage	$\|I_O\|$<1 µA								
		V_{DD} = 5V	4.95		4.95	5		4.95		
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		
V_{IL}	LOW Level Input Voltage	$\|I_O\|$<1 µA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	
V_{IH}	HIGH Level Input Voltage	$\|I_O\|$<1 µA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		
I_{OL}	LOW Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		
	(Note 3)	V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		
I_{OH}	HIGH Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		
	(Note 3)	V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	

Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics (Note 4)

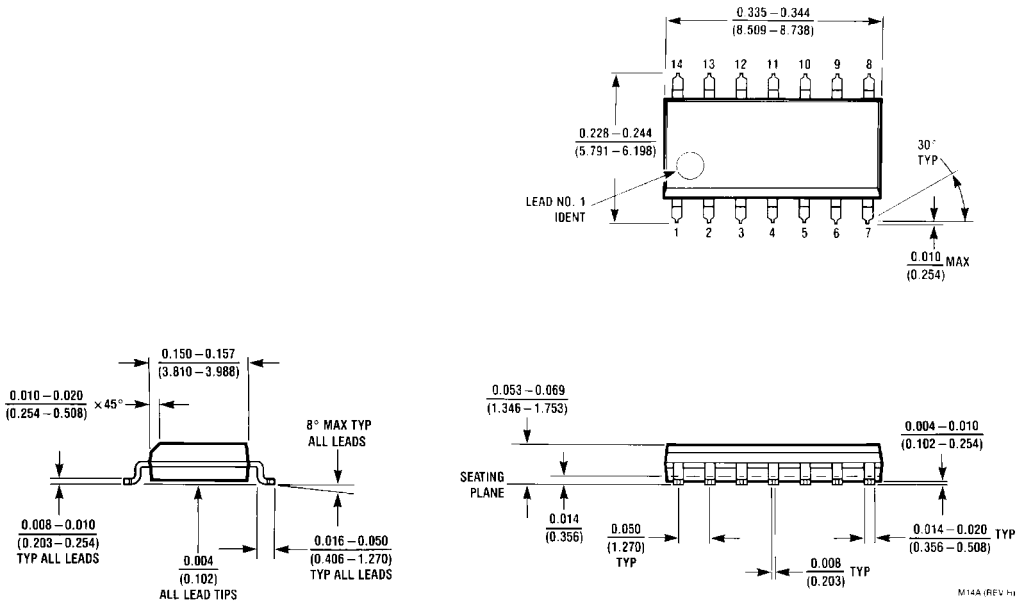
$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ k, t_r and $t_f = 20$ ns unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		185	350	
	to Q1 Output	$V_{DD} = 10V$		85	125	ns
		$V_{DD} = 15V$		70	100	
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	
t_{WL}, t_{WH}	Minimum Input Pulse Width	$V_{DD} = 5V$		75	200	
		$V_{DD} = 10V$		40	110	ns
		$V_{DD} = 15V$		35	90	
t_{RCL}, t_{FCL}	Input Rise and Fall Time	$V_{DD} = 5V$			15	
		$V_{DD} = 10V$			10	µs
		$V_{DD} = 15V$			8	
f_{CL}	Maximum Input Pulse Frequency	$V_{DD} = 5V$	1.5	5		
		$V_{DD} = 10V$	4	12		MHz
		$V_{DD} = 15V$	5	15		
t_{PHL}	Reset Propagation Delay Time	$V_{DD} = 5V$		185	350	
		$V_{DD} = 10V$		85	125	ns
		$V_{DD} = 15V$		70	100	
t_{WH}	Reset Minimum Pulse Width	$V_{DD} = 5V$		185	350	
		$V_{DD} = 10V$		85	125	ns
		$V_{DD} = 15V$		70	100	
C_{IN}	Input Capacitance (Note 5)	Any Input		5	7.5	pF

Note 4: AC Parameters are guaranteed by DC correlated testing.

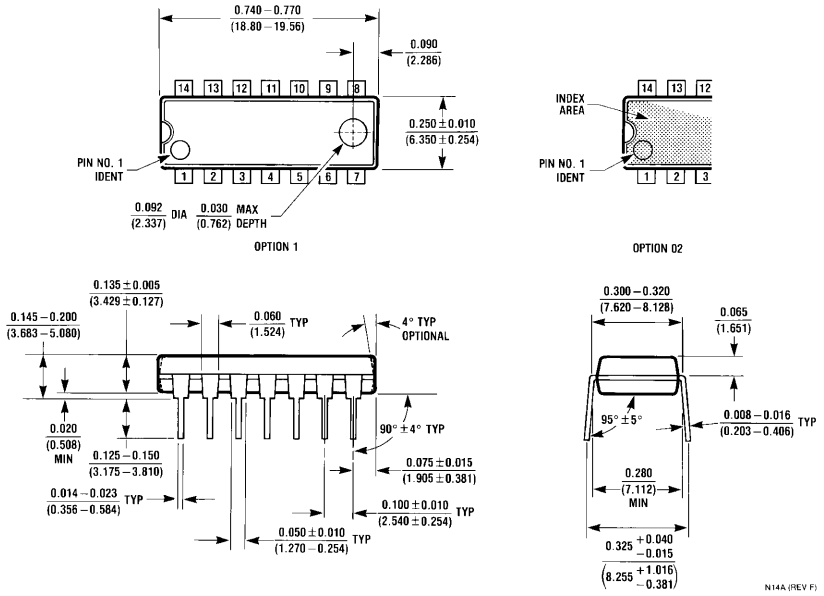
Note 5: Capacitance is guaranteed by periodic testing.

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

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