International
IOR Rectifier

IRGS4630DPbF
IRGB4630DPbF
IRGP4630D(-E)PbF

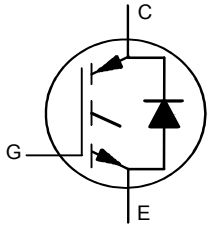
Insulated Gate Bipolar Transistor with Ultrafast Soft Recovery Diode

V_{CES} = 600V

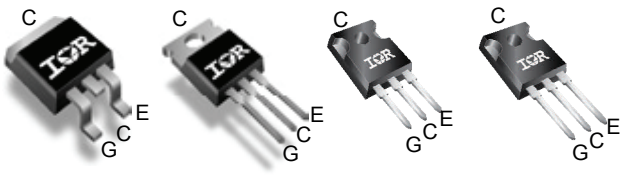
I_C = 30A, T_C =100°C

$t_{SC} \geq$ 5µs, $T_{J(max)}$ = 175°C

$V_{CE(ON)}$ typ. = 1.65V @ I_C = 18A



n-channel



IRGS4630DPbF D²Pak | IRGB4630DPbF TO-220AC | IRGP4630DPbF TO-247AC | IRGP4630D-EPbF TO-247AD

G	C	E
Gate	Collector	Emitter

Applications

- Appliance Drives
- Inverters
- UPS

Features →	Benefits
Low $V_{CE(ON)}$ and switching losses	High efficiency in a wide range of applications and switching
Square RBSOA and maximum junction temperature 175°C	Improved reliability due to rugged hard switching performance and high power capability
Positive $V_{CE\ (ON)}$ temperature coefficient and tight distribution of parameters	Excellent current sharing in parallel operation
5µs Short Circuit SOA	Enables short circuit protection scheme
Lead-Free, RoHS Compliant	Environmentally friendly

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRGS4630DPbF	D²Pak	Tube	50	IRGS4630DPbF
		Tape and Reel Right	800	IRGS4630DTRRPbF
		Tape and Reel Left	800	IRGS4630DTRLPbF
IRGB4630DPbF	TO-220AB	Tube	50	IRGB4630DPbF
IRGP4630DPbF	TO-247AC	Tube	25	IRGP4630DPbF
IRGP4630D-EPbF	TO-247AD	Tube	25	IRGP4630D-EPbF

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	47	A
I_C @ T_C = 100°C	Continuous Collector Current	30	
I_{CM}	Pulse Collector Current, V_{GE}=15V	54	
I_{LM}	Clamped Inductive Load Current, V_{GE}=20V ①	72	
I_F @ T_C = 25°C	Diode Continuous Forward Current	30	
I_F @ T_C = 100°C	Diode Continuous Forward Current	18	
I_{FM}	Diode Maximum Forward Current ④	72	
V_{GE}	Continuous Gate-to-Emitter Voltage	±20	V
	Transient Gate to Emitter Voltage	±30	
P_D @ T_C = 25°C	Maximum Power Dissipation	206	W
P_D @ T_C = 100°C	Maximum Power Dissipation	103	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-40 to +175	C
	Soldering Temperature, for 10 sec. (1.6mm from case)	300	
	Mounting Torque, 6-32 or M3 Screw (TO-220, TO-247)	10 lbf·in (1.1 N·m)	

Notes ① through ⑥ are on page 7

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Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$ (IGBT)	Thermal Resistance Junction-to-Case (D^2Pak, TO-220) ②	—	—	0.73	°C/W
	Thermal Resistance Junction-to-Case (TO-247) ②	—	—	0.78	
$R_{\theta JC}$ (Diode)	Thermal Resistance Junction-to-Case (D^2Pak, TO-220) ②	—	—	2.0	
	Thermal Resistance Junction-to-Case (TO-247) ②	—	—	2.1	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink (flat, greased surface)	—	0.5	—	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (PCB Mount - D^2Pak) ⑥	—	—	40	
	Thermal Resistance, Junction-to-Ambient (Socket Mount –TO-220)	—	—	62	
	Thermal Resistance, Junction-to-Ambient (Socket Mount –TO-247)	—	—	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 100µA ③
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.40	—	V/°C	V_{GE} = 0V, I_C = 1mA (25°C-175°C)
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.65	1.95	V	I_C = 18A, V_{GE} = 15V, T_J = 25°C
		—	2.05	—		I_C = 18A, V_{GE} = 15V, T_J = 150°C
		—	2.15	—		I_C = 18A, V_{GE} = 15V, T_J = 175°C
$V_{GE(th)}$	Gate Threshold Voltage	4.0	—	6.5	V	V_{CE} = V_{GE}, I_C = 500µA
$\Delta V_{GE(th)}/\Delta T_J$	Threshold Voltage Temp. Coefficient	—	-18	—	mV/°C	V_{CE} = V_{GE}, I_C = 1.0mA (25°C-175°C)
gfe	Forward Transconductance	—	12	—	S	V_{CE} = 50V, I_C = 18A, PW = 80µs
I_{CES}	Collector-to-Emitter Leakage Current	—	2.0	25	µA	V_{GE} = 0V, V_{CE} = 600V
		—	550	—		V_{GE} = 0V, V_{CE} = 600V, T_J = 175°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V
V_{FM}	Diode Forward Voltage Drop	—	2.3	3.3	V	I_F = 18A
		—	1.6	—		I_F = 18A, T_J = 175°C

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max	Units	Conditions
Q_g	Total Gate Charge	—	35	—	nC	I_C = 18A
Q_{ge}	Gate-to-Emitter Charge	—	10	—		V_{GE} = 15V
Q_{gc}	Gate-to-Collector Charge	—	15	—		V_{CC} = 400V
E_{on}	Turn-On Switching Loss	—	95	—	µJ	I_C = 18A, V_{CC} = 400V, V_{GE}=15V
E_{off}	Turn-Off Switching Loss	—	350	—		R_G = 22Ω, L = 200µH, L_S = 150nH,
E_{total}	Total Switching Loss	—	445	—		T_J = 25°C
$t_{d(on)}$	Turn-On delay time	—	40	—	ns	Energy losses include tail & diode
t_r	Rise time	—	25	—		reverse recovery ⑤
$t_{d(off)}$	Turn-Off delay time	—	105	—		
t_f	Fall time	—	25	—		
E_{on}	Turn-On Switching Loss	—	285	—	µJ	I_C = 18A, V_{CC} = 400V, V_{GE}=15V
E_{off}	Turn-Off Switching Loss	—	570	—		R_G = 22Ω, L = 200µH, L_S = 150nH,
E_{total}	Total Switching Loss	—	855	—		T_J = 175°C
$t_{d(on)}$	Turn-On delay time	—	40	—	ns	Energy losses include tail & diode
t_r	Rise time	—	25	—		reverse recovery ⑤
$t_{d(off)}$	Turn-Off delay time	—	120	—		
t_f	Fall time	—	40	—		
C_{ies}	Input Capacitance	—	1040	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	87	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	32	—		f = 1.0MHz
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				T_J = 175°C, I_C = 72A V_{CC} = 480V, Vp ≤ 600V R_G = 22Ω, V_{GE} = +20V to 0V
SCSOA	Short Circuit Safe Operating Area	5.0	—	—	µs	V_{CC} = 400V, Vp ≤ 600V R_G = 22Ω, V_{GE} = +15V to 0V
Erec	Reverse Recovery Energy of the Diode	—	260	—	µJ	T_J = 175°C
t_{rr}	Diode Reverse Recovery Time	—	100	—	ns	V_{CC} = 400V, I_F = 18A, V_{GE} = 15V,
I_{rr}	Peak Reverse Recovery Current	—	23	—	A	Rg = 22Ω, L = 200µH, L_S = 150nH

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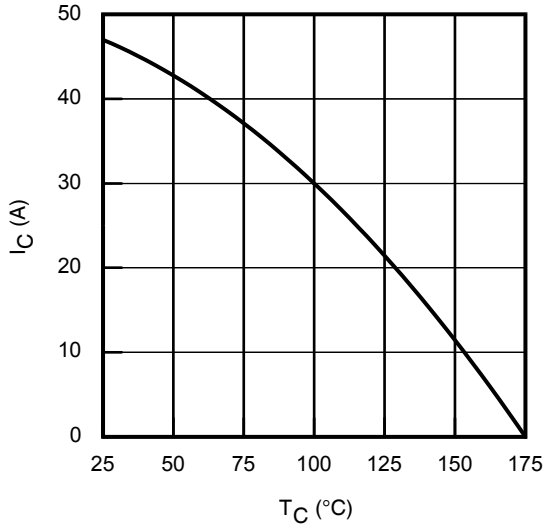


Fig. 1 - Maximum DC Collector Current vs. Case Temperature

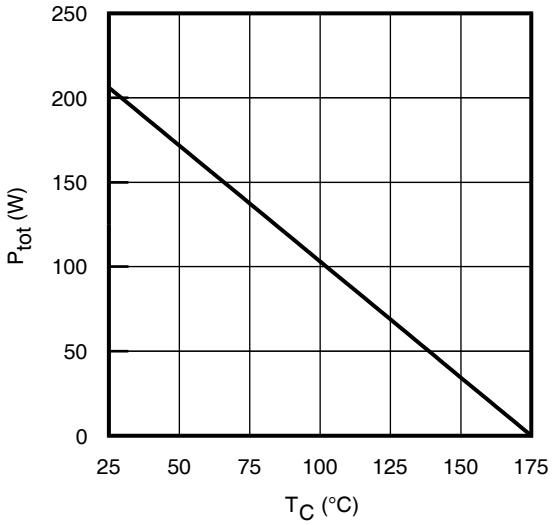


Fig. 2 - Power Dissipation vs. Case Temperature

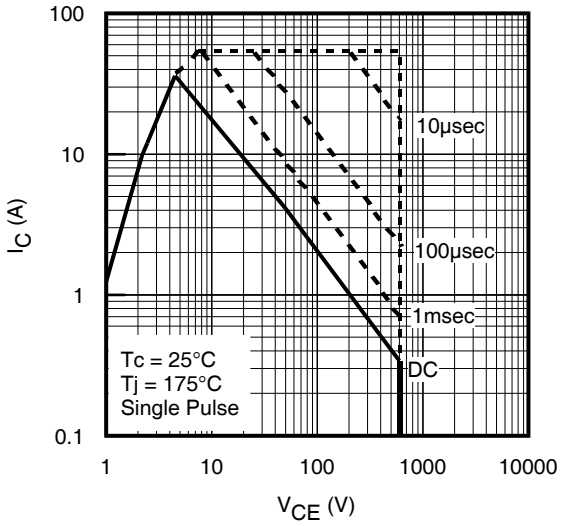


Fig. 3 - Forward SOA
T_C = 25°C; T_J ≤ 175°C; V_{GE} = 15V

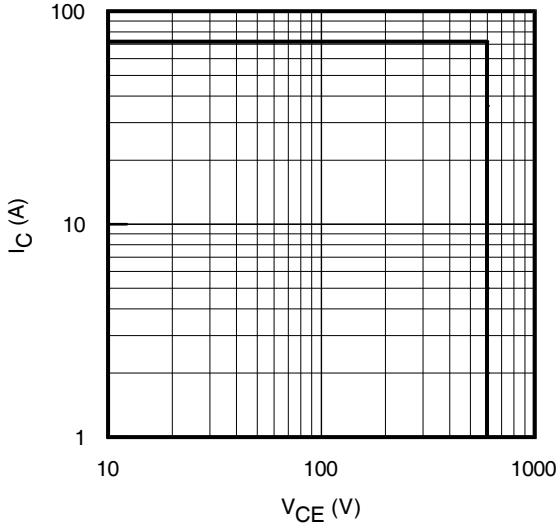


Fig. 4 - Reverse Bias SOA
T_J = 175°C; V_{GE} = 20V

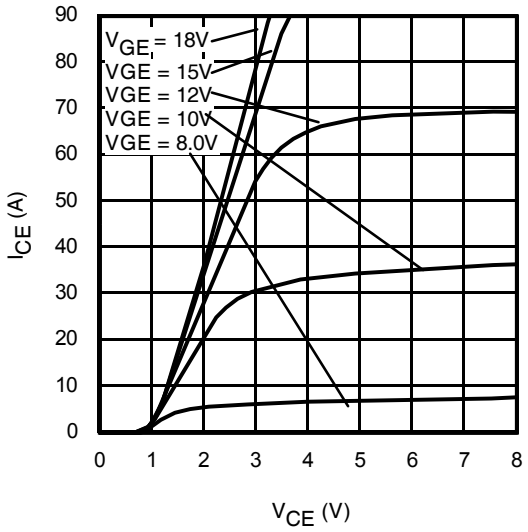


Fig. 5 - Typ. IGBT Output Characteristics
T_J = -40°C; tp = 80µs

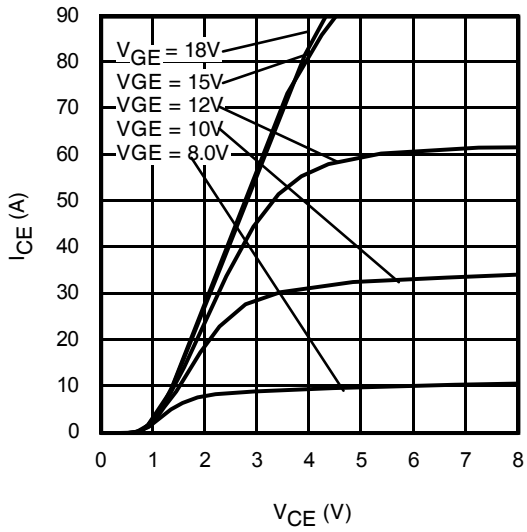


Fig. 6 - Typ. IGBT Output Characteristics
T_J = 25°C; tp = 80µs

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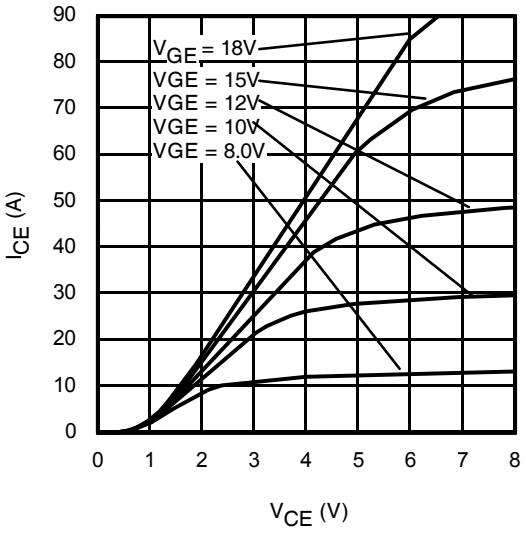


Fig. 7 - Typ. IGBT Output Characteristics
T_J = 175°C; tp = 80µs

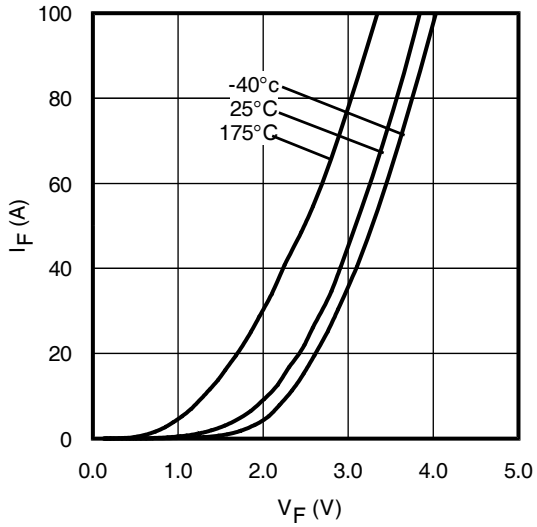


Fig. 8 - Typ. Diode Forward Voltage Drop Characteristics

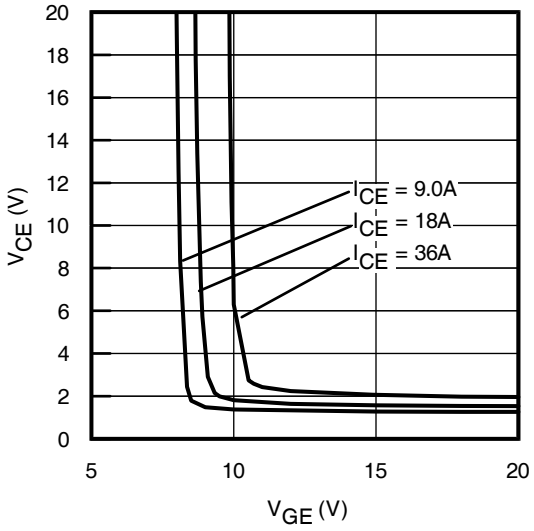


Fig. 9 - Typical V_{CE} vs. V_{GE}
T_J = -40°C

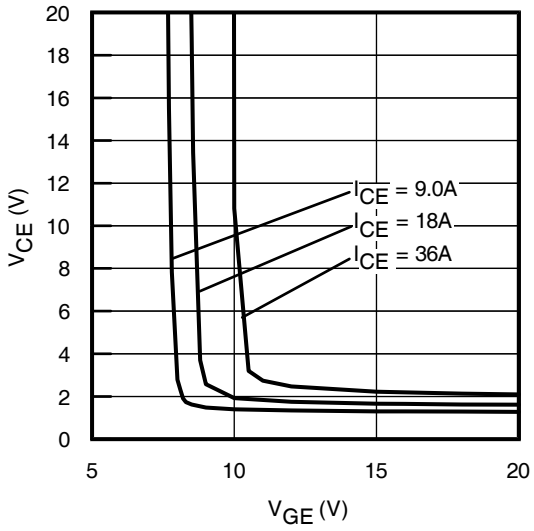


Fig. 10 - Typical V_{CE} vs. V_{GE}
T_J = 25°C

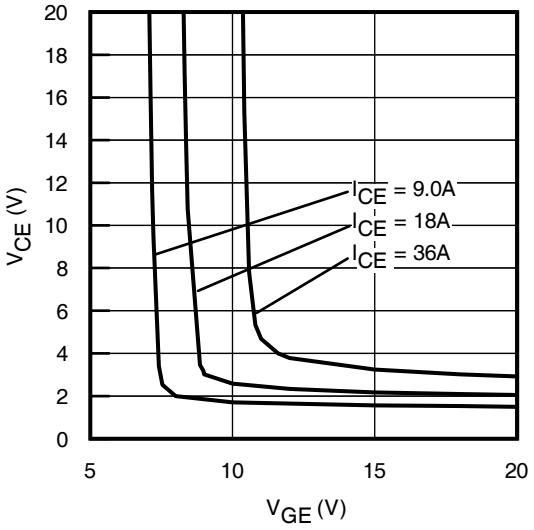


Fig. 11 - Typical V_{CE} vs. V_{GE}
T_J = 175°C

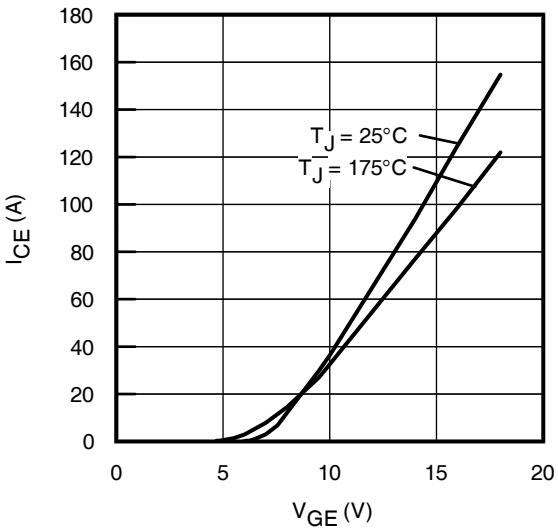


Fig. 12 - Typ. Transfer Characteristics
V_{CE} = 50V; tp = 10µs

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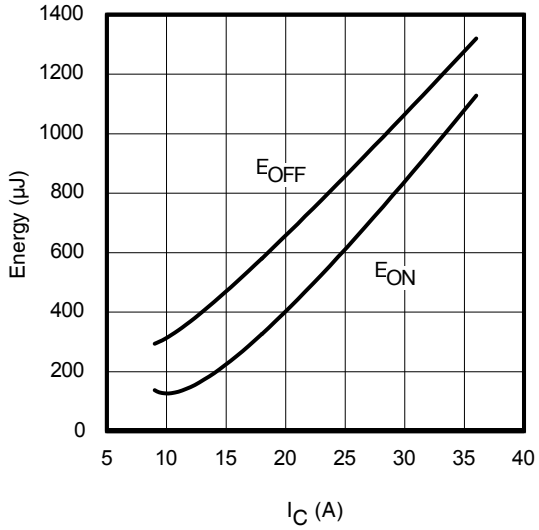


Fig. 14 - Typ. Energy Loss vs. I_C
T_J = 175°C; L = 200µH; V_{CE} = 400V, R_G = 22Ω; V_{GE} = 15V

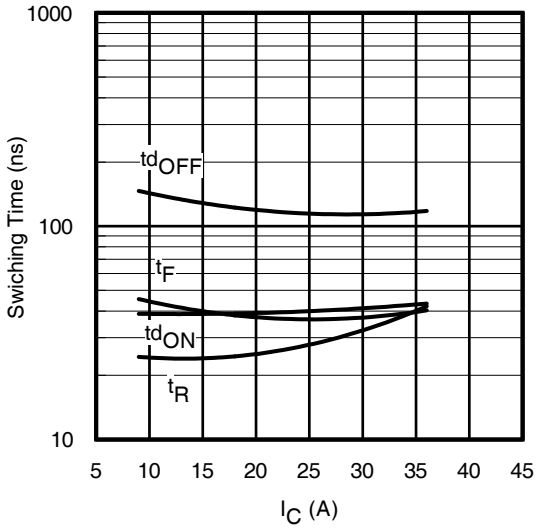


Fig. 15 - Typ. Switching Time vs. I_C
T_J = 175°C; L = 200µH; V_{CE} = 400V, R_G = 22Ω; V_{GE} = 15V

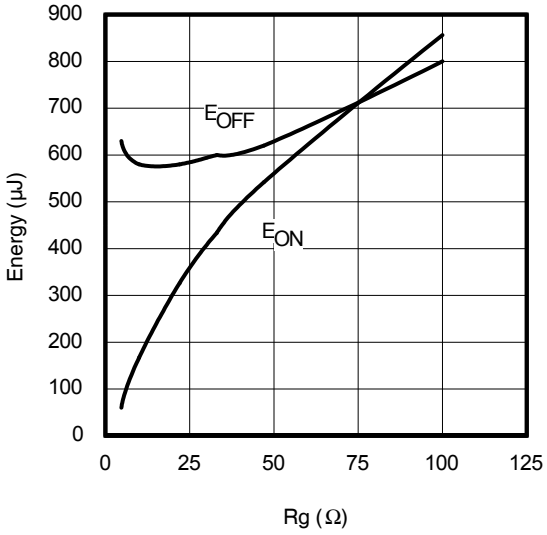


Fig. 16 - Typ. Energy Loss vs. R_G
T_J = 175°C; L = 200µH; V_{CE} = 400V, I_{CE} = 18A; V_{GE} = 15V

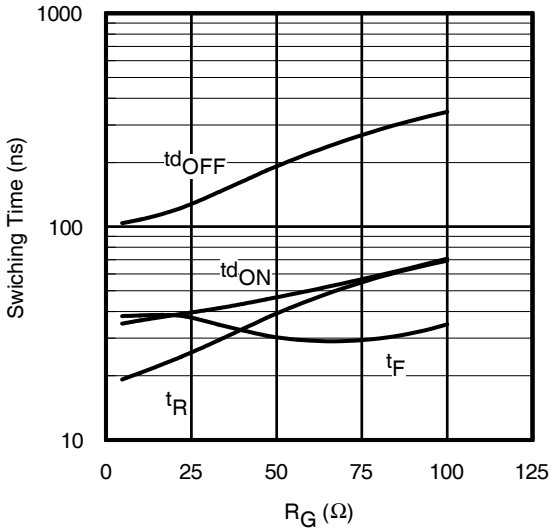


Fig. 17 - Typ. Switching Time vs. R_G
T_J = 175°C; L = 200µH; V_{CE} = 400V, I_{CE} = 18A; V_{GE} = 15V

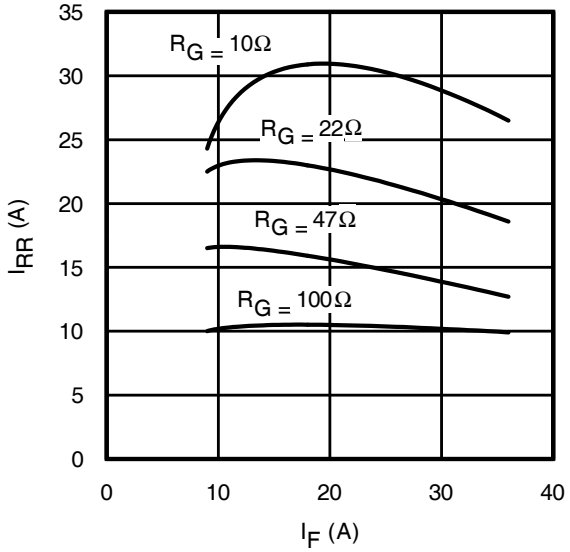


Fig. 18 - Typ. Diode I_{RR} vs. I_F
T_J = 175°C

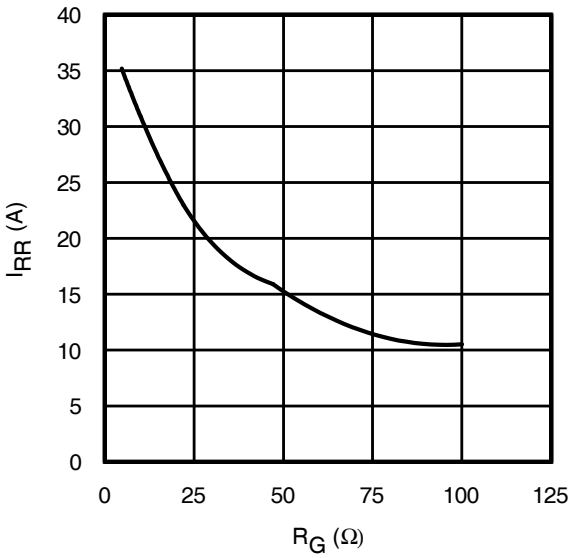


Fig. 19 - Typ. Diode I_{RR} vs. R_G
T_J = 175°C

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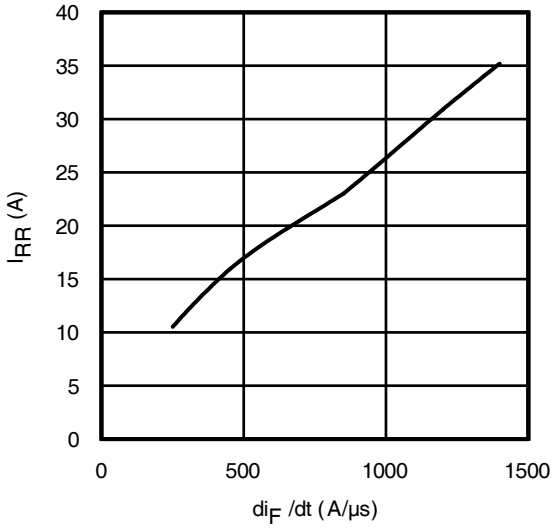


Fig. 20 - Typ. Diode I_{RR} vs. di_F/dt
V_{CC} = 400V; V_{GE} = 15V; I_F = 18A; T_J = 175°C

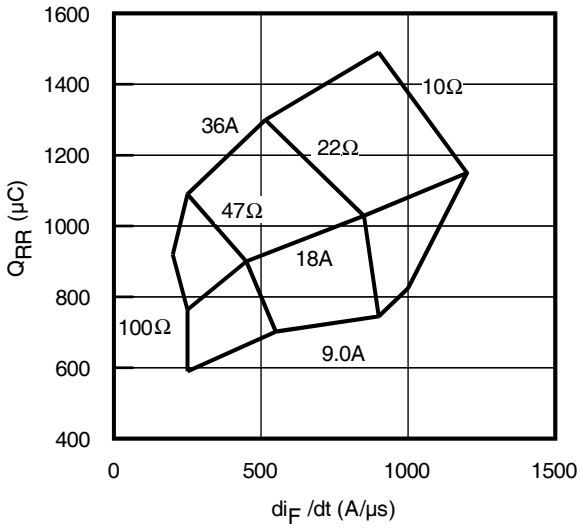


Fig. 21 - Typ. Diode Q_{RR} vs. di_F/dt
V_{CC} = 400V; V_{GE} = 15V; T_J = 175°C

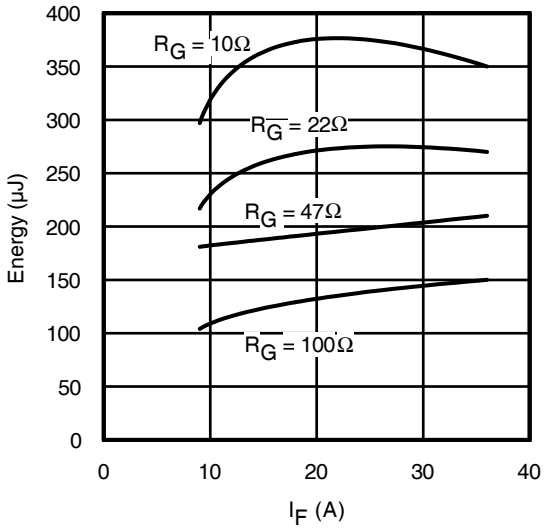


Fig. 22 - Typ. Diode E_{RR} vs. I_F
T_J = 175°C

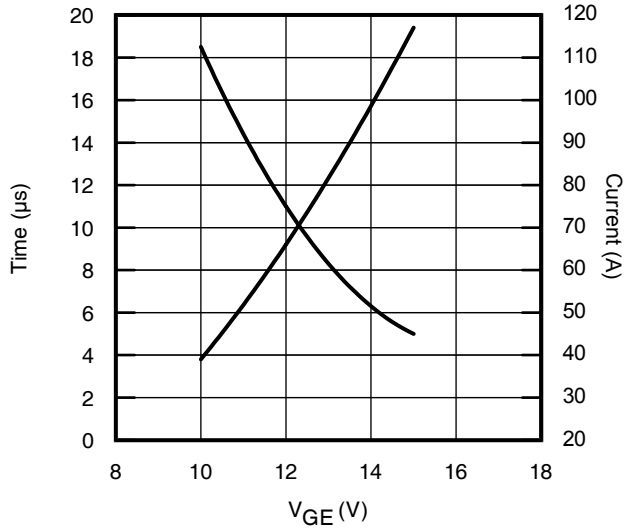


Fig. 23 - V_{GE} vs. Short Circuit Time
V_{CC} = 400V; T_C = 25°C

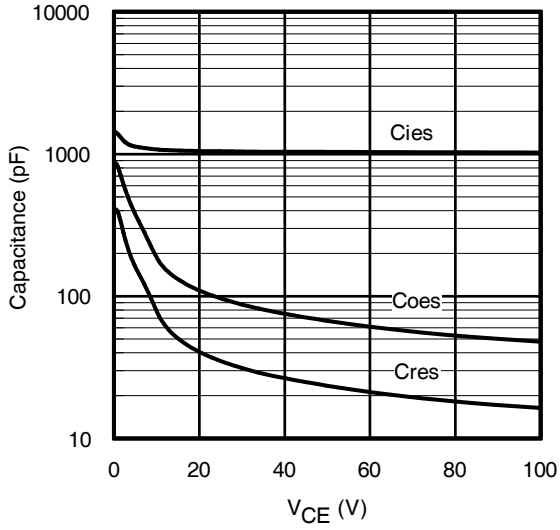


Fig. 24 - Typ. Capacitance vs. V_{CE}
V_{GE}= 0V; f = 1MHz

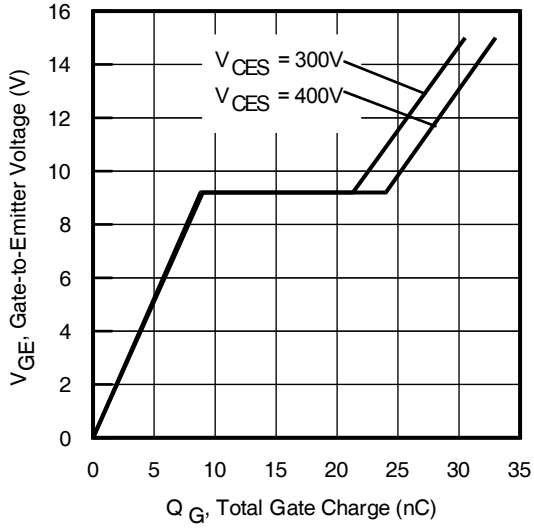


Fig. 25 - Typical Gate Charge vs. V_{GE}
I_{CE} = 18A; L = 600µH

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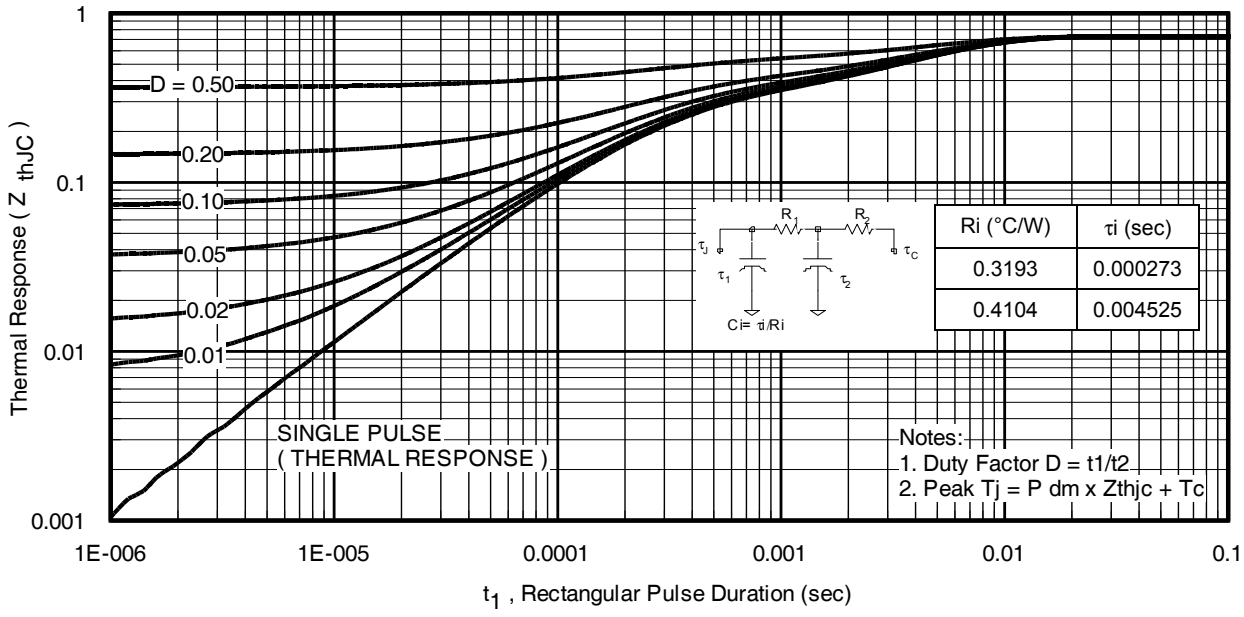


Fig. 26 - Maximum Transient Thermal Impedance, Junction-to-Case (IGBT)

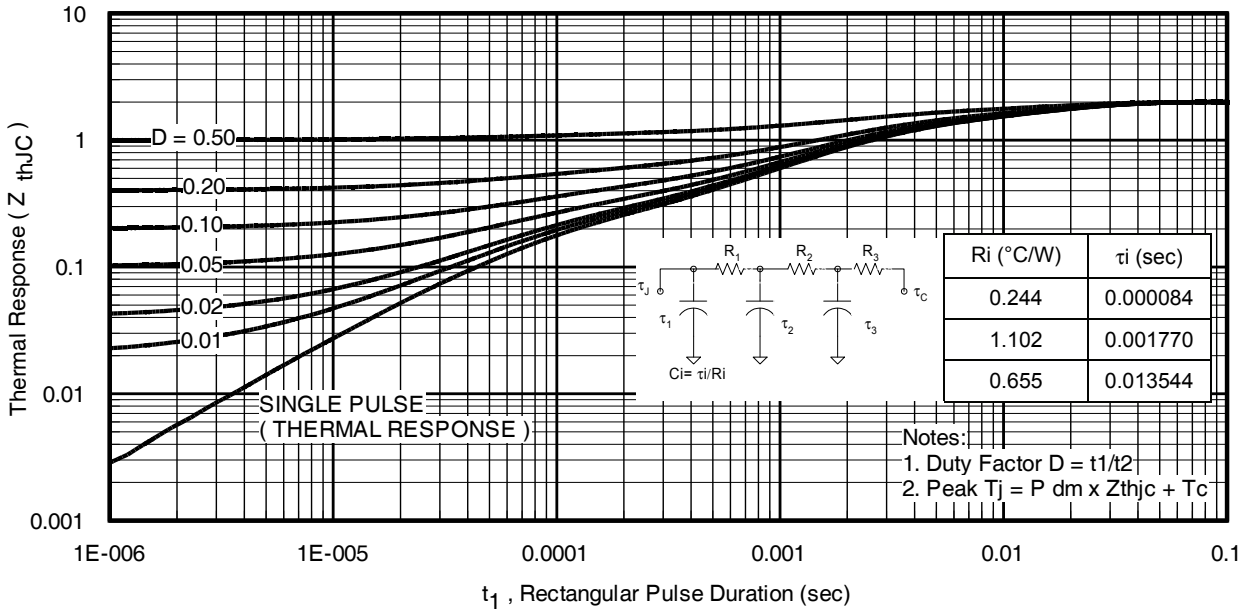


Fig. 27 - Maximum Transient Thermal Impedance, Junction-to-Case (DIODE)

Notes:

① V_{CC} = 80% (V_{CES}), V_{GE} = 20V, L = 100µH, R_G = 22Ω.

② R_θ is measured at T_J of approximately 90°C.

③ Refer to AN-1086 for guidelines for measuring $V_{(BR)CES}$ safely.

④ Pulse width limited by maximum junction temperature.

⑤ Values influenced by parasitic L and C in measurement.

⑥ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.http://www.irf.com/technical-info/appnotes/an-994.pdf

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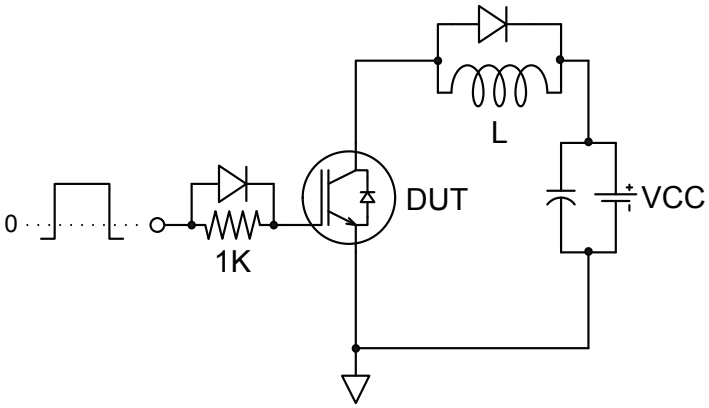


Fig.C.T.1 - Gate Charge Circuit (turn-off)

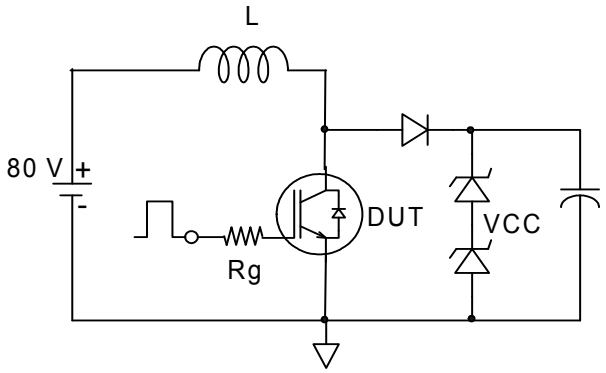


Fig.C.T.2 - RBSOA Circuit

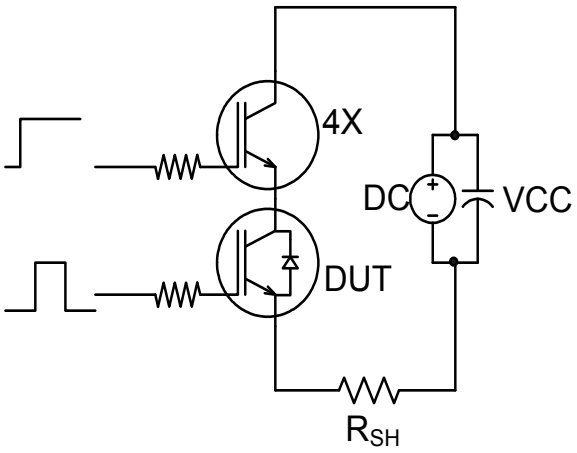


Fig.C.T.3 - S.C. SOA Circuit

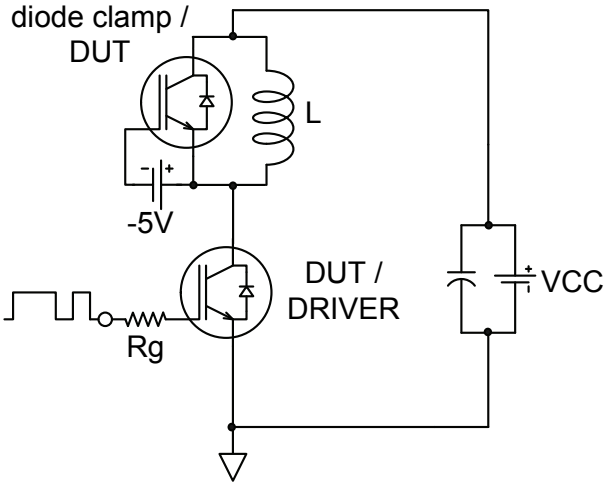


Fig.C.T.4 - Switching Loss Circuit

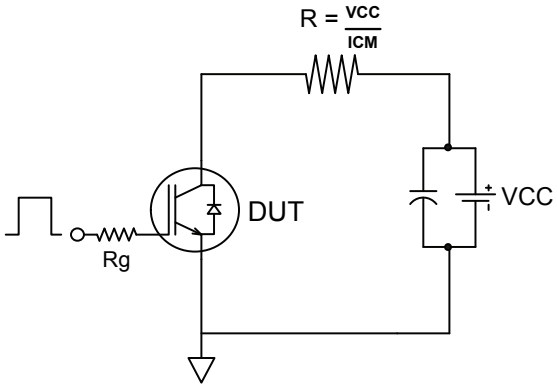


Fig.C.T.5 - Resistive Load Circuit

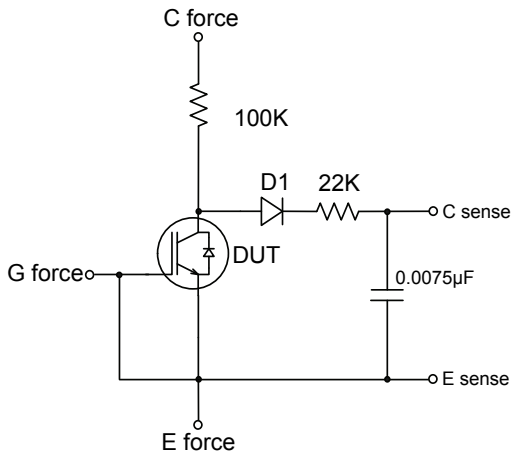


Fig.C.T.6 - BVCES Filter Circuit

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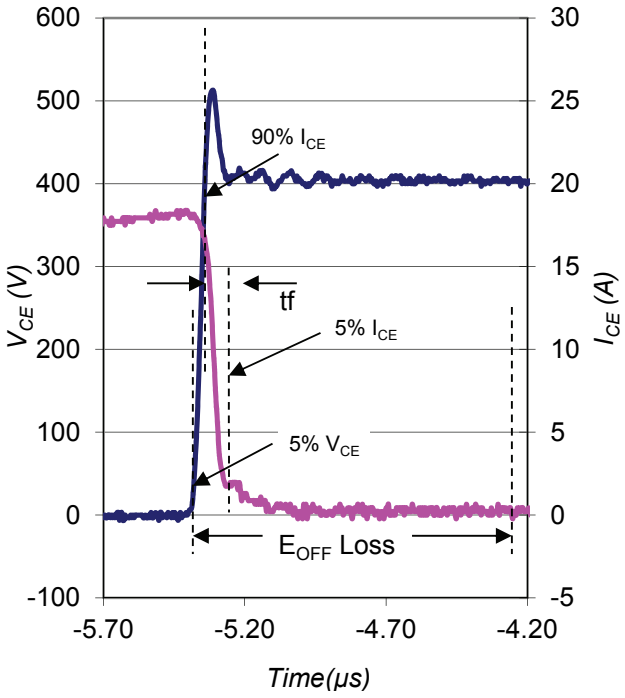


Fig. WF1 - Typ. Turn-off Loss Waveform
@ T_J = 175°C using Fig. CT.4

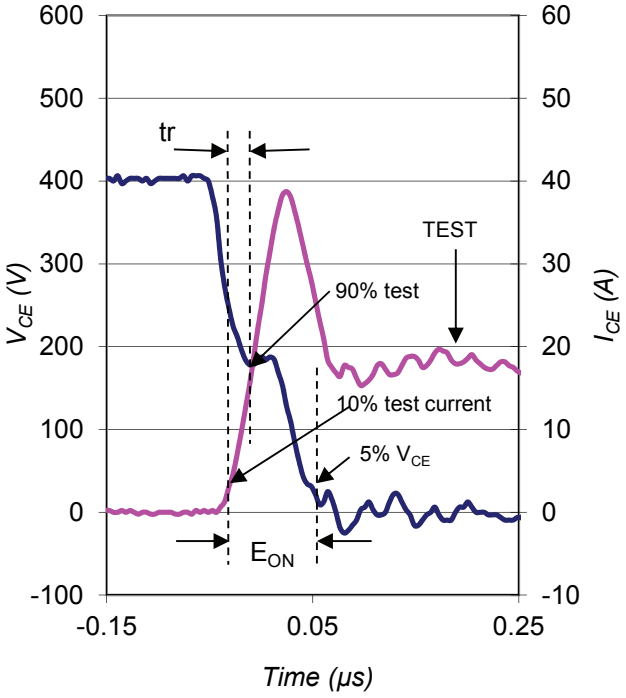


Fig. WF2 - Typ. Turn-on Loss Waveform
@ T_J = 175°C using Fig. CT.4

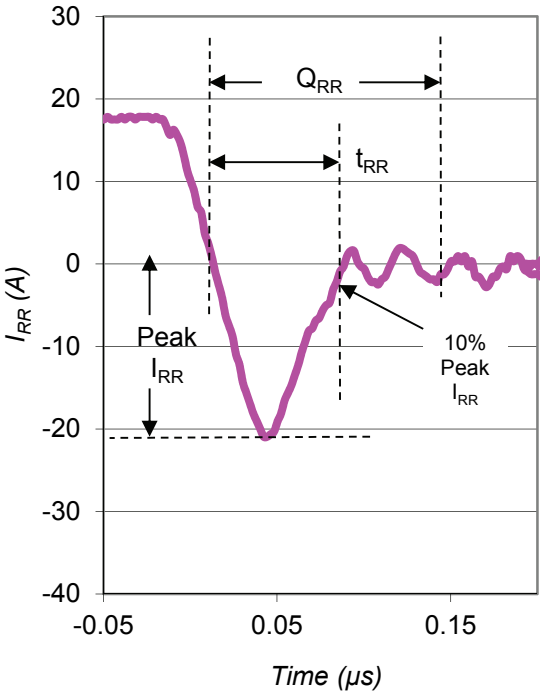


Fig. WF3 - Typ. Diode Recovery Waveform
@ T_J = 175°C using Fig. CT.4

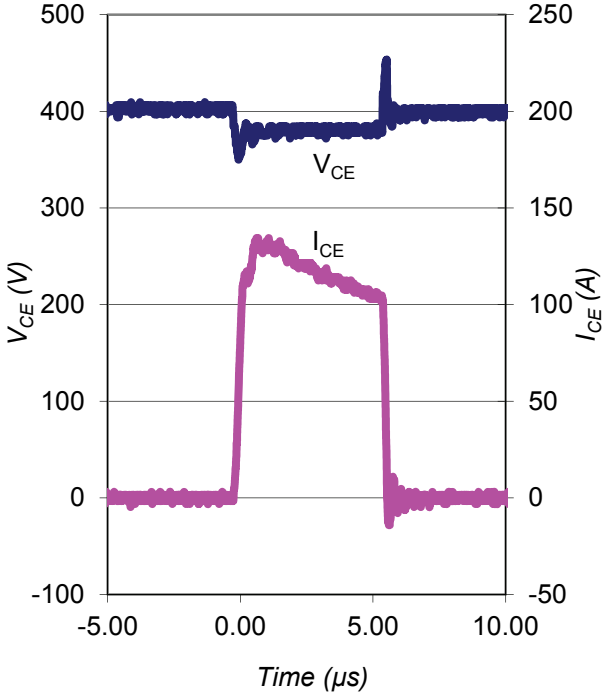
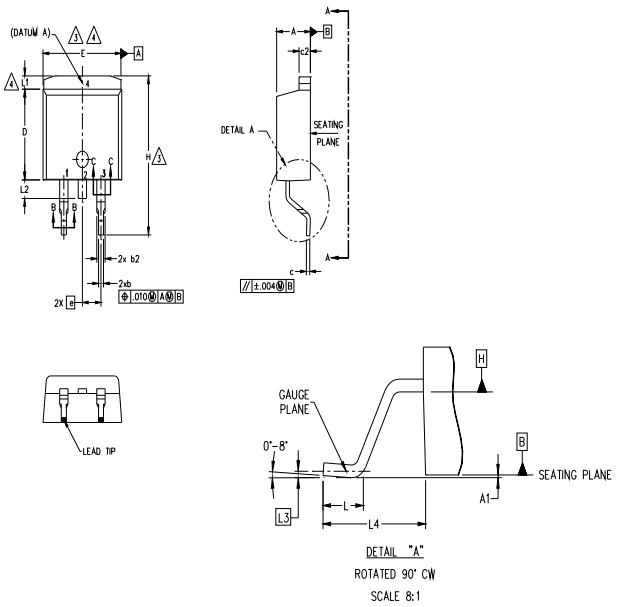


Fig. WF4 - Typ. S.C. Waveform
@ T_J = 150°C using Fig. CT.3

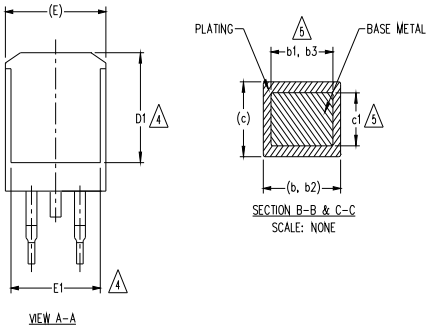
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D^2-PAK (TO-263AB) Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270		4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245		4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	–	1.65	–	.066	4
L2	–	1.78	–	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	



LEAD ASSIGNMENTS

DIODES

1.- ANODE (TWO DIE) / OPEN (ONE DIE)
2, 4.- CATHODE
3.- ANODE

HEXFET

1.- GATE
2, 4.- DRAIN
3.- SOURCE

IGBTs, CoPACK

1.- GATE
2, 4.- COLLECTOR
3.- EMITTER

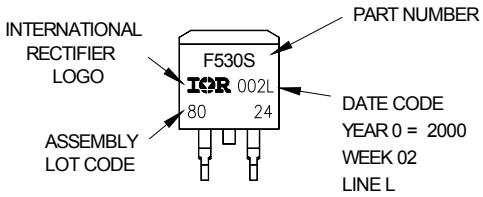
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

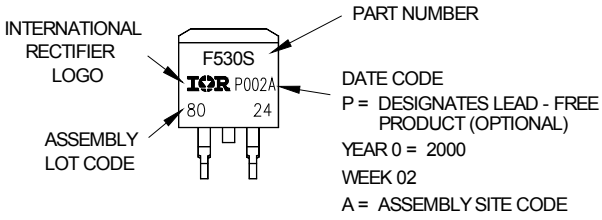
D^2-Pak (TO-263AB) Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position
indicates "Lead – Free"



OR

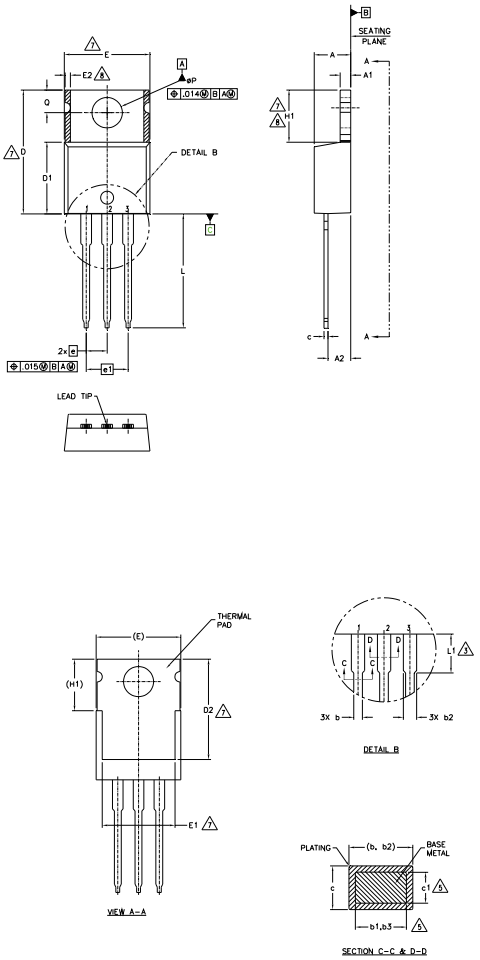


Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

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TO-220AB Package Outline

(Dimensions are shown in millimeters (inches))



NOTES:

1.– DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M– 1994.
2.– DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3.– LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4.– DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5.– DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
6.– CONTROLLING DIMENSION : INCHES.
7.– THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
8.– DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
9.– OUTLINE CONFORMS TO JEDEC TO–220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	1.14	1.40	.045	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	–	0.76	–	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE

IGBTs, CoPACK

1.– GATE
2.– COLLECTOR
3.– EMITTER

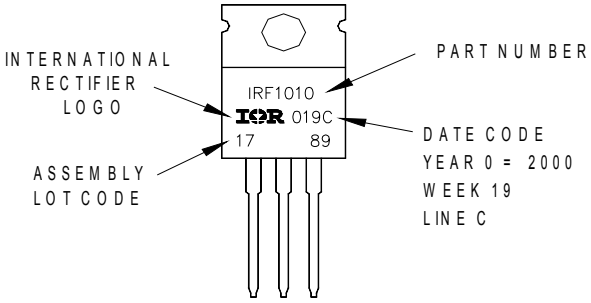
DIODES

1.– ANODE
2.– CATHODE
3.– ANODE

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 2000
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



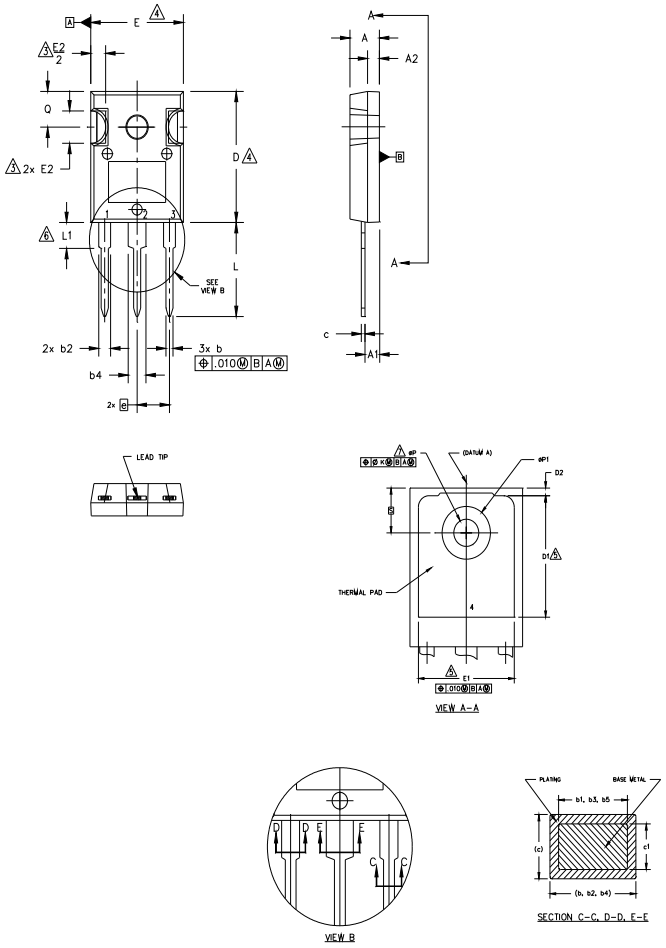
TO-220AB package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

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TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. øP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	–	13.08	–	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	–	13.46	–	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
øP	.140	.144	3.56	3.66	
øP1	–	.291	–	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

IGBTs, CoPACK

1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

DIODES

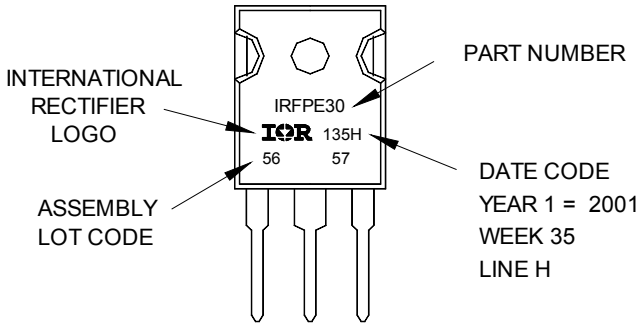
1.– ANODE/OPEN
2.– CATHODE
3.– ANODE

TO-247AC Part Marking Information

Notes: This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2001
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"



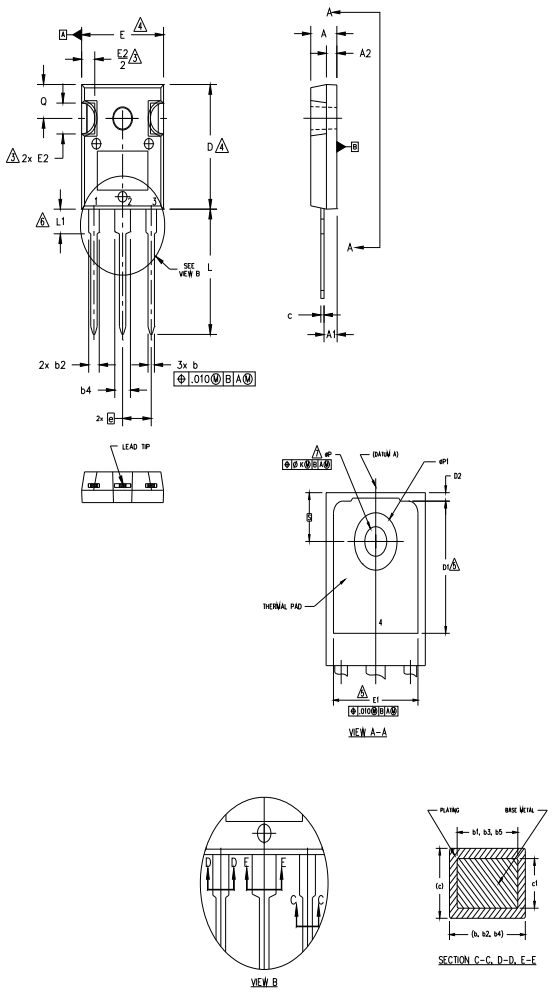
TO-247AC package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

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TO-247AD Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. øP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AD.

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	–	13.08	–	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	–	13.46	–	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
øk	.010		0.25		
L	.780	.827	19.57	21.00	
L1	.146	.169	3.71	4.29	
øP	.140	.144	3.56	3.66	
øP1	–	.291	–	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

IGBTs, CoPACK

1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

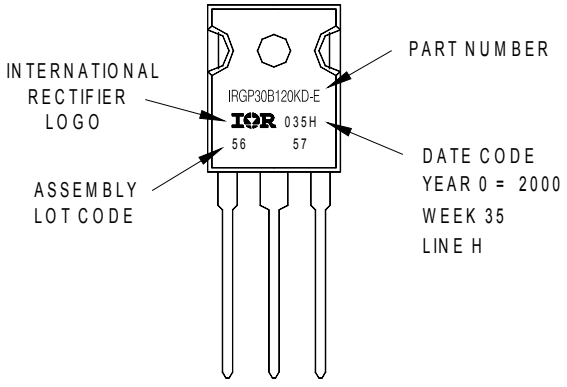
DIODES

1.– ANODE/OPEN
2.– CATHODE
3.– ANODE

TO-247AD Part Marking Information

EXAMPLE: THIS IS AN IRGP30B120KD-E
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2000
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"



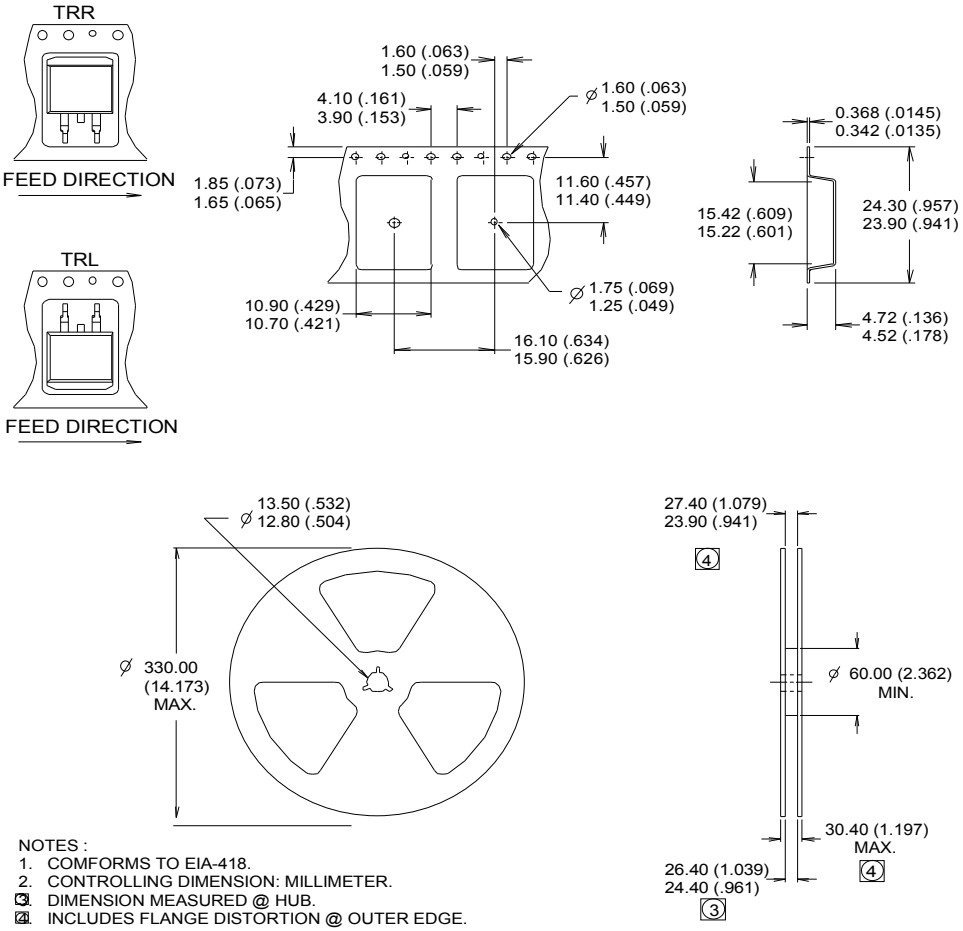
TO-247AD package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

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D^{2}Pak Tape & Reel Information

(Dimensions are shown in millimeters (inches))



NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

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Qualification Information†

Qualification Level	Industrial (per JEDEC JESD47F) ††	
Moisture Sensitivity Level	D^2Pak	MSL1
	TO-220AB	N/A
	TO-247AC	N/A
	TO-247AD	N/A
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: http://www.irf.com/product-info/reliability/

†† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
11/18/2014	• Added note ④ to I_{FM} Diode Maximum Forward Current on page 1. • Added note ⑤ from switching losses test condition on page 2. • Updated package outline on page 11.

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