NOVATEK
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Data Sheet

For NT68667FG/ NT68667HFG/ NT68667UFG Scaler

Flat Panel Monitor Controller

V 1.5

TABLE OF CONTENTS

1. REVISION HISTORY 4

2. FEATURES 5

3. GENERAL DESCRIPTION 7

4. BLOCK DIAGRAM 8

5. PINOUT INFORMATION 9

5.1. PIN DIAGRAM 9
5.2. PIN ASSIGNMENT 10
5.3. PIN DESCRIPTION 15

6. FUNCTIONAL DESCRIPTION 17

6.1. POWER CONTROL 17
6.2. ANALOG TO DIGITAL CONVERTER (ADC) 17
6.3. DVI RECEIVER 18
6.4. GRAPHIC PORT CAPTURE INTERFACE 18
6.5. VIDEO PORT CAPTURE INTERFACE 19
6.6. AUTO TUNE 19
6.7. VIDEO PROCESSOR 19
6.8. SYNC PROCESSOR 21
6.9. OSD FUNCTION 24
6.10. DPLL CLOCK CONTROL 32
6.11. DISPLAY INTERFACE 33
6.11.1. Scaler Display Data 33
6.11.2. Single/Dual pixel LVDS Transmitter 34
6.12. MISCELLANEOUS 36
6.12.1. PWM Output 36
6.13. MCU INTERFACE 37
6.13.1. IRQn Interrupt Sources 37
6.14. 8031 ON-CHIP MICROCONTROLLER 38

7. ELECTRICAL SPECIFICATIONS 39

7.1. DC ELECTRICAL CHARACTERISTICS 39
7.2. AC ELECTRICAL CHARACTERISTICS 44

8. REGISTERS MAPPING 47

8.1. ADC INTERFACE 48
8.2. DVI INPUT CONTROL 1 51
8.3. PRE-PATTERN CONTROL 53
8.4. GRAPHIC PORT CONTROL 53
8.5. VIDEO PORT CONTROL 61
8.6. COLOR SPACE CONVERSION CONTROL 63
8.7. VIDEO PORT CAPTURE CONTROL 64
8.8. BACK END IMAGE PROCESSING 65
8.9. NOISE REDUCTION FILTER CONTROL 67
8.10. GENERAL PURPOSE INPUT OUTPUT (GPIO) 68
8.11. PWM OUTPUT 69
8.12. ON SCREEN DISPLAY REGISTERS 71
8.13. SOURCE HSYNC DIGITAL PLL CONTROL 87
8.14. INDEX PORT ACCESS CONTROL 90

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8.15. AUTO GAIN/GAUGE ACCESS WINDOW CONTROL 91
8.16. DISPLAY DIGITAL PLL CONTROL 93
8.17. GRAPHIC INPUT GAUGE 95
8.18. PRODUCT ID 95
8.19. POWER CONTROL 96
8.20. AUTO TUNE 96
8.21. BRIGHT FRAME DISPLAY REGISTERS 102
8.22. DVI INPUT CONTROL 2 104
8.23. DISPLAY PORT CONTROL 105
8.24. SYNC PROCESSOR 115
8.25. LVDS OUTPUT CONTROL 123
8.26. SRGB CONTROL 126
8.27. HIGH-BANDWIDTH DIGITAL CONTENT PROTECTION SYSTEM 131
8.28. DITHERING FUNCTION 2 137
8.29. HORIZONTAL NON-LINEAR SCALING FUNCTION 140
8.30. BRIGHT FRAME BORDER FUNCTION 141
8.31. Y/C PEAKING CONTROL 144
8.32. ACE CONTROL 145
8.33. COLOR MANAGEMENT 147
8.34. DBC 150

9. ORDERING INFORMATION 153

PACKAGE INFORMATION 154

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1. Revision History

NT68667 Specification Revision History		
Version	Content	Data
0.1	First version released	Oct. 2007
0.2	Delete TCON feature	Dec. 2007
1.0	Release	Feb. 2008
1.1	Register , AC/DC spec. update	Mar. 2008
1.2	Add chip surface temperature	Mar. 2008
1.3	0x150~0x153 reg. update 0x13A, 0x13B remove	Mar. 2008
1.4	Block diagram update Non-linear ACE reg. update NR Reg. 0x068 , 0x06A update	Apr. 2008
1.5	0x338 update Add U type spec.	May. 2008

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2. Features

Analog Graphic Input

- Support RGB inputs **1440x900@75hz for NT68667FG , 1680x1050@75hz for NT68667HFG , 1920x1080@75hz for NT68667UFG** or YPbPr (**1080p**) inputs
- Triple 8bit ADCs (0.55~0.9V) with 500MHz bandwidth
- **166Mhz(NT68667FG)/188MHz(NT68667HFG)/190MHz(NT68667UFG)** HPLL with 64 steps phase adjust for each RGB channel
- Auto offset for component video
- Supports both non-interlaced and interlaced input signals
- ADC bandwidth adjust : 500M,450M,400M,350M,300M,250M,150M,75M

Digital Graphic and Video Inputs

- DVI receiver up to 165MHz with HDCP with HDCP 280 bytes sram
- Supports ITU-R BT.656 8-bit Input format

Video Processing

- Zoom and shrink engineer with non-linear scaling in horizontal direction for wide screen panels
- The 3rd generation Bright Frame with adaptive contrast control, 24 color tones adjustment , sRGB real color engine and edge enhancement functions
- Adjustable sharpness setting
- Support DBC to save system operation power
- Fixed 10 bit dither LSB & 10-8 dither enable
- Text Enahncement
- Enhance ghost cancellation

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Sync Processor

- Support TTL Sync-On-Green (SOG) (including Sync Slicer)
- Polarity detection
- Frequency measurement
- Fast mode change detection
- Interlace or non-interlace input detection
- Separate or composite sync auto switching (including Sync Separator)

Internal OSD

- Programmable multi-color RAM font as well as a bitmapped graphical OSD are supported
- Provide 1,2,3/4 bits/pixel RAM Fonts
- Optional 10x18, 12x18, 10x16, 12x16 dot matrix
- Internal SRAM allows up to 2048 characters, with programmable OSD frame size. Width is 64 column, and Height is 32 row
- Programmable shadow or border control for each character by each row
- Programmable blinking effects for each character
- Spacing control to avoid expansion distortion
- Supports simultaneous display of up to 4 OSD windows
- Maximum 4 times of global zoom for horizontal and vertical axis
- Separate row zoom control
- Support flexible FG or BG optional transparent, translucent, and opaque effects
- 256 palette with 64K color selectable
- Top-bottom flip, left-right mirror and 90 degree / 270 degree rotated
- Flexible Fade-in, Fade-out effect

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- Splitting OSD frame supported
- Gradient fade-in/fade –out
- Insert variable space by row
- Total provide 15K byte RAM size

Display Output

- Support 8/6bit single/dual port LVDS panel up to **1440x900@75 for NT68667FG , 1680x1050@75 for NT68667HFG and 1920x1080@75 for NT68667UFG**
- LVDS support up to **190MHz**
- All of output keep “low” after power up

Built-in Dual Pixel LVDS Transmitter

- Integrate the Dual Port, 4 Data Channel and Clock-Out Low-Voltage differential LVDS transmitter to supports single or dual pixel 6/8-bit display data transmission
- Suited for VGA, SVGA, XGA and dual pixel SXGA, WSXGA display transmission from controller to display with very low EMI

Embedded Microcontroller

- External SPI program memory supported
- 1 UART, 2 timers, 2 external Interrupts
- 2 x I2C master/slavers for DDC2Bi/2B+/Ci and EDID functions
- I/Os: 4 x 7bits ADC, 10 x PWM, totally 35 adjustable I/Os
- Support DDC 5V/3.3V compatible

Power

- 3.3V/1.8V power supply
- Normal operate less than 1W
- Embedded 3.3 to 1.8 LDO

Package

- QFP 128 pin

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3. General Description

The NT68667 is a highly integrated flat panel display controller that interfaces analog, digital, and video inputs. It combines a triple ADC, a DVI compliant TMDS receiver, a digital YUV receiver, a high quality zoom and shrink engine , a multi-color on screen display (OSD) controller , an advanced color engine , and many other functions in a single chip. It provides the user with a simple, flexible and cost-effective solution for various flat panel display products.

The NT68667 operates at frequencies up to **166Mhz/188MHz/190Mhz** suitable for LCD monitor up to **1440x900/1680x1050/1920x1080** resolution. The NT68667 also has a built-in noise reduction function to provide more stable video quality, spread spectrum to provide low EMI solution, sRGB for video color space convert and post pattern for manufacture test.

The display provided single/double pixel clock LVDS interface.

In addition, NT68667 includes an integrated 8-Bit Microcontroller (MCU). It contains an 8-bit 8031 micro-controller, 3,840 –bytes internal data memory, four 7-bit resolution A/D Converter, 10-channel 8-bit resolution PWM DAC, two16-bit timer/counters, and a UART. Except those, it has two-channel hardware DDC solution, and VESA 2Bi/2B+ master/slave I^2C bus interface.

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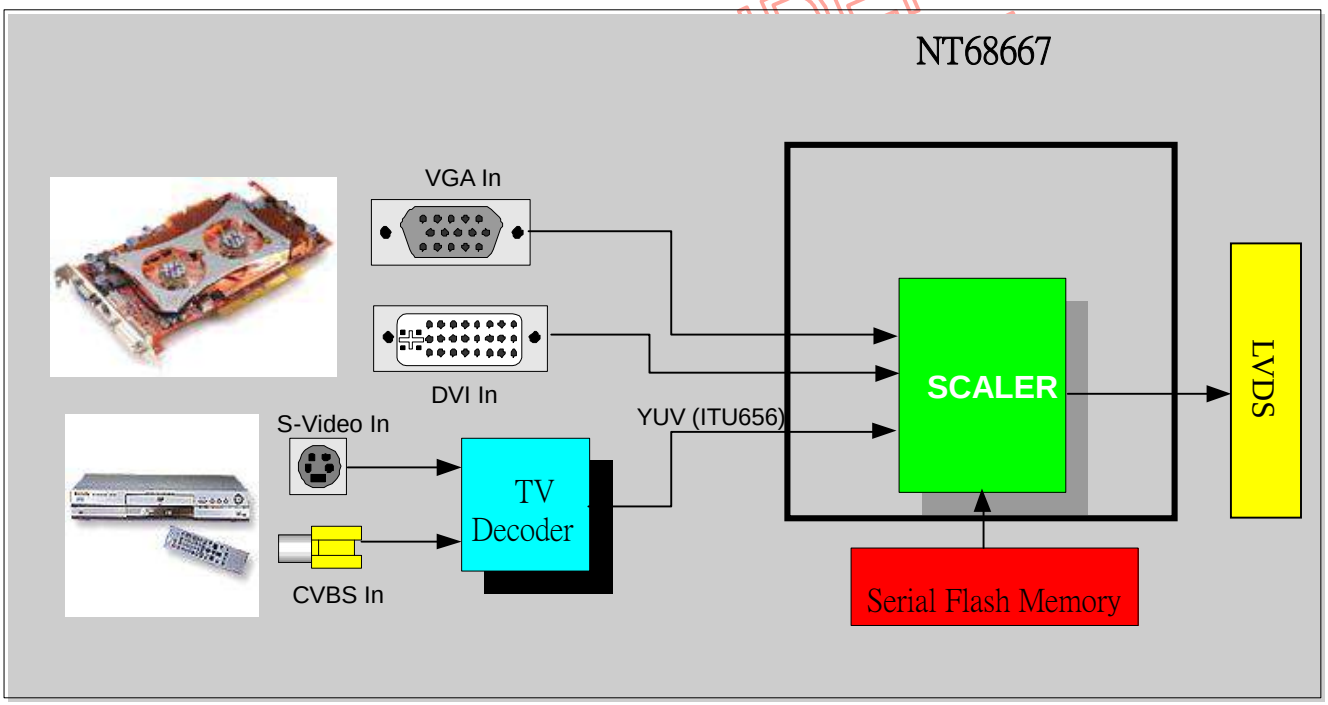

Figure 1 NT68667 System Design Example

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4. Block Diagram

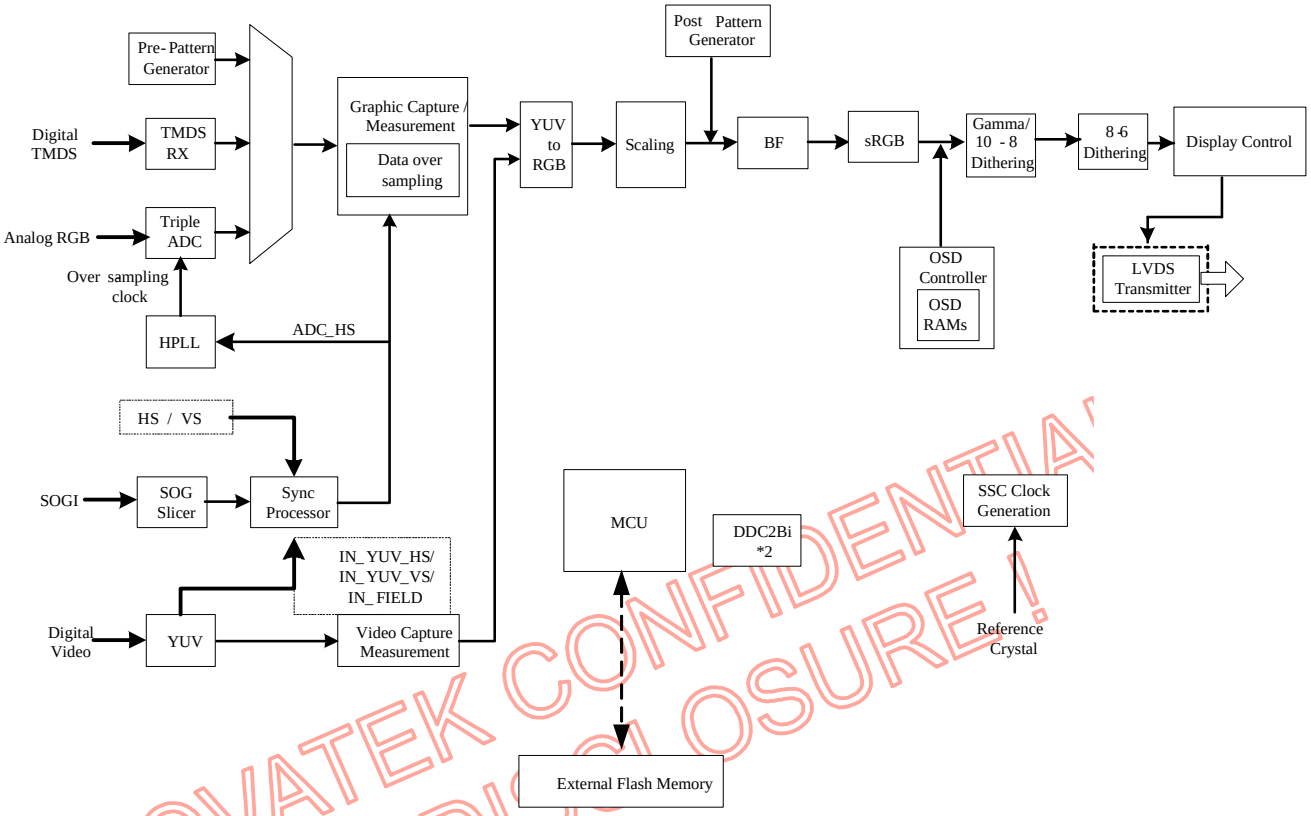

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Figure 4-1 Functional Block Diagram

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5. Pinout Information

5.1. Pin Diagram

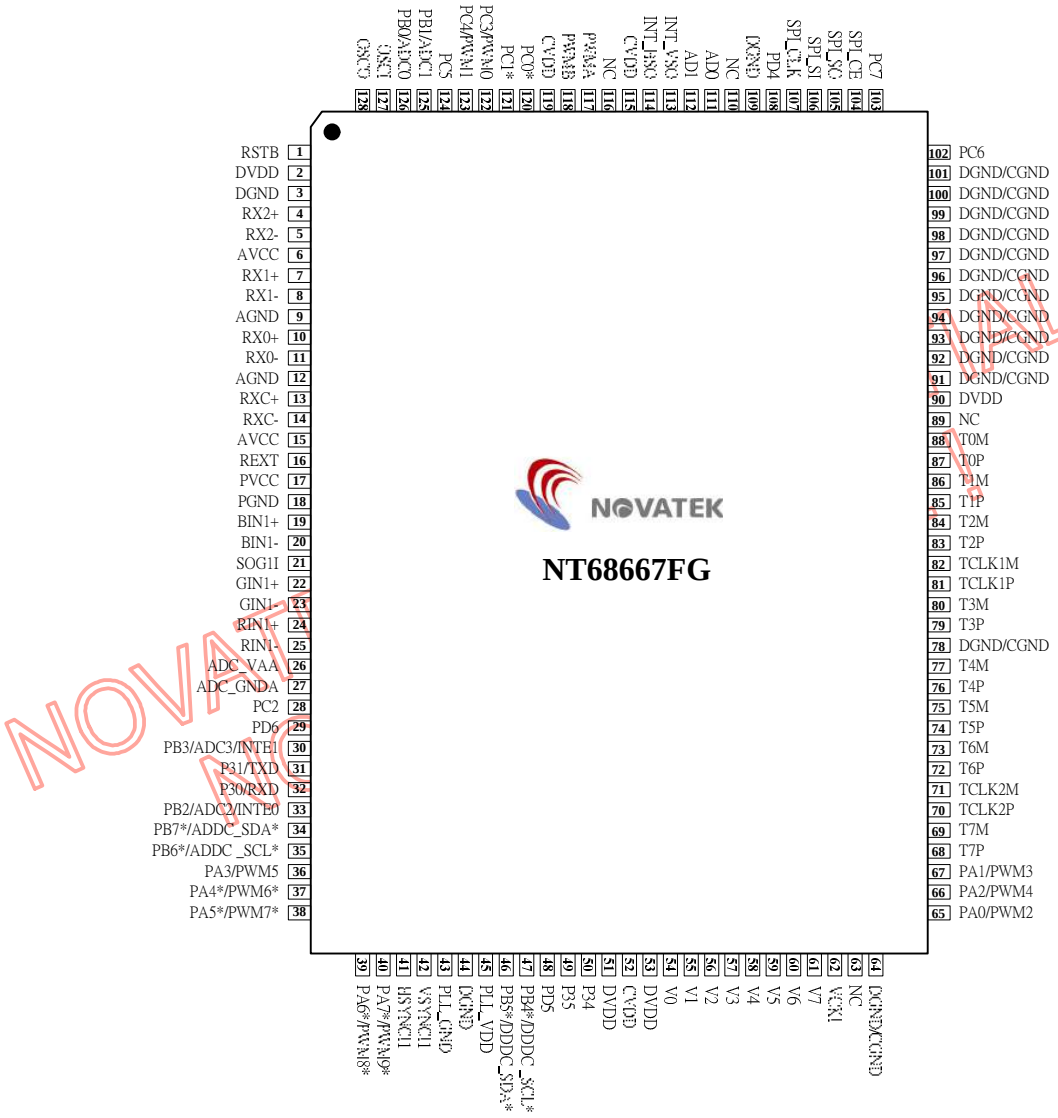

Figure 5.1-1 NT68667 Pin Diagram

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5.2. Pin Assignment

No.	Pin	Type	Operate Voltage	Definition
1	RSTB	I	0 ~ 3.47V	Active-Low Reset Input; with Schmitt Trigger Input
2	DVDD	Power	3.15V ~ 3.47V	Micro-controller +3.3V Power Supply Input
3	DGND	Power	0V	Micro-controller Power Ground
4	RX2+	I	0.15 ~ 1.2V	TMDS input channel 2+
5	RX2-	I	0.15 ~ 1.2V	TMDS input channel 2-
6	AVCC	Power	3.15V ~ 3.47V	TMDS Analog VCC must be set to 3.3V.
7	RX1+	I	0.15 ~ 1.2V	TMDS input channel 1+
8	RX1-	I	0.15 ~ 1.2V	TMDS input channel 1-
9	AGND	Power	0V	TMDS Analog GND.
10	RX0+	I	0.15 ~ 1.2V	TMDS input channel 0+
11	RX0-	I	0.15 ~ 1.2V	TMDS input channel 0-
12	AGND	Power	0V	TMDS Analog GND.
13	RXC+	I	0.15 ~ 1.2V	TMDS input clock pair
14	RXC-	I	0.15 ~ 1.2V	TMDS input clock pair
15	AVCC	Power	3.15V ~ 3.47V	TMDS Analog VCC must be set to 3.3V.
16	REXT	I		External termination resistor. A 1% 470 Ω resistor must be connected from this pin to AVCC. Notes: if this resistor not 1% , the compatibility is worse than 1% resistor .
17	PVCC	Power	3.15V ~ 3.47V	TMDS PLL Analog VCC must be set to 3.3V.
18	PGND	Power	0V	TMDS PLL Analog GND.
19	BIN1+	I		B channel positive analog video input
20	BIN1-	I		B channel negative analog video input
21	SOGI1	I		VGA Port Sync On Green Input with Schmitt trigger
22	GIN1+	I		G channel positive analog video input
23	GIN1-	I		G channel negative analog video input
24	RIN1+	I		R channel positive analog video input
25	RIN1-	I		R channel negative analog video input
26	ADC_VAA	Power	3.15V ~ 3.47V	ADC Analog power supply
27	ADC_GNDA	Power	0V	ADC Analog ground
28	PC2	I/O	0 ~ 3.47V	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
29	PD6	I/O	0 ~ 3.47V	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
30	PB3	I/O	0 ~ 3.47V	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
	ADC3	I	0 ~ 3.47V	A/D Converter Input-3; Hi-Z input
	INTE1	I	0 ~ 3.47V	External Interrupt input 1; Schmitt Trigger Input
31	P31	I/O	0 ~ 3.47V	GPIO Port-31 of Micro-Processor F8031

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	TXD	O	0 ~ 3.47V	UART TX Data Output of Micro-Processor F8031
32	P30	I/O	0 ~ 3.47V	GPIO Port-30 of Micro-Processor F8031
	RXD	I	0 ~ 3.47V	UART RX Data Input of Micro-Processor F8031
33	PB2	I/O	0 ~ 3.47V	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
	ADC2	I	0 ~ 3.47V	A/D Converter Input-2; Hi-Z input
	INTE0	I	0 ~ 3.47V	External Interrupt input 0, Schmitt Trigger Input
34	PB7*	I/O	0 ~ 5.25V	I/O Pin; Open-Drain with Schmitt Trigger Input
	ADDC_SDA*	I/O	0 ~ 5.25V	5V Open-Drain Serial Data I/O Pin for the VGA DDC Port and the slave/master I^2C-Bus Port
35	PB6*	I/O	0 ~ 5.25V	5V I/O Pin; Open-Drain with Schmitt Trigger Input
	ADDC_SCL*	I/O	0 ~ 5.25V	5V Open-Drain Serial Clock I/O Pin for the VGA DDC Port and the slave/master I^2C-Bus Port
36	PA3	I/O	0 ~ 3.47V	I/O Pin; Schmitt Trigger Input
	PWM5	O	0 ~ 3.47V	PWM-Type D/A Converter; 3.3V Push-Pull Structure
37	PA4*	I/O	0 ~ 5.25V	I/O Pin; Open-Drain Structure with Schmitt Trigger Input
	PWM6*	O	0 ~ 5.25V	PWM-Type D/A Converter; 5V Open-Drain Structure
38	PA5*	I/O	0 ~ 5.25V	I/O Pin; Open-Drain Structure with Schmitt Trigger Input
	PWM7*	O	0 ~ 5.25V	PWM-Type D/A Converter; 5V Open-Drain Structure
39	PA6*	I/O	0 ~ 5.25V	I/O Pin; Open-Drain Structure with Schmitt Trigger Input
	PWM8*	O	0 ~ 5.25V	PWM-Type D/A Converter; 5V Open-Drain Structure
40	PA7*	I/O	0 ~ 5.25V	I/O Pin; Open-Drain Structure with Schmitt Trigger Input
	PWM9*	O	0 ~ 5.25V	PWM-Type D/A Converter; 5V Open-Drain Structure
41	HSYNCI	I	0 ~ 5.25V	VGA Port Channel Horizontal Sync Input with Schmitt trigger
42	VSYNCI	O	0 ~ 5.25V	VGA Port Channel Vertical Sync Input with Schmitt trigger
43	PLL_ GND	Power	0V	Core Logic Ground pin for PLL.
44	DGND/CGND	Power	0V	Digital Ground/ Core Logic Ground
45	PLL_ VDD	Power	1.6V ~ 2.0V	Internal HPLL power supply (1.8V) output . External capacitor (0.1uF and 100uF) connected is recommended.
46	PB5*	I/O	0 ~ 5.25V	5V I/O Pin; Open-Drain with Schmitt Trigger Input
	DDDC_SDA*/	I/O	0 ~ 5.25V	5V Open-Drain Serial Data I/O Pin for the DVI DDC Port and the slave/master I^2C-Bus Port
47	PB4*	I/O	0 ~ 5.25V	5V I/O Pin; Open-Drain with Schmitt Trigger Input
	DDDC_SCL*/	I/O	0 ~ 5.25V	5V Open-Drain Serial Clock I/O Pin for the DVI DDC Port and the slave/master I^2C-Bus Port
48	PD5	I/O	0 ~ 3.47V	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
49	P35	I/O	0 ~ 3.47V	GPIO Port-35 of Micro-Processor F8031
	T1	I	0 ~ 3.47V	Counter/Timer T1 Input of Micro-Processor F8031
50	P34	I/O	0 ~ 3.47V	GPIO Port-34 of Micro-Processor F8031
	T0	I	0 ~ 3.47V	Counter/Timer T0 Input of Micro-Processor F8031
51	DVDD	Power	3.15V ~ 3.47V	Display Digital Power Supply
52	CVDD	Power	1.6V ~ 2.0V	Core logic power supply (1.8V) pin. External capacitor (0.1uF) connected is recommended.
53	DVDD	Power	3.15V ~ 3.47V	Display Digital Power Supply

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54	V0	I	0 ~ 3.47V	Video data input
55	V1	I	0 ~ 3.47V	Video data input
56	V2	I	0 ~ 3.47V	Video data input
57	V3	I	0 ~ 3.47V	Video data input
58	V4	I	0 ~ 3.47V	Video data input
59	V5	I	0 ~ 3.47V	Video data input
60	V6	I	0 ~ 3.47V	Video data input
61	V7	I	0 ~ 3.47V	/Video data input
62	YUV_CLK	I	0 ~ 3.47V	Video Port Clock
63	NC			
64	DGND/CGND	Power	0V	Digital Ground/ Core Logic Ground
65	PA0	I/O	0 ~ 3.47V	I/O Pin; Schmitt Trigger Input
	PWM2	O	0 ~ 3.47V	PWM-Type D/A Converter; 3.3V Push-Pull Structure
66	PA2	I/O	0 ~ 3.47V	I/O Pin; Schmitt Trigger Input
	PWM4	O	0 ~ 3.47V	PWM-Type D/A Converter; 3.3V Push-Pull Structure
67	PA1	I/O	0 ~ 3.47V	I/O Pin; Schmitt Trigger Input
	PWM3	O	0 ~ 3.47V	PWM-Type D/A Converter; 3.3V Push-Pull Structure
68	T7P	LVDSO	1.2 ± 0.10V ~ 1.2 ± 0.22V	Positive LVDS differential data output of channel 7
69	T7M	LVDSO	1.2 ± 0.10V ~ 1.2 ± 0.22V	Negative LVDS differential data output of channel 7
70	TCLK2P	LVDSO	1.2 ± 0.10V ~ 1.2 ± 0.22V	Positive LVDS differential clock 2 output
71	TCLK2M	LVDSO	1.2 ± 0.10V ~ 1.2 ± 0.22V	Negative LVDS differential clock 2 output
72	T6P	LVDSO	1.2 ± 0.10V ~ 1.2 ± 0.22V	Positive LVDS differential data output of channel 6
73	T6M	LVDSO	1.2 ± 0.10V ~ 1.2 ± 0.22V	Negative LVDS differential data output of channel 6
74	T5P	LVDSO	1.2 ± 0.10V ~ 1.2 ± 0.22V	Positive LVDS differential data output of channel 5
75	T5M	LVDSO	1.2 ± 0.10V ~ 1.2 ± 0.22V	Negative LVDS differential data output of channel 5
76	T4P	LVDSO	1.2 ± 0.10V ~ 1.2 ± 0.22V	Positive LVDS differential data output of channel 4
77	T4M	LVDSO	1.2 ± 0.10V ~ 1.2 ± 0.22V	Negative LVDS differential data output of channel 4
78	DGND/CGND	Power	0V	Digital Ground/ Core Logic Ground

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79	T3P	LVDSO	1.2 ± 0.10V ~ 1.2 ± 0.22V	Positive LVDS differential data output of channel 3
80	T3M	LVDSO	1.2 ± 0.10V ~ 1.2 ± 0.22V	Negative LVDS differential data output of channel 3
81	TCLK1P	LVDSO	1.2 ± 0.10V ~ 1.2 ± 0.22V	Positive LVDS differential clock 1 output
82	CLK1M	LVDSO	1.2 ± 0.10V ~ 1.2 ± 0.22V	Negative LVDS differential clock 1 output
83	T2P	LVDSO	1.2 ± 0.10V ~ 1.2 ± 0.22V	Positive LVDS differential data output of channel 2
84	T2M	LVDSO	1.2 ± 0.10V ~ 1.2 ± 0.22V	Negative LVDS differential data output of channel 2
85	T1P	LVDSO	1.2 ± 0.10V ~ 1.2 ± 0.22V	Positive LVDS differential data output of channel 1
86	T1M	LVDSO	1.2 ± 0.10V ~ 1.2 ± 0.22V	Negative LVDS differential data output of channel 1
87	T0P	LVDSO	1.2 ± 0.10V ~ 1.2 ± 0.22V	Positive LVDS differential data output of channel 0
88	T0M	LVDSO	1.2 ± 0.10V ~ 1.2 ± 0.22V	Negative LVDS differential data output of channel 0
89	NC			
90	DVDD	Power	3.15V ~ 3.47V	Display Digital Power Supply
91	DGND/CGND	Power	0V	Digital Ground/ Core Logic Ground
92	DGND/CGND	Power	0V	Digital Ground/ Core Logic Ground
93	DGND/CGND	Power	0V	Digital Ground/ Core Logic Ground
94	DGND/CGND	Power	0V	Digital Ground/ Core Logic Ground
95	DGND/CGND	Power	0V	Digital Ground/ Core Logic Ground
96	DGND/CGND	Power	0V	Digital Ground/ Core Logic Ground
97	DGND/CGND	Power	0V	Digital Ground/ Core Logic Ground
98	DGND/CGND	Power	0V	Digital Ground/ Core Logic Ground
99	DGND/CGND	Power	0V	Digital Ground/ Core Logic Ground
100	DGND/CGND	Power	0V	Digital Ground/ Core Logic Ground
101	DGND/CGND	Power	0V	Digital Ground/ Core Logic Ground
102	PC6	I/O	0~ 3.47V	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
103	PC7	I/O	0~ 3.47V	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
104	SPI_CE	O	0~ 3.47V	External flash SPI chip enable
105	SPI_SO	I	0~ 3.47V	External flash SPI chip serial data output
106	SPI_SI	O	0~ 3.47V	External flash SPI data serial data input

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107	SPI_CLK	O	0~ 3.47V	External flash SPI clock
108	PD4	I/O	0~ 3.47V	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
109	DGND	Power	0V	Digital Ground
110	NC			
111	AD0	I/O	0~ 3.47V	Slave address d0
112	AD1	I/O	0~ 3.47V	Slave address d1
113	INT_VSO	O	0~ 3.47V	Internal Vertical Sync output, this signal is by-pass the Sync-processor
114	INT_HSO	O	0~ 3.47V	Internal Horizontal Sync output, this signal is by-pass the Sync-processor
115	CVDD	Power	1.6V ~ 2.0V	Core logic power supply (1.8V) pin. External capacitor (0.1uF) connected is recommended.
116	NC			
117	PWMA*	O	0~ 3.47V	PWM type output Open-Drain Structure
118	PWMB*	O	0~ 5.25V	PWM type output Open-Drain Structure
119	CVDD	Power	1.6V ~ 2.0V	Core logic power supply (1.8V) pin. External capacitor (0.1uF) connected is recommended.
120	PC0*	I/O	0~ 5.25V	I/O Pin; 5V Open-Drain Structure with Schmitt Trigger Input
121	PC1*	I/O	0~ 5.25V	I/O Pin; 5V Open-Drain Structure with Schmitt Trigger Input
122	PC3	I/O	0~ 3.47V	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
	PWM0	O	0~ 3.47V	PWM-Type D/A Converter; Push-Pull Structure
123	PC4	I/O	0~ 3.47V	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
	PWM1	O	0~ 3.47V	PWM-Type D/A Converter; Push-Pull Structure
124	PC5	I/O	0~ 3.47V	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
125	PB1/ADC1	I/O	0~ 3.47V	I/O Pin; Push-Pull Structure with Schmitt Trigger Input A/D Converter Input-1; Hi-Z input
126	PB0/ADC0	I/O	0~ 3.47V	I/O Pin; Push-Pull Structure with Schmitt Trigger Input A/D Converter Input-0; Hi-Z input
127	OSCI	I		12~15MHz External Crystal OSC Output
128	OSCO	O		12~15MHz External Crystal OSC Input

Table 5.2-1 Pin List

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5.3.Pin Description

System Interface

Pin	Type	Definition
RSTB	I	System Reset

Graphic Analog Interface

Pin	Type	Definition
ADC_GNDA	Power	ADC analog ground
ADC_VAA	Power	ADC analog power supply
BIN1+	I	B channel positive analog video input
BIN1-	I	B channel negative analog video input
SOGI1	I	VGA Port 1 Sync On Green Input with Schmitt trigger
GIN1+	I	G channel positive analog video input
GIN1-	I	G channel negative analog video input
RIN1+	I	R channel positive analog video input
RIN1-	I	R channel negative analog video input
HSYNCI	I	VGA Port Horizontal Sync Input with Schmitt trigger
VSYNCI	I	VGA Port Vertical Sync Input with Schmitt trigger

Graphic TMDS Interface

Pin	Type	Definition
RX2+	I	TMDS input channel 2+
RX2-	I	TMDS input channel 2-
RX1+	I	TMDS input channel 1+
RX1-	I	TMDS input channel 1-
RX0+	I	TMDS input channel 0+
RX0-	I	TMDS input channel 0-
RXC+	I	TMDS input clock pair
RXC-	I	TMDS input clock pair
REXT	I	External termination resistor
AVCC	Power	TMDS Analog VCC must be set to 3.3V.
AGND	Power	TMDS Analog GND.
PVCC	Power	TMDS PLL Analog VCC must be set to 3.3V.
PGND	Power	TMDS PLL Analog GND.

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LVDS Panel Interface

Pin	Type	Definition
T0M	LVDSO	Negative LVDS differential data output of channel 0
T0P	LVDSO	Positive LVDS differential data output of channel 0
T1M	LVDSO	Negative LVDS differential data output of channel 1
T1P	LVDSO	Positive LVDS differential data output of channel 1
T2M	LVDSO	Negative LVDS differential data output of channel 2
T2P	LVDSO	Positive LVDS differential data output of channel 2
TCLK1M	LVDSO	Negative LVDS differential clock 1 output
TCLK1P	LVDSO	Positive LVDS differential clock 1 output
T3M	LVDSO	Negative LVDS differential data output of channel 3
T3P	LVDSO	Positive LVDS differential data output of channel 3
T4M	LVDSO	Negative LVDS differential data output of channel 4
T4P	LVDSO	Positive LVDS differential data output of channel 4
T5M	LVDSO	Negative LVDS differential data output of channel 5
T5P	LVDSO	Positive LVDS differential data output of channel 5
T6M	LVDSO	Negative LVDS differential data output of channel 6
T6P	LVDSO	Positive LVDS differential data output of channel 6
TCLK2M	LVDSO	Negative LVDS differential clock 2 output
TCLK2P	LVDSO	Positive LVDS differential clock 2 output
T7M	LVDSO	Negative LVDS differential data output of channel 7
T7P	LVDSO	Positive LVDS differential data output of channel 7

Video ITU-R BT656 Interface

Pin	Type	Definition
V0~V7	O	Video Port Data[7:0] input
VCLK	O	Video Port Clock

Power Pin

Pin	Type	Definition
CVDD	Power	Core logic power supply (1.8V) pin. External capacitor (0.1uF) connected is recommended.
CGND /DVDD	Power	Core Logic Ground /Display Digital Power Supply
PLL_VDD	Power	Core logic power supply (1.8V) pin for PLL. External capacitor (0.1uF) connected is recommended.
PLL_GND	Power	Core Logic Ground pin for PLL.
AVCC	Power	TMDS Analog VCC must be set to 3.3V.
AGND	Power	TMDS Analog GND.
PVCC	Power	TMDS PLL Analog VCC must be set to 3.3V.
PGND	Power	TMDS PLL Analog GND.
ADC_VAA	Power	ADC analog power supply
ADC_GNDA	Power	ADC analog ground

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6. Functional Description

6.1. Power Control

NT68667 supports the whole chip power down function except MCU logic and Sync-processor (include SOG Slicer, and TMDS Sync Detect) when h/w reset .

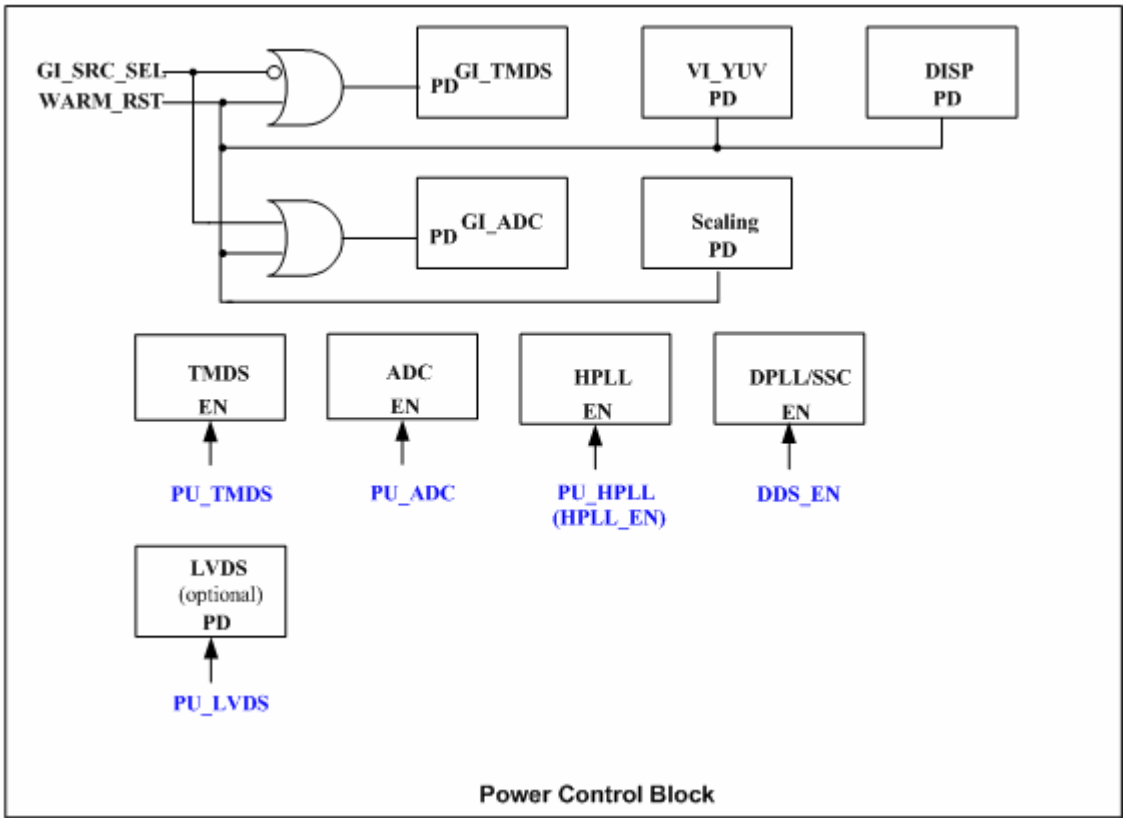

Figure 6.1-1 Power Control Block

6.2. Analog to Digital Converter (ADC)

NT68667 provides a clock-recovery circuit and an analog-to-digital converter to effectively save the cost of needing external expensive ADC and PLL. The gain and offset circuit is used to adjust the gain (Contrast) of input video amplitude and shift the DC offset voltage (Brightness). The clock-recovery circuit consisting of a high-speed phase lock loop (PLL) is used to generate the clock to sample analog RGB data. This circuit is locked to the HSYNC of the incoming video signal. The analog-to-digital converter (ADC) transfers the input analog RGB video to digital output data with each color 8-bit resolution.

Gain and Offset Control

RIN/GIN/BIN are high-impedance input pins that accept the RED, GREEN, and BLUE channel graphics signals. They accommodate input signals ranging from 0.55V to 0.9V full scale. Signals should be AC-couple to these pins.

Due to AC coupling, clamping pulse is needed to define the time during which the input signal is clamped to ground, establishing a black reference. Typically the clamping pulse is defined during the back porch period of the graphics signal. NT68667 generates the clamping pulse internally and the position and duration are programmable. The simpler clamp-timing generator clamping pulse-starting position and pulse width is defined in 0x021[7:0] and 0x022[7:0].

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NT68667 has three independent variable gain amplifiers for each channel with input signal range from 0.55V to 0.9V（p-p）, the full-scale range is set in three 9-bit registers.
NT68667 offset control shifts the entire input range, resulting in a change in image brightness. The three independent variable 8-bit registers provide independent settings for each channel.

Clamp Pulse generator
This block circuit called Clamp pulse generator generates clamp pulse to ADC. There are two input trigger sources of the clamp generator, one is signal Hin from separator and another is Row Hs from the HSYNCI0 / HSYNCI1. The polarity and the trigger edge of the clamp can be selected by using bit CLMP_POL and bit CLMP_EDG respectively. The trigger delay of the clamp is waiting CLMP_BEG [5:0] x REFCLK time. The pulse width of the clamp output may be selected by CLMP_WID [5:0].

➢ Clamp Pulse Timing

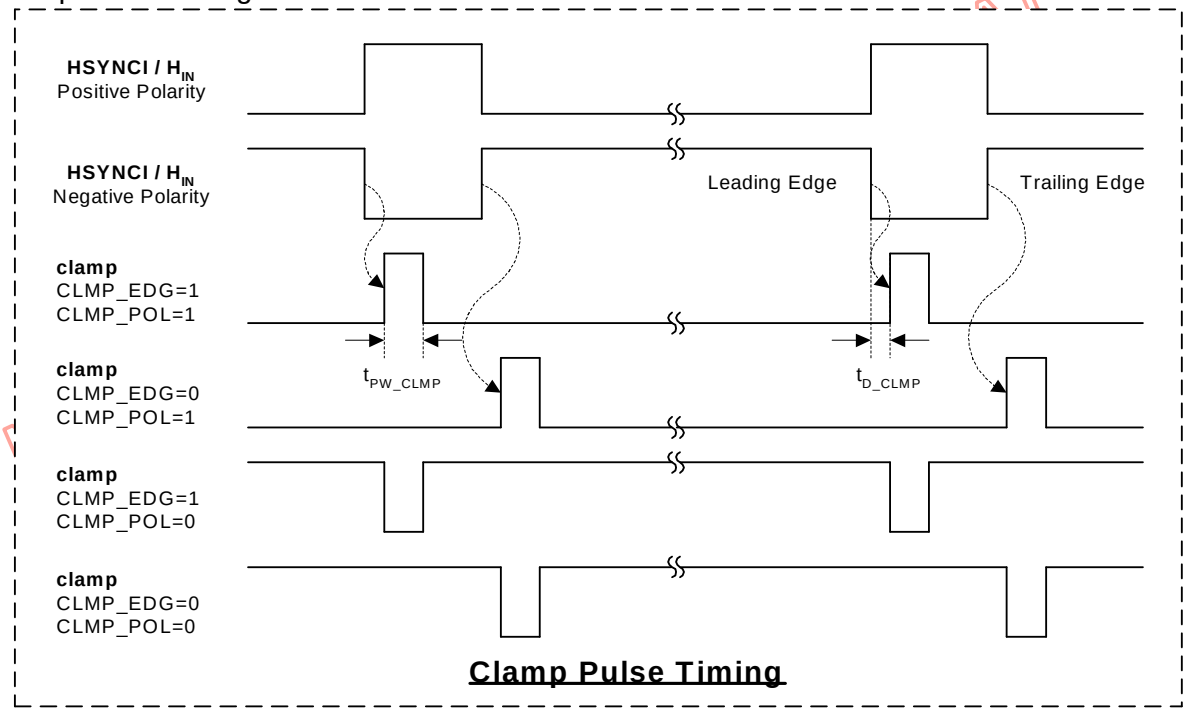

Figure 6.2-1 Clamp Pulse Timing

COAST
This function is used to cause the pixel clock generator to stop synchronizing with Hsync and continues producing a clock at its current frequency and phase. This is useful when processing composite sync that fails to produce horizontal sync pulses when in the vertical interval.

6.3. DVI Receiver

The DVI receiver uses Panel Link Digital technology to support input ranging from VGA to UXGA (25-165 MHz), which is ideal for desktop and specialty applications.

6.4. Graphic Port Capture Interface

The function of Graphic Port Capture Interface is to provide two interfaces between NT68667 and external input devices. It can process non-interlaced and interlaced RGB graphic input, and DVI input. User should select the video input source from Graphic Port (VGA or DVI) and the polarity of external control signal, and then program the H/V captures size registers to indicate the display area.

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6.5. Video Port Capture Interface

The function of Video Port Capture Interface is to provide Digital YUV interface between NT68667 and video decoder. It can process non-interlaced and interlaced digital YUV video ITU BT656 input. It includes color space conversion for YUV to RGB color space conversion.

6.6. Auto Tune

The Auto Tune function consists of Auto Gain, Auto Position, and Auto Phase. With such auto adjustment support it is possible to measure the correct phase, frequency, gain, and offset of ADC. The horizontal and vertical back porches of input image and the horizontal and vertical active regions can also be measured.

6.7. Video Processor

Video processor consists of Interpolation Control, RGB Gain Control, RGB Offset Control, Hue and Saturation Control, Dithering Control, Gamma Correction Control and sRGB Support.
NT68667 enhanced interpolation method makes the zoomed display image look more smooth and comfortable.
User can adjust the RGB Gain (Contrast) and RGB Offset (Brightness) by the registers in the ADCPLL block, or registers in the Video processor block. But for YUV video input, it is suitable to adjust Contrast and Brightness at here. In addition, it supports all YUV color controls including brightness, contrast, hue and saturation.
Dithering function can provide 16.7 million colors space for 6-bit/color panel. It is recommended to open the dithering function while a 6-bit panel is used.
NT68667 provide independently horizontal and vertical zoom scaler with adjustable zoom factor from 1/4x to 4x. Each of the zoom scaler uses variable sharpness filter to provide high quality scaling of real-time video and still graphic images.

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Interpolation
1. Flexible Sharpness Filter
NT68667 include flexible sharpness filter for horizontal and vertical sharpness adjusting. Users can use them by register programming.
2. Vertical Spatial Interpolation
When interlaced video or images are applied, the NT68667 vertical scaling engines will de-interlace the input fields spatially and reposition them to align the display's line map.
3. Advanced Filter
With the aid of two selectable advanced filters when zooming up horizontally, NT68667 provides the most undistorted image from the original one.

sRGB Support
sRGB is a standard for color exchange proposed by Microsoft and HP. The sRGB controls can be used to make LCD monitors sRGB compliant.

$$\begin{bmatrix} R'_{sRGB} \\ G'_{sRGB} \\ B'_{sRGB} \end{bmatrix} = \begin{bmatrix} A0 & B0 & C0 \\ A1 & B1 & C1 \\ A2 & B2 & C2 \end{bmatrix} \begin{bmatrix} R_{sRGB} \\ G_{sRGB} \\ B_{sRGB} \end{bmatrix} + \begin{bmatrix} Offset_R \\ Offset_G \\ Offset_B \end{bmatrix} \quad \text{----------[1]}$$

Gamma Correction
- Provides 10-bit gamma correction function
- F/W needs to define total 256 end-point value in advance

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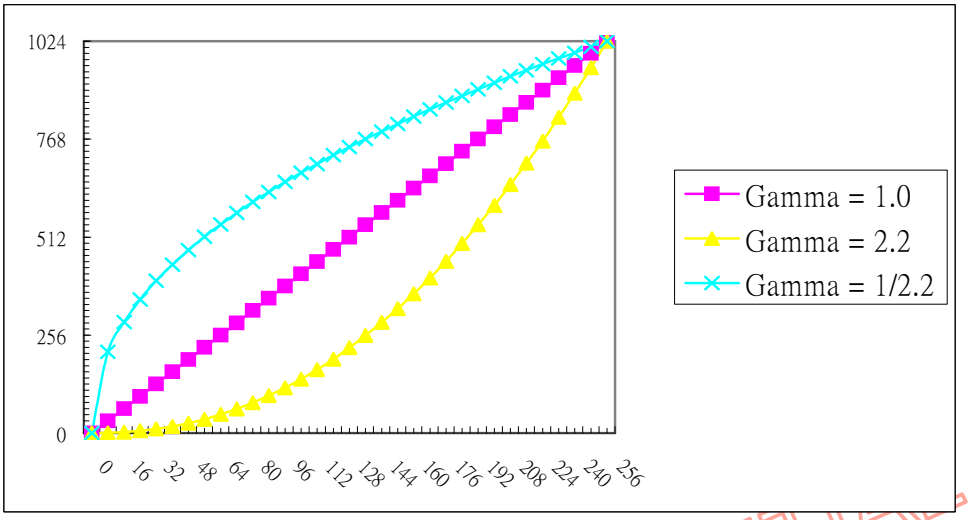

Figure 6.7-1 Gamma Correction Curve

Index Address	Gamma Table	Value
0		LSB0 (2 bits)+MSB0 (8 bits)
1		LSB1+MSB1
2		LSB2+MSB2
….	….	
254		LSB254+MSB254
255		LSB255+MSB255

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6.8. Sync Processor

The NT68667 has a Sync Processor block providing the capability of measuring the horizontal and vertical timing parameters of the input video source. This information may be used to determine the video format and to detect a change in the input timing. It is also capable of detecting the field type of interlaced formats.

Hsync /Vsync Frequency and Polarity Detection

GI_HCNT, the 13 bits Hsync period counter counts the time of 32xHSYNC period, then loads the result into the GI_HCNT latch. The output value will be [((REFCLK / 4 x 32)/Hfreq)], updated once per VSYNC/CVSYNC period when VSYNC/CVSYNC is present or continuously updated when VSYNC/CVSYNC is non-present.

GI_VCNT, the 13 bits Vsync period counter counts the time between two VSYNC pulses, then loads the result into the GI_VCNT latch. The output value will be [(REFCLK/(256 x Vfreq))], updated every VSYNC/CVSYNC period. An extra overflow bit indicates the condition of H/V counter overflow.

The polarity functions detect the input HSYNC/VSYNC high and low pulse duty cycle. If the high pulse duration is longer than that of the low pulse, the negative polarity is asserted; otherwise, positive polarity is asserted. The INT_HPOL interrupt is set when the GI_HPOL value changes. The INT_VPOL interrupt is set when the GI_VPOL value changes.

H/V Present Check

The Hsync present function checks the input HSYNCI pulse, GI_HPRE flag is set when HSYNCI is over HSYNC Present High Counter Threshold (HPRE_THR_HI) or cleared when HSYNC is under HSYNC Present Low Counter Threshold (HPRE_THR_LO). The Vsync present function checks the input VSYNCI pulse, the GI_VPRE flag is set when VSYNCI is over VSYNC Present High Counter Threshold (VPRE_THR_HI) or cleared when VSYNC is under VSYNC Present Low Counter Threshold (VPRE_THR_LO). The INT_HPRE interrupt is set when the GI_HPRE value changes. The INT_VPRE interrupt is set when the GI_VPRE /GI_CSPRE value change.

Timing Change Detection

The INT_VFREQ/INT_HFREQ interrupt is set when GI_VCNT / GI_HCNT value changes or overflows.

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Extract Vsync from Composite/SOG Signal

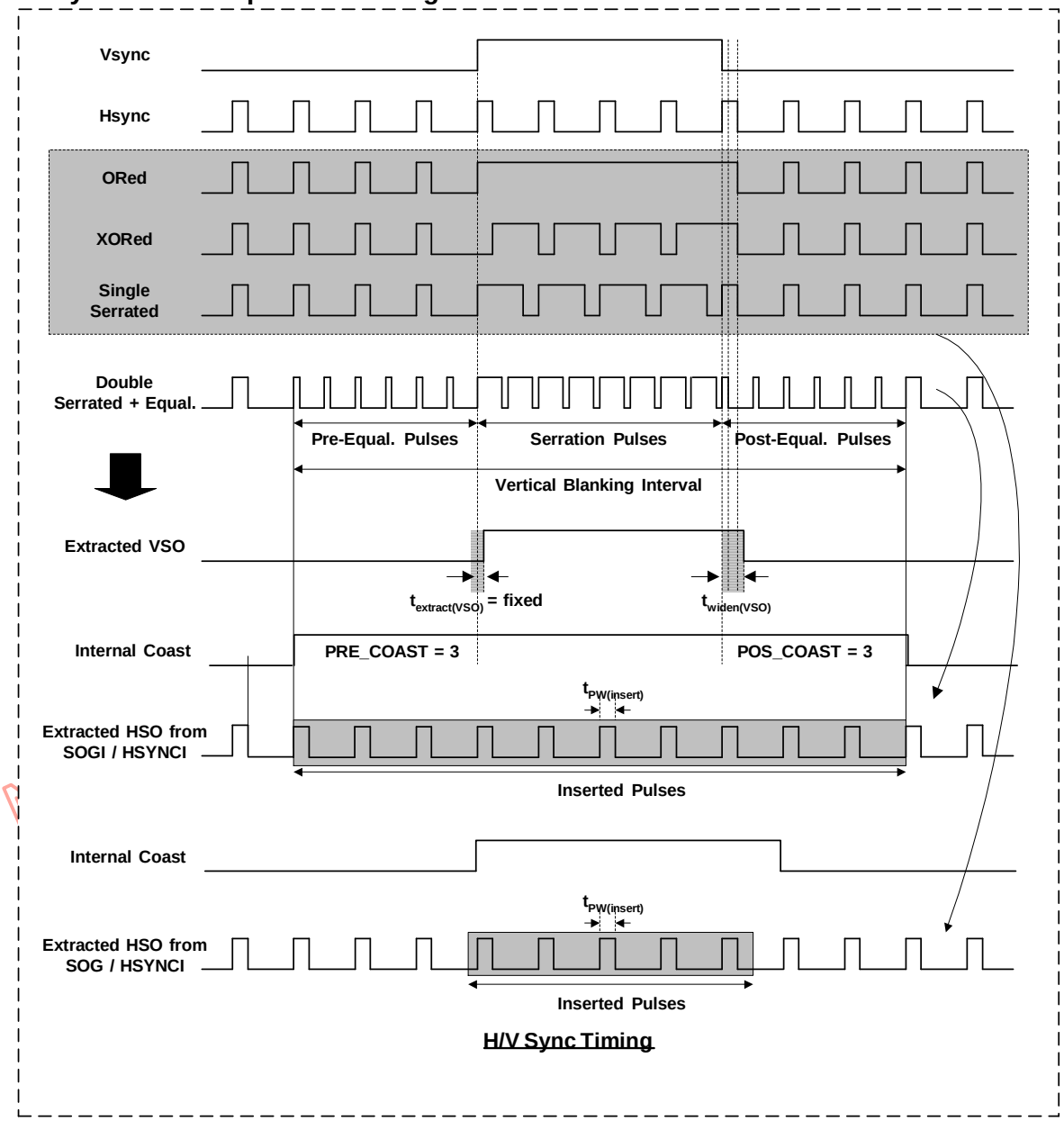

Figure 6.8-1 H/V Timing

Internal Odd/Even Field Detection

Included in the sync detector is circuitry to determine which field is currently being input for interlaced input. To determine the field based on position of VSYNC relative to HSYNC, the GI_FLD_WINBEG (3:0) and GI_FLD_WINEND (3:0) registers are used for Graphic Port and the VI_FLD_WINBEG (3:0) and VI_FLD_WINEND (3:0) registers are used for Video Port. The NT68667 divides each horizontal line into 16 equal intervals. The FLD_WINBEG bits are used to specify at which 1/16th of a line to start looking for the leading edge of VSYNC. The FLD_WINEND bits are used to specify at which 1/16th of a line to stop looking. If the leading edge of VSYNC occurs between during or after the 1/16th line specified by FLD_WINBEG, but no later than the 1/16th line specified by FLD_WINEND, the current field is marked as odd. Otherwise, a leading edge transition outside these boundaries will cause the current field to be marked even.

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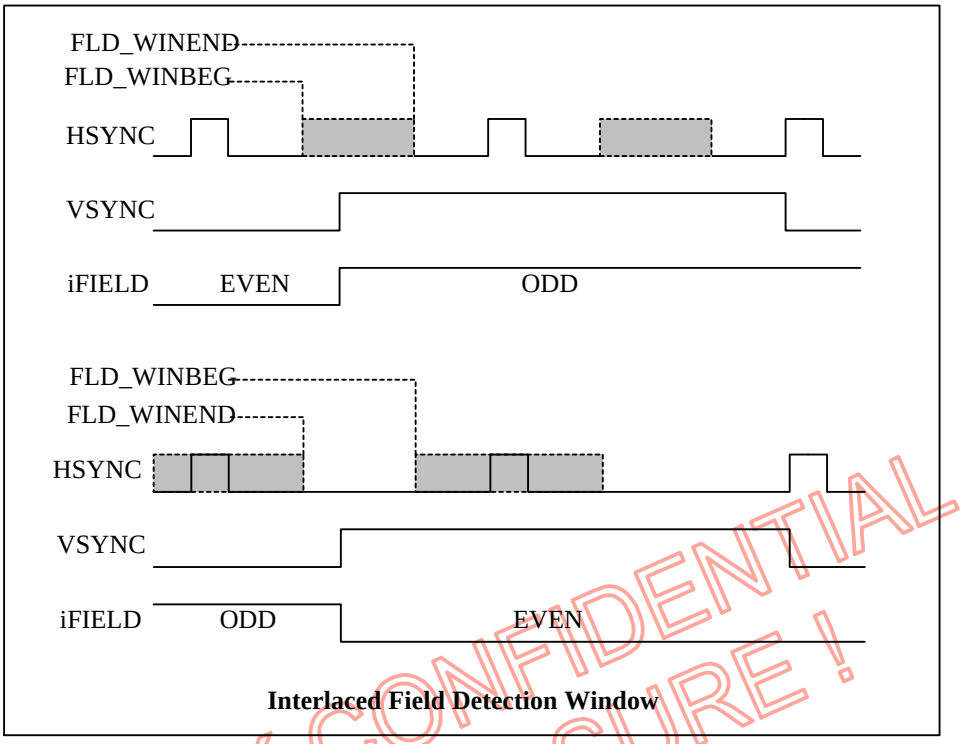

Figure 6.8-2 Interlaced Field Detection Window

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Free Run Timing Generator

This Block can generate various free-running outputs to satisfy various application requirements. The pulse width of the H_{FREE} output is fixed 15 x REFCLK and the V_{FREE} is 3 HFREEs. User can properly set the content of HSO Free Run divider, HFREE_DIV, to get the need frequency of the HSO, and set the content VSO Free Run divider, VFREE_DIV, to get the frequency of the VSO. Details refer to the descriptions of the free-run registers HFREE_DIV and VFREE_DIV. Refer to the descriptions of the register for details to get user's need frequencies.
Users can disable H/V free run output by clearing GI_HRUN_EN /GI_VRUN_EN.

Sync On Green Slicer

This function is provided to assist with processing signals with embedded sync, typically on the GIN channel. The circuit sliced the signals that with embedded sync, and apply to Sync Separator for extracting Hsync and Vsync.

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6.9. OSD Function

OSD Font's Attribute and Code Format, Palette Format Definition:

OSD Palette Format

15:11	10:5	4:0
R	G	B

OSD Code Format

7:0
Font Index

OSD Attribute Format

15:8	7:4	3:2	1	0
PA_Index [7:0]	BG_Index [3:0]	CA_Bit	Mix	Blink

Figure 6.9-1

- Blink : 0 – No blinking
  1 – Blinking (All color is blinking except background color)
- Mix : 0 – Normal
  1 – Translucent ((1- TP_LEVEL_ONE) Display + (TP_LEVEL_ONE) OSD_BG)
- CA_Bit [1:0] : Character attribute bits/pixel number
  00: one bit/pixel color Font (0-255 font index)
  01: one bit/pixel color Font (256-511 font index)
  10: two bits/pixel color Font
  11: three/four bits/pixel color Font
- PA_Index [7:0] / BG_Index [3:0]: Attribute color palette index

Case A: Pixel is outside an active window
One Bit per pixel.
Foreground '1' Pixel [7:0] <= PA_Index [7:0] + 1
Background '0' Pixel [7:0] <= BG_Index [3:0]

Two Bit per pixel.
Foreground '11' Pixel [7:0] <= PA_Index [7:0] + '11'
Foreground '10' Pixel [7:0] <= PA_Index [7:0] + '10'
Foreground '01' Pixel [7:0] <= PA_Index [7:0] + '01'
Background '00' Pixel [7:0] <= BG_Index [3:0]

Four Bit per pixel.
Foreground '1111' Pixel [7:0] <= PA_Index [7:0] + '1111'
Foreground '1110' Pixel [7:0] <= PA_Index [7:0] + '1110'
Foreground '1101' Pixel [7:0] <= PA_Index [7:0] + '1101'
Foreground '1100' Pixel [7:0] <= PA_Index [7:0] + '1100'
Foreground '1011' Pixel [7:0] <= PA_Index [7:0] + '1011'
Foreground '1010' Pixel [7:0] <= PA_Index [7:0] + '1010'
Foreground '1001' Pixel [7:0] <= PA_Index [7:0] + '1001'
Foreground '1000' Pixel [7:0] <= PA_Index [7:0] + '1000'
Foreground '0111' Pixel [7:0] <= PA_Index [7:0] + '0111'

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Foreground ‘0110’ Pixel [7:0] <= PA_Index [7:0] + ‘0110’
Foreground ‘0101’ Pixel [7:0] <= PA_Index [7:0] + ‘0101’
Foreground ‘0100’ Pixel [7:0] <= PA_Index [7:0] + ‘0100’
Foreground ‘0011’ Pixel [7:0] <= PA_Index [7:0] + ‘0011’
Foreground ‘0010’ Pixel [7:0] <= PA_Index [7:0] + ‘0010’
Foreground ‘0001’ Pixel [7:0] <= PA_Index [7:0] + ‘0001’

Note: If BG_Index [3:0] = ”0000”, indicates that this background color is transparent
If BG_Index [3:0] = “0001”, Background <= PA_Index [7:0]

Case B: Pixel is inside an active window

One Bit per pixel.
Foreground ‘1’ Pixel [7:0] <= PA_Index [7:0] + ‘1’
Background ‘0’ Pixel [7:0] <= WINx_ATTR [7:0]

Two Bit per pixel.
Foreground ‘11’ Pixel [7:0] <= PA_Index [7:0] + ‘11’
Foreground ‘10’ Pixel [7:0] <= PA_Index [7:0] + ‘10’
Foreground ‘01’ Pixel [7:0] <= PA_Index [7:0] + ‘01’
Background ‘00’ Pixel [7:0] <= WINx_ATTR [7:0]

Four Bit per pixel.
Foreground ‘1111’ Pixel [7:0] <= PA_Index [7:0] + ‘1111’
Foreground ‘1110’ Pixel [7:0] <= PA_Index [7:0] + ‘1110’
Foreground ‘1101’ Pixel [7:0] <= PA_Index [7:0] + ‘1101’
Foreground ‘1100’ Pixel [7:0] <= PA_Index [7:0] + ‘1100’
Foreground ‘1011’ Pixel [7:0] <= PA_Index [7:0] + ‘1011’
Foreground ‘1010’ Pixel [7:0] <= PA_Index [7:0] + ‘1010’
Foreground ‘1001’ Pixel [7:0] <= PA_Index [7:0] + ‘1001’
Foreground ‘1000’ Pixel [7:0] <= PA_Index [7:0] + ‘1000’
Foreground ‘0111’ Pixel [7:0] <= PA_Index [7:0] + ‘0111’
Foreground ‘0110’ Pixel [7:0] <= PA_Index [7:0] + ‘0110’
Foreground ‘0101’ Pixel [7:0] <= PA_Index [7:0] + ‘0101’
Foreground ‘0100’ Pixel [7:0] <= PA_Index [7:0] + ‘0100’
Foreground ‘0011’ Pixel [7:0] <= PA_Index [7:0] + ‘0011’
Foreground ‘0010’ Pixel [7:0] <= PA_Index [7:0] + ‘0010’
Foreground ‘0001’ Pixel [7:0] <= PA_Index [7:0] + ‘0001’
Background ‘0000’ Pixel [7:0] <= WINx_ATTR [7:0]

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Palette Address and map

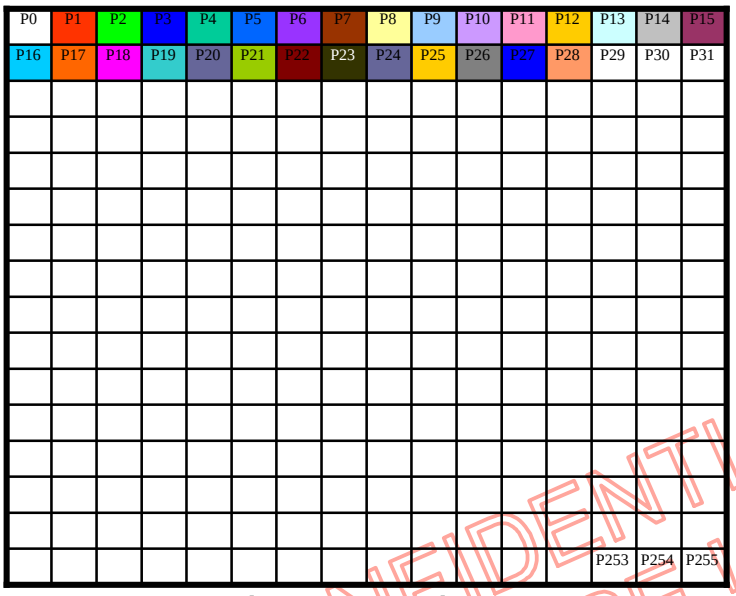

Figure 6.9-2 Palette

Palette N	Palette Address	Bits [15:11]	Bits [10:5]	Bits [4:0]
Palette 0	0 (0x00H)	R0 [4:0]	G0 [5:0]	B0 [4:0]
Palette 1	1 (0x01H)	R1 [4:0]	G1 [5:0]	B1 [4:0]
Palette 2	2 (0x02H)	R2 [4:0]	G2 [5:0]	B2 [4:0]
…	…			
Palette 15	15 (0x0FH)	R15 [4:0]	G15 [5:0]	B15 [4:0]
Palette 16	16 (0x04H)	R16 [4:0]	G16 [5:0]	B16 [4:0]
Palette 17	17 (0x05H)	R17 [4:0]	G17 [5:0]	B17 [4:0]
…	…			
Palette 254	254 (0xFEH)	R254 [4:0]	G254 [5:0]	B254 [4:0]
Palette 255	255 (0xFFH)	R255 [4:0]	G255 [5:0]	B255 [4:0]

Figure 6.9-3 Palette address and map

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OSD Character Map

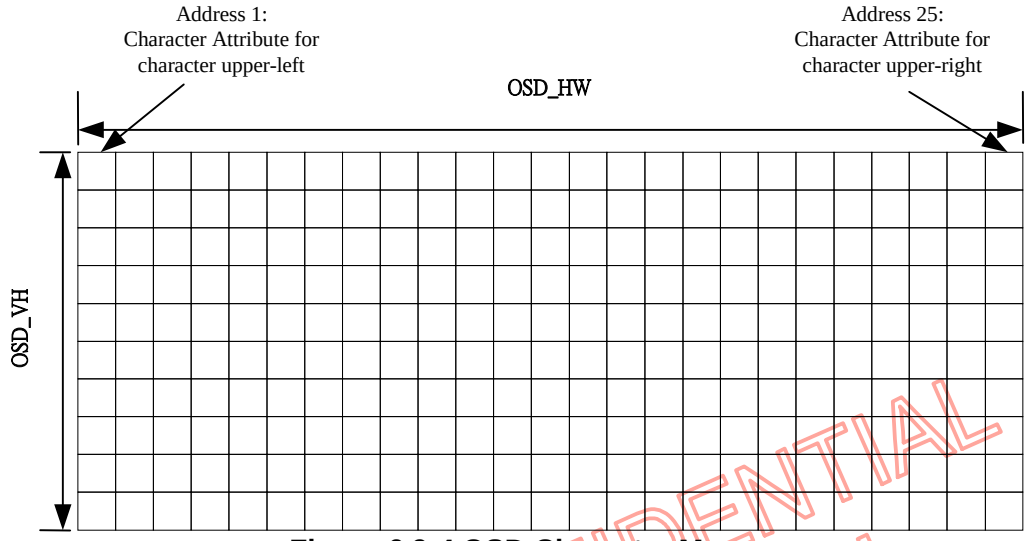

Figure 6.9-4 OSD Character Map

OSD Font Definitions
One Bit per pixel

One bit per pixel font definitions are arranged in Color Character Font SRAM Memory on a 12-bit by 18-address grid. The One bit per pixel OSD programmable font start address is specified in Register 0x089 ~ 0x088. Odd font definitions are stored in SRAM bits [11:0], and even font definitions are stored in SRAM bits [23:12].

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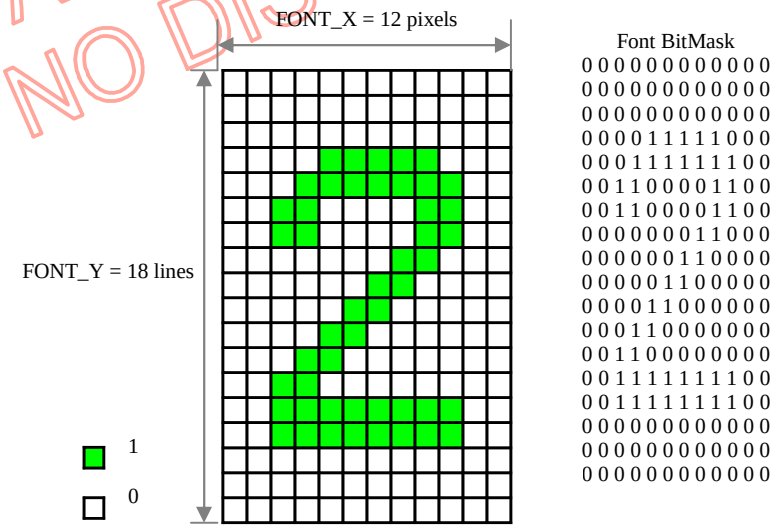

Figure 6.9-5 One Bit Per Pixel Font

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Two Bit per pixel

Two bits per pixel font definitions are arranged in Color Character Font SRAM Memory on a 24-bit by 18 addresses. The two bit per pixel OSD programmable font start address is specified in Register 0x08B ~ 0x08A. Font definitions are stored in SRAM bits [23:0].

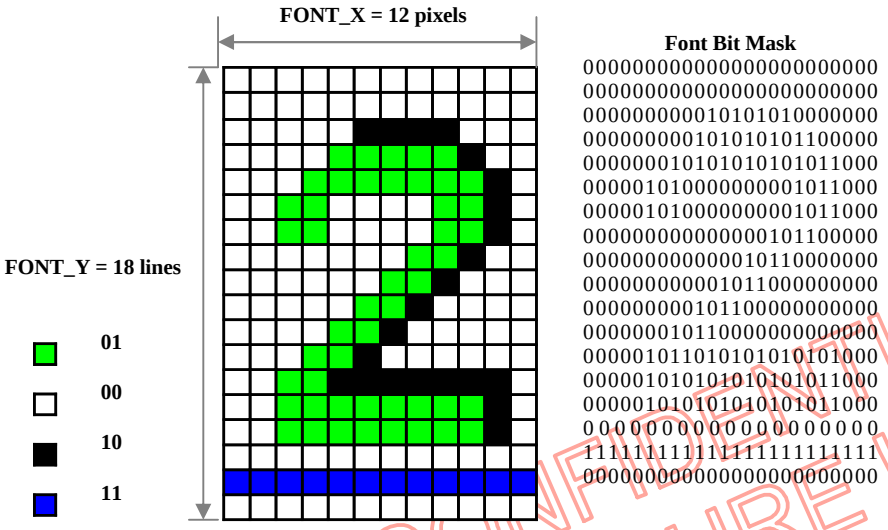
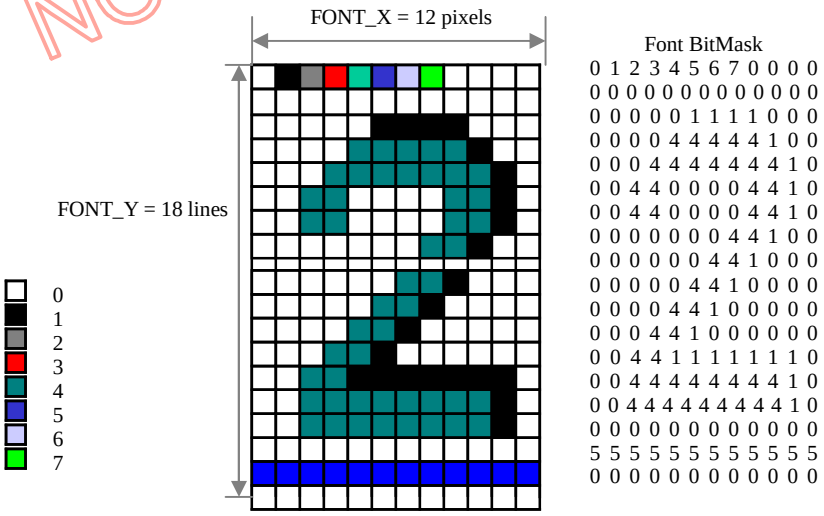


Figure 6.9-6 Two Bit Per Pixel Font

Three Bit per pixel

Three bits per pixel font definitions are arranged in Color Character Font SRAM Memory on a 24-bit by 36 addresses. The four bit per pixel OSD programmable font start address is specified in Register 0x08D ~ 0x08C. Each pixel row of a font contains up 12 pixels, with the font row broken up across two consecutive Color Character Font SRAM Memory addresses.



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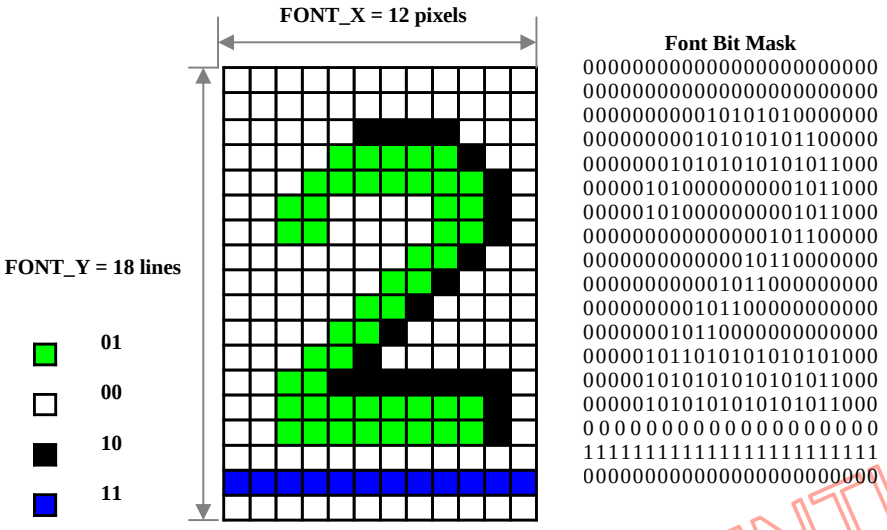

Figure 6.9-7 Three Bit Per Pixel Font

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Four Bit per pixel

Four bits per pixel font definitions are arranged in Color Character Font SRAM Memory on a 24-bit by 36 addresses. The four bit per pixel OSD programmable font start address is specified in Register 0x08D ~ 0x08C. Each pixel row of a font contains up 12 pixels, with the font row broken up across two consecutive Color Character Font SRAM Memory addresses.

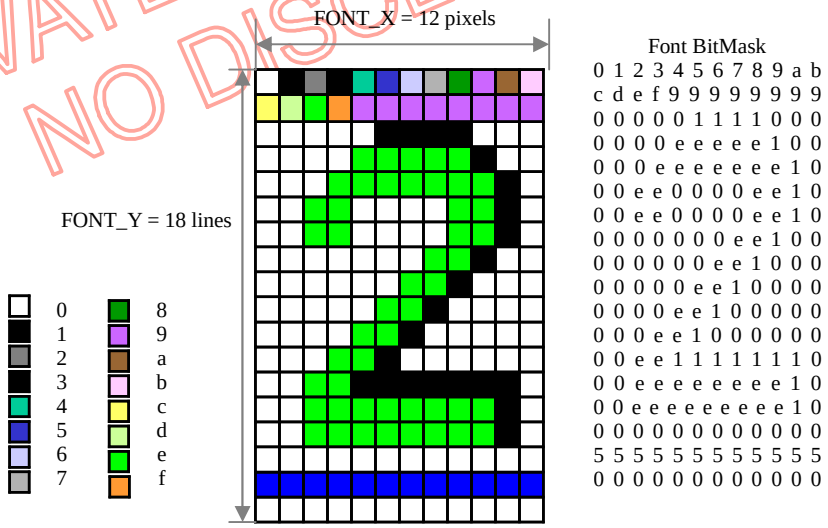

Figure 6.9-8 Four Bit Per Pixel Font

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OSD Color Character Font SRAM Memory Arrangement Map:

A single ported SRAM (4096-words × 24-bits) is used for storing character attribute, code index, and programmable fonts. The following example illustrates the contents of SRAM memory for a sample OSD. The OSD is three rows by four columns.

Note: That the OSD Frame SRAM and Font SRAM share the same on Color Character Font SRAM Memory. Thus, the size of the memory map can be traded off against the number of different memory definitions. In particular, the size of the OSD frame and the number of font data must fit in the Color Character Font SRAM Memory. That is, the following inequality must be satisfied.

(OSD_HW+1)×(OSD_VH+1) + 18×CELING (Number of 1-bit per pixel fonts / 9) × 9 +
2×18×CELING (Number of 2-bit pixel fonts / 9) × 9 +
3/4×18×CELING (Number of 4-bit pixel fonts / 9) × 9 <= 5120

The programmable font start address setting:

OSD One Bit Font Address (FONT1B_ADDR) = (OSD_HW+1)×(OSD_VH+1)

OSD Two Bits Font Address (FONT2B_ADDR) = OSD One Bit Font Address (FONT1B_ADDR) + (Number of 1-bit per pixel fonts) ×(12×18/24)

OSD Three/Four Bits Font Address (FONT3B_ADDR/ FONT4B_ADDR) = OSD Two Bit Font Address (FONT2B_ADDR) + (Number of 2-bit per pixel fonts) ×(2×12×18/24)

Note: The following inequality must be satisfied

MOD (Number of 1-bit pixel fonts / 9) = 0
MOD (Number of 2-bit pixel fonts / 9) = 0
MOD (Number of 4-bit pixel fonts / 9) = 0

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OSD Frame Definition:

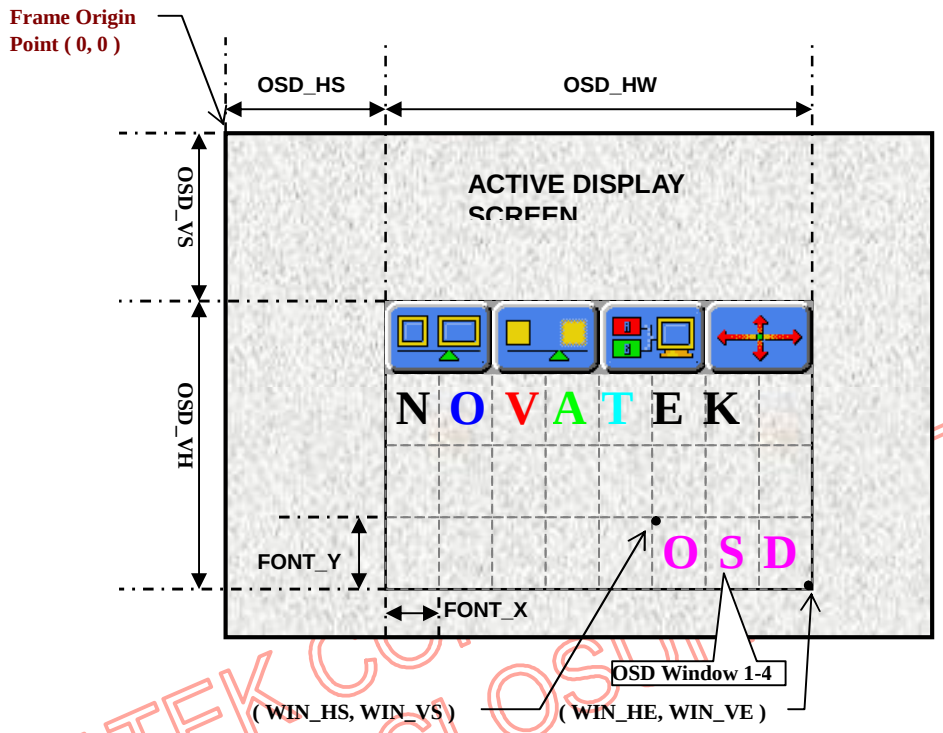

Figure 6.9-9 OSD Active Frame And Windows

OSD_HS : OSD Frame Horizontal Start (0 – 2047 pixels)
OSD_HW : OSD Frame Horizontal Width (1 – 64 chars)
OSD_VS : OSD Frame Vertical Start (0 – 2047 pixels)
OSD_VH : OSD Frame Vertical Height (1 – 32 chars)
WIN_HS : OSD Window Horizontal Start (1 – 64 chars)
WIN_HE : OSD Window Horizontal End (1 – 64 chars)
WIN_VS : OSD Window Vertical Start (1 – 32 chars)
WIN_VE : OSD Window Vertical End (1 – 32 chars)
FONT_X : Font X size (12/10 pixels)
FONT_Y : Font Y size (16/18 lines)

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6.10. DPLL Clock Control

NT68667 Display PLL (Bandwidth 170MHz) for display timing generator.

Formula:
Fout = (Reference-Freq × DDDS_RATIO [21:0]) / 2^{17}
Fref = 12.000 MHz
Note: The value (Reference-Freq × DDDS_RATIO [21:0] / 2^{17}) must be large to 100 MHz

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6.11. DISPLAY INTERFACE

NT68667 display interface supports single (24-bit) or dual (48-bit) pixel out format, and supports the 6-bit/color or 8-bit/color LCD panel. Built in internal PLL locking to the reference clock generates all of the display timing to various LCD panels.
NT68667 also provides the programmable display driving capacity to reduce EMI influence as well as programmable clock delay to compensate clock skew.

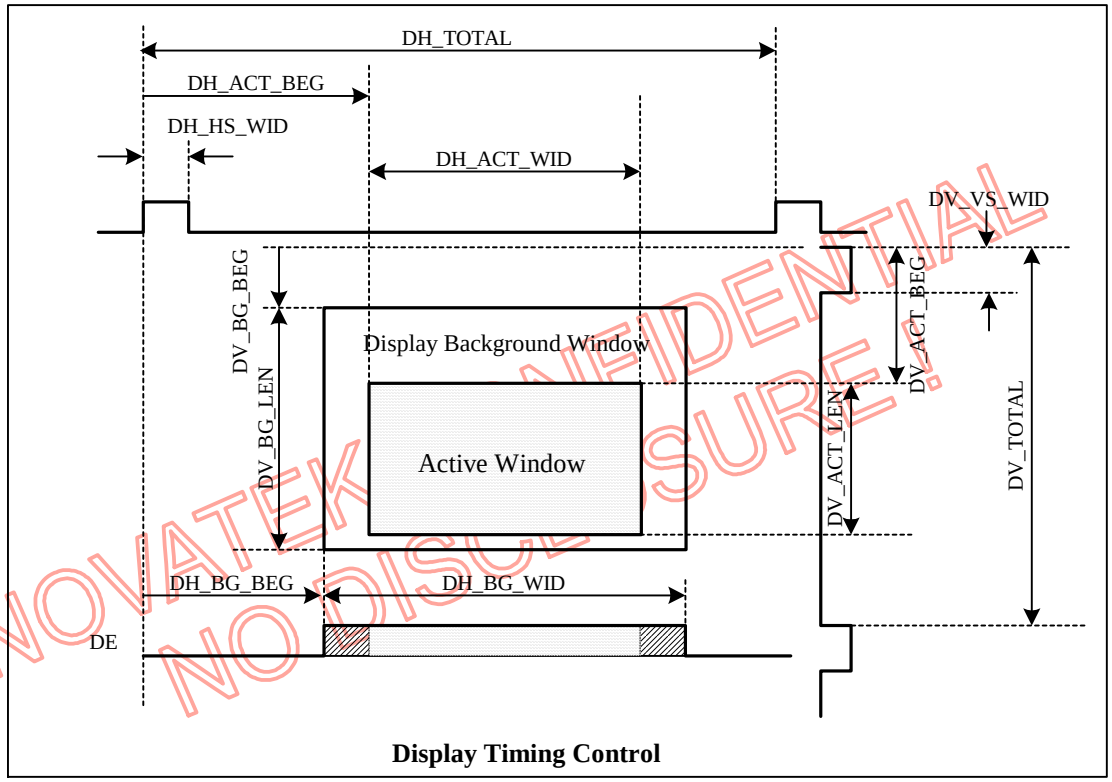

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Figure 6.11-1 Display Timing Control

6.11.1. Scaler Display Data

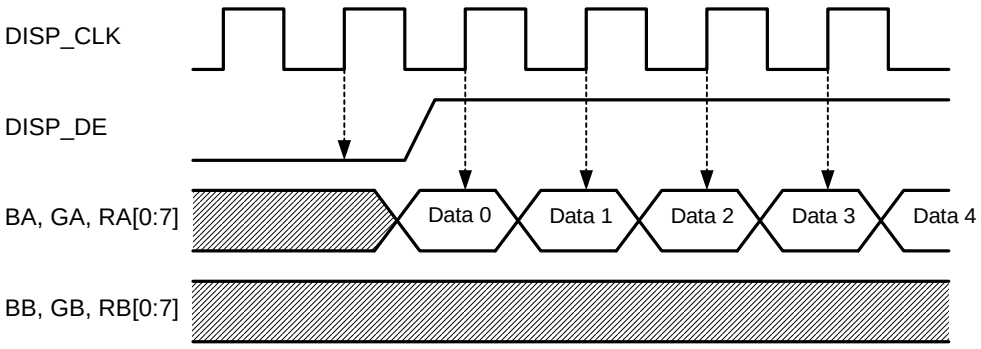

Figure 6.11-2 Single Pixel Width Display Data

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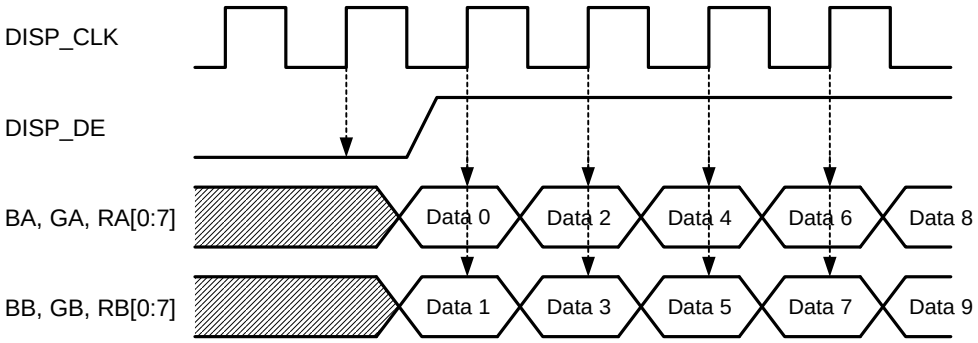

Figure 6.11-3 Double Pixel Width Display Data

6.11.2. Single/Dual pixel LVDS Transmitter

The NT68667 transmitter is de-signed to support single or dual pixel data transmission between Scaler and Flat Panel Display up to WSXGA resolutions. For single pixel mode, the transmitter converts 24 bits (single Pixel 24-bit color) data into 4 LVDS (Low Voltage Differential Signaling) data streams. For dual pixel mode, the transmitter converts 48 bits (Dual Pixel 24-bit color) data into 8 LVDS (Low Voltage Differential Signaling) data streams Control signals (VSYNC, HSYNC, DE and two user-defined signals) are sent during blanking intervals.

The LVDS transmitter can support the following:

1. Single or double pixel mode
2. 24/48-bit panel mapping to the LVDS channels
3. 18/36-bit panel mapping to the LVDS channels
4. Programmable even/odd LVDS swapping
5. Programmable channel swapping (the clocks are fixed)
6. Support up to WSXGA 75Hz output

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Panel Data Mappings

Dual Pixel mode (When DP_BIT_SHF = 0)								
Channel 0 / Channel 4	R0, R1, R2, R3, R4, R5, G0							
Channel 1 / Channel 5	G1, G2, G3, G4, G5, B0, B1							
Channel 2 / Channel 6	B2, B3, B4, B5, HS, VS, DE							
Channel 3 / Channel 7	R6, R7, G6, G7, B6, B7, RSVD							
LVDS channel 0 (T0)	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	GA0	RA5	RA4	RA3	RA2	RA1	RA0
LVDS channel 1 (T1)	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	BA1	BA0	GA5	GA4	GA3	GA2	GA1
LVDS channel 2 (T2)	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	VS	HS	BA5	BA4	BA3	BA2
LVDS channel 3 (T3)	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	RSVD	BA7	BA6	GA7	GA6	RA7	RA6
LVDS channel 4 (T4)	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	GB0	RB5	RB4	RB3	RB2	RB1	RB0
LVDS channel 5 (T5)	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	BB1	BB0	GB5	GB4	GB3	GB2	GB1
LVDS channel 6 (T6)	LVDS output	D26	D25	D24	D22	D21	D20	D19

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LVDS channel 7 (T7)	Data order	DE	NA	NA	BB5	BB4	BB3	BB2
	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	BB7	BB6	GB7	GB6	RB7	RB6

Dual Pixel mode (When DP_BIT_SHF = 1)								
Channel 0 / Channel 4	R2, R3, R4, R5, R6, R7, G2							
Channel 1 / Channel 5	G3, G4, G5, G6, G7, B2, B3							
Channel 2 / Channel 6	B4, B5, B6, B7, HS, VS, DE							
Channel 3 / Channel 7	R0, R1, G0, G1, B0, B1, RSVD							
LVDS channel 0 (T0)	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	GA2	RA7	RA6	RA5	RA4	RA3	RA2
LVDS channel 1 (T1)	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	BA3	BA2	GA7	GA6	GA5	GA4	GA3
LVDS channel 2 (T2)	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	VS	HS	BA7	BA6	BA5	BA4
LVDS channel 3 (T3)	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	RSVD	BA1	BA0	GA1	GA0	RA1	RA0
LVDS channel 4 (T4)	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	GB2	RB7	RB6	RB5	RB4	RB3	RB2
LVDS channel 5 (T5)	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	BB3	BB2	GB7	GB6	GB5	GB4	GB3
LVDS channel 6 (T6)	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	BB7	BB6	BB5	BB4
LVDS channel 7 (T7)	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	BB1	BB0	GB1	GB0	RB1	RB0

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6.12. Miscellaneous

6.12.1. PWM Output

There are two Pulse Width Modulation signal pins available for controlling the LCD back light or audio volume, PWMA and PWMB. The duty cycle and Frequency of these signals is programmable.

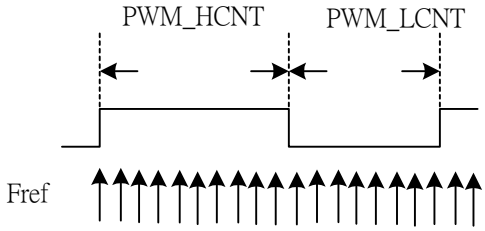

Figure 6.12-1 Pulse Width Modulation Signal (PWM)

When clock source select from reference clock

$$F_{PWM_CLK} = F_{REFCLK} / (PWM_DIV\ 1 \times PWM_DIV\ 2)$$

When clock source select from Display Hsync

$$F_{PWM_CLK} = F_{DISP_HS} / (PWM_DIV\ 1 \times PWM_DIV\ 2)$$

$$F_{PWM} = \frac{F_{PWM_CLK}}{(PWM_HCNT + PWM_LCNT)}$$

$$Duty = \frac{PWM_HCNT}{(PWM_HCNT + PWM_LCNT)}$$

$$PWM_HCNT = \frac{Duty \times F_{PWM_CLK}}{F_{PWM}}$$

$$PWM_LCNT = \frac{(1 - Duty) \times F_{PWM_CLK}}{F_{PWM}}$$

PWM_HCNT	PWM_LCNT	PWM Output
0	0~255	DC '0'
1~255	0	DC '1'
1~255	1~255	PWM pulse

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6.13. MCU Interface

6.13.1. IRQn Interrupt Sources

NT68667 provides an internal interrupt request output IRQn to internal MCU. The following figure shows the detail structure of the IRQn sources.

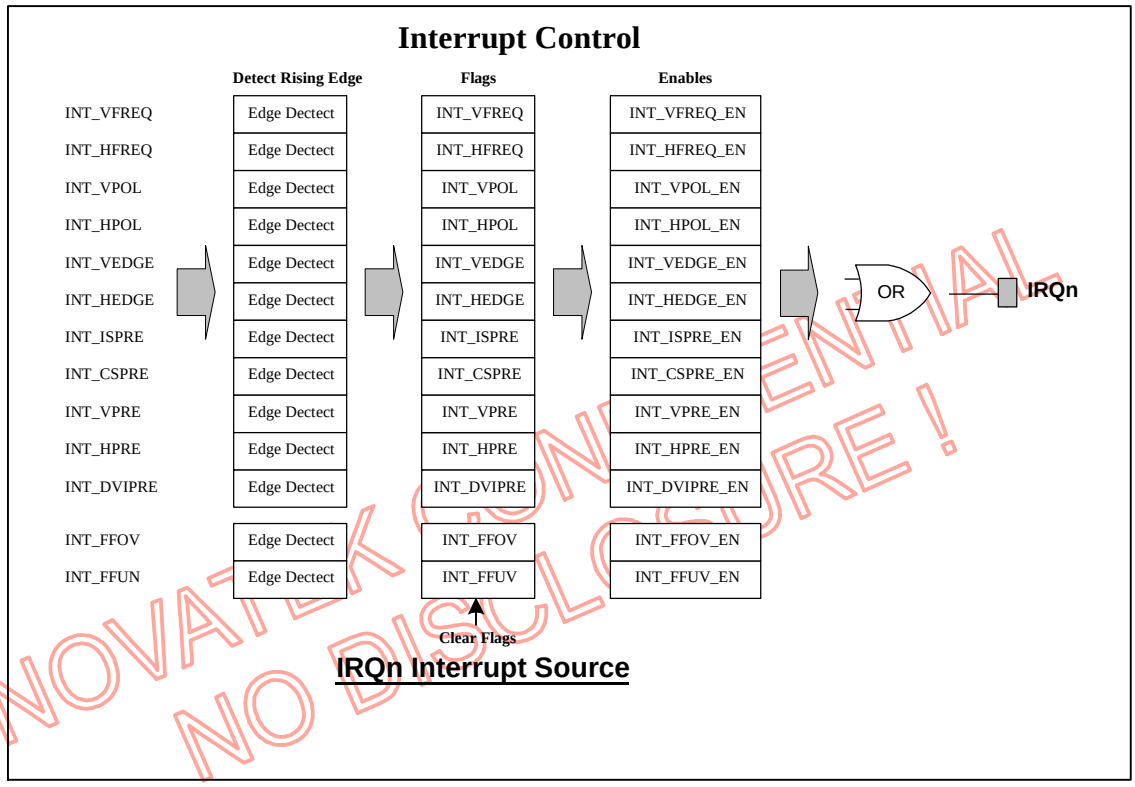

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Figure 6.13-1 IRQn Interrupt Block Diagram

INTHV_IRQ	Meaning	Action
INT_VFREQ	Vsync Frequency Change	It will be activated when the Input frequency of Vsync changes.
INT_HFREQ	Hsync Frequency Change	It will be activated when the Input frequency of Hsync changes.
INT_VPOL	V-Polarity Change INT	It will be activated when the Input Polarity of Vsync changes.
INT_HPOL	H-Polarity Change INT	It will be activated when the Input Polarity of Hsync changes.
INT_VEDGE	Vsync Edge INT	It will be activated when the Vsync rising edge is occur.
INT_HEDGE	Hsync Edge INT	It will be activated when the Hsync rising edge is occur.
INT_ISPRE	Interlaced Sync INT	It will be activated when the Interlaced Sync is present.
INT_ CSPRE	Composite Sync INT	It will be activated when the Composite Sync is present.
INT_VPRE	Vsync Present INT	It will be activated when the Vsync is present.
INT_HPRE	Hsync Present INT	It will be activated when the Hsync is present.
INT_DVIPRE	DVI sync Present INT	It will be activated when the DVI sync is present.

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INT_FFOV	FIFO Overflow INT	It will be activated when the FIFO is overflow
INT_ FFUV	FIFO Underflow INT	It will be activated when the FIFO is underflow
INT_UPD_DDC0	DDC0 updated INT	It will be activated when DDC0 Ram-Buffer contents updated.
INT_ UPD_DDC1	DDC1 updated INT	It will be activated when DDC1 Ram-Buffer contents updated.

Table 6.13-1 IRQn Interrupt

6.14. 8031 On-Chip Microcontroller

Reference NT68667 MCU Spec.

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7. Electrical Specifications

Absolute Maximum Ratings

3.3V Supply voltage range, $V_{3.3}$ (see Note1)……-..0.3V to 4V
Output voltage range, V_O……-0.3V to V_{33} +0.3V
Input voltage range (5V Tolerant), V_I……-0.3V to V_{5V} +0.3V
Electrostatic Discharge, V_{ESD}……±2.0KV
ESD MM …… ±200V (Class 2)
Latch Up …… .±200mA (Class 3)
MSL……...Class 3
Ambient Operating temperature, T_A……....0°C to 70°C
Lead temperature 1, 6 mm (1/16 inch) from case for 10 seconds……260°C
Junction temperature……...150°C
Surface temperature.....125°C
Storage temperature range, Tstg……...-40°C to 125°C
Storage humidity……< 60% HR
Storage Life (Storage Temperature < 30 ℃)……1 year

- Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.
- Note1: Includes pins ADC_VAA, AVCC, PVCC, DVDD.
- Note2: Includes pins CVDD, PLL_VDD

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7.1. DC Electrical Characteristics

(T_A = 25°C, Oscillator freq. = 12.000MHz, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Power Requirements						
V_{CVDD}	1.8 V digital power supply	1.6	1.8	2.0	V	CVDD
V_{PLL}	PLL power supply	1.6	1.8	2.0	V	PLL_VDD
V_{ADC}	R/G/B channel ADC analog power supply	3.15	3.3	3.47	V	ADC_VAA,
V_{TMDSA}	TMDS analog power supply	3.15	3.3	3.47	V	AVCC
V_{TMDSP}	TMDS PLL power supply	3.15	3.3	3.47	V	PVCC
V_{DDD}	Display interface power supply	3.15	3.3	3.47	V	DVDD
I_{ADC}	ADC power supply current		150		mA	
I_{TMDS}	TMDS power supply current		160		mA	
I_{DD33}	3.3 V Operating current		200		mA	Except ADC, TMDS
I_{DDPD33}	3.3 V Power down current		20		mA	Inculde ADC,TMDS.DVDD
Digital Outputs						
V_{OH}	Output high voltage	2.0		V_{DD}	V	IN_HSO, IN_VSO

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V_{OL}	Output low voltage	GND		0.8	V	
V_{OH}	Output high voltage for open drain type			5	V	PWM[6:9],PWMA, PWMB, DDC_SCL[1:0], DDC_SCL[1:0], PC0,PC1
I_{OZ}	Tri-State Leakage Current	-25		25	uA	
I_{OH}	Output high current	-16		-2	mA	(V_{OH} = 2.5V) DISP_DE, DISP_VS, DISP_HS, DISP_CLK GPO[8:1]
I_{OL}	Output low current	2		16	mA	(V_{OL} = 0.4V) DISP_DE, DISP_VS, DISP_HS, DISP_CLK GPO[8:1]
LVDS Outputs						
$\|V_{OD}\|$	Differential Steady-state Output Voltage Magnitude	240			mV	R_L = 100 , See Figure 7.1.1
$\triangle\|V_{OD}\|$	Change in the Steady-state Differential Output Voltage Magnitude between Opposite binary States			35	mV	
$V_{OC(SS)}$	Steady-state Common-mode Output Voltage	1.125		1.475	V	See Figure 7.1.1
$V_{OC(PP)}$	Peak-to-peak Common-mode Output Voltage		80	150	mV	
I_{OS}	Short-circuit Output Current			±24	mA	$V_{O(TP)}$ = 0
				±12	mA	V_{OD} = 0
I_{OZ}	Output Tri-State Current		±1		μA	V_O = 0 to Vcc
Analog Input						
V_{IAMIN}	Minimum Input Voltage Range			0.55	V p-p	
V_{IAMAX}	Maximum Input Voltage Range			0.9	V p-p	V_{IAMAX}
DVI Input						
V_{ID}	Differential Input Voltage	150		1200	mV	See Figure 7.1.3
V_{ICOM}	Input Common Mode Voltage	AVCC - 300m		AVCC-37mV	mV	See Figure 7.1.3

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		V				
V_{BTD}	Behavior when Transmitter is disabled	AVCC - 10mV		AVCC + 10mV	mV	See Figure 7.1.3
Digital Input						
V_{IH}	Input high voltage	2.0		V_{DD}	V	Y[7:0],
V_{IL}	Input low voltage	GND		0.8	V	
$V_{T+(HSYNC)}$	Schmitt Trigger Positive Going Threshold Voltage for HSYNC Inputs	1.5	1.6	2.2	V	HSYNCI0, HSYNCI1
$V_{T-(HSYNC)}$	Schmitt Trigger Negative Going Threshold Voltage for HSYNC Inputs	0.7	1.1	1.4	V	HSYNCI0, HSYNCI1
$V_{T+(VSYNC)}$	Schmitt Trigger Positive Going Threshold Voltage for VSYNC Inputs		1.8	2.0	V	VSYNCI0, VSYNCI1
$V_{T-(VSYNC)}$	Schmitt Trigger Negative Going Threshold Voltage for VSYNC Inputs	0.8	1.5		V	VSYNCI0, VSYNCI1
V_{IHC}	Clock high voltage	2.0		V_{DD}	V	YUV_CLK,
V_{ILC}	Clock low voltage	GND		0.4	V	
I_{IH}	Input high current	-25		25	μA	(V_{IH} = 2.5V)
I_{IL}	Input low current	-25		25	μA	(V_{IL} = 0.4V)

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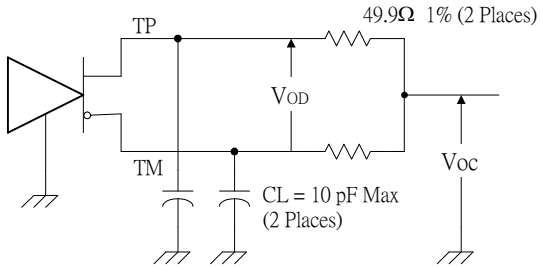
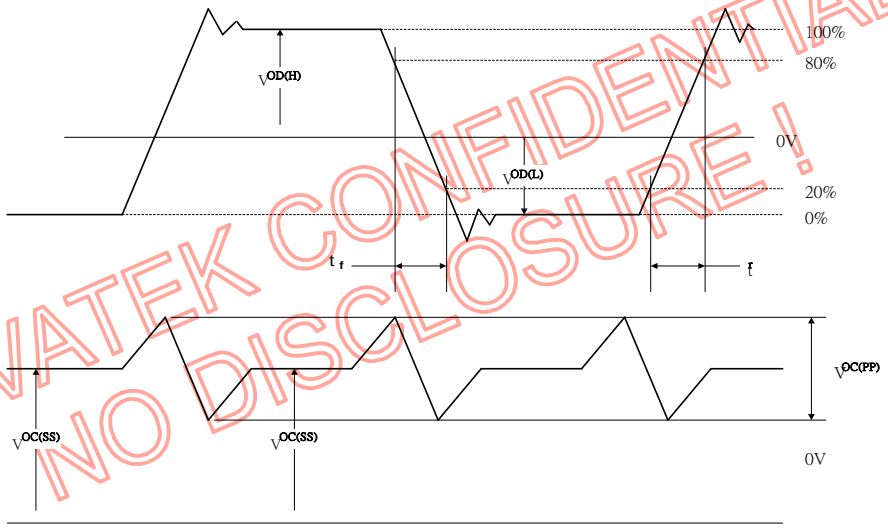


(a)SCHEMATIC



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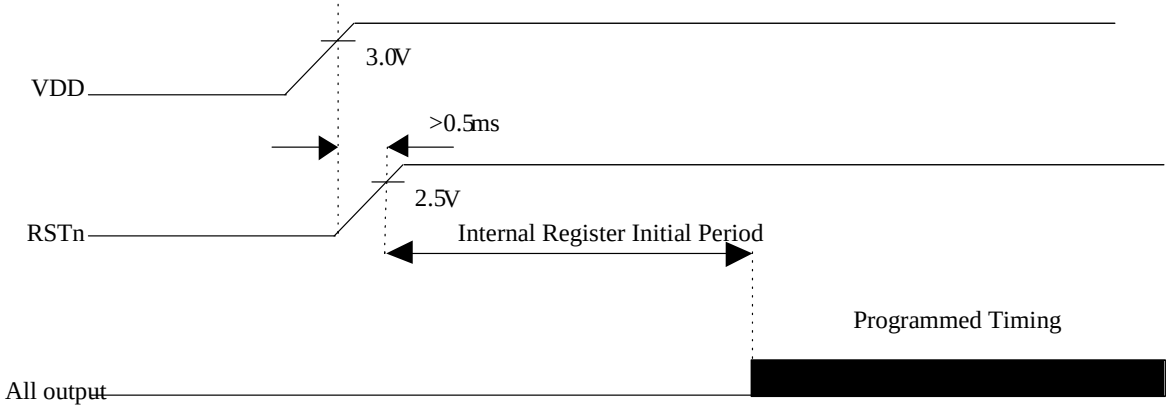
7 WAVEFORMS

Figure 7.1-1 Test Load and Voltage Definitions for LVDS Outputs



Power -up Sequence

Figure 7.1-2 Power-up Sequence

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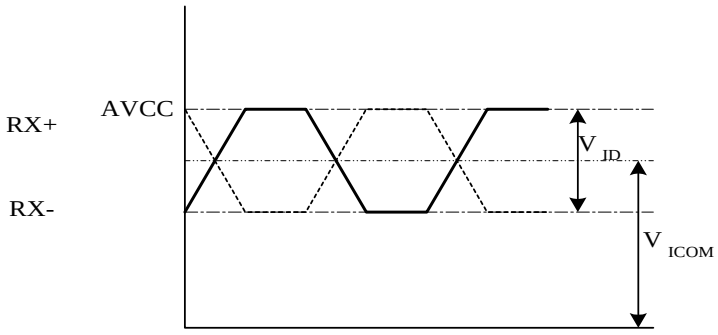

Figure 7.1-3 DVI Single-ended Differential Signal

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7.2. AC Electrical Characteristics

(VDD=3.3V, TA=25°C, Oscillator freq.=12MHz, unless otherwise specified)

ADCPLL

Phase-locked loop						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
j_{PLL}	Short term jitter	fclkout=188MHz	-	120	-	ps
	Long term jitter	fclkout=188MHz	-	0.6	-	ns
DR	Divider ratio	-	2	-	4096	
f_{CLKIN}	Input HS frequency range	-	15	-	110	KHz
f_{CLKOUT}	Output clock frequency range	For normal type	**15**	-	**166**	MHz
		For H type	**15**	-	**188**	
		For U type	**15**		**190**	
t_{CAP}	PLL capture time	In start-up conditions	-	-	5	ms
δ	CKOUT clock duty cycle	165 MHz output	45	50	55	%

Clamping Pulse						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
t_{DELAY}	Clamp pulse delay time	CLAMP_BEG<5:0>=0x00	-	0	-	4/CKOUT
		CLAMP_BEG<5:0>=0x0F	-	15	-	4/CKOUT
t_{WIDTH}	Clamp pulse width	CLAMP_WID<5:0>=0x01	-	1	-	4/CKOUT
		CLAMP_WID<5:0>=0x0F	-	15	-	4/CKOUT
t_{COR1}	Clamp correction time to within ±10 mV	±100mV black level input variation; clamp capacitor = 4.7nF	-	-	300	ns
t_{COR2}	Clamp correction time to less than 1 LSB	±100mV black level input variation; clamp capacitor = 4.7nF	-	-	10	Lines

Analog-to-Digital Converter						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
fs	Sampling frequency	For normal type	**15**	**-**	**166**	MHz
		For H type	**15**		**188**	
		For U type	**15**		**190**	
G_{MATCH}	Channel to channel match	-	-	2	5	%
Vin(p-p)	Input signal voltage (peak-peak)	Corresponding to full scale output	0.55	0.7	0.9	V
DNL	DC differential non linearity	From analog input to digital output; ramp input;	-	±0.5		LSB

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INL	DC integral non linearity	From analog input to digital output; ramp input;	-	±0.6		LSB
ENOB	Effective number of bits	From analog input to digital output;10KHz sine wave input; ramp input	-	7	-	bits
THD		Input 1V(p-p) and 10MHz	-	-	1	%

No Missing Codes is guaranteed.

Signal-to-Noise Ratio						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
S/N	Signal-to-noise ratio	Maximum gain	-	45	-	dB
		Minimum gain	-	44	-	dB

TMDS Receiver

TMDS Receiver						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
f_{OP}	Operating Frequency range		25	-	165	MHz
t_{JJT}	Jitter tolerance		2	-	-	ns
t_{START}	Receiver Startup Time		-	-	10	ms
t_{DPS}	Intra-Pair (+ to -) Differential Input Skew	165MHz 1 pixel/clock			250	ps
t_{CCS}	Channel to Channel Differential Input Skew	165MHz 1 pixel/clock			5.0	ns
C_{IN}	TMDS Input Pin Capacitance		-	7	-	pF

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Sync Processor (Oscillator freq.=12MHz)

H/V Sync Processor						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
f_{VSYNC}	Vsync Input Frequency	Vsync Duty Cycle = 40%	15	-	250	Hz
f_{VCLK}	Vsync Input Frequency for DDC-1 Mode	Supply VCLK for DDC-1 mode only	-	-	25	KHz
t_{VPW}	VSYNC input Pulse Width	Vsync Duty Cycle < 40%	-	-	2.5	ms
f_{HSYNC}	Hsync Input Frequency	Hsync Duty Cycle = 40%	15	-	250	KHz
t_{HPW}	HSYNC input Pulse Width	Hsync Duty Cycle < 40%	-	-	8.66	us
$t_{HPW(COMP)}$	HSYNC input Pulse Width	Hsync Duty Cycle < 40%	-	-	8.66	us
$t_{HTTT(COMP)}$	Horizontal total time		8.66			us

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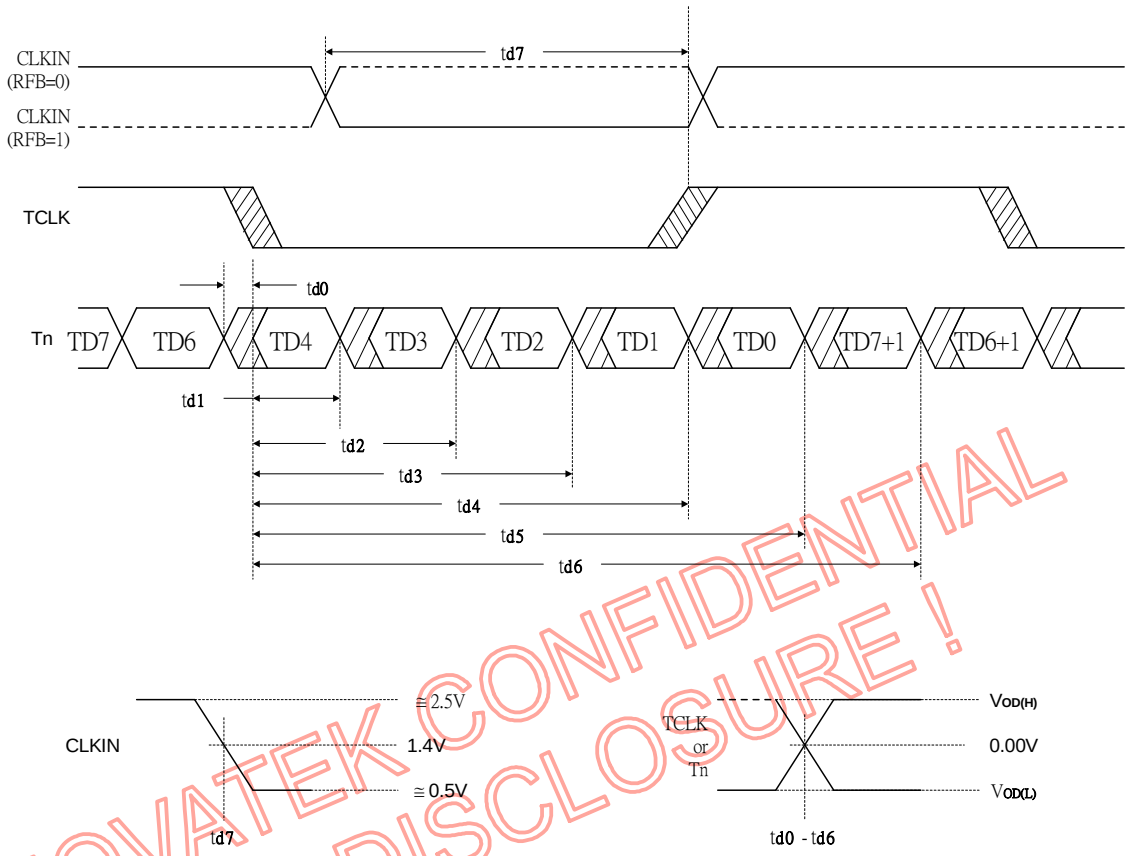

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Figure 7.2-1 LVDS Timing Definitions

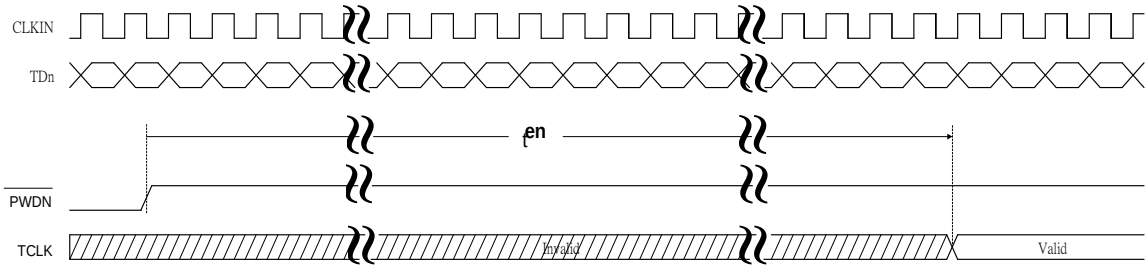

Figure 7.2-2 LVDS Enable Time Waveforms

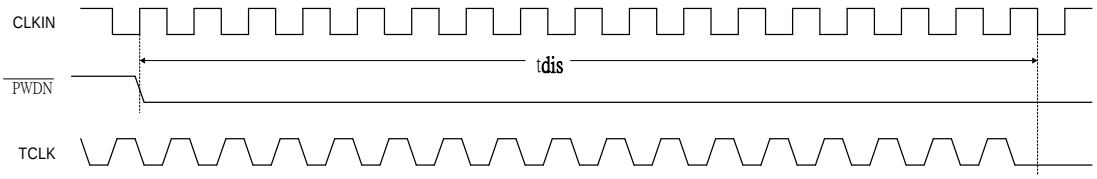

Figure 7.2-3 LVDS Disable Time Waveforms

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8. Registers Mapping

	Block Name		Byte Offset		
	ADC PLL Interface	Page 0	0x000 ~ 0x017		
	DVI Input Control 1		0x018 ~ 0x01E		
	Graphic Port Control		0x020 ~ 0x03F		
	Video Port Control		0x040 ~ 0x05F		
	Back End Image Processing		0x060 ~ 0x064		
	NR Control		0x068 ~ 0x06F		
	GPIO Control		0x070 ~ 0x073		
	PWM Control		0x074 ~ 0x077		
	DDC Control		0x078 ~ 0x07D		
	OSD Control		0x080 ~ 0x0CF		
	Index Port Access Control		0x0E0 ~ 0x0E3		
	Misc. Access Control		0x0E5 ~ 0x0E6		
	HS Digital PLL		0x0D0 ~ 0x0EF		
	Display Digital PLL & SSC		0x0F0 ~ 0x0F7		
	Power Control	Page 1	0x101 ~ 0x102		
	Auto Tune		0x106 ~ 0x12F		
	Bright Frame Display		0x130 ~ 0x13B		
	Display General Control		0x150 ~ 0x18F		
	Sync Processor		0x196 ~ 0x1B0		
	sRGB Control		0x1D0 ~ 0x1DF		
	Timing Control	Page 2	0x200 ~ 0x2FF		
	HDCP	Page 3	0x300 ~ 0x36F		
	Dithering Control		0x370 ~ 0x371		
	Non-Linear Scaling Adjust		0x380 ~ 0x38B		
	Bright Frame		0x390 ~ 0x3FE		
	Dynamic Backlight Control	Page 4	0x430 ~ 0x43F		

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8.1. ADC Interface

0x000		ADCPLL Control	R/W
Bits	Name	Description	
7-5		Reserved	
4	HPLL_HSYNC_SEL	HPLL Hsync input signal selection 0: HSYNCI (from HSYNCI) 1: SYNC_HS (from sync processor)	
3	HSYNC_SEL	HPLL Hsync input signal selection 0: HSYNCI (from HSYNCI) 1: SOGI	
2-0		Reserved	

Default: 1010 0000B

0x001		Red Channel Gain Control	R/W
Bits	Name	Description	
7-0	RGAIN[8:1]	The RAGAIN[7:0] that sets the gain of the R channel. The ADC can accommodate input signals with a full-scale range of between 0.55V and 0.9Vp-p. Note that increasing RGAIN results in the picture having less contrast.	

Default: 1000 0000B

0x002		ADC Common Mode	R/W
Bits	Name	Description	
7-0		ADC common voltage compensation	

Default: 1000 0000B

0x003		Red Channel DC Shift Control	R/W
Bits	Name	Description	
7-0	RCSC [7:0]	Control the R channel DC shift value to compensate the color excursion. Bigger value gives less brightness.	

Default: 1000 0000B

0x004		Green Channel Gain Control	R/W
Bits	Name	Description	
7-0	GGAIN[8:1]	The GAGAIN[7:0] that sets the gain of the G channel. The ADC can accommodate input signals with a full-scale range of between 0.55V and 0.9Vp-p. Note that increasing GGAIN results in the picture having less contrast.	

Default: 1000 0000B

0x005		ADC GAIN RANGE	R/W
Bits	Name	Description	
7-0		ADC gain range compensation	

Default: 0000 0000B

0x006		Green Channel DC Shift Control	R/W
Bits	Name	Description	
7-0	GCSC [7:0]	Control the G channel DC shift value to compensate the color excursion. Bigger value gives less brightness.	

Default: 1000 0000B

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0x007		Blue Channel Gain Control	R/W
Bits	Name	Description	
7-0	BGAIN[8:1]	The BAGAIN[7:0] that sets the gain of the B channel. The ADC can accommodate input signals with a full-scale range of between 0.55V and 0.9Vp-p. Note that increasing BGAIN results in the picture having less contrast.	

Default: 1000 0000B

0x008		ADC Channel and MID Clamp Control	R/W
Bits	Name	Description	
7-3		Reserved	
2	CHANNEL_SEL	ADC channel 0: Disable 1: Enable	
1	BMID	Blue Clamp Select 0: Clamp to ground 1: Clamp to midscale	
0	RMID	Red Clamp Select 0: Clamp to ground 1: Clamp to midscale	

Default: 0000 0100B

0x009		Blue Channel DC Shift Control	R/W
Bits	Name	Description	
7-0	BCSC[7:0]	Control the B channel DC shift value to compensate the color excursion. Bigger value gives less brightness.	

Default: 1000 0000

0x00A ~ 0x00D : Reserved

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0x00E		ADC PLL Power-up Control	R/W
Bits	Name	Description	
7-6		Reserved	
5	BGAIN[0]	BGAIN bit 0	
4	GGAIN[0]	GGAIN bit 0	
3	RGAIN[0]	RGAIN bit 0	
2	PU_B_ADC	1= Power-up B channel A2D converter.	
1	PU_G_ADC	1= Power-up G channel A2D converter.	
0	PU_R_ADC	1= Power-up R channel A2D converter.	

Default: 1111 1111B

0x00F : Reserved

0x010		Analog Bandwidth Control	R/W
Bits	Name	Description	
7-3		Reserved	
2-1	ADC_BW [2:0]	Analog bandwidth select , Bit2 set from 0x1ED.5 011:500M 111:450M 110:400M	

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		101:350M 010:300M 100:250M 001:150M 000:75M
0		Reserved

Default: 0000 0110B

0x011 : Reserved

0x012		SOG Slicer Control	R/W
Bits	Name	Description	
7-3	SOG_THR [4:0]	The comparator threshold of the Sync-on-Green Slicer to be adjusted. This register adjust it in steps of 10 mV, with the setting 100 mV <= SOG_THR <=400 mV	
2	EN_SOG_SLICER	Enable internal SOG Slicer. 0 = Disable 1 = Enable	
1-0		Reserved	

Default: 0111 1100B

0x013		White Balance Control	R/W
Bits	Name	Description	
7-2		Reserved	
1-0	VREF[1:0]	Select the signal source for VGA input. When VR1 is selected, the PLL will go into free-run state. 00: VR0. Internal zero voltage. 01: Add resistor between external RGB and A/D circuit , the ADC bandwidth is decided by the two bit and 0x010[2:1] 10: VR1. Internal reference voltage 1. (0.7V) 11: Normal. From external RGB input pin.	

Default: 0000 0011B

0x014		Hsync Trigger Level Control	R/W
Bits	Name	Description	
7		Reserved	
6-4	HS_THR_H	The trigger level threshold of the sync high level to be adjusted. This register adjust it in steps of 100 mV, with the setting 1500 mV <= HS_THR_H <=2000 mV	
3		Reserved	
2-0	HS_THR_L	The trigger level threshold of the sync low level to be adjusted. This register adjust it in steps of 100 mV, with the setting 950 mV <= HS_THR_L<=1400 mV	

Default: 0000 0000B

0x015		Vsync Trigger Level Control	R/W
Bits	Name	Description	
7	VS_SCHMITT	VSI □uality triggle 0: Disable 1: Enable	
6-4	VS_THR_H	The trigger level threshold of the sync high level to be adjusted.	

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		This register adjust it in steps of 100 mV, with the setting 1500 mV <= VS_THR_H <=2000 mV
3		Reserved
2-0	VS_THR_L	The trigger level threshold of the sync low level to be adjusted. This register adjust it in steps of 100 mV, with the setting 950 mV <= VS_THR _L<=1400 mV

Default: 0000 0000B

8.2. DVI Input Control 1

0x016		DVI Clock Detection	R
Bits	Name	Description	
7-0	DVI_CLK	DVI clock detection , unit : Mhz	

Default: XXXX XXXXB

0x017 : Reserved

0x018		DVI Control	R/W
Bits	Name	Description	
7-5		Reserved	
4		For internal circuit DVI control , force to “0” for normal operate	
3	SYNC_SEL	Sync is generated from R channel or B channel 0 = From B Channel (RX0) 1 = From R Channel (RX2)	
2-0		Reserved	

Default: 0000 0000B

0x019		DVI Control	R/W
Bits	Name	Description	
7-0		For internal circuit DVI control	

Default: 0000 0000B

0x01A : Reserved

0x01B		DVI Control	R/W
Bits	Name	Description	
7-4		Reserved	
3-1	DVI_FILT_ADJ	DVI noise filter 000 : Weakness 111 : Strength	
0	DVI_NOISE_FIL	Noise filter 0: Disable 1: Enable	

Default: 0000 0000B

0x01C : Reserved

0x01D		DVI Control	R/W
Bits	Name	Description	
7-4		Reserved	

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3-0	DVI_PLL_BW	DVI PLL frequence range control 0000 : Low frequency 1111 : High frequency

Default: 0000 0000B

0x01E	DVI Control	R/W
Bits	Name	Description
7-0	DVI_EQ_DATA	Equalizer bias current control

Default: 0000 0000B

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8.3. Pre-Pattern Control

0x01F	Pre-Pattern Control	R/W
Bits	Name	Description
7	PRE_PATT_EN	Pre-Pattern Enable. 0 = Disable 1 = Enable
6	PRE_INV	Pre-Pattern Data invert 0 = Normal 1 = Invert the RGB Data
5	PRE_CBAR_EN	Paste a Cross Bar on the built-in Pre-pattern and the Bar's gray level is controlled via CBAR_FG[7:0] register (0x15A) 0 = Disable 1 = Enable
4	PRE_PATT_BK	Built-in pre-pattern bank Select 0 = Bank 0 1 = Bank 1
3-0	PRE_PATT_SEL [3:0]	Select built-in pre-pattern type Pattern number = 0~7 If PRE_PATT_BK = Bank 0 0000 = Reserved 0001 = Dot Moiré 0010 = Vertical Line Moire (1B1W) 0011 = Vertical Line Moire (2B1W) 0100 = Vertical Line Moire (2B2W) 0101 = 256 V_Gray Bar 0110 = 256 H_Gray Bar 0111 = Horizontal Line Moire (1B1W) 1000 = Horizontal Line Moire (2B1W) 1001 = Horizontal Line Moire (2B2W) 1010 = Chat Pattern 1011 = White Pattern 11xx = Rectangular pattern, outline width is defined by xx bits. 00 = 1 pixel 01 = 3 pixels 10 = 5 pixels 11 = 7 pixels If PATT_BK = Bank 1 0000 = Black pattern 0001~1111 = Reserved

Default: 0000 0000B

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8.4. Graphic Port Control

- ADC/TMDS/Digital input source selection
- Clamp pulse
- Interlace decision window
- Mask window
- Capture window

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General Control

0x020		Graphic Port Control	R/W
Bits	Name	Description	
7	GI_VSYNC_EDGE	Mask window and capture Vsync referenced edge 0 = Leading edge 1 = Trailing edge	
6	GI_IFLD_INV	Invert the internal field reference signal for data merging priority 0 = Normal 1 = Invert	
5	GI_MKWIN_EN	Mask Window Enable. When GI_MKWIN_EN =1, GI_HMASK_BEG, GI_HMASK_END, GI_VMASK_BEG and GI_VMASK_END are used to set the window around the HSYNC and VSYNC during which the captured data is 0x000 and auto tune is ignored. This filters out noise occurring on the RGB channels around the HSYNC and VSYNC pulse. 0 = Disable 1 = Enable	
4	GI_WRAP_SEL	Wrap around method select. (see the figure as below) 0 = Wrap around 1 = Wrap black	
3	GI_HSYNC_EDGE	Mask window and capture H sync referenced edge. 0 = Leading edge 1 = Trailing edge	
2	GI_INTE_EN	Interlaced input enable. When GI_INTE_EN =1, the field status is reference to internal field detector. 0 = Non-interlaced 1 = Interlaced	
1	GI_SRC_SEL	Graphic input source select 0 = ADC 1 = TMDS	
0	GI_CAP_EN	Graphic input capture enable 0 = Disable 1 = Enable	

Default: 0000 0000B

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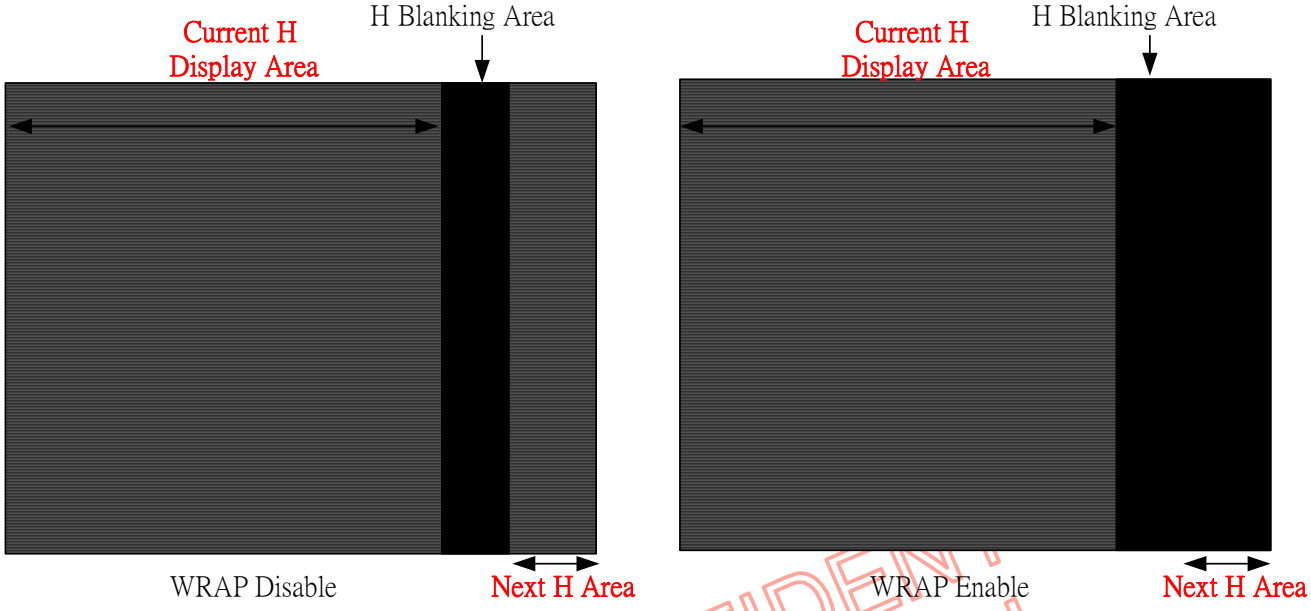

0x021		Clamp Pulse Begin	R/W
Bits	Name	Description	
7	CLAMP_EDG	Clamp Pulse Reference Edge 0 = GHS rising edge 1 = GHS falling edge	
6	CLAMP_POL	Clamp Pulse Polarity. 0 = Active Low 1 = Active High	
5-0	CLAMP_BEG [5:0]	Clamp Pulse Begin. (Unit 4xCLP_REFCLK = 4xCapture Clock) CLAMP_BEG =5, means waiting 5 x 4CLP_REFCLK after GHS edge to begin the pulse.	

Default: 0000 0000B

0x022		Clamp Pulse Width	R/W
Bits	Name	Description	
7	CLAMP_EN	Clamp Pulse Enable 0 = Disable 1 = Enable	
6	CLP_CLK_SEL	Clamp Pulse Reference clock (CLP_REFCLK = Capture Clock) Select 0 = CLP_REFCLK 1 = 2 x CLP_REFCLK	
5-0	CLAMP_WID [5:0]	Clamp Pulse Width.(unit 4xCLP_REFCLK = Capture Clock) CLAMP_WID =5, means pulse width being 6 x 4CLP_REFCLK wide.	

Default: 0000 1111B

0x023		Digital Port Input Control	R/W
Bits	Name	Description	
7	YpbPr_EN	YpbPr Input Enable	
6	CLAMP_SOURCE	Clamp source select. 0 = Selects Row Hs to be used for clamping. 1 = Selects Sync Separated Hsync to be used for clamping.	
5	HS_DEJITTER_EN	For TMDS input mode, This bit enables/disable the HSYNC De-jitter	

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		function. 0 = Disable 1 = Enable
4	DEJITTER_RST	For TMDS input mode, De-jitter reset 0 = Normal 1 = Reset
3	HCAP_DE_EN	For TMDS input mode, active data is enclosed by DE signal. Hardware can automatically capture the first data and bypass the setting of capture begin registers (0x034~0x035). This bit is effective if DVI_SYNC_SEL=1 (0x196 bit 7). 0 = According to horizontal capture registers 1 = According to DE signal
2		Reserved
1	DVI_DE_AUTO	DVI DE auto detection control 0: Disable auto DE mode 1: Enable auto DE mode , if input negative DE then invert DE polarity
0	SYNC_SEL	Sync processor input path selection 0: Graphic 1: Video

Default: 0000 0000B

0x024	**Fast Mute Delay**	**R/W**
Bits	Name	Description
7-4	FAST_MUTE_DELAY	While input HS mute , delay this programmable delay time , fast mute enable . “1000” : 1024/Ref.CLK “1100” : 512/Ref.CLK “1110” : 256/Ref.CLK
3-0		Reserved

Default: 0000 0000B

0x025	**ADCLK Delay & Invert Control**	**R/W**
Bits	Name	Description
7		Reserved
6	CLKI_INV	Internal data latch clock invert 0 = Normal 1 = Invert
5-4		Reserved
3-0	CLKI_DLY	Internal data latch clock delay (0.5nS/step) 0~15 step

Default: 0000 0000B

0x026	**Data Delay & Swap Control**	**R/W**
Bits	Name	Description
7	CLAMP_MASK_EN	Clamping pulse mask in V blanking interval 0: Disable 1: Enable
6		Reserved
5	CAP_RB_SWAP	Capture R/B channel swap 0 = Normal 1 = Swap

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4-3		Reserved
2	CAP_BIT_SWAP	Capture data bit swap D7-D0 -> D0-D7 0 = Normal 1 = Swap
1-0		Reserved

Default: 0000 0000B

0x027 ~ 0x29 : Reserved

Mask Window Define

0x02A		**Horizontal Mask Window Begin**	**R/W**
Bits	Name	Description	
7-0	GI_HMASK_BEG [7:0]	Horizontal Mask Window Begin. When GI_MKWIN_EN =1, this register sets the number of clocks after the referenced edge (CR:0x020[3]) of the HSYNC pulse in which the captured data is ‘0x00’ and the auto-tune starts outside this window.	

Default: 0000 0000B

0x02B		**Horizontal Mask Window End**	**R/W**
Bits	Name	Description	
7-0	GI_HMASK_END [7:0]	Horizontal Mask Window End. When GI_MKWIN_EN =1, this register sets the number of clocks before the referenced edge (CR:0x020[3]) of the HSYNC pulse in which the captured data is ‘0x00’ and the auto-tune stops.	

Default: 0000 0000B

0x02C		**Vertical Mask Window Begin**	**R/W**
Bits	Name	Description	
7-0	GI_VMASK_BEG [7:0]	Vertical Mask Window Begin. When GI_MKWIN_EN =1, this register sets the number of lines after the referenced edge (CR:0x020[7]) of the VSYNC pulse in which the captured data is ‘0x00’ and auto-tune starts outside this window.	

Default: 0000 0000B

0x02D		**Vertical Mask Window End**	**R/W**
Bits	Name	Description	
7-0	GI_VMASK_END [7:0]	Vertical Mask Window End. When GI_MKWIN_EN =1, this register sets the number of lines before the referenced edge (CR:0x020[7]) of the VSYNC pulse in which the captured data is ‘0x00’ and the auto-tune stops.	

Default: 0000 0000B

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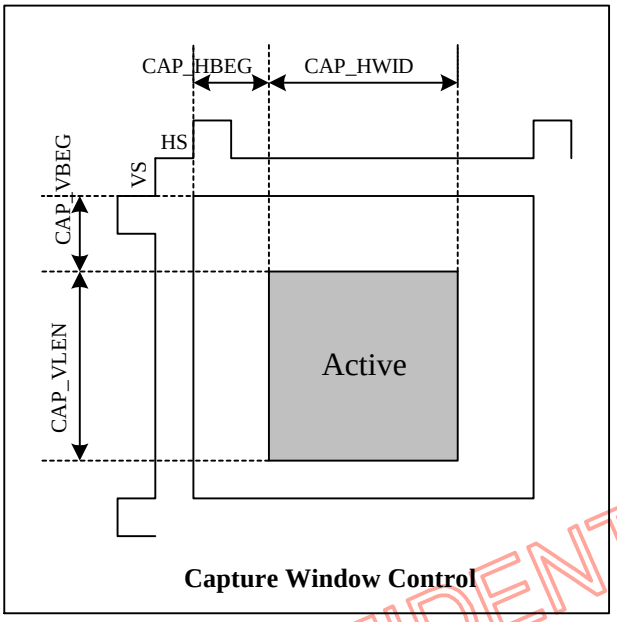

Figure 8.4-1

Capture Window Control

0x02E		Capture Vertical Begin for Odd Field –lo	R/W
Bits	Name	Description	
7-0	GI_CAP_VBEGO [7:0]	Vertical Capture Begin for Odd Field. GI_CAP_VBEGO indicates how many lines to wait after referenced edge (CR:0x020[7]) of VSYNC before starting image capture. GI_CAP_VBEGO =3, means waiting 3 lines to begin capture. This register is double-buffered.	

Default: 0000 0000B

0x02F		Capture Vertical Begin for Odd Field –hi	R/W
Bits	Name	Description	
7-3		Reserved	
2-0	GI_CAP_VBEGO [10:8]	MSB of GI_CAP_VBEGO. This register is double-buffered.	

Default: 0000 0000B

0x030		Capture Vertical Begin for Even Field –lo	R/W
Bits	Name	Description	
7-0	GI_CAP_VBEGE [7:0]	Vertical Capture Begin for Even Field. GI_CAP_VBEGE indicates how many lines to wait after referenced edge (CR:0x020[7]) of VSYNC before starting image capture. GI_CAP_VBEGE =3, means waiting 3 lines to begin capture. This register is double-buffered.	

Default: 0000 0000B

0x031		Capture Vertical Begin for Even Field –hi	R/W
Bits	Name	Description	
7-3		Reserved	
2-0	GI_CAP_VBEGE [10:8]	MSB of GI_CAP_VBEGE. This register is double-buffered.	

Default: 0000 0000B

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0x032		Capture Vertical Length –lo	R/W
Bits	Name	Description	
7-0	GI_CAP_VLEN [7:0]	Vertical Capture Length. GI_CAP_VLEN indicates how many lines to capture. GI_CAP_VLEN = 3, means capturing 3 lines. This register is double-buffered.	

Default: 0000 0000B

0x033		Capture Vertical Length –hi	R/W
Bits	Name	Description	
7-3		Reserved	
2-0	GI_CAP_VLEN [10:8]	MSB of GI_CAP_VLEN. This register is double-buffered.	

Default: 0000 0000B

0x034		Capture Horizontal Begin –lo	R/W
Bits	Name	Description	
7-0	GI_CAP_HBEG [7:0]	Horizontal Capture Begin. GH_CAP_HBEG indicates how many pixels to wait after referenced edge (CR:0x020[3]) of HSYNC before starting image capture. GH_CAP_HBEG =3, means waiting 3 pixels to begin capture. This register is double-buffered.	

Default: 0000 0000B

0x035		Capture Horizontal Begin –hi	R/W
Bits	Name	Description	
7-4		Reserved	
3-0	GI_CAP_HBEG [11:8]	MSB of GI_CAP_HBEG. This register is double-buffered.	

Default: 0000 0000B

0x036		Capture Horizontal Width –lo	R/W
Bits	Name	Description	
7-0	GI_CAP_HWID [7:0]	Horizontal Capture Width. GI_CAP_HWID indicates how many pixels to capture. GI_CAP_HWID = 3, means capturing 3 pixels. This register is double-buffered.	

Default: 0000 0000B

0x037		Capture Horizontal Width –hi	R/W
Bits	Name	Description	
7-4		Reserved	
3-0	GI_CAP_HWID [11:8]	MSB of GI_CAP_HWID. This register is double-buffered.	

Default: 0000 0000B

0x038		Capture CLK Invert	R/W
Bits	Name	Description	
7-5		Reserved	
4		Capture CLK invert	
3-0		Reserved	

Default: 0000 0000B

0x039 ~ 0x3B : Reserved

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0x03C		DVI Input Horizontal Active Width-lo	R
Bits	Name	Description	
7-0	DVI_CAP_HWID [7:0]	The active window horizontal width. The value is valid only for DVI interface is enabled and the SYNC input source is from DVI DE signal	

Default: XXXX XXXXB

0x03D		DVI Input Horizontal Active Width-hi	R
Bits	Name	Description	
3-0	DVI_CAP_HWID [11:8]	MSB of DVI_CAP_HWID	

Default: XXXX XXXXB

0x03E		DVI Input Vertical Active Length-lo	R
Bits	Name	Description	
7-0	DVI_CAP_VLEN [7:0]	The active window vertical length. The value is valid only for DVI interface is enabled and the SYNC input source is from DVI DE signal	

Default: XXXX XXXXB

0x03F		DVI Input Vertical Active Length-hi	R
Bits	Name	Description	
2-0	DVI_CAP_VLEN [10:8]	MSB of DVI_CAP_VLEN	

Default: XXXX XXXXB

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8.5. Video Port Control

General Control

0x040	Video Port Control 1	R/W
Bits	Name	Description
7-5		Reserved
4	UV_SWAP	Swap the order of received UV data. 0 = Normal 1 = Swap
3-2		Reserved
1	VI_INTE_EN	Interlaced input enable 0 = Non-interlaced 1 = Interlaced
0	VI_CAP_EN	Input capture enable 0 = Disabled 1 = Enabled

Default: 0000 0000B

0x041	Video Port Control 2	R/W
Bits	Name	Description
7-6		Reserved
5	VI_CAP_656_AUTO	For BT656 mode, when VI_CAP_656_AUTO = “1”. Hardware referee to the setting of capture registers to capture the active data 0 = Disable 1 = Enable
4	VI_MKWIN_EN	Mask Window Enable. When VI_MKWIN_EN =1, VI_HMASK_BEG, VI_HMASK_END, VI_VMASK_BEG and VI_VMASK_END are used to set the window around the HSYNC and VSYNC during which the captured data is 0x00 and auto tune is disabled. This filters out noise occurring on the RGB channels around the HSYNC and VSYNC pulse. 0 = Disable 1 = Enable
3	VI_WRAP_SEL	Wrap around method select 0 = Wrap around 1 = Wrap black
2	VI_SYNC_EDGE	Select the H/V sync reference edge. 0 = Leading edge 1 = Trailing edge
1	VCAP_656_EN	For BT656 mode, active data is enclosed by SAV/EAV code. Hardware can automatically capture the active data and bypass the setting of capture registers except the Horizontal Capture Width. 0 = According to vertical capture registers 1 = According to SAV/EAV code
0	HCAP_656_EN	For BT656 mode, active data is enclosed by SAV/EAV code. Hardware can automatically capture the active data and bypass the setting of capture registers except the Horizontal Capture Width. 0 = According to horizontal capture registers 1 = According to SAV/EAV code

Default: 0000 0000B

0x042	Polarity Control	R/W

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Bits	Name	Description
7-6		Reserved
5	VI_656CLK_INV	Invert the polarity of CLK for internal BT656 data processing unit 0 = Normal 1 = Invert
4	VI_IFLD_INV	Invert the internal field reference signal for data merging priority 0 = Normal 1 = Invert
3-0		Reserved

Default: 0000 0000B

0x043	VSYNC Delay	R/W
Bits	Name	Description
7-4		Reserved
3-0	VI_VSDLY [3:0]	Delay the video port VSYNC pulse by input pixel clock to avoid the confusion of 1st HSYNC recognized following VSYNC trailing edge. 0~15 pixels delay

Default: 0000 0001B

0x044 ~ 0x46 : Reserved

Mask Window Define

0x047	Horizontal Mask Window Begin	R/W
Bits	Name	Description
7-0	VI_HMASK_BEG [7:0]	Horizontal Mask Window Begin. When VI_MKWIN_EN =1, this register sets the number of clocks after the referenced edge (CR:0x041[2]) of the HSYNC pulse in which the captured data is '0x00' and the auto-tune starts outside this window.

Default: 0000 0000B

0x048	Horizontal Mask Window End	R/W
Bits	Name	Description
7-0	VI_HMASK_END [7:0]	Horizontal Mask Window End. When VI_MKWIN_EN =1, this register sets the number of clocks before the referenced edge (0x041[2]) of the HSYNC pulse in which the captured data is '0x00' and the auto-tune stops.

Default: 0000 0000B

0x049	Vertical Mask Window Begin	R/W
Bits	Name	Description
7-0	VI_VMASK_BEG [7:0]	Vertical Mask Window Begin. When VI_MKWIN_EN =1, this register sets the number of lines after the referenced edge (CR:0x041[2]) of the VSYNC pulse in which the captured data is '0x00' and auto-tune starts outside this window.

Default: 0000 0000B

0x04A	Vertical Mask Window End	R/W
Bits	Name	Description
7-0	VI_VMASK_END [7:0]	Vertical Mask Window End. When VI_MKWIN_EN =1, this register sets the number of lines before the referenced edge (CR:0x041[2]) of the VSYNC pulse in which the captured data is '0x00' and the auto-tune

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		stops.

Default: 0000 0000B

8.6. Color space conversion Control

Color Transfer Equation

R = Y_{601} + COEFA*(Cr-128)/512
G = Y_{601} – COEFB*(Cr-128)/512 – COEFC*(Cb-128)/512
B = Y_{601} + COEFD*(Cb-128)/512

SDTV

R = Y_{601} + 1.371(Cr-128)
G = Y_{601} – 0.698(Cr-128) – 0.336(Cb-128)
B = Y_{601} + 1.732(Cb-128)

HDTV

R = Y_{709} + 1.540(Cr-128)
G = Y_{709} – 0.459(Cr-128) – 0.183(Cb-128)
B = Y_{709} + 1.816(Cb-128)

Color Transfer Coefficient

0x04B		**Color Transfer Coefficient D –lo**	**R/W**
Bits	Name	Description	
7-0	COEFD [7:0]	Video YUV/YpbPr to RGB Color Transfer Coefficient. 0~1023	

Default: 1011 1110B

0x04C		**Color Transfer Coefficient D –hi**	**R/W**
Bits	Name	Description	
7-2		Reserved	
1-0	COEFD [9:8]	MSB of COEFD	

Default: 0000 0010B

0x04D		**Color Transfer Coefficient C –lo**	**R/W**
Bits	Name	Description	
7-0	COEFC [7:0]	Video YUV/YpbPr to RGB Color Transfer Coefficient. 0~1023	

Default: 0110 0101B

0x04E		**Color Transfer Coefficient C –hi**	**R/W**
Bits	Name	Description	
1-0	COEFC [9:8]	MSB of COEFC	

Default: 0000 0001B

0x04F		**Color Transfer Coefficient B –lo**	**R/W**
Bits	Name	Description	
7-0	COEFB [7:0]	Video YUV/YpbPr to RGB Color Transfer Coefficient. 0~1023	

Default: 1010 1100B

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0x050		Color Transfer Coefficient B –hi	R/W
Bits	Name	Description	
1-0	COEFB [9:8]	MSB of COEFB	

Default: 0000 0000B

0x051		Color Transfer Coefficient A –lo	R/W
Bits	Name	Description	
7-0	COEFA [7:0]	Video YUV/YpbPr to RGB Color Transfer Coefficient. 0~1023	

Default: 0111 0111B

0x052		Color Transfer Coefficient A –hi	R/W
Bits	Name	Description	
1-0	COEFA [9:8]	MSB of COEFA	

Default: 0000 0011B

8.7. Video Port Capture Control

Capture Window Control

0x053		Vertical Capture Begin for Odd Field –lo	R/W
Bits	Name	Description	
7-0	VI_CAP_VBEGO [7:0]	ODD Field Vertical Capture Begin. VI_CAP_VBEGO indicates how many lines to wait after referenced edge (CR:0x041[2]) of VSYNC before starting image capture. VI_CAP_VBEGO =3, means waiting 3 lines to begin capture. **This register is double-buffered.**	

Default: 0000 0000B

0x054		Vertical Capture Begin for Odd Field –hi	R/W
Bits	Name	Description	
2-0	VI_CAP_VBEGO [10:8]	MSB of VI_CAP_BEG. **This register is double-buffered.**	

Default: 0000 0000B

0x055		Vertical Capture Begin for Even Field –lo	R/W
Bits	Name	Description	
7-0	VI_CAP_VBEGE [7:0]	Even Field Vertical Capture Begin. VI_CAP_VBEGE indicates how many lines to wait after referenced edge (CR:0x041[2]) of VSYNC before starting image capture. VI_CAP_VBEGE =3, means waiting 3 lines to begin capture. **This register is double-buffered.**	

Default: 0000 0000B

0x056		Vertical Capture Begin for Even Field –hi	R/W
Bits	Name	Description	
2-0	VI_CAP_VBEGE [10:8]	MSB of VI_CAP_VBEGE. **This register is double-buffered.**	

Default: 0000 0000B

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0x057	Vertical Capture Length –lo	R/W
Bits	Name	Description
7-0	VI_CAP_VLEN [7:0]	Vertical Capture Length. VI_CAP_VLEN indicates how many lines to capture. VI_CAP_VLEN =3, means capturing 3 lines. **This register is double-buffered.**

Default: 0000 0000B

0x058	Vertical Capture Length –hi	R/W
Bits	Name	Description
2-0	VI_CAP_VLEN [10:8]	MSB of VI_CAP_VLEN. **This register is double-buffered.**

Default: 0000 0000B

0x059	Horizontal Capture Begin –lo	R/W
Bits	Name	Description
7-0	VI_CAP_HBEG [7:0]	Horizontal Capture Begin. VI_CAP_HBEG indicates how many pixels to wait after referenced edge (CR:0x041[2]) of HSYNC before starting image capture. VI_CAP_HBEG =3, means waiting 3 pixels to begin capture. **This register is double-buffered.**

Default: 0000 0000B

0x05A	Horizontal Capture Begin –hi	R/W
Bits	Name	Description
3-0	VI_CAP_HBEG [11:8]	MSB of VI_CAP_HBEG. **This register is double-buffered.**

Default: 0000 0000B

0x05B	Horizontal Capture Width –lo	R/W
Bits	Name	Description
7-0	VI_CAP_HWID [7:0]	Horizontal Capture Width. VI_CAP_HWID indicates how many pixels to capture. VI_CAP_HWID = 3, means capturing 3 pixels. **This register is double-buffered.**

Default: 0000 0000B

0x05C	Horizontal Capture Width –hi	R/W
Bits	Name	Description
3-0	VI_CAP_HWID [11:8]	MSB of VI_CAP_HWID **This register is double-buffered.**

Default: 0000 0000B

0x05D ~ 0x5F : Reserved

8.8. Back End Image Processing

- Back-end offset control
- Back-end gain control
- Back-end sharpness and smooth control

0x060	Back-end Horizontal Sharpness	R/W
Bits	Name	Description
7		Reserved

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6	BK_H_ASRP	Graphic horizontal adaptive sharpness adjusting. 0 = Disable 1 = Enable
5		Reserved
4	BK_H_SRPSMO	Graphic horizontal back-end smooth and sharpness select. 0 = sharpness 1 = smooth
3-0	BK_H_SRP [3:0]	Graphic horizontal back-end sharpness/smooth adjusting. 16 steps

Default: 0000 0000B

0x061 : Reserved

0x062	Gamma Fixed Bit	R/W
Bits	Name	Description
7-6		Reserved
5-4 3-2 1-0		B[1:0] fixed “00” , “01” , “10” , “11” G[1:0] fixed “00” , “01” , “10” , “11” R[1:0] fixed “00” , “01” , “10” , “11”

Default: 0000 0000B

0x063	Gamma Fixed Bit Enable	R/W
Bits	Name	Description
7-3		Reserved
2 1 0		B enable , gamma disable or gamma 10 bit out [1:0] = “00” G enable , R enable

Default: 0000 0000B

0x064	Interpolation Control	R/W
Bits	Name	Description
7-5	TEXT_EN [2:0]	Select the Text Mode type 000 = Normal Mode 001 = Level 1 Text Mode 010 = Level 2 Text Mode 011 = Level 3 Text Mode 1xx = Reserved
4-3	V_INTE_TYPE [1:0]	Select the Vertical interpolation type 00 = DSP (2-pixel) 01 = Bi-linear (2-pixel) 10 = Duplicate (2-pixel) 11 = Reserved
2-0	H_INTE_TYPE [2:0]	Select the Horizontal interpolation type 000 = Advanced DSP (4-pixel) 001 = Bi-linear (2-pixel) 010 = Duplicate (2-pixel) 011 = DSP (2-pixel) 100 = DSP (4-pixel) 101, 110, 111 = Reserved

Default: 0000 0000B

0x065	Gamma Control	R/W

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Bits	Name	Description
7	GAMMA_EN	Gamma Table Enable, When GAMMA_EN = 1, the Gamma Table can't read or write by host interface. When GAMMA_EN = 0 the display is bypass the Gamma table. 0 = Disable 1 = Enable
6-0		Reserved

Default: 0000 0000B

0x066	Back-end Vertical Sharpness	R/W
Bits	Name	Description
7-3		Reserved
2-0	INT_V_SHARP [2:0]	Vertical interpolation sharpness adjusting 8 steps

Default: 0000 0000B

0x067 : Reserved

8.9. Noise Reduction Filter Control

0x068	Noise Reduction Filter Control	R/W
Bits	Name	Description
7		Reserved
6	NR2_EN	Second Noise Reduction enable , NR2_THR[3:0] (CR: 0x06B) adjust the threshold (NR_TYPE = "001" , "010" , "011") 0 = Disable 1 = Enable
5	NR_ROUND	Noise Reduction round calculation enable (NR_TYPE = "001" , "010" , "011") 0 = Disable 1 = Enable
4	NR_EDGE_DET	Noise Reduction edge detection enable , NR_EDGE_THR[3:0] (0x069) adjust the threshold (NR_TYPE = "001" , "010" , "011") 0 = Disable 1 = Enable
3		Reserved
2-0	NR_TYPE	Select the Noise Reduction Filter type 000 = Normal Mode (NR disable) 001 = Mode 1 010 = Mode 2 011 = Mode 3 , NR_THR[3:0] (0x069) adjust the threshold 1xx = Reserved

Default: 0000 0000B

0x069	Noise Reduction threshold	R/W
Bits	Name	Description
7-4	NR_EDGE_THR [3:0]	Edge Threshold of the noise reduction filter adjusting. 0x068[4] must be set "1"
3-0	NR_THR [3:0]	Threshold of the noise reduction filter adjusting. 0x068[2:0] must be set "001" or "010" or "011"

Default: 0000 0000B

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0x06A	ADC High Pass Filter	R/W
Bits	Name	Description
7-6		Reserved
5	NR_DITHER _RST	NR random dither reset mode (0x06B.4 NR_DITHER must set random mode) 0 = Disable 1 = Enable
4	ADC_HPASS_EN	ADC high pass filter 0 = Disable 1 = Enable
3		Reserved
2-0	ADC_HPASS [2:0]	ADC high pass filter level

Default: 0000 0000B

0x06B	Seconded Noise Reduction threshold	R/W
Bits	Name	Description
7-6		Reserved
5	GHOST_CANCEL	Ghost cancellation 0 = Disable 1 = Enable
4	NR_DITHER	NR dither mode : 0: Order mode 1: Random mode
3-0	NR2_THR [3:0]	Threshold of the seconded noise reduction filter adjusting. CR: 0x068[6] must be set “1”

Default: 0000 0000B

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0x06C : Reserved

0x06D	NR Reset Dither Frame Invert	R/W
Bits	Name	Description
7-6		Reserved
5-4	NR_RST_INV	NR dither reset mode frame invert count 00: 1 frame 01: 2 frame 10: 3 frame 11: 4 frame
3-1		Reserved
0	NR_RST_INV	NR dither reset mode frame invert enable

Default: 0000 0000B

0x06E ~ 0x6F : Reserved

8.10. General Purpose Input Output (GPIO)

0x070	GPIO Port Control	R/W
Bits	Name	Description
5	PWMA_EN	PWMA output enable (open-drain) 0 = Disable 1 = PWMA Enable

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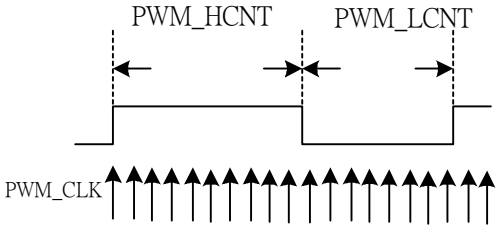
4	PWMB_EN	PWMB output enable (open-drain) 0 = Disable 1 = PWMB Enable
3-0		Reserved

Default: 0000 0000B

0x071 ~ 0x073 : Reserved

8.11. PWM Output

- Frequency programmable
- Duty cycle programmable



When clock source select from reference clock

$$F_{PWM_CLK} = F_{REFCLK} / (PWM_DIV\ 1 \times PWM_DIV\ 2)$$

When clock source select from Display Hsync

$$F_{PWM_CLK} = F_{DISP_HS} / (PWM_DIV\ 1 \times PWM_DIV\ 2)$$

$$F_{PWM} = \frac{F_{PWM_CLK}}{(PWM_HCNT + PWM_LCNT)}$$

$$Duty = \frac{PWM_HCNT}{(PWM_HCNT + PWM_LCNT)}$$

$$PWM_HCNT = \frac{Duty \times F_{PWM_CLK}}{F_{PWM}}$$

$$PWM_LCNT = \frac{(1 - Duty) \times F_{PWM_CLK}}{F_{PWM}}$$

PWM_HCNT	PWM_LCNT	PWM Output
0	0	Tri-state
0	1~255	DC '0'
1~255	0	DC '1'
1~255	1~255	PWM pulse

0x074	PWMB Low Period Counter	R/W
Bits	Name	Description
7-0	PWMB_LCNT [7:0]	PWMB pulse low period counter value. Count with 12M or display HS Double-buffered.

Default: 0000 0000B

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0x075	PWMB High Period Counter	R/W
Bits	Name	Description
7-0	PWMB_HCNT [7:0]	PWMB pulse high period counter value. Count with 12M or display HS Double-buffered.

Default: 0000 0000B

0x076	PWMA Low Period Counter	R/W
Bits	Name	Description
7-0	PWMA_LCNT [7:0]	PWMA pulse low period counter value. Count with 12M or display HS Double-buffered.

Default: 0000 0000B

0x077	PWMA High Period Counter	R/W
Bits	Name	Description
7-0	PWMA_HCNT [7:0]	PWMA pulse high period counter value. Count with 12M or display HS Double-buffered.

Default: 0000 0000B

0x078 ~ 0x7D : Reserved

0x07E	PWM Control 1	R/W
Bits	Name	Description
7	PWMA_VS_LOCK	PWMA counter lock to display vertical sync 0 = Roll PWM counter over continuously 1 = Load PWM on Display VS (DISP_VS) leading edge
6-5	PWMA_DIV1 [1:0]	First divider–PWMA clock divide of the selected clock by 00 = 1; 01 = 2; 10 = 4; 11 = 8
4	PWMA_CLK	PWMA clock source select 0 = Reference Clock 1 = Display HS (DISP_HS)
3	PWMB_VS_LOCK	PWMB counter lock to display vertical sync 0 = Roll PWM counter over continuously 1 = Load PWM on Display VS (DISP_VS) leading edge
2-1	PWMB_DIV1 [1:0]	First divider–PWMB clock divide of the selected clock by 00 = 1; 01 = 2; 10 = 4; 11 = 8
0	PWMB_CLK	PWMB clock source select 0 = Reference Clock 1 = Display HS (DISP_HS)

Default: 0000 0000B

0x07F	PWM Control 2	R/W
Bits	Name	Description
7	PWMA_VSRESET	PWMA reset counter on DSIP_VS leading edge 0 = Roll PWMA counter over continuously 1 = Reset PWMA on DISP_VS leading edge
6	PWMB_VSRESET	PWMB reset counter on DSIP_VS leading edge 0 = Roll PWMB counter over continuously 1 = Reset PWMB on DISP_VS leading edge
5-4		Reserved

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3-2	PWMA_ DIV2	Second divider–PWMA clock divide of the selected clock by 00 = 1; 01 = 16 10 = 256; 11 = 4096
1-0	PWMB_DIV2 [1:0]	Second divider–PWMB clock divide of the selected clock by 00 = 1; 01 = 16 10 = 256; 11 = 4096

Default: 0000 0000B

8.12. On Screen Display Registers

OSD Control

0x080	**OSD and Window Enable Control**	**R/W**
Bits	Name	Description
7	ROT_EN	Rotation control. 0: Normal 1: Rotated
6	FLIP_EN	Flip control 0: No flip 1: Flip ON
5	MIR_EN	Mirror control 0: No mirror 1: Mirror ON
4	WIN4_EN	Enable Window 4 0: Disable 1: Enable
3	WIN3_EN	Enable Window 3 0: Disable 1: Enable
2	WIN2_EN	Enable Window 2 0: Disable 1: Enable
1	WIN1_EN	Enable Window 1 0: Disable 1: Enable
0	OSD_EN	Enable OSD 0: Disable 1: Enable

Default: 0000 0000B

0x081	**OSD Frame Horizontal Start – Low byte**	**R/W**
Bits	Name	Description
7-0	OSD_HS [7:0]	OSD frame horizontal start low byte [7:0]. Specifies the horizontal starting position of the OSD in pixel units. This register is **double-buffered**.

Default: 0000 0000B

0x082	**OSD Frame Horizontal Start – High Byte**	**R/W**
Bits	Name	Description
7-4		Reserved
3-0	OSD_HS [11:8]	OSD frame horizontal start high byte [11:8]. Specifies the horizontal starting position of the OSD in pixel units. This register is **double-buffered**.

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Default: 0000 0000B

0x083		OSD Frame Horizontal Width	R/W
Bits	Name	Description	
7		Reserved	
5-0	OSD_HW [5:0]	Specifies the width of the OSD in font units. Range: 0~ 63 (OSD display width = 1~64)	

Default: 0000 0000B

0x084		OSD Frame Vertical Start Low byte	R/W
Bits	Name	Description	
7-0	OSD_VS [7:0]	OSD frame vertical start low byte [7:0]. Specifies the vertical starting position of the OSD in line units. This register is **double-buffered**.	

Default: 0000 0000B

0x085		OSD Frame Vertical Start High byte	R/W
Bits	Name	Description	
7-3		Reserved	
2-0	OSD_VS [10:8]	OSD frame vertical start high byte [10:8]. Specifies the vertical starting position of the OSD in line units. This register is **double-buffered**.	

Default: 0000 0101B

0x086		OSD Frame Vertical Height	R/W
Bits	Name	Description	
7-5		Reserved	
4-0	OSD_VH [4:0]	Specifies the height of the OSD in font units. Range: 0~31 (OSD display height = 1~32)	

Default: 0000 0000B

0x087		OSD Shift Row Offset	R/W
Bits	Name	Description	
4-0	OSD_SHIFT_ROW	Specifies the row of the OSD shift offset. Top row will shift to bottom and like rolling function . Range: 0~31	

Default: 0000 0000B

0x088		OSD One Bit Font Address – Low Byte	R/W
Bits	Name	Description	
7-0	FONT1B_ADDR [7:0]	OSD one bit per pixel programmable font start address high byte [7:0]. Specifies the start address for the On-Chip programmable font. Default for this 12 bit register = 1000 (dec)	

Default: 1110 1000B

0x089		OSD One bit Font Address – High Byte	R/W
Bits	Name	Description	
3-0	FONT1B_ADDR [11:8]	OSD one bit per pixel programmable font start address high byte [11:8]. Specifies the start address for the On-Chip programmable font Default for this 12 bit register = 1000 (dec)	

Default: 0000 0011B

0x08A		OSD Two Bit Font Address – Low Byte	R/W

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Bits	Name	Description
7-0	FONT2B_ADDR [7:0]	OSD two bit per pixel programmable font start address high byte [7:0]. Specifies the start address for the On-Chip programmable font. Default for this 12 bit register = 2656 (dec)

Default: 0110 0000B

0x08B	OSD Two Bit Font Address – High Byte	R/W
Bits	Name	Description
3-0	FONT2B_ADDR [11:8]	OSD two bit per pixel programmable font start address high byte [11:8]. Specifies the start address for the On-Chip programmable font Default for this 12 bit register = 2656 (dec)

Default: 0000 1010B

0x08C	OSD Three/Four Bit Font Address – Low Byte	R/W
Bits	Name	Description
7-0	FONT4B_ADDR [7:0]	OSD three/four bit per pixel programmable font start address high byte [7:0]. Specifies the start address for the On-Chip programmable font. If 0x09F[7] = “1” , this register for three bit font address low byte Default for this 12 bit register = 3808 (dec)

Default: 1110 0000B

0x08D	OSD Three/Four Bit Font Address – High Byte	R/W
Bits	Name	Description
3-0	FONT4B_ADDR [11:8]	OSD three/four bit per pixel programmable font start address high byte [11:8]. Specifies the start address for the On-Chip programmable font If 0x09F[7] = “1”, this register for three bit font address high byte Default for this 12 bit register = 3808 (dec)

Default: 0000 1110B

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OSD Fade in/out Control

0x08E	OSD Fade-in / Fade-out Step	R/W
Bits	Name	Description
7-4	FAD_V_STEP [3:0]	OSD Vertical side Fade-in / Fade-out Step (4 pixel/step) 0~15 step
3-0	FAD_H_STEP [3:0]	OSD Horizontal side Fade-in / Fade-out Step (4 pixel/step) 0~15 step

Default: 0000 0000B

0x08F	OSD Fade-in / Fade-out Frequency	R/W
Bits	Name	Description
7	FAD_EN	Fade-in / Fade-out function enable. 0: Fade-in / Fade-out disable 1: Fade-in / Fade-out enable
6-4	FAD_VFREQ [2:0]	OSD Fade-in / Fade-out Vertical Frequency for every step (4 frame/step)
3-0	FAD_HFREQ [3:0]	OSD Fade-in / Fade-out Horizontal Frequency for every step (4 frame/step)

Default: 0000 0000B

OSD Zoom Control

0x090	OSD Zoom Control for Separate Row Control Disable	R/W

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Bits	Name	Description
7-4		Reserved
3	VROW_ZMEN	Vertical Row Zoom Enable; Vertical zoom for all characters in one row defined in Reg 0x09A ~ 0x09D. 0: Disable 1: Enable.
2	HROW_ZMEN	Horizontal Row Zoom Enable; Horizontal zoom for all characters in one row defined in Reg 0x096 ~ 0x099. 0: Disable 1: Enable.
1	VGLOB_ZMEN	Vertical Global Zoom Enable; Vertical zoom for all characters in OSD frame. 0: Disable 1: Enable.
0	HGLOB_ZMEN	Horizontal Global Zoom Enable; Horizontal zoom for all characters in OSD frame. 0: Disable 1: Enable.

Default: 0000 0000B

0x090		**OSD Zoom Control for Separate Row Control Enable**	**R/W**
Bits	Name	Description	
7-6	ROW_V_ZMRNG1 [1:0]	Row zoom range This is a user definable zoom pattern. Pixels with '1' pattern that define at 0x092 ~ 0x094 are duplicated according to the zoom range.	
5-4	ROW_V_ZMRNG0 [1:0]	Row zoom range This is a user definable zoom pattern. Pixels with '0' pattern that define at 0x092 ~ 0x094 are duplicated according to the zoom range.	
3-1	ROW_SPACE	Separate Row vertical space , the row select at 0x09F[4:0]	
0	HGLOB_ZMEN	Row vertical zoom 0: Disable 1: Enable.	

Default: 0000 0000B

0x091		**OSD Font Horizontal Global Zoom Pattern – Low Byte**	**R/W**
Bits	Name	Description	
7-0	HZM_PATN [7:0]	Least significant 8 bits (7:0) of the horizontal zoom pattern. This is a user definable zoom pattern. Pixels with '1' pattern are duplicated according to the zoom range.	

Default: 0000 0000B

0x092		**OSD Font Horizontal/Vertical Global Zoom Pattern – High Byte**	**R/W**
Bits	Name	Description	
7-6		Reserved	
5-4	VZM_PATN [17:16]	Most significant 2 bits (17:16) of the vertical zoom pattern. This is a user definable zoom pattern. Pixels with '1' pattern are duplicated according to the zoom range.	
3-0	HZM_PATN [11:8]	Most significant 4 bits (11:8) of the horizontal zoom pattern. This is a user definable zoom pattern. Pixels with '1' pattern are duplicated according to the zoom range.	

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Default: 0000 0000B

0x093		OSD Font Vertical Global Zoom Pattern – Low Byte	R/W
Bits	Name	Description	
7-0	VZM_PATN [7:0]	Least significant 8 bits (7:0) of the vertical zoom pattern. This is a user definable zoom pattern. Pixels with '1' pattern are duplicated according to the zoom range.	

Default: 0000 0000B

0x094		OSD Font Vertical Global Zoom Pattern – Mid Byte	R/W
Bits	Name	Description	
7-0	VZM_PATN [15:8]	Bits (15:8) of the vertical zoom pattern. This is a user definable zoom pattern. Pixels with '1' pattern are duplicated according to the zoom range.	

Default: 0000 0000B

0x095		OSD Font Global Zoom Range	R/W
Bits	Name	Description	
7-6	VGLOB_ZMRNG1 [1:0]	Vertical Global Zoom Pattern (Reg 0x092 ~ 0x094) '1' Zoom Range 00: No Zoom 01: Vertical Zoom Pattern '1' bits are duplicated once 10: Vertical Zoom Pattern '1' bits are duplicated twice 11: Vertical Zoom Pattern '1' bits are duplicated three times	
5-4	HGLOB_ZMRNG1 [1:0]	Horizontal Global Zoom Pattern (Reg 0x091 ~ 0x092) '1' Zoom Range 00: No Zoom 01: Horizontal Zoom Pattern '1' bits are duplicated once 10: Horizontal Zoom Pattern '1' bits are duplicated twice 11: Horizontal Zoom Pattern '1' bits are duplicated three times	
3-2	VGLOB_ZMRNG0 [1:0]	Vertical Global Zoom Pattern (Reg 0x092 ~ 0x094) '0' Zoom Range 00: No Zoom 01: Vertical Zoom Pattern '0' bits are duplicated once 10: Vertical Zoom Pattern '0' bits are duplicated twice. 11: Vertical Zoom Pattern '0' bits are duplicated three times.	
1-0	HGLOB_ZMRNG0 [1:0]	Horizontal Global Zoom Pattern (Reg 0x091 ~ 0x092) '0' Zoom Range 00: No Zoom 01: Horizontal Zoom Pattern '0' bits are duplicated once 10: Horizontal Zoom Pattern '0' bits are duplicated twice 11: Horizontal Zoom Pattern '0' bits are duplicated three times	

Default: 0000 0000B

0x096		Horizontal Row Zoom Control Row 7 – 0	R/W
Bits	Name	Description	
7-0	HROW_ZMPN [7:0]	Horizontal Row Zoom Pattern 7-0 Zooms each row horizontally defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg 0x090 [2] must be set to '1'.	

Default: 0000 0000B

0x097		Horizontal Row Zoom Control Row 15 – 8	R/W
Bits	Name	Description	
7-0	HROW_ZMPN [15:8]	Horizontal Row Zoom Pattern 15-8 Zooms each row horizontally defined as zoom range according to each bit.	

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		Each bit controls a row correspondingly. Reg 0x090 [2] must be set to '1'.

Default: 0000 0000B

0x098		Horizontal Row Zoom Control Row 23 – 16	R/W
Bits	Name	Description	
7-0	HROW_ZMPN [23:16]	Horizontal Row Zoom Pattern 23-16 Zooms each row horizontally defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg 0x090 [2] must be set to '1'.	

Default: 0000 0000B

0x099		Horizontal Row Zoom Control Row 31 – 24	R/W
Bits	Name	Description	
7-0	HROW_ZMPN [31:24]	Horizontal Row Zoom Pattern 31-24 Zooms each row horizontally defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg 0x090 [2] must be set to '1'.	

Default: 0000 0000B

0x09A		Vertical Row Zoom Control Row 7 – 0	R/W
Bits	Name	Description	
7-0	VROW_ZMPN [7:0]	Vertical Row Zoom Pattern 7-0 Zooms each row vertically defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg 0x090 [3] must be set to '1'.	

Default: 0000 0000B

0x09B		Vertical Row Zoom Control Row 15 – 8	R/W
Bits	Name	Description	
7-0	VROW_ZMPN [15:8]	Vertical Row Zoom Pattern 15-8 Zooms each row vertically defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg 0x090 [3] must be set to '1'.	

Default: 0000 0000B

0x09C		Vertical Row Zoom Control Row 23 – 16	R/W
Bits	Name	Description	
7-0	VROW_ZMPN [23:16]	Vertical Row Zoom Pattern 23-16 Zooms each row vertically defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg 0x090 [3] must be set to '1'.	

Default: 0000 0000B

0x09D		Vertical Row Zoom Control Row 31 – 24	R/W
Bits	Name	Description	
7-0	VROW_ZMPN [31:24]	Vertical Row Zoom Pattern 31-24 Zooms each row vertically defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg 0x090 [3] must be set to '1'.	

Default: 0000 0000B

0x09E		OSD Font Row Zoom Range	R/W
Bits	Name	Description	
7-4		Reserved	
3-2	VROW_ZMRNG [1:0]	Vertical Row Zoom Range; The rows assigned by Vertical Row Zoom Control registers will be zoomed up. 00: Vertical Zoom 1x for all fonts in the row	

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		01: Vertical Zoom 2x for all fonts in the row 10: Vertical Zoom 3x for all fonts in the row 11: Vertical Zoom 4x for all fonts in the row
1-0	HROW_ZMRNG [1:0]	Horizontal Row Zoom Range; The rows assigned by Horizontal Row Zoom Control registers will be zoomed up. 00: Horizontal Zoom 1x for all fonts in the row 01: Horizontal Zoom 2x for all fonts in the row 10: Horizontal Zoom 3x for all fonts in the row 11: Horizontal Zoom 4x for all fonts in the row

Default: 0000 0000B

0x09F		Separate ROW Control	R/W
Bits	Name	Description	
7	Three_BIT_FONT	Three bit font 0: Disable 1: Enable	
6	SEPARATE_ROW_EN	32 separat row control 0: Disable 1: Enable	
5	ROW_ACCESS	Row access 0: Disable 1: Enable	
4-0	ROW_SELECT	32 row select	

Default: 0000 0000B

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OSD Translucent and Blinking Control

0x0A0		OSD Blink Control	R/W
Bits	Name	Description	
7		Reserved	
6	OSD_BLINK	Blink 0=Blink control from font attribute bit 0. 1=OSD frame blink enable, don't care the attribute bit 0.	
5	BS_BLINK	Mask Border/Shadow at Blink 0= Character border/shadow will blink with the foreground of the character. 1=Character border/shadow will not blink with the foreground of the character.	
4-2	BLINK_FREQ [2:0]	Blink Frequency 000: Character foreground's blinking period is 4 frames. 001: Character foreground's blinking period is 8 frames. 010: Character foreground's blinking period is 16 frames. 011: Character foreground's blinking period is 32 frames. 100: Character foreground's blinking period is 64 frames.	
1-0	BLINK_RATE [1:0]	Blink Rate 00: Character foreground is turned 25% on / 75% off. 01: Character foreground is turned 50% on / 50% off. 10: Character foreground is turned 75% on / 25% off. 11: Reserved.	

Default: 0000 0001B

0x0A1		OSD Character Translucent Level	R/W
Bits	Name	Description	
7-6		Reserved	

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5-3	TP_LEVEL_TWO [2:0]	When the attribute BG_Index is set to ”0001”, these 3-bits set the translucent level of the character background color. Translucent level refers to the percentage of color composition that is OSD. “111” = 0% “110” = 12.25% “101” = 25% “100” = 37.5% “011” = 50% “010” = 62.5% “001” = 75% “000” = 87.5%
2-0	TP_LEVEL_ONE [2:0]	When the attribute BG_Index is set to “0000” ~ “1111” except “0001”, these 3-bits set the translucent level of the character background color. Translucent level refers to the percentage of color composition that is OSD. “111” = 0% “110” = 12.25% “101” = 25% “100” = 37.5% “011” = 50% “010” = 62.5% “001” = 75% “000” = 87.5%

Default: 0000 0000B

OSD Spacing Control

0x0A2	**OSD Space**	**R/W**
Bits	Name	Description
7	V_FS_SEL	Vertical Font size selection 0: 18 font size for Vertical 1: 16 font size for Vertical
6	H_FS_SEL	Horizontal Font size selection 0: 12 font size selected for Horizontal 1: 10 font size selected for Horizontal
5-3	VSPACE [2:0]	OSD vertical space. These 3 bits define the vertical scan pixel of background color added to above and below of each character. Range: 0~7
2-0	HSPACE [2:0]	OSD horizontal space. These 3 bits define the horizontal scan pixel of background color added to left and right of each character. Range: 0~7

Default: 0000 0000B

0x0A3	**OSD Window/Font Gradient Control – 1**	**R/W**
Bits	Name	Description
7	GRD_B_POL	Windrow/Font gradient Blue polarity 0: Increase 1: Decrease
6	GRD_G_POL	Windrow/Font gradient Green polarity 0: Increase 1: Decrease
5	GRD_R_POL	Windrow/Font gradient Red polarity 0: Increase 1: Decrease
4	GRD_DIRECT	Windrow gradient direction 0: Horizontal direction 1: Vertical direction
3	GRD_B_EN	Windrow gradient Blue 0: Disable 1: Enable

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2	GRD_G_EN	Windrow gradient Green 0: Disable 1: Enable
1	GRD_R_EN	Windrow gradient Red 0: Disable 1: Enable
0	WIN_GRD_EN	Windrow gradient , the palette index define at 0x0AB 0: Background gradient enable 1: Foreground gradient enable

Default: 0000 0000B

0x0A4	**OSD Window Gradient Control -2**	**R/W**
Bits	Name	Description
7-4	WIN_GRD_STEP	Window gradient step , define decrease or increase level each step
3-0	WIN_GRD_PIX	Window gradient pixel , define how many pixel decrease or increase level each step

Default: 0000 0000B

OSD Window Control

0x0A5	**OSD Window Select**	**R/W**
Bits	Name	Description
7	WIN8_EN	Enable Window 8 0: Disable 1: Enable
6	WIN7_EN	Enable Window 7 0: Disable 1: Enable
5	WIN6_EN	Enable Window 6 0: Disable 1: Enable
4	WIN5_EN	Enable Window 5 0: Disable 1: Enable
3		Reserved
2-0	WIN_SEL [2:0]	This register is used to select which window is to be accessed or modified. It is programmed prior to accessing the registers Reg 0x0A6h ~ 0x0Afh “000” = Window1 “001” = Window2 “010” = Window3 “011” = Window4 “100” = Window5 “101” = Window6 “110” = Window7 “111” = Window8

Default: 0000 0000B

0x0A6	**OSD Window Horizontal Start**	**R/W**
Bits	Name	Description
7-6		Reserved
5-0	WIN_HS [5:0]	Horizontal starting position relative to the OSD for the selected window. The unit is in font. Range: 0~63

Default: 0000 0000B

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0x0A7		OSD Window Horizontal End	R/W
Bits	Name	Description	
7-6		Reserved	
5-0	WIN_HE [5:0]	Horizontal ending position relative to the OSD for the selected window. The unit is in font. The OSD Window Horizontal Width = (WIN_HE+1) – WIN_HS Range: 0~63	

Default: 0000 0000B

0x0A8		OSD Window Vertical Start	R/W
Bits	Name	Description	
4-0	WIN_VS [4:0]	Vertical starting position relative to the OSD for the selected window. The unit is in font. Range: 0~31	

Default: 0000 0000B

0x0A9		OSD Window Vertical End	R/W
Bits	Name	Description	
7-5		Reserved	
4-0	WIN_VE [4:0]	Vertical ending position relative to the OSD for the selected window. The unit is in font. The OSD Window 1 Vertical Height = (WIN1_VE+1) – WIN1_VS Range: 0~31	

Default: 0000 0000B

0x0AA		OSD Window Attribute	R/W
Bits	Name	Description	
7	WIN_BLEN	Window bevel enable Bevel size is specified in 0x0AD[2:0] : WIN_BL_WIDTH	
6-5	WIN_BL_TYPE	Window bevel type 00:Type1,Left/Bottom color define at 0x0AF,Right/Top color define at 0x0AC or 0x0AE 01:Type2,Left/Top color define at 0x0AF,Right/Bottom color define at 0x0AC or 0x0AE 10:Type3,Top/Bottom color define at 0x0AF,Left/Right color define at 0x0AC or 0x0AE 11:Reserved	
4	WIN_MIX	Window translucent enable for the selected window 0 – Normal 1 – Translucent ((1- TP_LEVEL_ONE) * Display + (TP_LEVEL_ONE) * OSD_BG)	
3-2	WIN_SDSZ [1:0]	Shadow Size for the selected window when window shadow enable 00: 2 pixels in width and 2 lines in height. 01: 4 pixels in width and 4 lines in height. 10: 6 pixels in width and 6 lines in height. 11: 8 pixels in width and 8 lines in height.	
1	WIN_SDEN	Window Shadow Enable for the selected window Shadow size is specified in bits 3:2. 1= Shows a shadow for Window. 0= No shadow	

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0	WIN_FADE	Window gradient fade in/out 0: Disable 1: Enable

Default: 0000 0000B

0x0AB		OSD Window Color	R/W
Bits	Name	Description	
7-0	WIN_CL [7:0]	Color index for the selected OSD Window. This color will cover the character background color when Window is enabled.	

Default: 0000 0000B

0x0AC		OSD Gradient Font Color	R/W
Bits	Name	Description	
7-0	GRAD_COLOR [7:0]	Color index for foreground gradient color	

Default: 0000 0000B

	0x0AB	0x0AC	0x0AE	0x0AF
Gradient Disable	Window Color	X	Bevel top/right side , shadow color	Bevel bottom/left side color
Background Gradient	Window Color	X	Bevel top/right side , shadow color	Bevel bottom/left side color
Foreground Gradient	Window Color	Font Color	Bevel top/right side , shadow color	Bevel bottom/left side color

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0x0AD		OSD Window Bevel Width	R/W
Bits	Name	Description	
7-3	WIN_FADE_SPEED	Window gradient fade in/out speed , based on VS count	
2-0	WIN_BL_WIDTH [2:0]	Specifies the width of the window bevel units. Range: 1~8 , units : pixel	

Default: 0000 0000B

0x0AE		OSD Window Bevel Right / Shadow Color	R/W
Bits	Name	Description	
7-0	WIN_BL_RCL [7:0]	Color index for all eight window's top/right side bevel and shadow	

Default: 0000 0000B

0x0AF		OSD Window Bevel Left Color	R/W
Bits	Name	Description	
7-0	WIN_BL_LCL [7:0]	Color index for all eight window's bottom/left side bevel	

Default: 0000 0000B

OSD Border And Shadow Control

0x0B0	OSD Shadow Control Row 7 – 0	R/W

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Bits	Name	Description
7-0	OSD_SCR [7:0]	Character Row Shadow Enable for 7-0. Each bit controls each row correspondingly. Used only in one bit per pixel font. 1= Enable shadow for a row.

Default: 0000 0000B

0x0B1	OSD Shadow Control Row 15 – 8	R/W
Bits	Name	Description
7-0	OSD_SCR [15:8]	Character Row Shadow Enable for 15-8. Each bit controls each row correspondingly. Used only in one bit per pixel font. 1= Enable shadow for a row.

Default: 0000 0000B

0x0B2	OSD Shadow Control Row 23 – 16	R/W
Bits	Name	Description
7-0	OSD_SCR [23:16]	Character Row Shadow Enable for 23-16. Each bit controls each row correspondingly. Used only in one bit per pixel font. 1= Enable shadow for a row.

Default: 0000 0000B

0x0B3	OSD Shadow Control Row 31 – 24	R/W
Bits	Name	Description
7-0	OSD_SCR [31:24]	Character Row Shadow Enable for 31-24. Each bit controls each row correspondingly. Used only in one bit per pixel font. 1= Enable shadow for a row.

Default: 0000 0000B

0x0B4	OSD Border Control Row 7 – 0	R/W
Bits	Name	Description
7-0	OSD_BCR [7:0]	Character Row Border Enable for 7-0. Each bit controls each row correspondingly. Used only in one bit per pixel font. 1= Enable border for a row.

Default: 0000 0000B

0x0B5	OSD Border Control Row 15-8	R/W
Bits	Name	Description
7-0	OSD_BCR [15:8]	Character Row Border Enable for 15-8. Each bit controls each row correspondingly. Used only in one bit per pixel font. 1= Enable border for a row.

Default: 0000 0000B

0x0B6	OSD Border Control Row 23-16	R/W
Bits	Name	Description
7-0	OSD_BCR [23:16]	Character Row Border Enable for 23-16. Each bit controls each row correspondingly. Used only in one bit per pixel font. 1= Enable border for a row.

Default: 0000 0000B

0x0B7	OSD Border Control Row 31-24	R/W
Bits	Name	Description
7-0	OSD_BCR	Character Row Border Enable for 31-24. Each bit controls each row

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	[31:24]	correspondingly. Used only in one bit per pixel font. 1= Enable border for a row.

Default: 0000 0000B

0x0B8		OSD Border & Shadow Color Row 1 – 0	R/W
Bits	Name	Description	
7-4	OSD_BSCR1 [3:0]	Character Border/Shadow Color Index For Row 1. Used only in one bit per pixel font.	
3-0	OSD_BSCR0 [3:0]	Character Border/Shadow Color Index For Row 0. Used only in one bit per pixel font.	

Default: 0000 0000B

0x0B9		OSD Border & Shadow Color Row 3 – 2	R/W
Bits	Name	Description	
7-4	OSD_BSCR3 [3:0]	Character Border/Shadow Color Index For Row 3. Used only in one bit per pixel font.	
3-0	OSD_BSCR2 [3:0]	Character Border/Shadow Color Index For Row 2. Used only in one bit per pixel font.	

Default: 0000 0000B

0x0BA		OSD Border & Shadow Color Row 5 – 4	R/W
Bits	Name	Description	
7-4	OSD_BSCR5 [3:0]	Character Border/Shadow Color Index For Row 5. Used only in one bit per pixel font.	
3-0	OSD_BSCR4 [3:0]	Character Border/Shadow Color Index For Row 4. Used only in one bit per pixel font.	

Default: 0000 0000B

0x0BB		OSD Border & Shadow Color Row 7- 6	R/W
Bits	Name	Description	
7-4	OSD_BSCR7 [3:0]	Character Border/Shadow Color Index For Row 7. Used only in one bit per pixel font.	
3-0	OSD_BSCR6 [3:0]	Character Border/Shadow Color Index For Row 6. Used only in one bit per pixel font.	

Default: 0000 0000B

0x0BC		OSD Border & Shadow Color Row 9 – 8	R/W
Bits	Name	Description	
7-4	OSD_BSCR9 [3:0]	Character Border/Shadow Color Index For Row 9. Used only in one bit per pixel font.	
3-0	OSD_BSCR8 [3:0]	Character Border/Shadow Color Index For Row 8. Used only in one bit per pixel font.	

Default: 0000 0000B

0x0BD		OSD Border & Shadow Color Row 11 – 10	R/W
Bits	Name	Description	
7-4	OSD_BSCR11 [3:0]	Character Border/Shadow Color Index For Row 11. Used only in one bit per pixel font.	
3-0	OSD_BSCR10 [3:0]	Character Border/Shadow Color Index For Row 10. Used only in one bit per pixel font.	

Default: 0000 0000B

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0x0BE		OSD Border & Shadow Color Row 13 – 12	R/W
Bits	Name	Description	
7-4	OSD_BSCR13 [3:0]	Character Border/Shadow Color Index For Row 13. Used only in one bit per pixel font.	
3-0	OSD_BSCR12 [3:0]	Character Border/Shadow Color Index For Row 12. Used only in one bit per pixel font.	

Default: 0000 0000B

0x0BF		OSD Border & Shadow Color Row 15 – 14	R/W
Bits	Name	Description	
7-4	OSD_BSCR15 [3:0]	Character Border/Shadow Color Index For Row 15. Used only in one bit per pixel font.	
3-0	OSD_BSCR14 [3:0]	Character Border/Shadow Color Index For Row 14. Used only in one bit per pixel font.	

Default: 0000 0000B

0x0C0		OSD Border & Shadow Color Row 17 – 16	R/W
Bits	Name	Description	
7-4	OSD_BSCR17 [3:0]	Character Border/Shadow Color Index For Row 17. Used only in one bit per pixel font.	
3-0	OSD_BSCR16 [3:0]	Character Border/Shadow Color Index For Row 16. Used only in one bit per pixel font.	

Default: 0000 0000B

0x0C1		OSD Border & Shadow Color Row 19 – 18	R/W
Bits	Name	Description	
7-4	OSD_BSCR19 [3:0]	Character Border/Shadow Color Index For Row 19. Used only in one bit per pixel font.	
3-0	OSD_BSCR18 [3:0]	Character Border/Shadow Color Index For Row 18. Used only in one bit per pixel font.	

Default: 0000 0000B

0x0C2		OSD Border & Shadow Color Row 21 – 20	R/W
Bits	Name	Description	
7-4	OSD_BSCR21 [3:0]	Character Border/Shadow Color Index For Row 21. Used only in one bit per pixel font.	
3-0	OSD_BSCR20 [3:0]	Character Border/Shadow Color Index For Row 20. Used only in one bit per pixel font.	

Default: 0000 0000B

0x0C3		OSD Border & Shadow Color Row 23- 22	R/W
Bits	Name	Description	
7-4	OSD_BSCR23 [3:0]	Character Border/Shadow Color Index For Row 23. Used only in one bit per pixel font.	
3-0	OSD_BSCR22 [3:0]	Character Border/Shadow Color Index For Row 22. Used only in one bit per pixel font.	

Default: 0000 0000B

0x0C4		OSD Border & Shadow Color Row 25 – 24	R/W
Bits	Name	Description	

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7-4	OSD_BSCR25 [3:0]	Character Border/Shadow Color Index For Row 25. Used only in one bit per pixel font.
3-0	OSD_BSCR24 [3:0]	Character Border/Shadow Color Index For Row 24. Used only in one bit per pixel font.

Default: 0000 0000B

0x0C5		OSD Border & Shadow Color Row 27 – 26	R/W
Bits	Name	Description	
7-4	OSD_BSCR27 [3:0]	Character Border/Shadow Color Index For Row 27. Used only in one bit per pixel font.	
3-0	OSD_BSCR26 [3:0]	Character Border/Shadow Color Index For Row 26. Used only in one bit per pixel font.	

Default: 0000 0000B

0x0C6		OSD Border & Shadow Color Row 29 – 28	R/W
Bits	Name	Description	
7-4	OSD_BSCR29 [3:0]	Character Border/Shadow Color Index For Row 29. Used only in one bit per pixel font.	
3-0	OSD_BSCR28 [3:0]	Character Border/Shadow Color Index For Row 28. Used only in one bit per pixel font.	

Default: 0000 0000B

0x0C7		OSD Border & Shadow Color Row 31 – 30	R/W
Bits	Name	Description	
7-4	OSD_BSCR31 [3:0]	Character Border/Shadow Color Index For Row 31. Used only in one bit per pixel font.	
3-0	OSD_BSCR30 [3:0]	Character Border/Shadow Color Index For Row 30. Used only in one bit per pixel font.	

Default: 0000 0000B

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OSD Splitting Control

0x0C8		OSD Horizontal Splitting Control	R/W
Bits	Name	Description	
7	H_SPL_EN	Horizontal Splitting Enable 0: Disable 1: Enable	
6-0	SPL_HP [6:0]	Splitting horizontal begin position relative to the OSD frame for the selected window. The unit is in 1 horizontal font size. Range: 0~127	

Default: 0000 0000B

0x0C9		OSD Horizontal Splitting width Control	R/W
Bits	Name	Description	
7-0	SPL_HW [7:0]	Splitting horizontal width relative to the OSD frame. The unit is in 8 pixels. Range: 0~255	

Default: 0000 0000B

0x0CA		OSD Vertical Splitting Control	R/W
Bits	Name	Description	
7	V_SPL_EN	Vertical Splitting Enable 0: Disable	

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		1: Enable
6		Reserved
5-0	SPL_VP [5:0]	Splitting vertical begin position relative to the OSD frame. The unit is in 1 vertical font size. Range: 0~64

Default: 0000 0000B

0x0CB		OSD Vertical Splitting Height Control	R/W
Bits	Name	Description	
7-0	SPL_VH [7:0]	Splitting vertical height relative to the OSD frame. The unit is in 8 lines. Range: 0~255	

Default: 0000 0000B

OSD Attribute Control and OSD Fast Clear Control

0x0CC		OSD Attribute LSB	R/W
Bits	Name	Description	
7-0	OSD_ATTR [7:0]	OSD Attribute LSB. The register OSD_ATTR [15:0] is use for fast clear and update code from host and attribute from Register. This value is appended with the character font code. When update OSD SRAM code from host and “attribute from Reg 0x0CC ~ 0x0CD is selected in Reg 0x0E0 [7:4]. If fast clear is enable, the hardware will fill the entire SRAM with the values in Reg 0x0CE (Code) and Reg 0x0CC ~ 0x0CD (Attribute).	

Default: 0000 0000B

0x0CD		OSD Attribute MSB	R/W
Bits	Name	Description	
7-0	OSD_ATTR [15:8]	OSD attribute MSB. The register OSD_ATTR [15:0] is use for fast clear and update code from host and attribute from Register. This value is appended with the character font code. When update OSD SRAM code from host and attribute from Reg 0x0CC ~ 0x0CD is selected in Reg 0x0E0 [7:4]. If fast clear is enable, the hardware will fill the entire SRAM with the values in Reg 0x0CE (Code) and Reg 0x0CC ~ 0x0CD (Attribute).	

Default: 0000 0000B

0x0CE		OSD SRAM Code Value For Fast Clear	R/W
Bits	Name	Description	
7-0	CODE_FC [7:0]	SRAM code for fast clear.	

Default: 0000 0000B

0x0CF		Fast Clear and Fade Mode Control	R/W
Bits	Name	Description	
7-6	FADE_MODE	Fade-in/Fade-out mode select 00:Left-Top corner 01:Right-Top corner 10:Left-Bottom corner 11:Right-Bottom corner	
5	BG_MIX_EN	Background translucent enables.	
4	FG_MIX_EN	Foreground translucent enables.	

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3		Reserved
2	FONT_MIX_EN	Border/Shadow translucent enable.
1	FC_MASK	Fast Clear area mask 0: SRAM on OSD frame 1: SRAM on 0x0000 to One bit Font Address
0	FC_EN (W)/ FC_RDY I	Fast Clear Enable, When enable this bit, the hardware will fill the entire SRAM with the values in Reg 0x0CE (Code) and Reg 0x0CC ~ 0x0CD (Attribute). 1: Enable the fast clear. If fast clear is finished, this bit FC_RDY will be clear to '0'. 0: No Effect

Default: 0000 0000B

Translucent

	BG = "001"	BG = "000" ~ "1111" except "0001"	0x0CF	0x0A1[2:0] TP_LEVEL	0x0A1[5:3] TP_LEVEL	0x0AA[4] WIN_MIX
Character	★		Bit 4 = 1		★	
Character		★	Bit 4 = 1	★		
Character Background	★		Bit 5 = 1		★	
Character Background		★ except "0000"	Bit 5 = 1	★		
Win Color	★				★	★
Win Color		★			★	★
Border/Shadow	★		Bit 2 = 1		★	
Border/Shadow		★	Bit 2 = 1		★	

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8.13. Source Hsync Digital PLL Control

0x0D0		HS DDS PLL Control	R/W
Bits	Name	Description	
7		Reserved	
6	VER_DOUB_BYPASS	Vertical double buffer bypass 0: Normal (DBL_EN define PLL load at VS blanking or disable PLL data load) 1: Bypass (realtime PLL update)	
5	DBL_EN	Double buffer load data at VSYNC Blanking 0: Disable (VER_DOUB_BYPASS define realtime update or disable PLL data load) 1: Enable	
4-1		Reserved	

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0	DDS_EN	DDS enable 0: Disable 1: Ensable

Default: 0000 0000B

0x0D1	HS Frequency Control	R/W
Bits	Name	Description
6-4		Reserved
3	HSDDS_DIV_CTRL	HS DDS Divide control 0: Enable 1: Disable
2		Reserved
1-0	HPLL_FREQ_RANGE [1:0]	HS DDS output frequency range control 00: 100~200MHz 01: 50~100MHz 10: 25~50MHz 11: 12.5~25MHz

Default:0001 0000B

0x0D2	HS PLL Frequency Control Ratio – lo	R/W
Bits	Name	Description
7-0	HSDDS_RATIO [7:0]	HS PLL frequency control ration (for manual mode)

Default: 0000 0000B

0x0D3	HS PLL Frequency Control Ratio – mi	R/W
Bits	Name	Description
7-0	HSDDS_RATIO [15:8]	HS PLL frequency control ration (for manual mode)

Default: 0000 0000B

0x0D4	HS PLL Frequency Control Ratio – hi	R/W
Bits	Name	Description
5-0	HSDDS_RATIO [21:16]	HS PLL frequency control ration (for manual mode)

Default: 0001 0000B

0x0D5	HS PLL phase lock control	R/W
Bits	Name	Description
7-4		Reserved
3	HS_INV	HSYNC Invert 0: Normal 1: Inverted
2		HPLL manual mode 0: Auto 1: Manual
1		Reserved
0	HPLL_EN	HS PLL DDS enable 0: Disable 1: Enable

Default: 0000 0011B

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0x0D6	HS PLL control	R/W
Bits	Name	Description
7	HPLL_LOCK_EN	HS PLL phase lock enable
6-5	HPLL_PLOOP_FIT [1:0]	HS PLL phase lock error correction ratio
4-0		Reserved

Default: 0011 1111B

0x0D7	HS PLL divider – lo	R/W
Bits	Name	Description
7-0	HSDDS_DIVIDER [7:0]	Clock divides value in the feedback loop of the HS PLL. The HS PLL reference is the input Hsync signal. CR:0D1[3] must be set “1”

Default: 0000 0000B

0x0D8	HS PLL divider – hi	R/W
Bits	Name	Description
3-0	HSDDS_ DIVIDER [11:8]	The low byte [7:0] of HS PLL divider value. The register is **double-buffered**. Divider = HSDDS_ DIVIDER <11:0> + 1 f_{HPPL} = Divider * f_{HS}

Default: 0000 1000B

0x0D9	HS PLL phase control 1	R/W
Bits	Name	Description
7-6	CLK_DLY_SEL	Select clock channel with clock delay adjusting. 00 = R 01 = G 10 = B 11 = Reserved
5-0	HS_PHASE_STEP [5:0]	HS PLL 64 step phase adjust

Default: 1000 0000B

0x0DA	HS PLL Phase control 2	R/W
Bits	Name	Description
7-4		Reserved
3-0	ADC_CK_DELAY[3:0]	To ADC Clock delay control

Default: 0000 0000B

0x0DB	HS PLL Line count Select	R/W
Bits	Name	Description
7-5		Reserved

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4-0	HS_LINE_CNT_SEL[4:0]	Horizontal Sync Line Count Select (count with 12Mhz) 00000: 2^0 Line 00001: 2^1 Line 00010: 2^2 Line . . 11110: 2^{30} Line 11111: 2^{31} Line HS = 12M/(HS_CNT_RESULT[21:0] / HS_LINE_CNT_SEL[4:0])

Default: 0000 0100B

0x0DC	HS_DDS DPLL Output Control	R/W
Bits	Name	Description
7-2		Reserved
1	CAP_CKO_INV	Capture clock output polarity invert 0: Normal 1: Inverted
0		Reserved

Default: 0000 0000B

0x0DD	HS HPLL Frequency Read back– lo	R
Bits	Name	Description
7-0	HS_CNT_RESULT [7:0]	HS DPLL Frequency read back [7:0] HS = 12M/(HS_CNT_RESULT[21:0] / HS_LINE_CNT_SEL[4:0])

Default: XXXX XXXXB

0x0DE	HS HPLL Frequency Read back – mi	R
Bits	Name	Description
7-0	HS_CNT_RESULT [15:8]	HS DPLL Frequency read back [15:8]

Default: XXXX XXXXB

0x0DF	HS HPLL Frequency Read back – hi	R
Bits	Name	Description
5-0	HS_CNT_RESULT [21:16]	HS DPLL Frequency read back [21:16]

Default: XXXX XXXXB

8.14. Index Port Access Control

0x0E0	Index Access Port	R/W
Bits	Name	Description
7-4	TBL_SEL INDEX_ADDR [7:0] INDEX_ADDR [7:0] INDEX_ADDR [7:0] INDEX_ADDR [7:0] INDEX_ADDR [11:0] INDEX_ADDR [11:0] INDEX_ADDR [11:0]	Table Select 0000: Red Gamma Table (Read/Write) (10 bits/word) 0001: Green Gamma Table (Read/Write) (10 bits/word) 0010: Blue Gamma Table (Read/Write) (10 bits/word) 0011: R/G/B Gamma Tables modified simultaneously (Write only) (10 bits/word) 0100: OSD SRAM code only (Read/Write) (8 bits/word) 0101: OSD SRAM attribute MSB (Read/Write) (8 bits/word) 0110: OSD SRAM attribute LSB (Read/Write) (8 bits/word)

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	INDEX_ADDR [11:0] INDEX_ADDR [11:0] INDEX_ADDR [11:0] INDEX_ADDR [9:0] INDEX_ADDR [7:0] INDEX_ADDR [7:0] INDEX_ADDR [7:0] INDEX_ADDR [7:0] INDEX_ADDR [7:0]	0111: OSD SRAM attribute (Read/Write) (16 bits/word) 1000: OSD SRAM code and attribute (Read/Write) (24 bits/word) 1001: OSD SRAM code from host and attribute from Reg 0x0CC ~ 0x0CD (Read/Write) (8 bits/word) 1010: OSD Programmable 1 Bit Color Font (Read/Write) (24 bits/word) 1011: OSD Programmable 2 Bit Color Font (Read/Write) (24 bits/word) 1100: OSD Programmable 4 Bit Color Font (Read/Write) (24 bits/word) 1101: OSD Palette (Read/Write) (16 bits/word) 1110: HDCP Data(Read/Write) (8 bits/word) 1111: OD SDRAM index port access
3	PORT_RW	Port Read/Write 0: Write 1: Read
2	DIRECT_WR_GAMMA	Gamma write directly 0: Write gamma table must set gamma disable 1: Write gamma table directly
1-0		Reserved

Default: 0000 0000B

0x0E1		Index Address Port – Low Byte	R/W
Bits	Name	Description	
7-0	INDEX_ADDR [7:0]	Table Address – low bits	

Default: 0000 0000B

0x0E2		Index Address Port – High Byte	R/W
Bits	Name	Description	
7-0	INDEX_ADDR [15:8]	Table Address – upper bits	

Default: 0000 0000B

0x0E3		Index Data Port	R/W
Bits	Name	Description	
7-0	PORT_DATA [7:0]	Data port for the SRAM, Palette, and Programmable Font.	

Default: 0000 0000B

Note: 1. If The Index Port's access is over 8 bit data length, the host interface will transfer or receive data from LSB to MSB.

0x0E4 ~ 0x0E5: Reserved

8.15. Auto Gain/Gauge Access Window Control

0x0E6		Auto Gain/Gauge Window Odd field Vertical Begin –lo	R/W
Bits	Name	Description	
7-0	GI_CAP_VBEGO [7:0]	Vertical Capture Begin for Odd Field. GI_CAP_VBEGO indicates how many lines to wait after referenced edge of VSYNC before starting image capture. GI_CAP_VBEGO =3, means waiting 3 lines to begin capture. This register is double-buffered.	

Default: 0000 0000B

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0x0E7		Auto Gain/Gauge Window Odd field Vertical Begin –hi	R/W
Bits	Name	Description	
7-3		Reserved	
2-0	GI_CAP_VBEGO [10:8]	MSB of GI_CAP_VBEGO. This register is double-buffered.	

Default: 0000 0000B

0x0E8		Auto Gain/Gauge Window Even field Vertical Begin –lo	R/W
Bits	Name	Description	
7-0	GI_CAP_VBEGE [7:0]	Vertical Capture Begin for Even Field. GI_CAP_VBEGE indicates how many lines to wait after referenced edge of VSYNC before starting image capture. GI_CAP_VBEGE =3, means waiting 3 lines to begin capture. This register is double-buffered.	

Default: 0000 0000B

0x0E9		Auto Gain/Gauge Window Even field Vertical Begin –hi	R/W
Bits	Name	Description	
2-0	GI_CAP_VBEGE [10:8]	MSB of GI_CAP_VBEGE. This register is double-buffered.	

Default: 0000 0000B

0x0EA		Auto Gain/Gauge Window Vertical Length –lo	R/W
Bits	Name	Description	
7-0	GI_CAP_VLEN [7:0]	Vertical Capture Length. GI_CAP_VLEN indicates how many lines to capture. GI_CAP_VLEN = 3, means capturing 3 lines. This register is double-buffered.	

Default: 0000 0000B

0x0EB		Auto Gain/Gauge Window Vertical Length –hi	R/W
Bits	Name	Description	
2-0	GI_CAP_VLEN [10:8]	MSB of GI_CAP_VLEN. This register is double-buffered.	

Default: 0000 0000B

0x0EC		Auto Gain/Gauge Window Horizontal Begin –lo	R/W
Bits	Name	Description	
7-0	GI_CAP_HBEG [7:0]	Horizontal Capture Begin. GH_CAP_HBEG indicates how many pixels to wait after referenced edge of HSYNC before starting image capture. GH_CAP_HBEG =3, means waiting 3 pixels to begin capture. This register is double-buffered.	

Default: 0000 0000B

0x0ED		Auto Gain/Gauge Window Horizontal Begin –hi	R/W
Bits	Name	Description	
7-4		Reserved	
3-0	GI_CAP_HBEG [11:8]	MSB of GI_CAP_HBEG. This register is double-buffered.	

Default: 0000 0000B

0x0EE	Auto Gain/Gauge Window Horizontal Width –lo	R/W

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Bits	Name	Description
7-0	GI_CAP_HWID [7:0]	Horizontal Capture Width. GI_CAP_HWID indicates how many pixels to capture. GI_CAP_HWID = 3, means capturing 3 pixels. This register is double-buffered.

Default: 0000 0000B

0x0EF	Auto Gain/Gauge Window Horizontal Width –hi	R/W
Bits	Name	Description
7-4		Reserved
3-0	GI_CAP_HWID [11:8]	MSB of GI_CAP_HWID. This register is double-buffered.

Default: 0000 0000B

8.16. Display Digital PLL Control

0x0F0	Display DDS PLL Control	R/W
Bits	Name	Description
7-4		DDS debug mode
3	DDDS_RST	Display DDS Reset 0: Normal 1: Reset
2		Reserved
0	DDDS_EN	Display DDS enable 0: Disable 1: Enable

Default: 0000 0000B

0x0F1	Display Frequency Control	R/W
Bits	Name	Description
7-2		Reserved
1-0	DISPLAY_PORT	Display data port control 00: Dual port 01: Single port

Default: 0001 0000B

0x0F2	Display PLL Frequency Control Ratio – lo	R/W
Bits	Name	Description
7-0	DDDS_RATIO [7:0]	Display DDS frequency control ratio

Default: 0000 0000B

0x0F3	Display PLL Frequency Control Ratio – mi	R/W
Bits	Name	Description
7-0	DDDS_RATIO [15:8]	Display DDS frequency control ratio

Default: 0000 0000B

0x0F4	Display PLL Frequency Control Ratio – hi	R/W
Bits	Name	Description
5-0	DDDS_RATIO [21:16]	Display DDS frequency control ratio

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Default: 0000 1010B

Fout = (Reference-Freq × DDDS_RATIO [21:0]) / 2^{17}
Fref = 12.000 MHz

0x0F5	SSC Control	R/W
Bits	Name	Description
7-5	SSC_MOD_FREQ	Display PLL spread spectrum modulation frequency control “111” = REFCLK/4 “110” = REFCLK/8 “101” = REFCLK/16 “100” = REFCLK/32 “011” = REFCLK/64 “010” = REFCLK/128 “001” = REFCLK/256 “000” = REFCLK/512
4-1	SSC_RATIO	DDDS PLL spread spectrum ratio “1000” = 1/4 “0111” = 1/8 “0110” = 1/16 “0101” = 1/32 “0100” = 1/64 “0011” = 1/128 “0010” = 1/256 “0001” = 1/512 “0000” = 1/1024
0	SSC_EN	DDS PLL spread spectrum enable 0: Disable 1: Enable

Default: 0000 1010B

0x0F6 : Reserved

0x0F7	Gauge Control 1	R/W
Bits	Name	Description
7-1		Reserved
0	GAUGE_MOD_SEL	Gauge Detection Area mode select 0 = Detecting area is defined by capture registers 1 = Detecting area is defined by Auto Gain/Gauge window registers.

Default: 0000 0000B

0x0F8	Gauge Control 2	R/W
Bits	Name	Description
7	GAUGE_EN	To Gauge the distribution of input data. When GAUGE_EN set “1”, the function is enable, then if the gauge is finished this bit is cleared to “0”. , repeat read gauge this bit must set “0” follow set “1” 0 = Disable 1 = Enable
6-5		Reserved
4-3	GAUGE_SEL	Gauge Source Select 00: Blue Channel 01: Green Channel 10: Red Channel 11: Reserved
2-0	GAUGE_STEP [7:0]	The step of gauge Data 000: 1 Step 100: 16 Step 001: 2 Step 101: 32 Step 010: 4 Step 110: Reserved 011: 8 Step 111: Reserved

Default: 0000 0000B

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0x0F9	Gauge Result Read Back Area Select	R/W
Bits	Name	Description
7-3		Reserved
2-0	GAUGE_AREA	The Gauge Result Read back area select 0~7

Default: 0000 0000B

0x0FA	Gauge Offset	R/W
Bits	Name	Description
7-0	GAUGE_OFFSET	The level of R/G/B Input when Gauge function is enable

Default: 0000 0000B

0x0FB	Gauge Result – lo	R
Bits	Name	Description
7-0	GAUGE_RESULT [7:0]	The gauge result of input data in capture window

Default: XXXX XXXXB

0x0FC	Gauge Result – mi	R
Bits	Name	Description
7-0	GAUGE_RESULT [15:8]	The gauge result of input data in capture window

Default: XXXX XXXXB

0x0FD	Gauge Result – hi	R
Bits	Name	Description
7-0	GAUGE_RESULT [23:16]	The gauge result of input data in capture window

Default: XXXX XXXXB

0x0FE : Reserved

8.17. Graphic Input Gauge

0x0FF	Accessing Register Page Enable	R/W
Bits	Name	Description
D7-2		Reserved
D1-0	REG_PAGE_SEL	Register Page Enable 000: Enable register Page0. 001: Enable register Page1. 010: Enable register Page2. 011: Enable register Page3. 011: Enable register Page4.

Default: 0000 0000B

8.18. Product ID

0x100	Product ID	R
Bits	Name	Description
7-4		Reserved
3-0	CHIP_ID	Chip ID = 1011

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8.19. Power Control

0x101	Power Control	R/W
Bits	Name	Description
7		Reserved
6	PU_LVDSA	LVDS A Port power up control. 0 = Power down 1 = Power up
5	WARM_RST	Chip Warm Reset. When WARM_RST=1, all state machines will be reset other than the all of register's value. 0 = Normal 1 = Reset
4		Reserved
3	GCLK_OFF	Graphic Port Clock Off. When GCLK_OFF=1, Graphic Port clock is disabled to conserve power
2	VCLK_OFF	Video Port Clock Off. When VCLK_OFF=1, Video Port clock is disabled to conserve power
1		Reserved
0	DCLK_OFF	Display Clock Off. When DCLK_OFF=1, display clock is disabled to conserve power

Default: 0000 1101B

0x102	Power Down Control 2	R/W
Bits	Name	Description
7-6		Reserved
5	PU_HPLL	HPLL Power up control. 0 = Power down 1 = Power up
4		Reserved
3	PU_ADC	ADC Power up control. 0 = Power down 1 = Power up
2		Reserved
1	PU_TMDS	TMDS PD power up mode. When PU_TMDS = '0', TMDS circuit will go into power down state. 0 = Power down 1 = Power up
0		Reserved

Default: 0000 0000B

0x103 ~ 0x105 : Reserved

8.20. Auto Tune

Graphic Auto Tune Control

0x106	Graphic Auto Tune Control	R/W
Bits	Name	Description
7	GI_AGPD_MOD	Auto Gain and Phase Detection Area mode select , if this bit set "1" then GI_AUTO_WIN don't care . 0 = Normal/ Original (depend on GI_AUTO_WIN) 1 = Detecting area is defined by Auto Gain/Gauge window registers. (0x0E6 ~ 0x0EF)

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6-5	GI_AUTO_WIN	Auto Gain and Phase Detection Area select 00 : Whole frame 01 : Capture 1x : Mask window
4	GI_POS_DE	Enable Position Detection depending on DE signal when TMDS is enabled. If GI_POS_DE =1, 0xFF data is input to RGB channel for position detection instead of data from graphic port when DE is '1'.
3-2	GI_GAINPHS_SEL [1:0]	Graphic Input Gain and Phase Detection Type Select. 00 = Phase Tune 1 (sum of difference calculate mode 1) 01 = Phase Tune 2 (sum of difference calculate mode 2) 10 = Min RGB Gain (read back CR:0x113 ~ 0x116) 11 = Max RGB Gain (read back CR:0x113 ~ 0x116)
1	GI_GAINPHS_EN/ GI_GAINPHS_RDY	Graphic Input Gain and Phase Detection Enable. When GI_GAINPHS_EN = 1, detection will start from next VSYNC. When detection is finished, this bit is cleared to '0'. 0 = Disable 1 = Enable
0	GI_POS_EN/ GI_POS_RDY	Graphic Input Active Window Position Detection Enable. When GI_POS_EN = 1, detection will start from next VSYNC. When detection is finished, this bit is cleared to '0'. 0 = Disable. 1 = Enable

Default: 0001 1100B

Graphic Auto Position

0x107	**Auto Position Black Threshold**	**R/W**
Bits	Name	Description
7-0	GI_POS_THR [7:0]	Graphic data lager then GI_POS_THR will be considered to be non-black pixel for position detecting.

Default: 0000 1111B

0x108	**Auto Position Vertical Begin for Odd Field –lo**	**R**
Bits	Name	Description
7-0	GI_POS_VBEGO [7:0]	Active Window Vertical Begin for Odd Field. GI_POS_VBEGO= 3 means there are 3 blanking lines.

Default: XXXX XXXXB

0x109	**Auto Position Vertical Begin for Odd Field –hi**	**R**
Bits	Name	Description
2-0	GI_POS_VBEGO [10:8]	MSB of GI_POS_VBEGO

Default: XXXX XXXXB

0x10A	**Auto Position Vertical Begin for Even Field –lo**	**R**
Bits	Name	Description
7-0	GI_POS_VBEGE [7:0]	Active Window Vertical Begin for Even Field. GI_POS_VBEGE= 3 means there are 3 blanking lines.

Default: XXXX XXXXB

0x10B	**Auto Position Vertical Begin for Even Field –hi**	**R**
Bits	Name	Description

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2-0	GI_POS_VBEGE [10:8]	MSB of GI_POS_VBEGE

Default: XXXX XXXXB

0x10C	Auto Position Vertical Length –lo	R
Bits	Name	Description
3-0	GI_POS_VLEN [7:0]	The active window vertical length. GI_POS_VLEN = 3 means there are 3 active lines.

Default: XXXX XXXXB

0x10D	Auto Position Vertical Length –hi	R
Bits	Name	Description
2-0	GI_POS_VLEN [10:8]	MSB of GI_POS_VLEN

Default: XXXX XXXXB

0x10E	Auto Position Horizontal Begin –lo	R
Bits	Name	Description
7-0	GI_POS_HBEG [7:0]	The active window horizontal begin. GI_POS_HBEG = 3 means there are 3 blanking pixels.

Default: XXXX XXXXB

0x10F	Auto Position Horizontal Begin –hi	R
Bits	Name	Description
3-0	GI_POS_HBEG [11:8]	MSB of GI_POS_HBEG

Default: XXXX XXXXB

0x110	Auto Position Horizontal Width –lo	R
Bits	Name	Description
3-0	GI_POS_HWID [7:0]	The active window horizontal width. GI_POS_HWID = 3 means there are 3 active pixels.

Default: XXXX XXXXB

0x111	Auto Position Horizontal Width –hi	R
Bits	Name	Description
3-0	GI_POS_HWID [11:8]	MSB of GI_POS_HWID

Default: XXXX XXXXB

Graphic Auto Phase and Gain

0x112	Auto Phase Bit Mask	R/W
Bits	Name	Description
7-3		Reserved
2-0	GI_PHS_MASK [2:0]	Decide how many LSB bits will be masked out, and then the difference between adjacent pixels will be added to the sum of difference accumulator.

Default: 0000 0100B

0x113	Auto Phase Sum of Difference –lo	R
Bits	Name	Description

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7-0	GI_PHS_SDIFF [7:0]	Auto Phase Sum of Difference (LSB). GI_PHS_SDIFF specifies how the phase locking quality in ADCPLL block.
	R_MINMAX [7:0]	The minimum or maximum value of red channel data in one frame.

Default: XXXX XXXXB

0x114	Auto Phase Sum of Difference – 2'nd	R
Bits	Name	Description
7-0	GI_PHS_SDIFF [15:8]	Second byte of GI_PHS_SDIFF
	G_MINMAX [7:0]	The minimum or maximum value of green channel data in one frame.

Default: XXXX XXXXB

0x115	Auto Phase Sum of Difference – 3'rd	R
Bits	Name	Description
7-0	GI_PHS_SDIFF [23:16]	Third byte of GI_PHS_SDIFF
	B_MINMAX [7:0]	The minimum or maximum value of blue channel data in one frame.

Default: XXXX XXXXB

0x116	Auto Phase Sum of Difference –hi	R
Bits	Name	Description
7-0	GI_PHS_SDIFF [31:24]	MSB of GI_PHS_SDIFF

Default: XXXX XXXXB

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Graphic Auto Clock

0x117	Auto Clock Reference Width –lo	R/W
Bits	Name	Description
7-0	GI_CLK_REF [7:0]	Auto Clock Reference Width. This register provides the reference value for calibrating the frequency of sampling clock in ADCPLL block.

Default: 0000 0000B

0x118	Auto Clock Reference Width –hi	R/W
Bits	Name	Description
7-4		Reserved
3-0	GI_CLK_REF [11:8]	MSB of AUTO_CLK_REF

Default: 0000 0000B

0x119	Auto Clock Detecting Result	R
Bits	Name	Description
7-6	GI_CLK_COMP [1:0]	Auto Clock Comparing Relation. GI_CLK_COMP specifies the comparing relation between GI_POS_HWID and GI_CLK_REF 00: GI_POS_HWID = GI_CLK_REF 01: GI_POS_HWID < GI_CLK_REF 1X: GI_POS_HWID > GI_CLK_REF
5-0	GI_CLK_DIFF	Difference of |GI_POS_HWID – GI_CLK_REF|

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	[5:0]	The difference value is clamped to 0x3F if difference ≥ 0x3F

Default: XXXX XXXXB

0x11A : Reserved

Video Auto Tune Control

0x11B	Video Auto Tune Control	R/W
Bits	Name	Description
7-6		Reserved
5	VI_AUTO_MASK	Gain Detection Area masking when VI_GAIN_AREA = "1" 0 = Detecting area is whole frame 1 = Detecting area is defined by mask window registers. (define by CR: 0x047 ~ 0x04A)
4		Reserved
3	VI_GAIN_AREA	Gain Detection Area Define Enable. 0 = Detecting area is over one frame except the area defined by mask window registers. 1 = Detecting area is defined by capture registers.
2	VI_GAIN_SEL	Video Input Gain Type Select 0 = Min Y Gain 1 = Max Y Gain
1	VI_GAIN_EN/ VI_GAIN_RDY	Video Input Y Min/Max Data Detection Enable. When VI_GAIN_EN = 1, detection will start from next VSYNC. When detection is finished, this bit is cleared to '0'. 0 = Disable 1 = Enable
0	VI_POS_EN/ VI_POS_RDY	Video Input Active Window Position Detection Enable. When VI_POS_EN = 1, detection will start from next VSYNC. When detection is finished, this bit is cleared to '0'. 0 = Disable 1 = Enable

Default: 0000 0000B

Video Auto Position

0x11C	Auto Position Black Threshold	R/W
Bits	Name	Description
7-0	VI_POS_THR [7:0]	Video data lager than VI_POS_THR will be considered to be non-black pixel for position detecting.

Default: 0000 1111B

0x11D	Auto Position Vertical Total –lo	R
Bits	Name	Description
7-0	VI_VTOTAL [7:0]	Vertical Period Total. VI_VTOTAL =99 means total 99 lines.

Default: XXXX XXXXB

0x11E	Auto Position Vertical Total –hi	R
Bits	Name	Description
2-0	VI_VTOTAL [10:8]	MSB of VI_VTOTAL.

Default: XXXX XXXXB

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0x11F		Auto Position Vertical Begin for Odd Field –lo	R
Bits	Name	Description	
7-0	VI_POS_VBEGO [7:0]	Active Window Vertical Begin for Odd Field. VI_POS_VBEGO =9 means 9 blanking lines.	

Default: XXXX XXXXB

0x120		Auto Position Vertical Begin for Odd Field –hi	R
Bits	Name	Description	
2-0	VI_POS_VBEGO [10:8]	MSB of VI_POS_VBEGO.	

Default: XXXX XXXXB

0x121		Auto Position Vertical Begin for Even Field –lo	R
Bits	Name	Description	
7-0	VI_POS_VBEGE [7:0]	Active Window Vertical Begin for Even Field. VI_POS_VBEGE =9 means 9 blanking lines.	

Default: XXXX XXXXB

0x122		Auto Position Vertical Begin for Even Field –hi	R
Bits	Name	Description	
2-0	VI_POS_VBEGE [10:8]	MSB of VI_POS_VBEGE.	

Default: XXXX XXXXB

0x123		Auto Position Vertical Length –lo	R
Bits	Name	Description	
7- 0	VI_POS_VLEN [7:0]	Active Window Vertical Length. VI_POS_VLEN =99 means 99 active lines.	

Default: XXXX XXXXB

0x124		Auto Position Vertical Length –hi	R
Bits	Name	Description	
7-3		Reserved	
2-0	VI_POS_VLEN [10:8]	MSB of VI_POS_VLEN.	

Default: XXXX XXXXB

0x125		Auto Position Horizontal Total –lo	R
Bits	Name	Description	
7-0	VI_HTOTAL [7:0]	Horizontal Period Total. VI_HTOTAL=99, means total 99 pixels.	

Default: XXXX XXXXB

0x126		Auto Position Horizontal Total –hi	R
Bits	Name	Description	
7-4		Reserved	
3-0	VI_HTOTAL [11:8]	MSB of VI_HTOTAL.	

Default: XXXX XXXXB

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0x127		Auto Position Horizontal Begin –lo	R
Bits	Name	Description	
7-0	VI_POS_HBEG [7:0]	Active Window Horizontal Begin. VI_POS_HBEG =3 means 3 blanking pixels.	

Default: XXXX XXXXB

0x128		Auto Position Horizontal Begin –hi	R
Bits	Name	Description	
7-4		Reserved	
3-0	VI_POS_HBEG [11:8]	MSB of VI_POS_HBEG	

Default: XXXX XXXXB

0x129		Auto Position Horizontal Width –lo	R
Bits	Name	Description	
7-0	VI_POS_HWID [7:0]	Active Window Horizontal Width. VI_POS_HWID =99 means 99 active pixels.	

Default: XXXX XXXXB

0x12A		Auto Position Horizontal Width –hi	R
Bits	Name	Description	
3-0	VI_POS_HWID [11:8]	MSB of VI_POS_HWID	

Default: XXXX XXXXB

Video Auto Gain

0x12B		Video Min/Max Y Value	R
Bits	Name	Description	
7-0	Y_MINMAX [7:0]	The minimum or maximum value of Y channel data in one frame.	

Default: XXXX XXXXB

0x12C ~ 0x12F : Reserved

8.21. Bright Frame Display Registers

Bright Frame Control

Note–When both Bright Frames are enabled and if two windows are overlapped frame2 has higher priority than frame 1.

0x130		Bright Frame Enable Control	R/W
Bits	Name	Description	
7-5		Reserved	
4	BRIGHT_REF_CTL	Bright Frame Active reference 0: Front (Capture) 1: Post (Display)	
3-2		Reserved	
1	BRIGHT_FRM2_EN	Enable Bright Frame 2 0: Disable 1: Enable	

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0	BRIGHT_FRM1_EN	Enable Bright Frame 1 0: Disable 1: Enable

Default: 0000 0000B

0x131		Bright Frame access index Select	R/W
Bits	Name	Description	
7-1		Reserved	
0	BRIGHT_FRM_SEL [0]	This register is used to select which frame is to be accessed or modified. It is programmed prior to accessing the registers Reg 0x132 ~ 0x13B "0" = Bright Frame 1 "1" = Bright Frame 2	

Default: 0000 0000B

0x132		Bright Frame Horizontal Start – Low byte	R/W
Bits	Name	Description	
7-0	BRIGHT_FRM_HS [7:0]	Bright Frame horizontal start low byte [7:0]. Specifies the horizontal starting position of the Bright Frame in pixel units. This register is **double-buffered**.	

Default: 0000 0000B

0x133		Bright Frame Horizontal Start – High Byte	R/W
Bits	Name	Description	
7-4		Reserved	
3-0	BRIGHT_FRM_HS [11:8]	Bright Frame horizontal start high byte [11:8]. Specifies the horizontal starting position of the Bright Frame in pixel units. This register is **double-buffered**.	

Default: 0000 0000B

0x134		Bright Frame Horizontal Width – Low byte	R/W
Bits	Name	Description	
7-0	BRIGHT_FRM_HW [7:0]	Bright Frame horizontal Width low byte [7:0]. Specifies the width of the Bright Frame in pixel units. . This register is **double-buffered**.	

Default: 0000 0000B

0x135		Bright Frame Horizontal Width – High byte	R/W
Bits	Name	Description	
7-4		Reserved	
3-0	BRIGHT_FRM_HW [11:8]	Bright Frame horizontal Width low byte [11:8]. Specifies the width of the Bright Frame in pixel units. . This register is **double-buffered**.	

Default: 0000 0000B

0x136		Bright Frame Vertical Start – Low byte	R/W
Bits	Name	Description	
7-0	BRIGHT_FRM_VS [7:0]	Bright Frame vertical start low byte [7:0]. Specifies the vertical starting position of the Bright Frame in pixel units. This register is **double-buffered**.	

Default: 0000 0000B

0x137		Bright Frame Vertical Start – High Byte	R/W
Bits	Name	Description	
7-4		Reserved	

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3-0	BRIGHT_FRM_VS [10:8]	Bright Frame vertical start high byte [10:8]. Specifies the vertical starting position of the Bright Frame in pixel units. This register is **double-buffered**.

Default: 0000 0000B

0x138	**Bright Frame Vertical Height – Low byte**	**R/W**
Bits	Name	Description
7-0	BRIGHT_FRM_VH [7:0]	Bright Frame vertical Width low byte [7:0]. Specifies the width of the Bright Frame in pixel units. . This register is **double-buffered**.

Default: 0000 0000B

0x139	**Bright Frame Vertical Height – High byte**	**R/W**
Bits	Name	Description
7-4		Reserved
2-0	BRIGHT_FRM_VH [10:8]	Bright Frame vertical Width low byte [10:8]. Specifies the width of the Bright Frame in pixel units. . This register is **double-buffered**.

Default: 0000 0000B

0x13A~0x142 : Reserved

8.22. DVI Input Control 2

0x143	**DVI Control**	**R/W**
Bits	Name	Description
7	TMDS_PLL_PD	TMDS PLL power down control
6-3		Reserved
2	TMDS_PWN	TMDS R terminal power down
1	TMDS_PWN	TMDS G terminal power down
0	TMDS_PWN	TMDS B terminal power down

Default: 0000 0000B

0x144	**DVI Control**	**R/W**
Bits	Name	Description
7-1		Reserved
0	TMDS_IPDS_PD	Power down control of three channel impedances (□uality□ct) only for data pair , clock channel power down by 0x146.6

Default: 0000 0000B

0x145 : Reserved

0x146	**DVI Control**	**R/W**
Bits	Name	Description
7		Reserved
6		0: DVI clock channel power down 1: normal
5-0		Reserved

Default: 1111 0011B

0x147~0x14F : Reserved

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8.23. Display Port Control

- Display timing control
- Single pixel or dual pixel output
- Output signals drive current and slew rate control
- Phase delay adjustment for accessing clock to external LCD
- Dithering function supports 24-bit quality for 18-bit panel
- Mute display control

Display Video Special mode Control
Display General Control

0x150	Display Control	R/W
Bits	Name	Description
7	DP_BIT_SHF	When display bus is 6-bit/color, this bit enable will shift the data RA[7:2], GA[7:2], BA[7:2] to RA[5:0], GA[5:0], BA[5:0] and RB[7:2], GB[7:2], BB[7:2] to RB[5:0], GB[5:0], BB[5:0]. When display bus is 8-bit/color, this bit enable will rotate the data RA[7:0], GA[7:0], BA[7:0] and RB[7:0], GB[7:0], BB[7:0] to right 2 bits 0 = Normal 1 = Shift / Rotate
6	DP_LOCK	Display lock event control. Under frame-sync display mode, this bit select the way of display locking to input image. For manual lock mode, the lock position is defined by DV_LOCK and DH_LOCK registers. 0 = Manual lock 1 = Auto lock
5	DP_AUTO	Display timing auto control. Under frame-sync display mode, this bit select the way of display timing generation. 0 = Manual 1 = Auto
4		Reserved
3	DP_COLDEP	Display Color Depth 0 = 8-bit/color 1 = 6-bit/color
2	DP_BUSWID	Display Bus Width 0 = Double pixel 48-bit 1 = Single pixel 24-bit
1	DP_DE	Panel supports DE mode 0 = Panel supports Sync mode, display Hs/Vs signal is at normal state 1 = Panel supports DE mode, display Hs/Vs signal will be pulled low
0	DP_EN	Display Enable 0 = Disable 1 = Enable

Default: 0110 0000B

0x151	DV_LOCK	R/W
Bits	Name	Description
7-0		Display sync manual mode V lock

Default: 0000 0000B

0x152	DH_LOCK	R/W

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Bits	Name	Description
7-0		Display sync manual mode H lock control low byte

Default: 0000 0000B

0x153	DH_LOCK	R/W

Bits	Name	Description
7-0		Display sync manual mode H lock control high byte

Default: 0000 0000B

0x154	Display Mute and Color Control	R/W

Bits	Name	Description
7-4	DP_PATT [3:0]	Select built-in display pattern Pattern number = 0~15 If PATT_BK = Bank 0 0000 = Gamma Correction pattern 0001 = Dot Moiré 0010 = Vertical Line Moire (1B1W) 0011 = Vertical Line Moire (2B1W) 0100 = Vertical Line Moire (2B2W) 0101 = 256 V_Gray Bar 0110 = 256 H_Gray Bar 0111 = Horizontal Line Moire (1B1W) 1000 = Horizontal Line Moire (2B1W) 1001 = Horizontal Line Moire (2B2W) 1010 = Chat Pattern 1011 = White Pattern 11xx = Rectangular pattern, outline width is defined by xx bits. 00 = 1 pixel 01 = 3 pixels 10 = 5 pixels 11 = 7 pixels If PATT_BK = Bank 1 0000 = Black pattern 0001~1111 = Reserved
3	PATT_BK	Built-in pattern bank Select 0 = Bank 0 1 = Bank 1
2	CBAR_EN	Paste a Cross Bar on the built-in display pattern and the Bar's gray level is controlled via CBAR_FG[7:0] register (0x15A) 0 = Disable 1 = Enable
1-0	DP_MUTE [1:0]	Display Mute Mode Select 00 = Normal display, RGB channel output controlled via DP_RGB 01 = Mute input with output built-in display pattern, pattern color decided by DP_RGB registers. (Display free-run) 10 = Mute input with output OSD and background color, background color decided by DP_BG_R/G/B registers. (Display free-run) 11 = Pull low all display signals including data, clock and control lines

Default: 0000 0000B

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0x155 : Reserved

0x156	Display Drive and Polarity Control	R/W
Bits	Name	Description
7	DDE_POL	Display DE 1 = Active High 0 = Active Low
6	DCLK_POL	Display Clock 0 = Normal 1 = Inverted
5	DHS_POL	Display Hsync 1 = Active High 0 = Active Low
4	DVS_POL	Display Vsync 1 = Active High 0 = Active Low
3-0		Reserved

Default: 1011 0010B

0x157	Display Clock and Data Delay Control	R/W
Bits	Name	Description
7		Reserved
6-5	DCLK_SYNC_SEL	Display clock synchronous mode select 00 = Display clock free-run 01 = Display clock is synchronized to input(default by TCON enable) 10 = Display clock free-run and DISP_DE synchronized to DISP_CLK 11 = Reserved
4-0	DCLK_DLY [4:0]	Select panel interface CLOCK delay time. (0.5nS/step) 0~32 step

Default: 0010 0000B

0x158	Display Dithering Control	R/W
Bits	Name	Description
7-4	DITH_MODE [3:0]	Dithering mode select
3	GAMMA_DITH_EN	Gamma dithering enable. (10 to 8) (0x1EE[2] must set “0”) 0 = Disable 1 = Enable (gamma table set 4.0) , 0x390.4 set “0” , gamma after OSD
2	DITH_8BIT/ GAMMA_RANDOM	Rounded 10 bit gamma data output to 8 bit for dithering 0 = Disable 1 = Enable 8 Bit dithering If GAMMA_DITH_EN = “1” (0x158[3]), this bit is for gamma dithering random mode control
1	DITH_TURBO	0 = Disable 1 = Enable , 0x1DA[5:4] must disable 0x158[7:4] set “0000” for check
0	DITH_EN	Dithering enable. When DITH_EN =0, the LSB bits of display data will be truncated if display color depth is less than internal data resolution. 0 = Disable 1 = Enable

Default: 0000 0000B

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0x159		Display Channel Select	R/W
Bits	Name	Description	
7	INT_FAST_EN	Mute mode with Free Run timing when graphic input sync fail (when input change HS/VS polarity , frequency) 0: Disable 1: Enable	
6		Reserved	
5	MUTE_FR_EN	Mute mode with Free Run timing Enable, this display Horizontal sync timing reference to Reg. 0x179~0x17A.(Vertical free run follow display V_{TOTAL} 0x15B,0x15C) 0: Disable 1: Enable	
3		Reserved	
2-0	DP_RGB [2:0]	Select RGB channel for display 000 = RGB normal display 001 = R channel only 010 = G channel only 011 = B channel only 100 = R & G channels 101 = R & B channels 110 = G & B channels 111 = RGB inverted display	

Default: 0000 0000B

0x15A		Cross Bar Gray Level	R/W
Bits	Name	Description	
7-0	CBAR_FG [7:0]	Select the foreground gray level of Cross Bar for burn-in display pattern. R=G=B= 0~255	

Default: 0000 0000B

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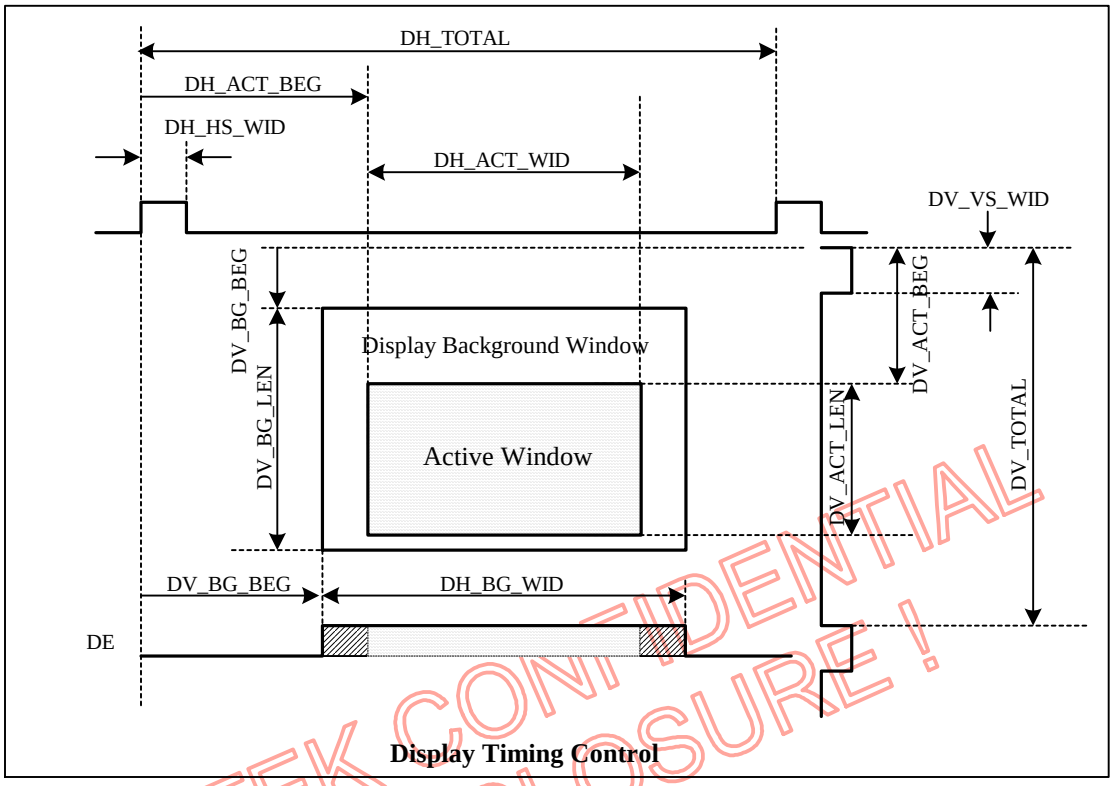

Figure 8.23-1 Display Timing

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Display Sync Timing Control

0x15B	Display Vertical Total –lo	R/W
Bits	Name	Description
7-0	DV_TOTAL [7:0]	Display Vertical Total Lines. DV_TOTAL = 3 means there are 4 total lines.

Default: 0000 0000B

0x15C	Display Vertical Total –hi	R/W
Bits	Name	Description
2-0	DV_TOTAL [10:8]	MSB of DV_TOTAL

Default: 0000 0000B

0x15D	Display VSYNC Pulse Width	R/W
Bits	Name	Description
7-0	DV_VS_WID [7:0]	Display VSYNC Pulse Width. DV_VS_WID =3, means pulse width is 3 lines wide.

Default: 0000 0000B

0x15E	Display Horizontal Total –lo	R/W
Bits	Name	Description
7-0	DH_TOTAL [7:0]	Display Horizontal Total Pixels. DH_TOTAL = 3 means there are 4 total pixels.

Default: 0000 0000B

0x15F	Display Horizontal Total –hi	R/W

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Bits	Name	Description
7-4		Reserved
3-0	DH_TOTAL [11:8]	MSB of DH_TOTAL

Default: 0000 0000B

0x160	Display HSYNC Pulse Width	R/W
Bits	Name	Description
7-0	DH_HS_WID [7:0]	Display HSYNC Pulse Width. DH_HS_WID =3, means pulse width is 3 pixels wide.

Default: 0000 0000B

0x161		R/W
Bits	Name	Description
7-2		Reserved
1	DR_VUPDATE_EN	Display Registers update enable on next DVS when DR_VDOUBLE_EN = "1"
0	DR_VDOUBLE_EN	Display Registers update on next DVS enable, When this bit enable will causes display registers update on next DVS. Otherwise, display registers will direct update. 0 = Disable 1 = Enable

Default: 0000 0010B

Display Background Window Control

0x162	Display Background Window Vertical Begin –lo	R/W
Bits	Name	Description
7-0	DV_BG_BEG [7:0]	Display Background Window Vertical Begin. DV_BG_BEG indicates how many lines to wait after DVSYNC leading edge before starting image display. DV_BG_BEG =3, means waiting 3 lines to begin display.

Default: 0000 0000B

0x163	Display Background Window Vertical Begin –hi	R/W
Bits	Name	Description
7-3		Reserved
2-0	DV_BG_BEG [10:8]	MSB of DV_BG_BEG

Default: 0000 0000B

0x164	Display Background Window Vertical Length –lo	R/W
Bits	Name	Description
7-0	DV_BG_LEN [7:0]	Display Background Window Vertical Length. DV_BG_LEN indicates how many lines to display. DV_BG_LEN =3, means displaying 3 lines.

Default: 0000 0000B

0x165	Display Background Window Vertical Length –hi	R/W
Bits	Name	Description
7-3		Reserved
2-0	DV_BG_LEN [10:8]	MSB of DV_BG_LEN

Default: 0000 0000B

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0x166		Display Background Window Horizontal Begin –lo	R/W
Bits	Name	Description	
7-0	DH_BG_BEG [7:0]	Display Background Window Horizontal Begin. DH_BG_BEG indicates how many pixels to wait after DHSYNC leading edge before starting image display. DH_BG_BEG =3, means waiting 3 pixels to begin display.	

Default: 0000 0000B

0x167		Display Background Window Horizontal Begin –hi	R/W
Bits	Name	Description	
7-4		Reserved	
3-0	DH_BG_BEG [11:8]	MSB of DH_BG_BEG	

Default: 0000 0000B

0x168		Display Background Window Horizontal Width –lo	R/W
Bits	Name	Description	
7-0	DH_BG_WID [7:0]	Display Background Window Horizontal Width. DV_BG_WID indicates how many pixels to display. DV_BG_WID =3, means displaying 3 pixels.	

Default: 0000 0000B

0x169		Display Background Window Horizontal Width –hi	R/W
Bits	Name	Description	
7-4		Reserved	
3-0	DH_BG_WID [11:8]	MSB of DH_BG_WID	

Default: 0000 0000B

0x16A			R/W
Bits	Name	Description	
7-5		Reserved	
4	DP_PORT_SWAP	A /B Port Swap Control 0: Normal 1: A/B Port Swap	
3	DP_BYTE_SWAPB	Display Bus Port B Byte Swap Control 0: Normal 1: B Port R/B Channel Byte Swap	
2	DP_BYTE_SWAPA	Display Bus Port A Byte Swap Control 0: Normal 1: A Port R/B Channel Byte Swap	
1	DP_BIT_SWAPB	Display Bus Port B Bit Swap Control 0: Normal 1: B Port Bit Swap	
0	DP_BIT_SWAPA	Display Bus Port A Bit Swap Control 0: Normal 1: Port A Bit Swap (RGB bit7~bit0 in 8 bit Mode, bit5~bit0 in 6 bit Mode)	

Default: 0000 0000B

Display Background Color Control

0x16B		Display Background Color – Red	R/W
Bits	Name	Description	

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7-0	DP_BG_R [7:0]	Display Background Window Red Color.

Default: 0000 0000B

0x16C	Display Background Color – Green	R/W
Bits	Name	Description
7-0	DP_BG_G [7:0]	Display Background Window Green Color.

Default: 0000 0000B

0x16D	Display Background Color – Blue	R/W
Bits	Name	Description
7-0	DP_BG_B [7:0]	Display Background Window Blue Color.

Default: 0000 0000B

Graphic Display Active Window Control

0x16E	Graphic Display Window Control	R/W
Bits	Name	Description
7	VD_EN	Video Display Window Enable 0 = Disable 1 = Enable
6-3		Reserved
2-1	GD_FLD [1:0]	Select the field to display for interlaced graphic input 00 = Display both odd and even field mode 01 = Display only odd field mode 10 = Display only even field mode 11 = Spatial Interlace mode
0	GD_EN	Graphic Display Window Enable 0 = Disable 1 = Enable

Default: 0000 0110B

0x16F	Graphic Display Active Window Vertical Begin –lo	R/W
Bits	Name	Description
7-0	GDV_ACT_BEG [7:0]	Graphic Display Active Window Vertical Begin. GDV_ACT_BEG indicates how many lines to wait after DVSYNC leading edge before starting graphic image display. GDV_BG_BEG =3, means waiting 3 lines to begin display.

Default: 0000 0000B

0x170	Graphic Display Active Window Vertical Begin –hi	R/W
Bits	Name	Description
7-3		Reserved
2-0	GDV_ACT_BEG [10:8]	MSB of GDV_ACT_BEG

Default: 0000 0000B

0x171	Graphic Display Active Window Vertical Length –lo	R/W
Bits	Name	Description
7-0	GDV_ACT_LEN [7:0]	Graphic Display Active Window Vertical Length. GDV_ACT_LEN indicates how many lines to display. GDV_ACT_LEN =3, means displaying 3 lines.

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Default: 0000 0000B

0x172		Graphic Display Active Window Vertical Length –hi	R/W
Bits	Name	Description	
7-3		Reseerved	
2-0	GDV_ACT_LEN [10:8]	MSB of GDV_ACT_LEN	

Default: 0000 0000B

0x173		Graphic Display Active Window Horizontal Begin –lo	R/W
Bits	Name	Description	
7-0	GDH_ACT_BEG [7:0]	Graphic Display Active Window Horizontal Begin. GDH_ACT_BEG indicates how many pixels to wait after DHSYNC leading edge before starting graphic image display. GDH_ACT_BEG =3, means waiting 3 pixels to begin display.	

Default: 0000 0000B

0x174		Graphic Display Active Window Horizontal Begin –hi	R/W
Bits	Name	Description	
7-4		Reserved	
3-0	GDH_ACT_BEG [11:8]	MSB of GDH_ACT_BEG	

Default: 0000 0000B

0x175		Graphic Display Active Window Horizontal Width –lo	R/W
Bits	Name	Description	
7-0	GDH_ACT_WID [7:0]	Graphic Display Active Window Horizontal Width. GDH_ACT_WID indicates how many pixels to display. GDH_ACT_WID =3, means displaying 3pixels.	

Default: 0000 0000B

0x176		Graphic Display Active Window Horizontal Width –hi	R/W
Bits	Name	Description	
7-4		Reserved	
3-0	GDH_ACT_WID [11:8]	MSB of GDH_ACT_WID	

Default: 0000 0000B

0x177		H Lock	R
Bits	Name	Description	
7-0	LOCK_RD_H [7:0]	Lock H position read back low byte	

Default: XXXX XXXXB

0x178		V Lock	R
Bits	Name	Description	
7-4	LOCK_RD_V [3:0]	Lock V position read back	
3-0	LOCK_RD_H [11:8]	Lock H position read back high byte	

Default: XXXX XXXXB

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Free Run Htotal Control

0x179	Free Run Horizontal Total –lo	R/W
Bits	Name	Description
7-0	FRH_TOTAL [7:0]	Free Run Horizontal Total Pixels. This register is used when MUTE_FR_EN = “1” (Reg. 0x159[5]). DH_TOTAL = 3 means there are 4 total pixels.

Default: 0000 0000B

0x17A	Free Run Horizontal Total –hi	R/W
Bits	Name	Description
7-4		Reserved
3-0	FRH_TOTAL [11:8]	MSB of DH_TOTAL

Default: 0000 0000B

0x17B~0x181 : Reserved

0x182	Auto Control H-total Read Back	R
Bits	Name	Description
7-0		Display auto mode H total read back

Default: XXXX XXXXB

0x183	Auto Control H-total Read Back	R
Bits	Name	Description
3-0		Display auto mode H total read back

Default: XXXX XXXXB

0x184	Residual Display HSYNC Control	R
Bits	Name	Description
7-0		Display manual mode residual HS count read back

Default: XXXX XXXXB

0x185	Residual Display HSYNC Control	R
Bits	Name	Description
7-0		Display manual mode residual HS count read back

Default: XXXX XXXXB

0x186	Residual Display Mode Control	R//W
Bits	Name	Description
7-0		0x00 for normal display HS/VS 0x10 for average HS , last HS cycle is same as others

Default: 00000 0000B

0x187~0x18C : Reserved

0x18D	Residual Display Mode Control	R/W
Bits	Name	Description
5		Internal circuit option for display manual mode , default “0x00”

Default: 0000 0000B

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FIFO Over/Under-flow Interrupt

0x18E	FIFO Interrupt Flag	R
Bits	Name	Description
1	INT_FFOV	FIFO over-flow interrupt flag
0	INT_FFUN	FIFO under-flow interrupt flag

Default: XXXX XXXXB

0x18E	FIFO Interrupt Flag Clear	W
Bits	Name	Description
1	CLR_FFOV	Writing '1' will clear INT_FFOV flag
0	CLR_FFUN	Writing '1' will clear INT_FFUN flag

Default: 0000 0000B

0x18F	FIFO Interrupt Enable	R/W
Bits	Name	Description
7-2		Reserved
1	INT_FFOV_EN	FIFO over-flow interrupt enable
0	INT_FFUN_EN	FIFO under-flow interrupt enable

Default: 0000 0000B

0x190 : Reserved

0x191	FIFO Control	R/W
Bits	Name	Description
7	BP_VI	Bypass the VI (vertical interpolation) data and power down the clock For up scaling
6	BP_HI	Bypass the HI (horizontal interpolation) data and power down the clock For up scaling
5	BP_SRGB	Bypass the SRGB data and power down the clock
4	BP_VC	Bypass the VC (vertical compression) data and power down the clock For down scaling
3	BP_HC	Bypass the HC (horizontal compression) data and power down the clock For down scaling
2	GR_AUTO_CLK	FIFO reference clock control auto select enable 0 = Disable 1 = Enable
1-0	GR_FIFO_CLK_SEL [1:0]	FIFO reference clock control source select 00 = Graphic clock 01 = Video clock

Default: 0000 0100B

0x192 ~ 0x195 : Reserved

8.24. Sync Processor

- H/V sync frequency counter & polarity detection
- H/V sync frequency change detection
- Composite/separate auto-switch
- Interlaced/progressive input detection
- Programmable free-run H/V frequency
- Status change interrupt

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Graphic Sync Processor Control

0x196	Graphic SYNC Processor Control 1	R/W
Bits	Name	Description
7	DVI_SYNC_SEL	Select the SYNC input source when DVI interface is enabled. 0 = From DVI DE signal 1 = From DVI HS/VS signal
6	HPLL_HS_INV	Invert the HPLL output HS polarity 0 = Normal 1 = Invert
5-4	GI_HS_SRC [1:0]	Select the HSYNC input source to sync processor and core logic. 00 = HPLL_HS -> sync processor and core logic 01 = RAW_HS -> sync processor and core logic 10 = RAW_HS -> sync processor and HPLL_HS -> core logic 11 = SOG_HS-> sync processor and core logic
3-2	GI_VCNT_BIT [1:0]	Select the bit number of GI_VCNT. 00 = 11-bit. Overflow freq = 27.32Hz 01 = 12-bit. Overflow freq = 13.66Hz 1X = 13-bit. Overflow freq = 6.83Hz
1-0	GI_SYNC_TYPE [1:0]	Graphic sync type select. 00 = Separate SYNC 01 = Composite SYNC 1X = Reserved

Default: 0001 0110B

0x197	Graphic SYNC Processor Control 2	R/W
Bits	Name	Description
7-6		Reserved
5	GI_VRUN_EN	VSYNC output free run enable 0 = Disable 1 = Enable
4	GI_HRUN_EN	HSYNC output free run enable 0 = Disable 1 = Enable
3	GI_VSO_POL	VSYNC output polarity control 0 = Active low 1 = Active high
2	GI_HSO_POL	HSYNC output polarity control 0 = Active low 1 = Active high
1	INT_VSO_EN	Internal VS output pin-113 enable 0 = Enable 1 = Disable
0	INT_HSO_EN	Internal HS output pin-114 enable 0 = Enable 1 = Disable

Default: 1000 1111B

Interlace Detector Control

0x198	Graphic Field Decision Window	R/W
Bits	Name	Description

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7-4	GI_FLD_WINEDN [3:0]	Define the end position of graphic field decision window.
3-0	GI_FLD_WINBEG [3:0]	The G_HS period is divided into 16 segments; a field decision window is defined by GI_FLD_WINBEG and GI_FLD_WINEND. GI_FLD_WINBEG defines the window begin position, and GI_FLD_WINEND defines the end position. If the G_VS reference edge locates inside the window, it means ODD field.

Default: 0100 1100B

0x199	Graphic SYNC Processor Control 3	R/W
Bits	Name	Description
7-2		Reserved
1	GI_FLD_EDGE	Select the reference edge of VSYNC in Graphic Field Detector 0 = Leading edge 1 = Trailing edge
0	GI_FLD_INV	Invert the polarity of Graphic Field Detector output signal from sync processor 0 = Normal 1 = Invert

Default: 0000 0000B

Sync Status

0x19A	Graphic Sync Processor Status	R
Bits	Name	Description
7	GI_VCNT_OV	GI_VCNT overflow flag 0 = Non-overflow 1 = Overflow
6	GI_HCNT_OV	GI_HCNT overflow flag 0 = Non-overflow 1 = Overflow
5	GI_CSPRE	Composite SYNC present flag 0 = Non-present 1 = Present
4	GI_VPRE	VSYNC present flag 0 = Non-present 1 = Present
3	GI_HPRE	HSYNC present flag 0 = Non-present 1 = Present
2	GI_INTE	Interlace input detected flag 0 = Progressive input 1 = Interlaced input
1	GI_VPOL	VSYNC polarity 0 = Active low 1 = Active high
0	GI_HPOL	HSYNC polarity 0 = Active low 1 = Active high

Default: XXXX XXXXB

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H/V Sync Counter

0x19B	Graphic HSYNC Counter –lo	R
Bits	Name	Description
7-0	GI_HCNT [7:0]	Hsync period counter. GI_HCNT is the number of clock (=REFCLK/4) in the period of 32x HSYNC. Hfreq = (REFCLK x 32)/(4 x GI_HCNT) Hz

Default: XXXX XXXXB

0x19C	Graphic HSYNC Counter –hi	R
Bits	Name	Description
4-0	GI_HCNT [12:8]	MSB of GI_HCNT

Default: XXXX XXXXB

0x19D	Graphic VSYNC Counter –lo	R
Bits	Name	Description
7-0	GI_VCNT [7:0]	Vsync period counter. GI_VCNT is a 12-bit counter; counter value is the number of clock (=REFCLK/256) between two VSYNC pulses. Vfreq = REFCLK/(256 x GI_VCNT)

Default: XXXX XXXXB

0x19E	Graphic VSYNC Counter –hi	R
Bits	Name	Description
4-0	GI_VCNT [12:8]	MSB of GI_VCNT.

Default: XXXX XXXXB

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H/V Free Run Divider

0x19F	HSO Free Run Divider –lo	R/W
Bits	Name	Description
7-0	HFREE_DIV [7:0]	HSYNC output to sync processor free-run divider value. HSYNC pulse width = 15x REFCLK Hfreq (free-run) = REFCLK/(HFREE_DIV+1) 0~511

Default: 0010 0111B

0x1A0	HSO Free Run Divider –hi	R/W
Bits	Name	Description
7-1		Reserved
0	HFREE_DIV [8]	MSB of HFREE_DIV

Default: 0000 0001B

0x1A1	VSO Free Run Divider –lo	R/W
Bits	Name	Description
7-0	VFREE_DIV [7:0]	VSYNC output to sync processor free-run divider value. VSYNC pulse width = 3x HFREE Vfreq (free-run) = Hfreq (free-run)/ (VFREE_DIV+1) 0~2048

Default: 0010 0110B

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0x1A2		VSO Free Run Divider –hi	R/W
Bits	Name	Description	
7-3		Reserved	
2-0	VFREE_DIV [10:8]	MSB of VFREE_DIV	

Default: 0000 0011B

H/V Present Threshold

0x1A3		HSYNC Present Low Count Threshold	R/W
Bits	Name	Description	
7		Reserved	
6-0	HPRE_THR_LO [6:0]	Hsync non-present counter threshold 1 (0H)~127 (7EH) Not-present when Hfreq < REFCLK / (4 x 8192 x HPRE_THR_LO) Hz	

Default: 0010 1101B

0x1A4		HSYNC Present High Count Threshold	R/W
Bits	Name	Description	
7		Reserved	
6-0	HPRE_THR_HI [6:0]	Hsync present counter threshold 1 (0H)~127 (7EH) Present when Hfreq > REFCLK / (4 x 8x HPRE_THR_HI) Hz	

Default: 0010 1100B

0x1A5		VSYNC Present Low Count Threshold	R/W
Bits	Name	Description	
7		Reserved	
6-0	VPRE_THR_LO [6:0]	Vsync non-present counter threshold 1 (0H)~127 (7EH) Not-present when Vfreq < REFCLK / (4 x 8192 x VPRE_THR_LO) Hz	

Default: 0010 1100B

0x1A6		VSYNC Present High Count Threshold	R/W
Bits	Name	Description	
7		Reserved	
6-0	VPRE_THR_HI [6:0]	Vsync present counter threshold 1 (0H)~127 (7EH) Present when Vfreq > REFCLK / (4 x 2048x VPRE_THR_HI) Hz	

Default: 0010 1100B

H/V Frequency Change Threshold

0x1A7		HSYNC Freq Change Threshold	R/W
Bits	Name	Description	
7-0	HCNT_THR [7:0]	HSYNC counter value change threshold for mode change detection. 1~256	

Default: 0000 0000B

0x1A8		VSYNC Freq Change Threshold	R/W
Bits	Name	Description	
7-5	H_CHANG_CNT	The INT_HFREQ will occur if the times out of HSYNC frequency change	

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		time are more than CHANG_CNT setting. 000~111: 1, 4, 8, ~ 28 times
4-0	VCNT_THR [4:0]	VSYNC counter value change threshold for mode change detection. 1~32

Default: 0000 0000B

Interrupt Control

0x1A9		**SYNC Interrupt Enable 1**	**R/W**
Bits	Name	Description	
7	INT_INV	Invert the polarity of IRQn output signal 0 = Normal 1 = Invert	
5	INT_VFREQ_EN	VSYNC frequency change interrupt enable 0 = Disable 1 = Enable	
4	INT_HFREQ_EN	HSYNC frequency change interrupt enable 0 = Disable 1 = Enable	
3	INT_VPOL_EN	VSYNC polarity change interrupt enable 0 = Disable 1 = Enable	
2	INT_HPOL_EN	HSYNC polarity change interrupt enable 0 = Disable 1 = Enable	
1	INT_VEDGE_EN	VSYNC rising edge occur interrupt enable 0 = Disable 1 = Enable	
0	INT_HEDGE_EN	HSYNC rising edge occur interrupt enable 0 = Disable 1 = Enable	

Default: 1000 0000B

0x1AA		**SYNC Interrupt Enable 2**	**R/W**
Bits	Name	Description	
7-5		Reserved	
4	INT_DVIPRE_EN	DVI SYNC present or non-present interrupt enable 0 = Disable 1 = Enable	
3	INT_ISPRE_EN	Interlaced SYNC present or non-present interrupt enable 0 = Disable 1 = Enable	
2	INT_CSPRE_EN	Composite SYNC present or non-present interrupt enable 0 = Disable 1 = Enable	
1	INT_VPRE_EN	VSYNC present or non-present interrupt enable 0 = Disable 1 = Enable	
0	INT_HPRE_EN	HSYNC present or non-present interrupt enable 0 = Disable 1 = Enable	

Default: 0000 0000B

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0x1AB		SYNC Interrupt Flag 1	R
Bits	Name	Description	
5	INT_VFREQ	VSYNC frequency change interrupt	
4	INT_HFREQ	HSYNC frequency change interrupt	
3	INT_VPOL	VSYNC polarity change interrupt	
2	INT_HPOL	HSYNC polarity change interrupt	
1	INT_VEDGE	VSYNC rising edge occur interrupt	
0	INT_HEDGE	HSYNC rising edge occur interrupt	

Default: XXXX XXXXB

0x1AC		SYNC Interrupt Flag 2	R
Bits	Name	Description	
4	INT_DVIPRE	DVI SYNC present or non-present interrupt	
3	INT_ISPRE	Interlaced SYNC present or non-present interrupt	
2	INT_CSPRE	Composite SYNC present or non-present interrupt	
1	INT_VPRE	VSYNC present or non-present interrupt	
0	INT_HPRE	HSYNC present or non-present interrupt	

Default: XXXX XXXXB

0x1AB		SYNC Interrupt Flag 1 Clear	W
Bits	Name	Description	
7-6		Reserved	
5	CLR_VFREQ	Writing ‘1’ will clear INT_VFREQ flag	
4	CLR_HFREQ	Writing ‘1’ will clear INT_HFREQ flag	
3	CLR_VPOL	Writing ‘1’ will clear INT_VPOL flag	
2	CLR_HPOL	Writing ‘1’ will clear INT_HPOL flag	
1	CLR_VEDGE	Writing ‘1’ will clear INT_VEDGE flag	
0	CLR_HEDGE	Writing ‘1’ will clear INT_HEDGE flag	

Default: 0111 1111B

0x1AC		SYNC Interrupt Flag 2 Clear	W
Bits	Name	Description	
7-5		Reserved	
4	CLR_DVIPRE	Writing ‘1’ will clear INT_DVIPRE flag	
3	CLR_ISPRE	Writing ‘1’ will clear INT_ISPRE flag	
2	CLR_CSPRE	Writing ‘1’ will clear INT_CSPRE flag	
1	CLR_VPRE	Writing ‘1’ will clear INT_VPRE flag	
0	CLR_HPRE	Writing ‘1’ will clear INT_HPRE flag	

Default: 0000 0000B

0x1AD		DVI Sync Status	R
Bits	Name	Description	
7-2		Reserved	
1	DVI_DEPOL	DVI DE polarity. 0 = Active low 1 = Active high	
0	DVI_SCDT	DVI Sync Detect. 0 = When DE is inactively, indicating the link is down 1 = When DE is actively toggling indicating that the link is alive. The SCDT output itself, however, remains in the active mode at all times.	

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Default: XXXX XXXXB

Video Sync Processor Control

0x1AE	Video Sync Processor Status	R
Bits	Name	Description
2	VI_INTE	Interlace input detected flag 0 = Progressive input 1 = Interlaced input
1	VI_VPOL	VSYNC polarity 0 = Active low 1 = Active high
0	VI_HPOL	HSYNC polarity 0 = Active low 1 = Active high

Default: XXXX XXXXB

0x1AF	HS Auto De-bouncing	R/W
Bits	Name	Description
7	V_FRONT_BOUNCE	Read-back V front status 0: No bouncing happen 1: Bouncing happen at V front porch , write “1” to clear this flag
6	V_BACK_BOUNCE	Read-back V back status 0: No bouncing happen 1: Bouncing happen at V back porch , write “1” to clear this flag
5	DEBOUNCE_DEL	De-bounce manual mode delay enable 0: Disable 1: Enable
4	DEBOUNCE_AUTO	0: De-bounce auto mode 1: De-bounce manual mode
3		Reserved
2	DEBOUNCE_EN	De-bounce enable
1		Reserved
0	COMP_H_INS	Composite H insertion mode

Default: 0000 1100B

0x1B0	Field Polarity Control	R/W
Bits	Name	Description
7-1		Reserved
0	VI_FLD_INV	Invert the polarity of Video Field Detector output signal 0 = Normal 1 = Invert

Default: 0000 0000B

0x1B1	Hsync Pulse width counter	R/W
Bits	Name	Description
7-0	GI_HS_WID [7:0]	Hsync pulse width counter. GI_HS_WID is the number of REFCLK in the period of HSYNC. Hpswid = (1/REFCLK x GI_HS_WID)

Default: 0110 0100B

0x1B2	Vsync Pulse width counter	R/W

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Bits	Name	Description
7-0	GI_VS_WID [7:0]	Vsync pulse width counter. GI_VS_WID is the number of clock in the period of HSYNC.

Default: 0000 0000B

0x1B3		R/W
Bits	Name	Description
7-0	PRE_COAST	Sets the number of Hsync periods that coast becomes active prior to Vsync to separate input composite sync

Default: 0000 0000B

0x1B4		R/W
Bits	Name	Description
7-0	POS_COAST	Sets the number of Hsync periods that coast stays active following Vsync to separate input composite sync

Default: 0000 0000B

0x1B5	Graphic Vtotal Counter-lo	R
Bits	Name	Description
7-0	GI_VTOTAL [7:0]	Vertical total counter. GI_VTOTAL is an 11-bit counter, counter value is the number of Hsync between two VSYNC pulses.

Default: XXXX XXXXB

0x1B6	Graphic Vtotal Counter-hi	R
Bits	Name	Description
2-0	GI_VTOTAL [10:8]	MSB of GI_VTOTAL

Default: XXXX XXXXB

0x1B7 : Reserved

8.25. LVDS Output Control

0x1B8	LVDS Output Control	R/W
Bits	Name	Description
7	LVDS_POL_SWAP	LVDS Channel Polarity Swap (Positive/Negative) 0 = Normal 1 = Enable
6	LVDS_CH_SWAP	LVDS Channel Swap 0 = Normal 1 = Enable, When enable, T0/T3 swap, TCLK1/T1 swap, T4/T7 swap, TCLK2/T5 swap
5-3	LVDS_LEVEL [2:0]	Fine tune LVDS output differential voltage 000: Standard output 200 mVp-p 001: Output 250 mVp-p 010: Output 300 mVp-p 011: Output 450 mVp-p 100~111: Reserved

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2-1	LVDS_ICO [1:0]	Charge pump current 00 : 60uA 01 : 100uA 10 : 200uA 11 : 320uA
0	LVDS_RFB	Data strobe edge selection 0 = falling edge strobe 1 = rising edge strobe

Default: 0000 0000B

0x1B9	Display Output Interface Control	R/W
Bits	Name	Description
7-2		Reserved
1	DOS_SEL	Display output interface selection when timing controller disable 0 = LVDS
0		Reserved

Default: 0001 0000B

0x1BA : Reserved

0x1BB	Auto offset Control -1	R/W
Bits	Name	Description
7	AO_SATU_PRETECT	Auto offset saturation protect (for clamp 0V mode only) 0: Disable (for YpbPr mode) 1: Enable (for RGB mode)
6-5		Reserved
4-0	CALCUL_PERIOD	Define the period of data calculation that start from falling edge of clamp pulse + 8T Set “1” mean is 1x8+7=15 pixel be calculated for auto offset

Default: 0000 0000B

0x1BC	Auto offset Control -2	R/W
Bits	Name	Description
7	AO_LINE_MODE_RDY	Auto offset line mode ready, When detection is finished, this bit is set to “1”
6	AO_LINE_MODE	Auto offset line mode enable 0 = Disable 1 = Enable
5-1		Reserved
1		Default “1” for auto offset enable
0	AO_EN	Auto offset enable 0 = Disable 1 = Enable

Default: 0000 0000B

0x1BD	Auto offset target value of Red channel	R/W
Bits	Name	Description
7-0	AO_RVALUE	

Default: 0000 0000B

0x1BE	Auto offset target value of Green channel	R/W

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Bits	Name	Description
7-0	AO_GVALUE	

Default: 0000 0000B

0x1BF	Auto offset target value of Blue channel	R/W

Bits	Name	Description
7-0	AO_RVALUE	

Default: 0000 0000B

0x1C0	Auto offset adjust value – Red channel	R

Bits	Name	Description
7-0	AO_ADJ_RVALUE	

Default: 0000 0000B

0x1C1	Auto offset adjust value – Green channel	R

Bits	Name	Description
7-0	AO_ADJ_GVALUE	

Default: 0000 0000B

0x1C2	Auto offset adjust value – Blue channel	R

Bits	Name	Description
7-0	AO_ADJ_RVALUE	

Default: 0000 0000B

0x1C3	Auto offset mid value read back – Red channel	R

Bits	Name	Description
7-0	AO_MID_RVALUE	

Default: 0000 0000B

0x1C4	Auto offset mid value read back – Green channel	R

Bits	Name	Description
7-0	AO_MID_GVALUE	

Default: 0000 0000B

0x1C5	Auto offset mid value read back – Blue channel	R

Bits	Name	Description
7-0	AO_MID_RVALUE	

Default: 0000 0000B

0x1C6~0x1CB : Reserved

0x1CC	Asynchronous Random dithering Control	R/W

Bits	Name	Description
7-3		Reserved
2	DP_ARD_EN	Display asynchronous random dithering enable 0x1DA.4 or 0x1DA.5 must enable
1	GA_ARD_EN	Gamma asynchronous random dithering enable 0x158.2 set “1”
0	SRGB_ARD_EN	SRGB asynchronous random dithering enable

Default: 0000 0000B

0x1CD~0x1CF : Reserved

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8.26. sRGB Control

0x1D0	sRGB Control	R/W
Bits	Name	Description
7	BF_SRGB_EN	Bright frame sRGB enable
6	SRGB_TBL_SEL	sRGB access select 0: Normal sRGB 1: Bright frame sRGB
5	SRGB_DITH_EN	sRGB dithering enable , 0X1D0.0 must set “1”
4	RANDOM_DITH_EN	0: Static dithering enable 1: Random dithering enable
3	SRGB_FORCE_UPD	Force update sRGB 0: Disable 1: Force update the sRGB Coefficient to H/W , if 0x161[1:0] set “11” then these sRGB register update on next DVS
2-1	SRGB_BK_SEL	Select sRGB 3x3 matrix Row bank 00 = Row1 01 = Row2 10 = Row3 11 = Reserved
0	SRGB_En	sRGB Enable 0: Disable 1: Enable

Default: 0000 1000B

0x1D1	sRGB Transfer Coefficient R Channel – lo	R/W
Bits	Name	Description
7-0	SRGB_COLUM_1 [7:0]	sRGB 3x3 matrix Column 1 coefficient LSB -1024 ~ 1023

Default: 0000 0000B

0x1D2	sRGB Transfer Coefficient R Channel – hi	R/W
Bits	Name	Description
2-0	SRGB_COLUM_1 [10:8]	sRGB 3x3 matrix Column 1 coefficient MSB

Default: 0000 0001B

0x1D3	sRGB Transfer Coefficient G Channel – lo	R/W
Bits	Name	Description
7-0	SRGB_COLUM_2 [7:0]	sRGB 3x3 matrix Column 2 coefficient LSB -1024 ~ 1023

Default: 0000 0000B

0x1D4	sRGB Transfer Coefficient G Channel – hi	R/W
Bits	Name	Description
2-0	SRGB_COLUM_2 [10:8]	sRGB 3x3 matrix Column 2 coefficient MSB

Default: 0000 0000B

0x1D5	sRGB Transfer Coefficient B Channel – lo	R/W
Bits	Name	Description

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7-0	SRGB_COLUM_3 [7:0]	sRGB 3x3 matrix Column 3 coefficient LSB -1024 ~ 1023

Default: 0000 0000B

0x1D6	sRGB Transfer Coefficient B Channel – hi	R/W
Bits	Name	Description
2-0	SRGB_COLUM_3 [10:8]	sRGB 3x3 matrix Column 3 coefficient MSB

Default: 0000 0000B

0x1D7	sRGB Offset Coefficient	R/W
Bits	Name	Description
7-0	SRGB_COEF_OFFSET [7:0]	The offset coefficient of sRGB matrix -7F ~ 7F

Default: 1000 0000B

0x1D8	sRGB Dithering Control 1	R/W
Bits	Name	Description
7	RANDOM_RST	Display random dither reset mode (0x1ED[4] must set “1”) 0: Disabel 1: Enable
6		Reserved
5-4	DITH_10	“10” dithering type , 0x1D0.4 must set “0”
3		Reserved
2-0	DITH_01	“01” dithering type , 0x1D0.4 must set “0”

Default: 0000 0000B

0x1D9 : Reserved

0x1DA	Display Random Dithering Control	R/W
Bits	Name	Description
7		Reserved
6	RST_PERIOD	Random reset period setting 0 = 1 frame 1 = if DITH_TURBO (Reg. 0x158[1]) set to “1”, the period is 4 frame else the period is 16 frame
5	MIX_DITH_EN	Display Mix mode Dithering Enable 0: Disable 1: Enable
4	RANDOM_EN	Random dithering mode enable
3-2	STATIC_CNT	Static dithering active period counter 0x1DA.5 must enable
1-0	RANDOM_CNT	Random dithering active period counter 0x1DA.5 must enable

Default: 0000 0111B

0x1DB	Gamma Dithering Control	R/W
Bits	Name	Description
7-6		Reserved
5-4	DITH_10	“10” dithering type , 0x158.2 must set “0” , 0x1DB.7 set “0”
3		Reserved

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2-0	DITH_01	“01” dithering type , 0x158.2 must set “0” , 0x1DB.7 set “0”

Default: 0000 0000B

0x1DC ~ 0x1E5 : Reserved

0x1E6		ADC test mode Control	R/W
Bits	Name	Description	
7		Internal LDO 0: 1.8V (resistor) 1: 1.6V (bandgap)	
6		Reserved	
5		Internal LDO 0: 1.8V (resistor) 1: 1.6V (bandgap)	
4-1		Reserved	
0	RSTB	Reset ADC data to low 0: Reset 1: Normal	

Default：0000 0001B

0x1E7		HPLL LDO	R/W
Bits	Name	Description	
7-2		Reserved	
1	HPLL _LDO	HPLL LDO 0: 1.8V (bandgap) 1: 1.6V (resistor)	
0	PAGE3_OPTION	Page 3 function option 0: HDCP control 1: DVI auto equalize	

Default：0100 0000B

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0x1E8 ~ 0x1EC : Reserved

0x1ED		ADC Power Cotrol	R/W
Bits	Name	Description	
7		Reserved	
6	ADC_BIAS[3]	ADC OP bios select MSB , 0x1F1 for LSB	
5	BW[3]	ADC bandwidth MSB	
3	BG_SEL	ADC BIOS 0: Reseistor 1: Bandgap	
2-0		Reserved	

Default：0000 0000B

0x1EE		Power Down Control	R/W
Bits	Name	Description	
7		Reserved	
6	BF_PWN	BF bypass for power down	
5	OSD_PWN	OSD bypass for power down	
4	GAMMA_PWN	Gamma bypass for power down	
3	DIS_DITHER_PWN	Display dither bypass for power down	

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2	GAMMA_DITHER_PWN	Gamma dither bypass for power down
1		Reserved
0	sRGB_PWN	sRGB bypass for power down

Default：0000 0010B

0x1EF		LVDS Control	R/W
Bits	Name	Description	
7-3		Reserved	
2	LVDS_PWR	0: LVDS off 1: LVDS on	
1-0		Reserved	

Default：0000 0100B

0x1F0 : Reserved

0x1F1		ADC Control	R/W
Bits	Name	Description	
7-6		Reserved	
5-4	RADC_BIAS[1:0]	RADC OP bios select	
3-2	GADC_BIAS[1:0]	RADC OP bios select	
1-0	BADC_BIAS[1:0]	RADC OP bios select	

Default：0011 1111B

0x1F2 ~ 0x1F3 : Reserved

0x1F4		LVDS Control	R/W
Bits	Name	Description	
7-0		LVDS internal circuit control option	

Default：1000 0010B

0x1F5		LVDS Control	R/W
Bits	Name	Description	
7		Reserved	
6	LVDS_OFFSET	LVDS offset voltage source 0: Band gap 1: Resistor	
5		Reserved	
4	PULL_LOW	LVDS output power down buffer control 0: Pull low output 1: Tri-state output	
3-0		For internal circuit option	

Default：0000 0000B

0x1F6		LVDS Control	R/W
Bits	Name	Description	
7-0		LVDS internal circuit control option	

Default：0000 0000B

0x1F7		LVDS Control	R/W
Bits	Name	Description	

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7	PD_LV1	LVDS port A power control 0: Power down 1: Power up
6	PD_LV2	LVDS port B power control 0: Power down 1: Power up
5-0		Reserved

Default：0010 0010B

0x1F8 ~ 0x1F9 : Reserved

0x1FA		LVDS Control	R/W
Bits	Name	Description	
7		LVDS internal circuit control option	

Default：0000 0000B

0x1FB ~ 0x1FE : Reserved

0x1FF		Accessing Register Page Enable	R/W
Bits	Name	Description	
7-2		Reserved	
1-0	REG_PAGE_SEL	Register Page Enable 000: Enable register Page0. 001: Enable register Page1. 010: Enable register Page2. 011: Enable register Page3. 100: Enable register Page4.	

Default: 0000 0000B

0x200 ~ 0x2FE : Reserved

0x2FF		Accessing Register Page Enable	R/W
Bits	Name	Description	
7-2		Reserved	
1-0	REG_PAGE_SEL	Register Page Enable 000: Enable register Page0. 001: Enable register Page1. 010: Enable register Page2. 011: Enable register Page3. 100: Enable register Page4.	

Default: 0000 0000B

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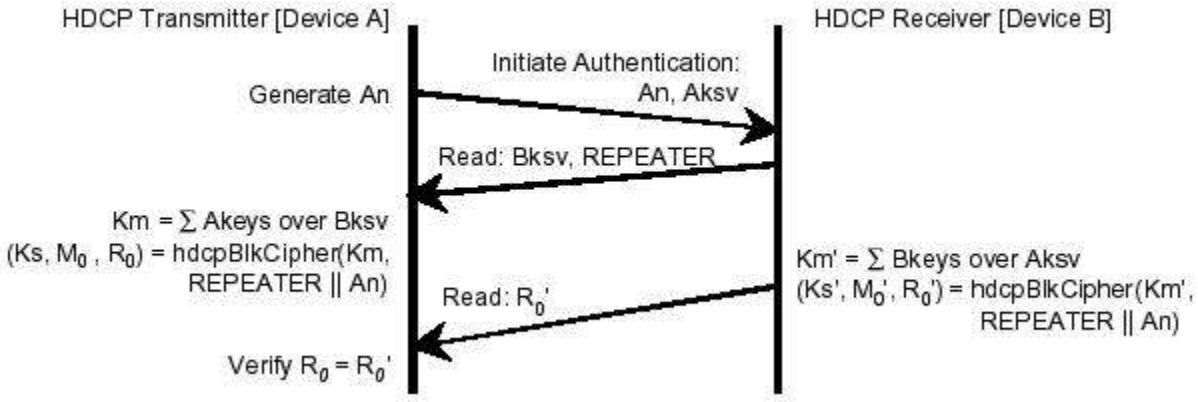
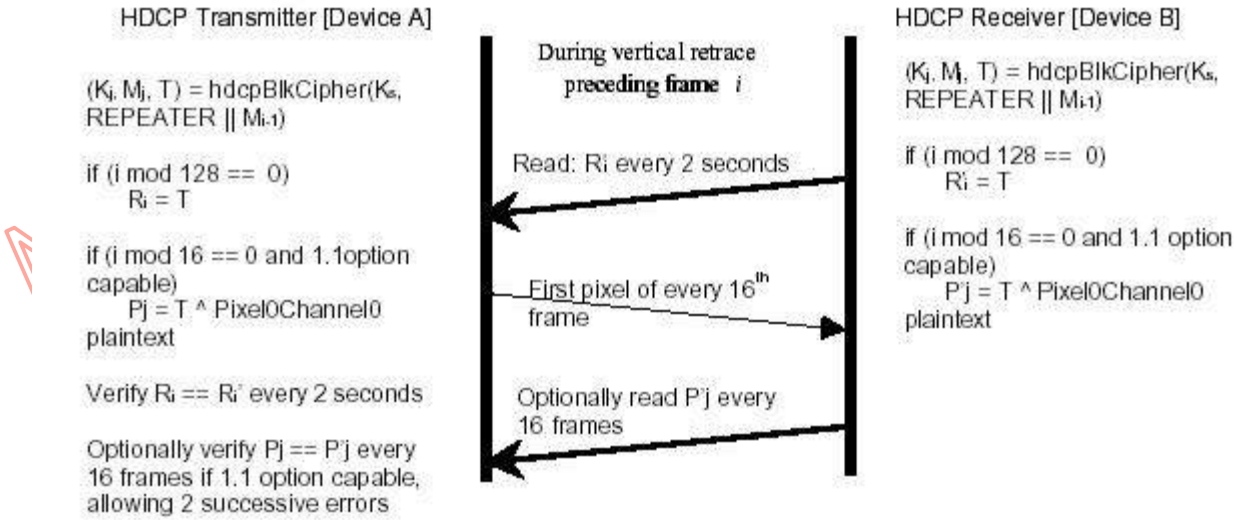
8.27. High-bandwidth Digital Content Protection System

HDCP Index Port Access Control

See section 9.14 Index Port Access Control

HDCP Control Register Map





ADDRESS	R/W	Register Name	Description
0x300 ~ 0x301 ~ 0x302 ~ 0x303 ~ 0x304	R	BKSV[7:0] BKSV[15:8] BKSV[23:16] BKSV[31:24] BKSV[39:32]	For transmitter read only Video receiver KSV. This value must always be available for reading, and may be used to determine that the video receiver is HDCP capable. Valid KSVs contain 20 ones and 20 zeros, a characteristic that must be verified by video transmitter hardware before encryption is enable.
0x305 ~ 0x307	R	RESERVED	Reserved All bytes read as 0x00
0x308 ~ 0x309	R	Ri'[7:0] Ri'[15:8]	For transmitter read only Link verification response. Updated every 128 th frame. It is recommended that graphics systems protect against errors in the I2C transmission by reading this value when unexpected values are received. This value must be available at all times between updates. R0' must be available a maximum of 100ms after AKSV is received. Subsequent Ri' values must be available a maximum of

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			128 pixel clocks following the assertion of CTL3
0x30A	R	Pj'	For transmitter read only (for HDCP V1.1) Enhanced Link Verification Response. Updated upon receipt of first video pixel received when frame counter value (j mod 16) == 0. The value is the XOR of the decrypted byte on channel zero of the first video pixel with the least significant byte of Rj. Rj is derived from the output function in the same manner as Ri, but is captured every 16th counted frame (rather than every 128th counted frame).
0x30B~0x30F	R	RESERVED	Reserved All bytes read as 0x00
0x310 ~ 0x311 ~ 0x312 ~ 0x313 ~ 0x314	R	AKSV[7:0] AKSV[15:8] AKSV[23:16] AKSV[31:24] AKSV[39:32]	For transmitter write only HDCP Transmitter KSV. Writes to this multi-byte value are written least significant byte first. The final write to 0x14 triggers the authentication sequence in the HDCP Receiver, and the current *Ainfo* value is copied from the port, takes effect, and the port is reset to the default value of zero.
0x315	R	Ainfo	For transmitter write only Bits 7-2: Reserved zeros. Bit 1: ENABLE_1.1_FEATURES. This bit enables the Advance Cipher option. If in DVI mode, it also enables the Enhanced Encryption Status Signaling (EESS) (in HDMI mode, EESS is enabled regardless of this bit setting). This bit resets to default zero when the HDCP Receiver becomes attached or active, or is reset, or the last byte of Aksv is written. A write to the last byte of Aksv copies the port value and causes it to take effect, and then resets the port value to the default value of zero. Thus the options must be explicitly enabled prior to each authentication. Bit 0: Reserved (must be zero).
0x316 ~0x317	R	RESERVED	Reserved All bytes read as 0x00
0x318 ~ 0x319 ~ 0x31A ~ 0x31B ~ 0x31C ~ 0x31D ~ 0x31E ~ 0x31F	R	An[7:0] An[15:8] An[23:16] An[31:24] An[39:32] An[47:40] An[55:48] An[63:56]	For transmitter write only Session random number. This multi-byte value must be written by the HDCP Transmitter before the KSV is written.
0x320~0x33F			Reserved
0x340	W	Bcaps	For transmitter read only Bit 7-5: Reserved Bit 4: FAST. When set to one, this device supports 400 KHz transfers. When zero, 100 KHz is the maximum transfer rate supported. Note that 400KHz transfers are not permitted to any device unless all devices on the I2C bus are capable of 400KHz transfer. The transmitter may not be able to determine if the EDID ROM, present on the HDCP Receiver, is capable of 400KHz operation. This bit does not change while the HDCP Receiver is active. Bits 3-2: Reserved (must be zero). Bit 1: 1.1_FEATURES. When set to one, this HDCP Receiver supports Enhanced

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			Encryption Status Signaling (EESS), Advance Cipher, and Enhanced Link Verification options. For the HDMI protocol, Enhanced Encryption Status Signaling (EESS) capability is assumed regardless of this bit setting. This bit does not change while the HDCP Receiver is active. Bit 0: FAST_REAUTHENTICATION. When set to 1, the receiver is capable of receiving (unencrypted) video signal during the session re-authentication. All HDMI-capable receivers shall be capable of performing the fast re-authentication even if this bit is not set. This bit does not change while the HDCP Receiver is active. Default: 8'h11
0x341 ~ 0x342			Reserved
0x343	R	Ri' Frame count	Frame count status for Ri' update Default: 8'h00
0x344	R	Frame Pj'	Pj' value for every frame Default: 8'h00
0x345	R	Frame Ri'(l)	Ri' low byte value for every frame Default: 8'h00
0x346	R	Frame Ri'(h)	Ri' high byte value for every frame Default: 8'h00
0x347	R	MISC CTRL Status	Bit 7~ 4: Frame count status for Pj' update Bit 3: Authentication ok Bit 2: Km calculation finished Bit 1: Aksv bytes are all received Bit 0: Ainfo in effect Default: 8'h00
0x348	R	Mi' byte0	Mi' byte0 value for every frame Default: 8'h00
0x349	R	Mi' byte1	Mi' byte1 value for every frame Default: 8'h00
0x34A	R	Mi' byte2	Mi' byte2 value for every frame Default: 8'h00
0x34B	R	Mi' byte3	Mi' byte3 value for every frame Default: 8'h00
0x34C	R	Mi' byte4	Mi' byte4 value for every frame Default: 8'h00
0x34D	R	Mi' byte5	Mi' byte5 value for every frame Default: 8'h00
0x34E	R	Mi' byte6	Mi' byte6 value for every frame Default: 8'h00
0x34F	R	Mi' byte7	Mi' byte7 value for every frame Default: 8'h00
0x350	R	Ks' byte0	Ks' byte0 value of session key Default: 8'h00
0x351	R	Ks' byte1	Ks' byte1 value of session key Default: 8'h00
0x352	R	Ks' byte2	Ks' byte2 value of session key Default: 8'h00

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0x353	R	Ks' byte3	Ks' byte3 value of session key Default: 8'h00
0x354	R	Ks' byte4	Ks' byte4 value of session key Default: 8'h00
0x355	R	Ks' byte5	Ks' byte5 value of session key Default: 8'h00
0x356	R	Ks' byte6	Ks' byte6 value of session key Default: 8'h00
0x357	R	Ki' byte0	Ki' byte0 for every frame Default: 8'h00
0x358	R	Ki' byte1	Ki' byte1 for every frame Default: 8'h00
0x359	R	Ki' byte2	Ki' byte2 for every frame Default: 8'h00
0x35A	R	Ki' byte3	Ki' byte3 for every frame Default: 8'h00
0x35B	R	Ki' byte4	Ki' byte4 for every frame Default: 8'h00
0x35C	R	Ki' byte5	Ki' byte5 for every frame Default: 8'h00
0x35D	R	Ki' byte6	Ki' byte6 for every frame Default: 8'h00
0x35E	R/W	Authentication Built in Self Test Status	Bit 7: Self test done (read status) Bit 6: BIST is working (read status) Bit 5: R0' fault Bit 4: M0' fault Bit 3: Ks' fault Bit 2: Km' fault Bit 1: Self test fault happens due to Bit5~Bit2 faults Bit 0: Authentication BIST enable (use internal 2 test keys) Default: 8'h00
0x35F	R/W	Key set pair select for Authentication Built in Self Test	Bit7~Bit2: Reserved Bit1~0: (for self test) 00: A1-B1 key pair 01: A1-B2 key pair 10: A2-B1 key pair 11: A2-B2 key pair Default: 8'h00
0x360	R/W	HDCP Input Control	Bit 7: HDCP clk input from 1: Ref clk (for start up load key to HDCP address from eeprom) 0: pixel clk(TMDS) for normal operate Bit 6: HDCP clk input invert mode (TMDS clk) 1: clk inverted 0: clk non-inverted Bit 5~3: HDCP input DE pipe delay selection 000: no delay 001: 1T delay 010: 2T delay 011: 3T delay 100: 4T delay others: 5T delay

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			Bit 2~0: HDCP input data pipe delay selection 000: no delay 001: 1T delay 010: 2T delay 011: 3T delay 100: 4T delay others: 5T delay Default: 8'h80
0x361	R/W	HDCP Input Sync Selection	Bit 7~4: Reserved Bit 3 : HDCP Key Set Decryption (for key set decode that from eeprom) Bit 2 : Reserved Bit 1 : V Sync selection from separated sync or decomposed sync 1: decomposed sync (for DE mode) 0: separated sync Bit 0 : H Sync selection from separated sync or decomposed sync 1: decomposed sync 0: separated sync default : 8'h00
0x362	R	SRAM Status0	Bit7~0: SRAM address[7:0] for SRAM access (for debug only) Default: 8'h00
0x363	R	SRAM_Status1	Bit0: SRAM address[8] for SRAM access (for debug only) Bit1: SRAM Arbitration (for debug only) 1: Servicing for HDCP cipher machine request 0: Servicing for MCU read/write request (for initial HDCP) Default: 8'h00
0x364	R/W	Ri Update Frame Count	Bit7:0 For every this (Ri_update_frame_count+1) value is reached, the Ri value will be updated for constantly link check, for example, if 127 is set, then for every 128th frame count, the Ri value will be updated Default : 8'h7F
0x365~0x367	R		Reserved
0x368	R/W	HDCP Slave Address	Bit7~1: HDCP Slave Address on DDC I2C bus Bit0 : HDCP reset , 0: Normal , 1: Reset Defaut: 0x74
0x369	R	HDCP Status	Bit 7: TMDS control status bit 3 (read TMDS control bit) Bit 6: TMDS control status bit 2 Bit 5: TMDS control status bit 1 Bit 4: TMDS control status bit 0 Bit 3: HDCP enable 1: HDCP clock enable 0: HDCP clock disable (for power down) Bit 2: HDCP interrupt enable 1: interrupt enable while receiver first authentication ready . 0: interrupt disable Bit 1: Authentication done flag , write '1' to this bit will clear this flag to 0 Bit 0: AKSV transfer done flag , write '1' to this but will clear this flag to 0 Default: 8'h00
0x36A	R/W	Window of	Bit 7~0: Low byte of window of opportunity lower bound for eess

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		Opportunity Lower Bound	(EESS valid window start) Receive TMDS control bit 3 ~ 0 at 512th ~ 528th pixel from VS start edge , if this code is “1001” then indicate this frame is encrypted . Default: 8’h00
0x36B	R/W	Window of Opportunity Lower Bound	Bit 7~0: High byte of window of opportunity lower bound for eess Default: 8’h02
0x36C	R/W	Window of Opportunity Upper Bound	Bit 7~0: Low byte of window of opportunity upper bound for eess (EESS valid window end) Default: 8’h10
0x36D	R/W	Window of Opportunity Upper Bound	Bit 7~0: High byte of window of opportunity upper bound for eess Default: 8’h02

0x306		**DVI Auto Equalize-1**	**R/W**
Bits	Name	Description	
7-2		Reserved	
1-0	DVI_AUTO_CH_SEL	Detect channel setecl , 0x1E7.0 must set “1” and read-back from 0x317 ~ 0x31B 00 : Blue 01 : Green 10 : Red	

Default: 0000 0000B

0x308		**DVI Auto Equalize-2**	**R**
Bits	Name	Description	
7-3		Reserved	
2		For R □uality , read-back data if “1” indicate input data decode maybe is error , 0x309.0 for enable this function	
1		For G □uality , read-back data if “1” indicate input data decode maybe is error , 0x309.0 for enable this function	
0		For B □uality , read-back data if “1” indicate input data decode maybe is error , 0x309.0 for enable this function	

Default: 0000 0000B

0x309		**DVI Auto Equalize-3**	**R/W**
Bits	Name	Description	
7-1		Reserved	
0		DVI decode data check , write “1” and if read back “0” mean is ready for 0x308 read back 0: Disable 1: Enable	

Default: 0000 0000B

0x310		**DVI Auto Equalize-4**	**R/W**
Bits	Name	Description	
7-0		Set 0x13 for 0x317 ~ 0x31B read-back function Bit-0 write “1” and if read back “0” mean is ready for 0x317 ~ 0x31B read back	

Default: 0000 0000B

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0x311		DVI Auto Equalize-5	R/W
Bits	Name	Description	
7-0		Set 0x55 for 0x317 ~ 0x31B check cycle is 1V	

Default: 0000 0000B

0x317 ~0x31B		DVI Auto Equalize-6	R
Bits	Name	Description	
7-0		DVI eye diagram quality check , more continue “0” mean is better signal □uality . Set 0x01E is “0x08 ~ 0x38” , “0xBF” , “0xEF” , “0xFF” to get better setting .	

Default: 0000 0000B

0x338		DVI AC Couple	R/W
Bits	Name	Description	
7		DVI CLK AC couple 0: Disable 1: Enable	
6-4		DVI RGB AC couple 0: Disable 1: Enable	
3-0		Reserved	

Default: 0111 1100B

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8.28. Dithering Function 2

0x370		Dither block blending control	R/W
Bits	Name	Description	
7	LSB10_BLEND_TYPE	0: Static and dynamic ordered blending . 1: Random and dynamic ordered blending .	
6	LSB01/11_BLEND_TYPE	0: Static and dynamic ordered blending . 1: Random and dynamic ordered blending .	
5	LSB10_BLEND_EN	0: Disable . 1: Enable .	
4-3	LSB10_BLEND_LOGIC_OP	00: Or . 01: Xor . 10: Xor . 11: And .	
2	LSB01/11_BLEND_EN	0: Disable . 1: Enable .	
1-0	LSB01/11_BLEND_LOGIC_OP	00: Or . 01: Xor . 10: Xor . 11: And .	

Default: 0000 0000B

0x371		Dither Toggle / Mix Control	R/W
Bits	Name	Description	
7		Reserved	
6		mix_3in1_dither_en(B) , 0x371.1 must set “1”	
5		mix_3in1_dither_en® , 0x371.1 must set “1”	

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4		mix_3in1_dither_en(G)
3-2		Reserved
1		0: R/G/B control depends on G channel 1: Use separate control registers
0	BLOCK_TOGGLE_EN	0: Disable . 1: Enable . .(0x370 blend must enable)

Default: 0000 0000B

0x372		Separate R Dithering Control-1	R/W
Bits	Name	Description	
7-4		R channel “10“ dithering option , 0x371.1 must set “1“	
3-0		R channel dither mode , , 0x371.1 must set “1“	

Default: 0000 0000B

0x373		Separate R Dithering Control-2	R/W
Bits	Name	Description	
7-6		Reserved	
5		Mixed dither enable	
4		Dynamic dither	
3-2		Dynnmic mode [1:0]	
1-0		Static mode [1:0]	

Default: 0000 0000B

0x374		Separate R Dithering Control-3	R/W
Bits	Name	Description	
7	LSB10_BLEND_TYPE	0: Static and dynamic ordered blending . 1: Random and dynamic ordered blending .	
6	LSB01_BLEND_TYPE	0: Static and dynamic ordered blending . 1: Random and dynamic ordered blending .	
5	LSB10_BLEND_EN	0: Disable . 1: Enable .	
4-3	LSB10_BLEND_LOGIC_OP	00: Or . 01: Xor . 10: Xor . 11: And .	
2	LSB01_BLEND_EN	0: Disable . 1: Enable .	
1-0	LSB01_BLEND_LOGIC_OP	00: Or . 01: Xor . 10: Xor . 11: And .	

Default: 0000 0000B

0x375		Separate B Dithering Control-1	R/W
Bits	Name	Description	
7-4		B channel “10“ dithering option , 0x371.1 must set “1“	
3-0		B channel dither mode [3:0] , , 0x371.1 must set “1“	

Default: 0000 0000B

0x376		Separate B Dithering Control-2	R/W
Bits	Name	Description	

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7-6		Reserved
5		Mixed dither enable
4		Dynamic dither
3-2		Dynnmic mode [1:0]
1-0		Static mode [1:0]

Default: 0000 0000B

0x377		**Separate B Dithering Control-3**	**R/W**
Bits	Name	Description	
7	LSB10_BLEND_TYPE	0: Static and dynamic ordered blending . 1: Random and dynamic ordered blending .	
6	LSB01_BLEND_TYPE	0: Static and dynamic ordered blending . 1: Random and dynamic ordered blending .	
5	LSB10_BLEND_EN	0: Disable . 1: Enable . 0x371.0 must set “1“	
4-3	LSB10_BLEND_LOGIC_OP	00: Or . 01: Xor . 10: Xor . 11: And .	
2	LSB01_BLEND_EN	0: Disable . 1: Enable . 0x371.0 must set “1“	
1-0	LSB01_BLEND_LOGIC_OP	00: Or . 01: Xor . 10: Xor . 11: And .	

Default: 0000 0000B

0x378~0x37F : Reserved

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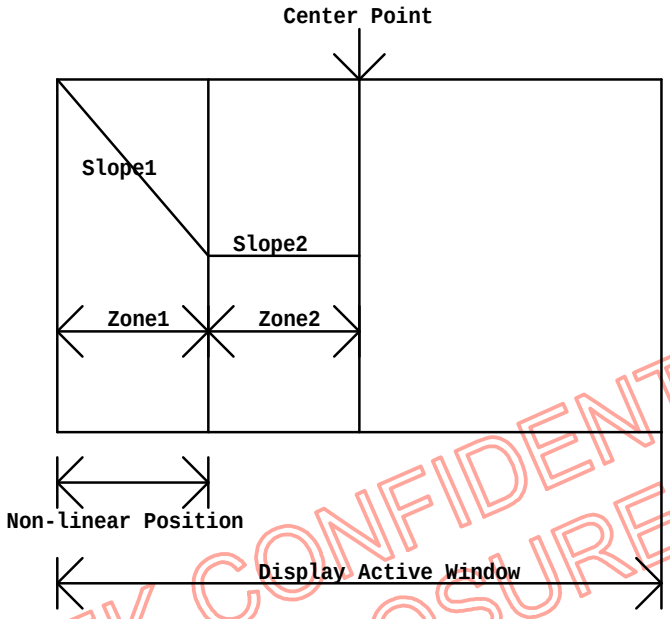
8.29. Horizontal Non-Linear Scaling Function



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0x380		Horizontal non-linear scaling Control	R/W
Bits	Name	Description	
7-1		Reserved	
0	NL_SCALING_EN	0 = normal linear scaling applied to entire image. 1 = enable non-linear scaling (16:9 display zoom ratio)	

Default: 0000 0000B

0x381		Non-linear scaling Offset Adjust	R/W
Bits	Name	Description	
7-0	NL_OFF[7:0]	Adjust the error for scaling factor.	

Default: 0000 0000B

0x382		Non-linear scaling Factor Zone1 end – Low Byte	R/W
Bits	Name	Description	
7-0	NL_ZONE1_END [7:0]	Sets the Scaling Factor in the first non-linear scaling region (ZONE1).	

Default: 0000 0000B

0x383		Non-linear scaling Factor Zone1 end – High Byte	R/W
Bits	Name	Description	
7-0	NL_ZONE1_END [15:8]	Sets the Scaling Factor in the first non-linear scaling region (ZONE1).	

Default: 0000 0000B

0x384		Non-linear scaling Zone1 Slope – Low Byte	R/W

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Bits	Name	Description
7-0	NL_SLOPE1 [7:0]	Sets the Slope Factor in the first non-linear scaling region (ZONE1).

Default: 0000 0000B

0x385		Non-linear scaling Zone1 Slope – High Byte	R/W
Bits	Name	Description	
7-0	NL_SLOPE1 [15:8]	Sets the Slope Factor in the first non-linear scaling region (ZONE1).	

Default: 0000 0000B

0x386		Non-linear scaling Factor Zone2 end – Low Byte	R/W
Bits	Name	Description	
7-0	NL_ZONE2_END [7:0]	Sets the Scaling Factor in the first non-linear scaling region (ZONE2).	

Default: 0000 0000B

0x387		Non-linear scaling Factor Zone2 end – High Byte	R/W
Bits	Name	Description	
7-0	NL_ZONE2_END [15:8]	Sets the Scaling Factor in the first non-linear scaling region (ZONE2).	

Default: 0000 0000B

0x388		Non-linear scaling Zone2 Slope – Low Byte	R/W
Bits	Name	Description	
7-0	NL_SLOPE2 [7:0]	Sets the Slope Factor in the first non-linear scaling region (ZONE2).	

Default: 0000 0000B

0x389		Non-linear scaling Zone2 Slope –High	R/W
Bits	Name	Description	
7-0	NL_SLOPE2 [15:8]	Sets the Slope Factor in the first non-linear scaling region (ZONE2).	

Default: 0000 0000B

0x38A		Non-linear Position – Low Byte	R/W
Bits	Name	Description	
7-0	NL_CBEG [7:0]	Sets the Position of ZONE1 and ZONE2.	

Default: 0000 0000B

0x38B		Non-linear Position – High Byte	R/W
Bits	Name	Description	
7-0	NL_CBEG [15:8]	Sets the Position of ZONE1 and ZONE2. .	

Default: 0000 0000B

0x38C~0x38F : Reserved

8.30. Bright Frame Border Function

0x390		Bright Frame Windows Border control	R/W
Bits	Name	Description	
7	BF1_BORDER_ EN	BF1 border 0 = Disable 1 = Enable	

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6	BF2_BORDER_ EN	BF2 border 0 = Disable 1 = Enable
5		Reserved
4	GAMMA_POSITION_SW	Switching Gamma position 0: After OSD block 1: Before BF block
3	BF2_ YUV2RGB _EN	BF2 YUV to RGB color space 0 = Disable. 1 = Enable
2	BF2_RGB2YUV_ EN	BF2 RGB to YUV color space 0 = Disable. 1 = Enable
1	BF1_YUV2RGB _EN	BF1 YUV to RGB color space 0 = Disable. 1 = Enable
0	BF1_RGB2YUV_ EN	BF1 RGB to YUV color space 0 = Disable. 1 = Enable

Default: 0000 0000B

0x391		**Bright Frame Border R color control**	**R/W**
Bits	Name	Description	
7-0	BF_BORDER_R[7:0]	Bright frame border color R[7:0] .	

Default: 0000 0000B

0x392		**Bright Frame Border G color control**	**R/W**
Bits	Name	Description	
7-0	BF_BORDER_G[7:0]	Bright frame border color G[7:0] .	

Default: 0000 0000B

0x393		**Bright Frame Border B color control**	**R/W**
Bits	Name	Description	
7-0	BF_BORDER_B[7:0]	Bright frame border color B[7:0] .	

Default: 0000 0000B

0x394		**Bright Frame Border enable control**	**R/W**
Bits	Name	Description	
7-3		Reserved	
2	BF_BORDER_TOP/BOT	Bright frame top/bottom border enable control 0: Disable 1: Enable.	
1	BF_BORDER_RIGHT	Bright frame right border enable control 0: Disable 1: Enable.	
0	BF_BORDER_LEFT	Bright frame left border enable control 0: Disable 1: Enable.	

Default: 0000 0000B

0x395~0x399 : Reserved

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0x39A		Sub-Pixel Dither Control	R/W
Bits	Name	Description	
7		Pattern 025_1 enable	
6-4		Pattern 025_0 enable	
2	10_SUBPIXEL	Pattern 05 sub-pixel enable , 0x371.4 set “1”	
1	01_SUBPIXEL	Pattern 025 sub-pixel enable , 0x371.4 set “1”	
0	MIX_ENABLE	Enable mix mode	

Default: 0000 0000B

0x39B		Sub-Pixel Dither Control	R/W
Bits	Name	Description	
7-5		Pattern 025_3 enable	
4-2		Pattern 025_2 enable	
1		Pattern 025_1 enable	
0		Pattern 025_1 enable	

Default: 0000 0000B

0x39C		Sub-Pixel Dither Control	R/W
Bits	Name	Description	
7-0		Pattern 05 enable	

Default: 0000 0000B

0x39D		Mix Dither Mode Control	R/W
Bits	Name	Description	
7-6		Reserved	
5	STATIC_CNT[2]	Static dithering active period counter for B channel 0x376[5:4] set “11” 0x376[3:2] for STATIC_CNT[1:0] 0x371[1] must set “1”	
4	RANDOM_CNT[2]	Random dithering active period counter for B channel 0x376[5:4] set “11” 0x376[1:0] for RANDOM _CNT[1:0] 0x371[1] must set “1”	
3	STATIC_CNT[2]	Static dithering active period counter for G channel 0x1DA[5:4] set “11” 0x1DA[3:2] for STATIC_CNT[1:0]	
2	RANDOM_CNT[2]	Random dithering active period counter for G channel 0x1DA[5:4] set “11” 0x1DA[1:0] for RANDOM_CNT[1:0]	
1	STATIC_CNT[2]	Static dithering active period counter for R channel 0x373[5:4] set “11” 0x373[3:2] for STATIC_CNT[1:0] 0x371[1] must set “1”	
0	RANDOM_CNT[2]	Random dithering active period counter for R channel 0x373[5:4] set “11” 0x373[1:0] for RANDOM _CNT[1:0] 0x371[1] must set “1”	

Default: 0000 0000B

0x39E	Mix 3 in 1Dither Mode Control	R/W

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Bits	Name	Description
7-6		Reserved
5-4	R_MIX3_TYPE	Mix 3 in 1 dithering mode random type for R channel 0x373 set “0x00” 0x371 set “0x72” 00: original (4/16 random) 01: 1/16 random 10: 2/16 random 11: Reserved
3-2		Reserved
1-0	G_MIX3_TYPE	Mix 3 in 1 dithering mode random type for G channel 0x1DA set “0x00” 0x371 set “0x72” 00: original (4/16 random) 01: 1/16 random 10: 2/16 random 11: Reserved

Default: 0000 0000B

0x39F	**Mix 3 in 1Dither Mode Control**	**R/W**
Bits	Name	Description
7-2		Reserved
1-0	B_MIX3_TYPE	Mix 3 in 1 dithering mode random type for B channel 0x376 set “0x00” 0x371 set “0x72” 00: original (4/16 random) 01: 1/16 random 10: 2/16 random 11: Reserved

Default: 0000 0000B

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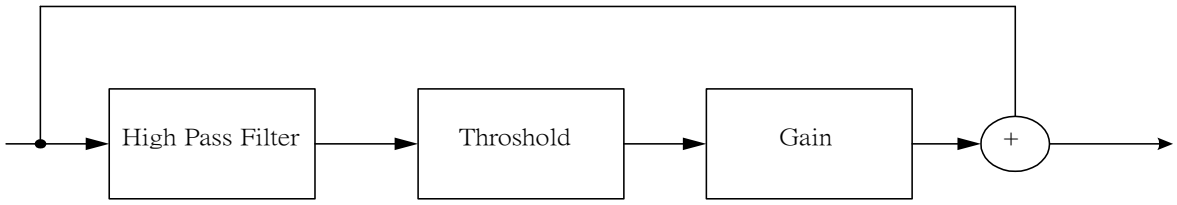
8.31. Y/C Peaking Control



Y/C peaking Block

0x3A0	**Y/C Peaking Function Control**	**R/W**
Bits	Name	Description
7-6		Reserved
5	CHROMA_PEAK_MEDIAN_EN	These bits set the chroma median peaking control. (average Cb,Cr high pass value) 0: Disabled 1: Enabled
4	CHROMA_PEAK_EN	These bits set the chroma peaking control. (Cb,Cr high pass) 0: Disabled

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		1: Enabled
3-2		Reserved
1	TEXT_ENHANCE	Text enhance , the priority higher than LUMA_PEAK_EN 0: disabled 1: enabled
0	LUMA_PEAK_EN	This bit enables the luma horizontal peaking control , 0: Disabled 1: Enabled

Default: 0010 0000B

0x3A1		Luma Peaking Range Control	R/W
Bits	Name	Description	
7-4	YCORING[3:0]	To control Luma Signal threshold (coring)	
3-2	YGAIN[1:0]	Luma Gain range control Y peaking : 1/2 , 1, 2 , 4	
1-0	YFREQ[1:0]	To control Luma freq range .	

Default: 0000 0000B

0x3A2		Chroma Peaking Range Control	R/W
Bits	Name	Description	
7-4	CCORING[3:0]	To control Chroma Signal threshold .	
3-2	CGAIN[1:0]	To control Chroma Gain range .	
1-0	CFREQ[1:0]	To control Chroma freq range .	

Default: 0000 0000B

0x3A3		Text Enhance Control	R/W
Bits	Name	Description	
7-0	LUM_NOISE_THD[7:0]	Luminace Noise Threshold Recommended value to 20h (10 bits)	

Default: 0010 0000B

0x3A4		Text Enhance Control	R/W
Bits	Name	Description	
7	DOUBLE_TEXT_ENHANCE	Text Enhance double effect	
6-4	LUMA_GAIN	Luminance gain level	
1-0	CHROMA_THD[1:0]	Chrominance Threshold Level, higher level enhances more color pixels 00: 128 01: 256 10: 512 11: 1024	

Default: XXXX XX11B

0x3A5~0x3AF : Reserved

8.32. ACE Control

0x3B0		ACE Function Control	R/W
Bits	Name	Description	
7		Reserved	
6	NON_LINEAR_MODE	Enable non-linear histogram mode (Only support BF1)	
5	DATA_PORT_SEL[1]	Data port access selection, This bit setting will reference to Reg. 0x3B1[4], {3B0[5], 3B1[4]}	

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		00 : histogram read, 01 : I-Gamma curve R/W 1x : Non-linear histogram point R/W
4	HIST_MODE	0: Mode 0 , pixel number accumulation mode . 1: Mode 1 ,frame number accumulation mode .
3-2	ACE_MODE[1:0]	00: 4 area histogram / I – Gamma curve . 01: 8 area histogram / I – Gamma curve . 10: 16 area histogram / I – Gamma curve . 11: Reserved
1	BF1_I-GAMMA_EN	BF1 , I-Gamma function 0: Disable 1: Enable
0	BF2_I-GAMMA_EN	BF2 , I-Gamma function 0: Disable 1: Enable

Default: 0000 0000B

0x3B1		**ACE Function Control**	**R/W**
Bits	Name	Description	
7	I-GAMMA_UPDATE	1: for update I-Gamma curve data .	
6	I-GAMMA_RW	0: Read I-Gamma curve . 1: Write I-Gamma curve .	
5	WINSEL	0 : For BF1 access . 1 : For BF2 access .	
4	DATA_PORT_SEL	If reg. 0x3B0[5] set to 0 1: for I-Gamma curve R/W, 0: for histogram read. If reg. 0x3B0[5] set to 1, the data port will access Non-linear histogram point R/W	
3-1	FRAME_MODE[2:0]	000 ~ 111: for 1 to 255 frame calculation .	
0	HIST_EN/HIST_RDY	0: Histogram Read ready 1: Enable histogram	

Default: 0000 0000B

Histogram read : 4 or 8 or 16 area pixel counts in entire frame , if HIST_MODE set “0”

Histogram read : 4 or 8 or 16 area over threshold frame counts in 256 frame , if HIST_MODE set “1”

0x3B2		**ACE R/W Data port**	**R/W**
Bits	Name	Description	
7-0	DATA_PORT[7:0]	Ace r/w data port[7:0]	

Default: 0000 0000B

0x3B3		**Frame mode threshold – Low Byte**	**R/W**
Bits	Name	Description	
7-0	FRAME_THRESHOLD[7:0]	Mode 1 threshold [7:0]	

Default: 0000 0000B

0x3B4		**Frame mode threshold – Mid Byte**	**R/W**
Bits	Name	Description	
7-0	FRAME_THRESHOLD[15:8]	Mode 1 threshold [15:8]	

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Default: 0000 0000B

0x3B5		Frame mode threshold – High Byte	R/W
Bits	Name	Description	
7-0	FRAME_THRESHOLD[23:16]	Mode 1 threshold[23:16]	

Default: 0000 0000B

0x3B6~0x3BF : Reserved

8.33. Color Management

0x3C0		CM Color Adjustment Control	R/W
Bits	Name	Description	
7	CM_UPDATE_FLAG	The status of updating new coefficients to controller right after any write to brightness, contrast, intensity, hue, and saturation. This flag is read-only bit. 0: Done 1: Busy	
6	CM_BRIGHT_EN	Brightness Adjust Function Enable, update adjustment in Vsync 0: Disable 1: Enable	
5	CM_CONTRAST_EN	Contrast Adjust Function Enable, update adjustment in Vsync 0: Disable 1: Enable	
4	CM_HUE_EN	Hue Adjust Function Enable, update adjustment in Vsync 0: Disable 1: Enable	
3	CM_SATURATION_EN	Saturation Adjust Function Enable, update adjustment in Vsync 0: Disable 1: Enable	
2	CM_INTENSITY_EN	Intensity Adjust Function Enable, update adjustment in Vsync 0: Disable 1: Enable	
1-0	Reserved		

Default: 0000 0000B

0x3C1		CM Brightness coefficient for Red	R/W
Bits	Name	Description	
7-0	CM_BRIGHTNESS_R	This parameter is active when CM_BRIGHT_EN is active. The value is from –128 to 127 in 2's complement, power on default is 0. R Display color = (Original value * Contrast coef.) + Brightness coef.	

Default: 0000 0000B

0x3C2		CM Brightness coefficient for Green	R/W
Bits	Name	Description	
7-0	CM_BRIGHTNESS_G	This parameter is active when CM_BRIGHT_EN is active. The value is from –128 to 127 in 2's complement, power on default is 0. G Display color = (Original value * Contrast coef.) + Brightness coef.	

Default: 0000 0000B

0x3C3		CM Brightness coefficient for Blue	R/W
Bits	Name	Description	

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7-0	CM_BRIGHTNESS_B	This parameter is active when CM_BRIGHT_EN is active. The value is from –128 to 127 in 2's complement, power on default is 0. B Display color = (Original value * Contrast coef.) + Brightness coef.

Default: 0000 0000B

0x3C4		CM Contrast Ratio coefficient for R	R/W
Bits	Name	Description	
7-0	CM_CONTRAST_R	This parameter is active when CM_CONTRAST_EN is active. The value is from 0(00 h) to2 (FF h), power on default is 1 (80h)..	

Default: 1000 0000B

0x3C5		CM Contrast Ratio coefficient for G	R/W
Bits	Name	Description	
7-0	CM_CONTRAST_G	This parameter is active when CM_CONTRAST_EN is active. The value is from 0(00 h) to2 (FF h), power on default is 1 (80h).	

Default: 1000 0000B

0x3C6		CM Contrast Ratio coefficient for B	R/W
Bits	Name	Description	
7-0	CM_CONTRAST_B	This parameter is active when CM_CONTRAST_EN is active. The value is from 0(00 h) to2 (FF h), power on default is 1 (80h).	

Default: 1000 0000B

0x3C7		CM Hue coefficient	R/W
Bits	Name	Description	
7-0	CM_HUE	This parameter is active when CM_HUE_EN is active. The value is from 00h to 7Fh, one step means 180/128 degree. Bit 7 is sign bit: 0: clockwise (negative rotation), 1: counterclockwise (positive rotation)	

Default: 0000 0000B

0x3C8		CM Hue coefficient	R/W
Bits	Name	Description	
7-0	CM_SATURATION	This parameter is active when CM_SATURATION_EN is active. The value is from 00 h to FF h.	

Default: 1000 0000B

0x3C9		CM Hue coefficient	R/W
Bits	Name	Description	
7-0	CM_INTENSITY	This parameter is active when CM_INTENSITY_EN is active. The value is from 00 h to FF h. (0~2)	

Default: 1000 0000B

0x3CA~0x3CB : Reserved

0x3CC		CM Color Enhancement Configuration	R/W
Bits	Name	Description	
7	HH_MAP_EN	Hue-Hue map 0: disable 1: enable	

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6	HS_MAP_EN	Hue-Saturation map 0: disable 1: enable
5	SS_MAP_EN	Saturation-Saturation map 0: disable 1: enable
4-2		Reserved
1	MAP_LOAD_EN	Mapping table load enable 0: Disable 1: enable
0	CM_CE_EN	CM Color Enhancement enable , 0: Disable 1: Enable

Default: 0000 0000B

0x3CD		CM Index Access Port Control	R/W
Bits	Name	Description	
7-2		Reserved	
1-0	CM_INDEX_SEL	Table Select: 00: no access, 01: Hue-Hue Table, 10: Hue-Saturation Table 11: Saturation-Saturation Table	

Default: 0000 0000B

0x3CE		CM Index Access Port Address	R/W
Bits	Name	Description	
7-5		Reserved	
4-0	CM_INDEX_ ADDR	Table Address: Hue-Hue address: 0~23 (24 entries), each step means 15 degree Hue-Saturation address: 0~23 (24 entries), each step means 15 degree Saturation-Saturation address: 0~16 (17 entries), each step means 1/16 full saturation scale	

Default: 0000 0010B

0x3CF		CM Index Access Port	R/W
Bits	Name	Description	
7-0	CM_INDEX_PORT	Hue-Hue Data Port: The value is from 00h to 7Fh, one step means 30/128 degree. Bit 7: 0 is clockwise, 1 is counterclockwise. Power on default is 00h. Hue-Saturation Data Port: The value is from 00h to FFh. (0~2). Power on default is 80h (1). Saturation-Saturation Data Port: The value is from 00 h to FF h. (0~1). Power on default is FFh (1).	

Default: 0000 0000B(HH), 1000 0000B(HS),1111 1111B(SS)

0x3D0~0x3FE : Reserved

0x3FF		Accessing Register Page Enable	R/W
Bits	Name	Description	

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7-2		Reserved
1-0	REG_PAGE_SEL	Register Page Enable 000: Enable register Page0. 001: Enable register Page1. 010: Enable register Page2. 011: Enable register Page3. 100: Enable register Page4.

Default: 0000 0000B

0x400~0x42F : Reserved

8.34. DBC

0x430		DBC Control	R/W
Bits	Name	Description	
7-4	ABRUPT_THD[3:0]	When Abrupt_Change_Enable =1, if the differences of the current and previous frame statistics are bigger than Abrupt_TH*16, it will considered as un-stable immediately.	
3	ABRUPT_EN	Abrupt_Change_Enable: 1: Abrupt Change function enabele 0: Abrupt Change function disabled	
2	DBC_DITH_EN	DBC_dither_enable: 1: DBC dither is disabled. 0: DBC dither is disabled	
1	DBC_DATA_EN	Modify RGB value according to PWM value 1: Enable Modification 0: Disable (No Change)	
0	DBC_BL_CON_EN	Dynamic Backlight Control Enable (PIN Selection by REG0EE[5]) 1:Enable 0:Disable	

Default: 1111 0100B

0x431		DBC Adjust	R/W
Bits	Name	Description	
7-4	DUTY_ADJ_RATE	Dynamic backlight control adjustment rate. PWM and color values will adjusted according to frame statistics at every (Adjust_Rate+1) stable frames	
3-0	DUTY_ADJ_STEP	PWM duty adjustment step size: the maximum step size when adjust the PWM duty at the adjust frame rate	

Default: 1000 0011B

0x432		PWM Min	R/W
Bits	Name	Description	
7-0	DBC_PWM_MIN	The lower bond of PWM duty cycle. No matter how PWM duty is modified according to frame statistics. The duty cycle will never lower than PWM_min/256. PWM_min must be no smaller than 8'h40.	

Default: 1000 0000B

0x433		PWM Divider 1	R/W
Bits	Name	Description	

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7-6	DBC_PWM_DUTY_MSB [1:0]	Used to add , 0/4, 1/4, 2/4,3/4 with duty[7:0]/1024
5	DBC_PWM_POL	PWM polarity control 1: Invert 0: Normal
4	REG_VSYNC_MODE	Load PWM control register on display Vsync leading edge
3-0	DBC_PWM_DIV1	First divider-- PWM clock divide of the selected clock by 0000 = 1; 0001 = 2; 0010 = 4; 0011 = 8; 0100 = 16; 0101 = 32;0110 = 64; 0111 = 128; 1000 = 256; 1001 = 512;1010 = 1024; 1011 = 2048; 1100 = 4096; 1101 = 8192; 1110 = 16384;11=16384;

Default: 0000 0111B

0x434		**PWM Divider 2**	**R/W**
Bits	Name	Description	
7-0	DBC_PWM_DIV2	DBC PWM period counter value. 1~256	

Default: 0101 0100B

0x435		**PWM Divider 2**	**R/W**
Bits	Name	Description	
7-0	DBC_PWM_DUTY [7:0]	DBC PWM Duty. 0.39% ~ 100% , (PWMB_DUTY[7:0] + 1)/256x100%	

Default: 1111 1111B

0x436		**DBC PWM Control**	**R/W**
Bits	Name	Description	
7	DBC_PWM_EN	DBC PWM function enable	
6	PWMA (PWM0)	DBC PWM function apply to PWMA	
5	PWMB (PWM1)	DBC PWM function apply to PWMB	
4	AVE_SAVING_MODE	When AVE_Saving_Mode=1, the power saving ratio is determined by average and maximum color in the frame	
3-0	ALLOW_DISTORT	When DISTORT is not “00”, the color value of “255-DISTORTX2” to 255 might to mapping to the same value	

Default: 0000 0000B

0x437		**PWM Offset**	**R**
Bits	Name	Description	
7-0	PWM_OFFSET	DBC PWM offset control	

Default: XXXX XXXXB

0x438		**Y AVE**	**R**
Bits	Name	Description	
7-0	Y_AVEARGE	The average value of luminance of the current frame. It is updated every frame and used for image stable criterion	

Default: XXXX XXXXB

0x439		**Effective Color Value**	**R**
Bits	Name	Description	
7-0	EFFE_COLOR	Effective color value for DBC control	

Default: XXXX XXXXB

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0x43A		RGB Compensator Value	R
Bits	Name	Description	
7-0	RGB_COMPEN[7:0]	RGB compensator	

Default: XXXX XXXXB

0x43B		PWM ACT	R
Bits	Name	Description	
7-0	PWM_ACT[7:0]	It is the final duty cycle value of PWM after dynamic backlight control. In fact PWM_act = PWM_set * max_color/256	

Default: 0000 0000B

0x43E		DBC Index Port Control	R/W
Bits	Name	Description	
7-6		Reserved	
5-4	DBC_TABLE_SEL	00: None 01: Y gray to Lightness mapping table 10: PWM to Lightness mapping table 11: PWM ration to Multiplier mapping table	
3-1		Reserved	
0	PORT_RW	Port Read/Write 0: Write 1: Read	

Default: 0000 0000B

0x43F		DBC Index Data Port	R/W
Bits	Name	Description	
7-0	PORT_DATA[7:0]	DBC Table R/W Data port [7:0]	

Default: 0000 0000B

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0x440 ~ 0x4FE: Reserved Register

0x4FF		Accessing Register Page Enable	R/W
Bits	Name	Description	
7-3		Reserved	
2-0	REG_PAGE_SEL	Register Page Enable 000: Enable register Page0. 001: Enable register Page1. 010: Enable register Page2. 011: Enable register Page3. 100: Enable register Page4.	

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9. Ordering Information

Order Code	Package	Note
NT68667FG	QFP 128L	Pb Free
NT68667HFG	QFP 128L	Pb Free
NT68667UFG	QFP 128L	Pb Free

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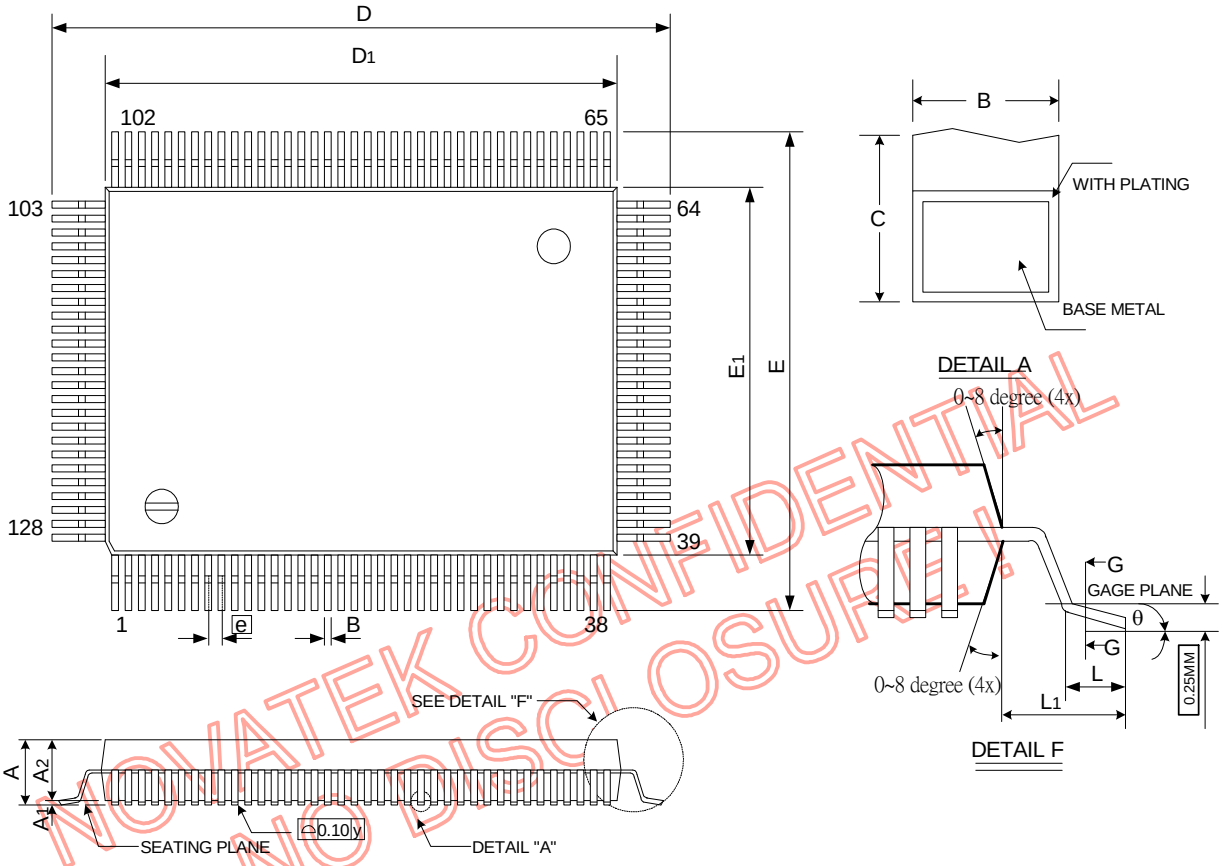
Package Information



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QFP 128L Outline Dimensions unit: inches/mm

Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	--	--	0.134	--	--	3.40
A1	0.010	--	--	0.25	--	--
A2	0.101	0.112	0.117	2.57	2.85	2.97
B	0.005	0.009	0.011	0.13	0.22	0.27
C	0.004	--	0.008	0.09	--	0.20
D	0.906	0.913	0.921	23.00	23.20	23.40
D1	0.783	0.787	0.791	19.90	20.00	20.10
E	0.669	0.667	0.685	17.00	17.20	17.40
E1	0.547	0.551	0.555	13.90	14.00	14.10
e	0.020 BSC			0.5 BSC		
L	0.029	0.035	0.041	0.73	0.88	1.03
L1	0.063 BSC			1.60 BSC		
Y	--	--	0.004	--	--	0.10
θ	0°	--	7°	0°	--	7°

Notes: 1.Dimensions D & E do not include resin fins.
2.Dimensions F, GD & GE are for PC Board surface mount pad pitch design reference only

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1 Trail : 66 pcs



1 Box : 10 Trail





DENTIAL
URE !

1 Carton : 6 Box



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