Datasheet Version 2.2, 04 Jul 2011

ICE2QS01

Quasi-resonant PWM Controller

Power Management & Supply

Never stop thinking.

ICE2QS01

Revision History:	**04 Jul 2011**	Datasheet
Previous Version:	2.1	

Page	Subjects (major changes since last revision)
16	revised outline dimension.

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Edition 2011-07-04

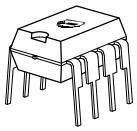
Published by
Infineon Technologies AG
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Quasi-Resonant PWM Controller



PG-DIP-8

Product Highlights

- **Active burst mode for low standby power**
- **Digital frequency reduction for better overall system efficiency**
- **Integrated power cell for IC self-power supply**

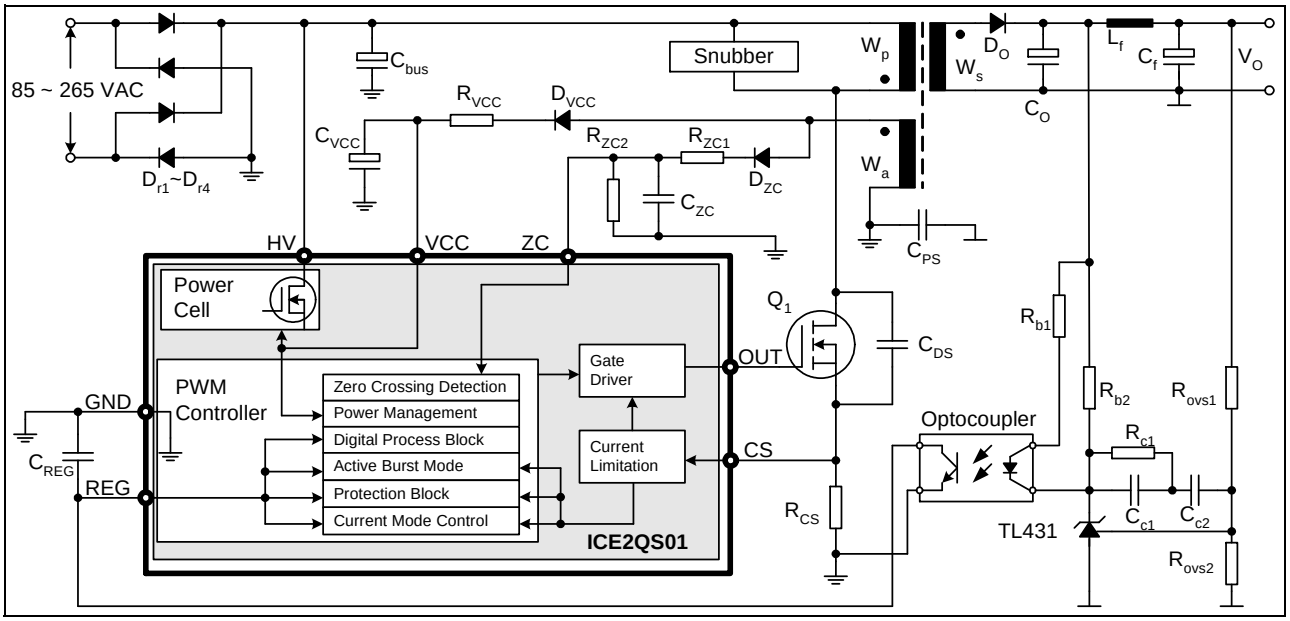
Features

- Quasiresonant operation till very low load
- Active burst mode operation at light load for low standby input power (< 1W)
- Digital frequency reduction with decreasing load
- Power cell for VCC pre-charging and IC power supply during latch-off, or standby mode operation when it is necessary
- Built-in digital soft-start
- Foldback correction and cycle-by-cycle peak current limitation
- Auto restart mode for VCC Overvoltage protection
- Auto restart mode for VCC Undervoltage protection
- Auto restart mode for openloop/overload protection
- Latch-off mode for adjustable output overvoltage protection
- Latch-off mode for Short-winding protection

Description

ICE2QS01 is a quasi-resonant PWM controller optimized for off-line switch power supply applications such as LCD TV, CRT TV and notebook adapter. The digital frequency reduction with decreasing load enables a quasi-resonant operation till very low load. As a result, the system efficiency is significantly improved compared to other conventional solutions. The active burst mode operation enables an ultra-low power consumption at standby mode with small and controllable output voltage ripple. The innovative power cell solves the IC power supply problem when the output voltage is pulled down during standby mode, or during latch-off mode. The numerous protection functions give a full protection of the power supply system in failure situations. All of these make the ICE2QS01 an outstanding controller for quasi-resonant flyback converter in the market.

Typical Application



Type	Marking	Package
ICE2QS01	ICE2QS01	PG-DIP-8

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1 Pin Configuration and Functionality

1.1 Pin Configuration

Pin	Symbol	Function
1	ZC	**Z**ero **C**rossing
2	REG	**Reg**ulation
3	CS	Primary **C**urrent **S**ensing
4, 5	HV	**H**igh **V**oltage input
6	OUT	gate driver **out**put
7	VCC	IC supply voltage
8	GND	Common ground

1.2 Package PG-DIP-8

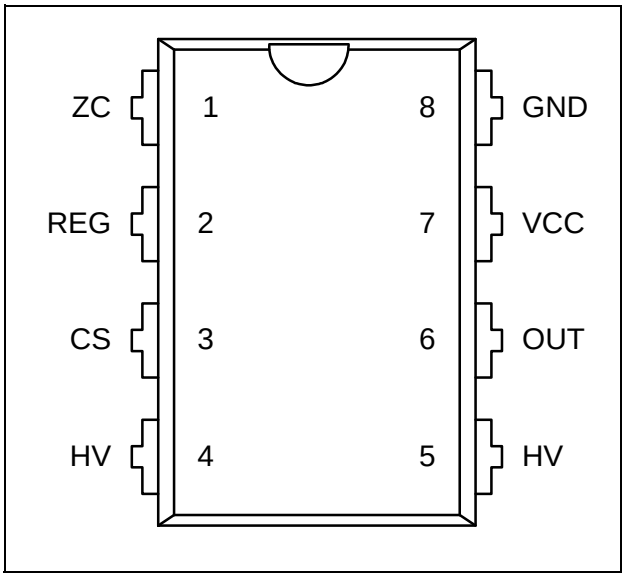


Figure 1 Pin Configuration PG-DIP-8(top view)

1.3 Pin Functionality

ZC (Zero Crossing)

At this pin, the voltage from the auxiliary winding after a time delay circuit is applied. Internally, this pin is connected to the zero-crossing detector for switch-on determination. Additionally, the output overvoltage detection is realized by comparing the voltage V_{zc} with an internal preset threshold.

REG (Regulation)

Normally, an external capacitor is connected to this pin for a smooth voltage V_{reg}. Internally, this pin is connected to the PWM signal generator for switch-off determination (together with the current sensing signal), the digital signal processing for the frequency reduction with decreasing load during normal operation, and the burst mode controller for entering burst mode operation determination and burst ratio control during burst mode operation. Additionally, the open-loop / over-load protection is implemented by monitoring the voltage at this pin.

CS (Current Sensing)

This pin is connected to the shunt resistor for the primary current sensing, externally, and the PWM signal generator for switch-off determination (together with the regulation voltage), internally. Moreover, short-winding protection is realised by monitoring the voltage V_{cs} during on-time of the main power switch.

HV (High Voltage)

The pin HV is connected to the bus voltage, externally, and to the power cell, internally. The current through this pin pre-charges the VCC capacitor once the supply bus voltage is applied. Additionally, the current through this pin supplies the IC in case that the output voltage is lowered during active burst mode operation, or during latch-off mode.

OUT (Gate drive output)

This output signal drives the external main power switch, which is a power MOSFET in most case.

VCC (Power supply)

This is the IC power supply pin. Externally, this pin is connected to the VCC capacitor, which is supplied by the inside power cell during VCC charge-up, burst mode operation at lowered output voltage or during latched-off of the IC, and the auxiliary winding during normal operation or burst mode operation with high enough voltage across the auxiliary winding. Based on this voltage, the VCC under- or over-voltage protection are implemented.

GND (Ground)

This is the common ground of the controller.

2 Representative block diagram

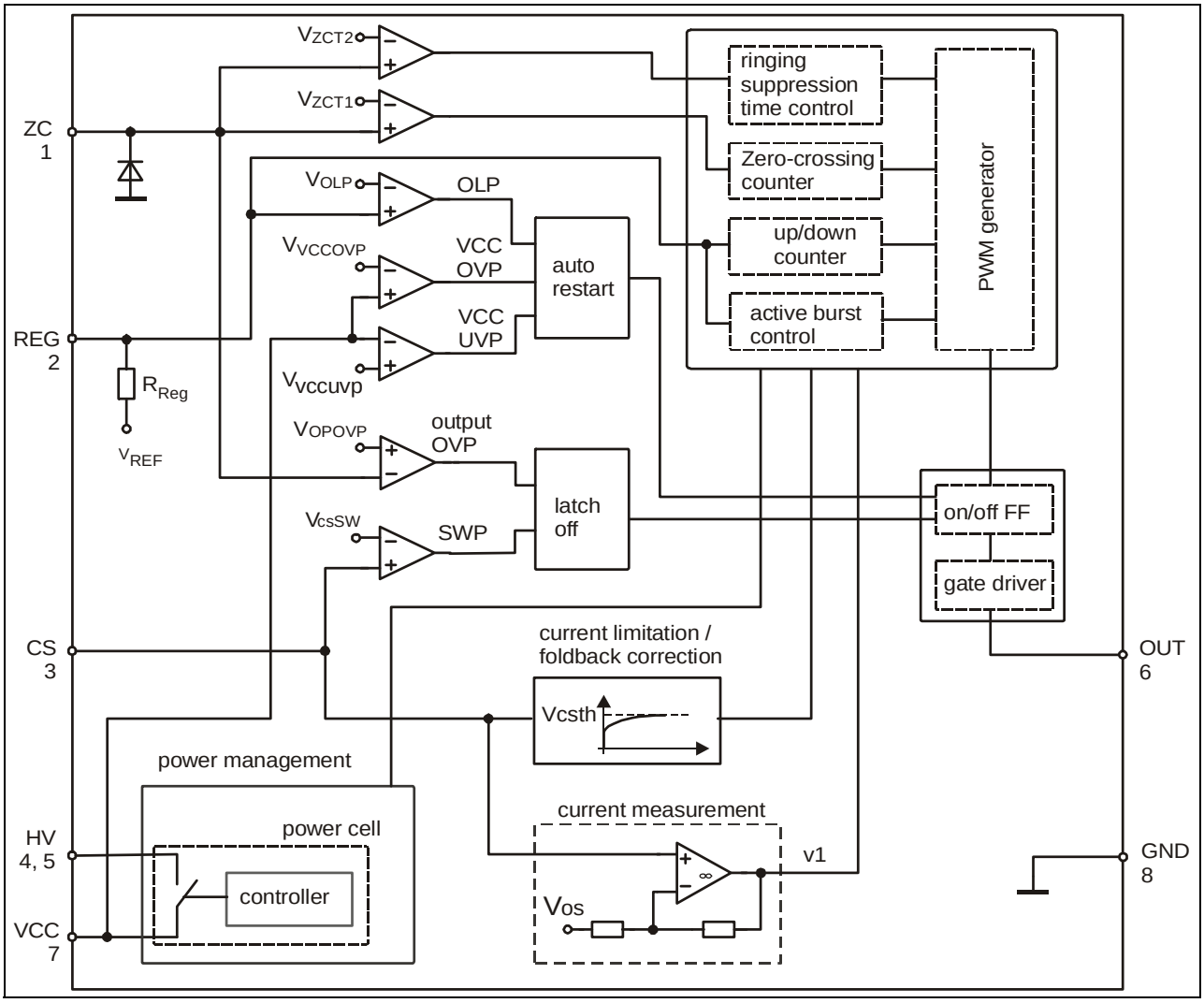


Figure 2 Representative Blockdigram

3 Functional Description

3.1 VCC Pre-Charging and Typical VCC Voltage During Start-up

In the controller ICE2QS01, a power cell is integrated. As shown in Figure 2, the power cell consists of a high voltage device and a controller, whereby the high voltage device is controlled by the controller. The power cell provides a pre-charging of the VCC capacitor till VCC voltage reaches the VCC turned-on threshold V_{VCCon} and the IC begins to operate, while it may keep the VCC voltage at a constant value during burst mode operation when the output voltage is pulled down or the power from the auxiliary winding is not enough, or when the IC is latched off in certain protection mode.

Once the mains input voltage is applied, a rectified voltage shows across the capacitor C_{bus}. The high voltage device provides a current to charge the VCC capacitor C_{vcc}. Before the VCC voltage reaches a certain value, the amplitude of the current through the high voltage device is only determined by its channel resistance and can be as high as several mA. After the VCC voltage is high enough, the controller controls the high voltage device so that a constant current around 1mA is provided to charge the VCC capacitor further, until the VCC voltage exceeds the turned-on threshold V_{VCCon}. As shown as the time phase I in Figure 3, the VCC voltage increase near linearly.

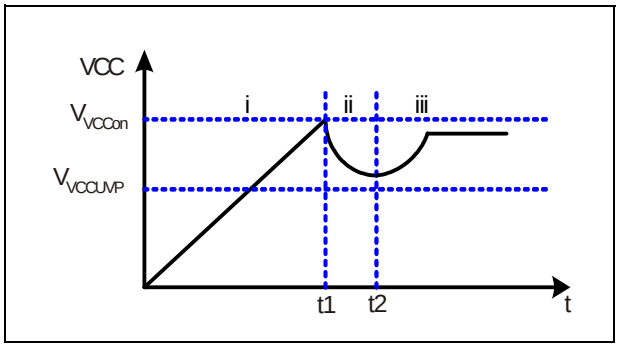


Figure 3 VCC voltage at start up

The time taking for the VCC pre-charging can then be approximately calculated as:

$$t_1 = \frac{V_{VCCon} \cdot C_{vcc}}{I_{VCCcharge2}} \quad [1]$$

where $I_{VCCcharge2}$ is the charging current from the power cell which is 1.05mA, typically.

Exceeds the VCC voltage the turned-on threshold V_{VCCon} of at time t_1, the power cell is switched off, and the IC begins to operate with a soft-start. Due to power consumption of the IC and the fact that still no energy from the auxiliary winding to charge the VCC capacitor before the output voltage is built up, the VCC voltage drops (Phase II). Once the output voltage is high enough, the VCC capacitor receives then energy from the auxiliary winding from the time point t_2 on. The VCC then will reach a constant value depending on output load.

Since there is a VCC undervoltage protection, the capacitance of the VCC capacitor should be selected to be high enough to ensure that enough energy is stored in the VCC capacitor so that the VCC voltage will never touch the VCC under voltage protection threshold V_{VCCUVP} before the output voltage is built up. Therefore, the capacitance should fulfill the following requirement:

$$C_{vcc} \geq \frac{I_{VCCop} \cdot (t_2 - t_1)}{V_{VCCon} - V_{VCCUVP}} \quad [2]$$

with I_{VCCop} the operating current of the controller.

3.2 Soft-start

At the time t_1, the IC begins to operate with a soft-start. By this soft-start the switching stresses for the switch, diode and transformer are minimised. The soft-start implemented in the ICE2QS01 is a digital time-based function. The preset soft-start time is **24ms** with 8 steps. The internal reference for the regulation voltage begins at 1.35V and with an increment of 0.35V for each following step.

3.3 Normal Operation

The PWM section of the IC can be divided into two main portions: PWM controller for normal operation and PWM controller for burst mode operation. The PWM controller for normal operation will be described in the following paragraphs, while the PWM controller for burst mode operation will be discussed in the next section.

The PWM controller for normal operation consists of digital signal processing circuit including an up/down counter, a zero-crossing counter (ZC-counter) and a comparator, and analog circuit including a current measurement unit and a comparator. The switch-on and -off time point is determined by the digital circuit and the analog circuit, respectively. As input information for the switch-on determination, the zero-crossing input signal and the value of the up/down counter are needed, while the feedback signal v_{REG} and the current sensing signal v_{CS} are necessary for the switch-off determination. Details about the operation of the PWM controller in normal operation are illustrated in the following paragraphs.

3.3.1 Switch-on Determination

As mentioned above, the digital signal processing circuit consists of an up/down counter, a zero-crossing counter and a comparator. A ringing suppression time

controller is implemented to avoid mistriggering by the ring after MOSFET is turned off. Functionality of these parts is described as in the following.

3.3.1.1 Up/down Counter

The up/down counter stores the number of zero crossing to be ignored before the main power switch is switched on after demagnetisation of the transformer. This value is a function of the regulation voltage, which contains information about the output power. Generally, a high output power results in a high regulation voltage. According to this information, the value in the up/down counter is changed to a low value in case of high regulation voltage, and to a high value in case of low regulation voltage. In ICE2QS01, the lowest value of the counter is 1 and the highest 7. Following text explains how the up/down counter value changes in responding to the regulation voltage v_{REG}. The regulation voltage v_{REG} is internally compared with three thresholds V_{RL}, V_{RH} and V_{RM}. According to the results, the value in the up/down counter is changed, which is summarised in Table 1 and Figure 4 respectively.

Table 1 Operation of the up/down counter

V_{REG}	**up/down counter action**
Always lower than V_{RL}	Count upwards till 7
Once higher than V_{RL}, but always lower than V_{RH}	Stop counting, no value changing
Once higher than V_{RH}, but always lower than V_{RM}	Count downwards till 1
Once higher than V_{RM}	Set up/down counter to 1

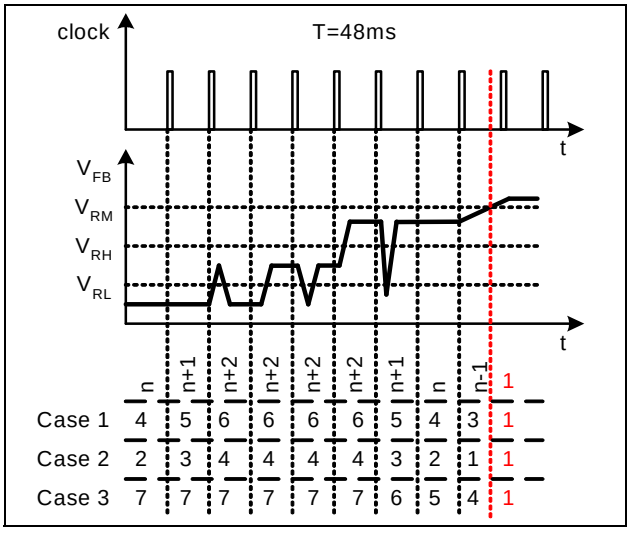


Figure 4 Up/down counter operation

According to the comparison results the up/down counter counts upwards, keeps unchanged or counts downwards. However, the value in up/down counter is limited between 1 and 7. If the counter tends to count beyond this range, the attempt is ignored.

In normal case, the up/down counter can only be changed by one each time at the clock period of 48ms. However, to ensure a fast response to sudden load increase, the counter is set to 1 in the following switching period after the regulation voltage v_{REG} exceeds the threshold V_{RM}.

3.3.1.2 Zero-Crossing Counter and Ringing Suppression Time Controller

In the system, the voltage from the auxiliary winding is applied to the zero-crossing pin through a RC network, which provides a time delay to the voltage from the auxiliary winding. Internally, this pin is connected to a clamping network, a zero-crossing detector, an output overvoltage (OP OVP) detector and a ringing suppression time controller.

During on-state of the power switch a negative voltage applies to the ZC pin. Through the internal clamping network, the voltage at the pin is clamped to certain level. However, it is highly recommended that a fast-recovery diode D_{zc} is added to block the negative voltage when the power switch is on. This is because the device in MOS technology is sensitive to negative voltage.

The voltage at the ZC pin v_{ZC} is compared with the threshold V_{ZCT1}. Once the voltage v_{ZC} crosses the threshold at its falling edge, a pulse is generated which is fed to the zero-crossing counter and the counter value increases by 1.

After MOSFET is turned on, there will be some oscillation on V_{DS}, which will also appear on the voltage on ZC pin. To avoid the MOSFET is turned on mistriggerred by such oscillation, a ringing suppression timer is implemented. The time is dependent on the voltage v_{ZC}. When the voltage v_{ZC} is lower than the threshold V_{ZCT2}, a longer preset time applies, while a shorter time is set when the voltage v_{ZC} is higher than the threshold.

The voltage v_{ZC} is used for the output overvoltage protection, as well. Once the voltage at this pin is higher than the threshold V_{OPOVP} during off-time of the main switch, the IC is latched off after a fixed blanking time.

To achieve the switch-on at voltage valley, the voltage from the auxiliary winding is fed to a time delay network (the RC network consists of D_{zc}, R_{zc1}, R_{zc2} and C_{zc} as shown in typical application circuit) before it is applied to the zero-crossing detector through the ZC pin. The needed time delay to the main oscillation signal Δt should be approximately one fourth of the oscillation period (by transformer primary inductor and drain-source capacitor) minus the propagation delay from the

detected zero-crossing to the switch-on of the main switch t_{delay}, theoretically:

$$\Delta t = \frac{T_{osc}}{4} - t_{delay} \quad [3]$$

This time delay should be matched by adjusting the time constant of the RC network which is calculated as:

$$\tau_{td} = C_{zc} \cdot \frac{R_{zc1} \cdot R_{zc2}}{R_{zc1} + R_{zc2}} \quad [4]$$

3.3.1.3 Switch-on Determination

In the system, turn-on of the power switch depends on the value of the up/down counter, the value of the zero-crossing counter and the voltage at the ZC pin v_{ZC}. Turn-on happens only when the value in the both counters are the same and the voltage at the ZC is lower than the threshold V_{ZCT1}. For comparison of the values from both counters, a digital comparator is used. Once these counters have the same value, the comparator generates a signal which sets the on/off flip-flop, only when the voltage v_{ZC} is lower than the threshold V_{ZCT1}.

Another signal which may trigger the digital comparator is the output of a T_{sMax} clock signal, which limits the maximum off time to avoid the low-frequency operation.

During active burst mode operation, the digital comparator is disabled and no pulse will be generated.

3.3.2 Switch-off Determination

In the converter system, the primary current is sensed by an external shunt resistor, which is connected between low-side terminal of the main power switch and the common ground. The sensed voltage across the shunt resistor v_{CS} is applied to an internal current measurement unit, and its output voltage v_1 is compared with the regulation voltage v_{reg}. Once the voltage v_1 exceeds the voltage v_{REG}, the output flip-flop is reset. As a result, the main power switch is switched off. The relationship between the v_1 and the v_{cs} is described by:

$$v_1 = 3.3 \cdot v_{CS} + 0.7 \quad [5]$$

To avoid mistriggering caused by the voltage spike across the shunt resistor after switch-on of the main power switch, a 330ns leading edge blanking time applies to output of the comparator.

3.3.3 Foldback Point Correction

In addition to the cycle-by-cylce primary current limitation, the IC incorporats a foldback point correction. The current limit on CS pin voltage is now a time dependent one. If the mains input voltage is high, the MOSFET on time will be short and the current limit will be low. In such a way, the maximum output power for the SMPS designed with ICE2QS01 will be nearly constant against the variations of mains input voltage. The current sense voltage limit versus the MOSFET maximum on time is shown in Figure 5.

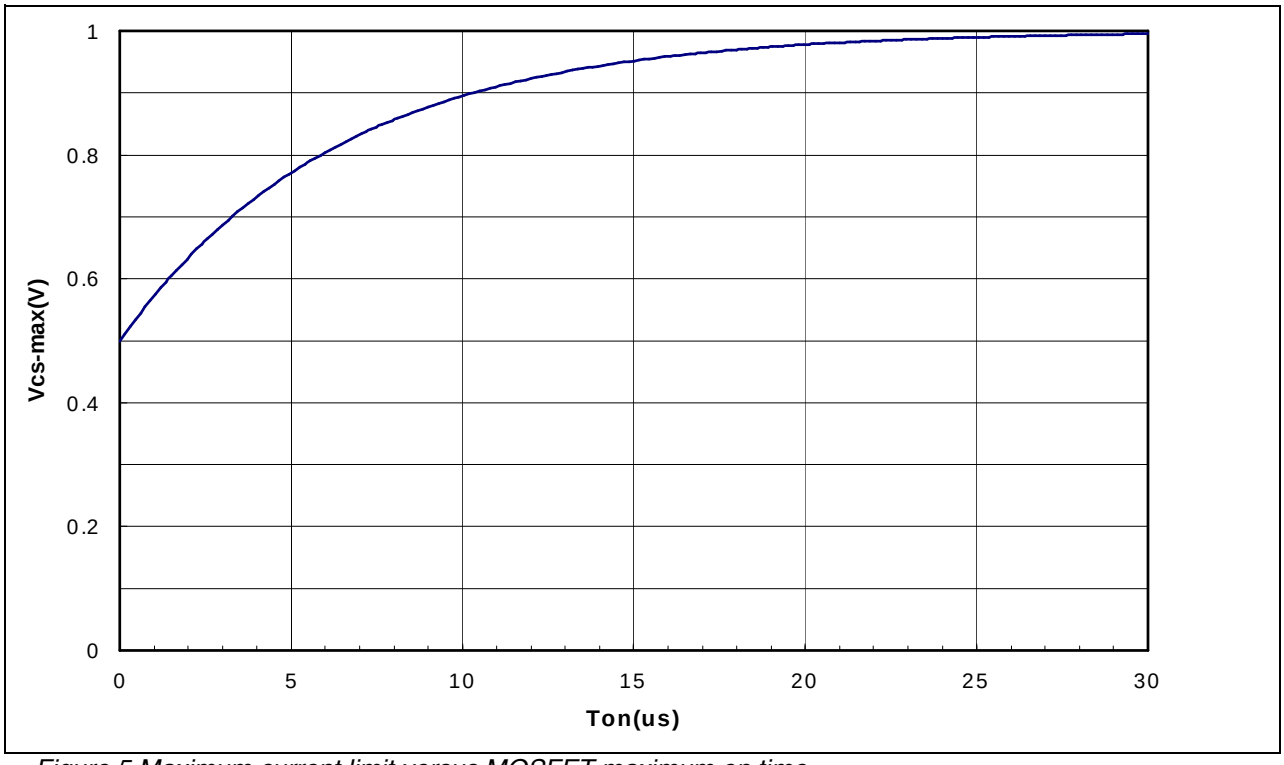


Figure 5 Maximum current limit versus MOSFET maximum on time

3.4 Active Burst Mode Operation

At very low load condition, the IC enters active burst mode operation to minimize the input power. Details about active burst mode operation are explained in the following paragraphs.

3.4.1 Entering Active Burst Mode Operation

For determination of entering active burst mode operation, three conditions apply:

the regulation voltage is lower than the threshold of V_{EB}(1.1V). Accordingly, the peak voltage across the shunt resistor is 0.11V;

the up/down counter has its maximal value of 7; and

a certain blanking time (24ms).

Once all of these conditions are fulfilled, the active burst mode flip-flop is set and the controller enters burst mode operation. This multi-conditional determination for entering active burst mode operation prevents mistriggering of entering active burst mode operation, so that the controller enters active burst mode operation only when the output power is really low during the preset blanking time.

3.4.2 During Active Burst Mode Operation

After entering the Active Burst Mode the regulation voltage rises as V_{OUT} starts to decrease due to the inactive PWM section. One comparator observes the regulation signal if the voltage level V_{BH} (3.6V) is exceeded. In that case the internal circuit is again activated by the internal bias to start with swtiching.

Turn-on of the power MOSFET is triggered by the timer. The PWM generator for burst mode operation composes of a timer with a fixed frequency of 80kHz, typically, and an analog comparator. Turn-off is resulted by comparison of the voltage signal v_1 with an internal threshold, by which the voltage across the shunt resistor V_{csB} is 0.25V, accordingly. A turn-off can also be triggered by the maximal duty ratio controller which sets the maximal duty ratio to 50%. In operation, the output flip-flop will be reset by one of these signals which come first.

If the output load is still low, the regulation signal decreases as the PWM section is operating. When regulation signal reaches the low threshold V_{BL}(3.0V), the internal bias is reset again and the PWM section is disabled until next time regultaion siganl increases beyond the V_{BH} threshold. If working in active burst mode the regulation signal is changing like a saw tooth between 3.0V and 3.6V shown in Figure 6.

3.4.3 Leaving Active Burst Mode

The regulation voltage immediately increases if there is a high load jump. This is observed by one comparator. As the current limit is 25% during active burst mode a certain load is needed so that regulation voltage can exceed V_{LB} (4.5V). After leaving active busrt mode, maximum current can now be provided to stabilize V_O. In addition, the up/down counter will be set to 1 immediately after leaving active burst mode. This is helpful to decrease the output voltage undershoot.

3.4.4 IC Power Supply During Active Burst Mode

During active burst mode operation, the power cell is activated again. Once the power from the auxiliary winding is not high enough to keep the VCC voltage above the preset value of V_{VCCBL}, the power cell keeps the VCC voltage at the preset value V_{VCCBL}. Otherwise, if the VCC voltage is still above this value, no current flows through the power cell though it is activated.

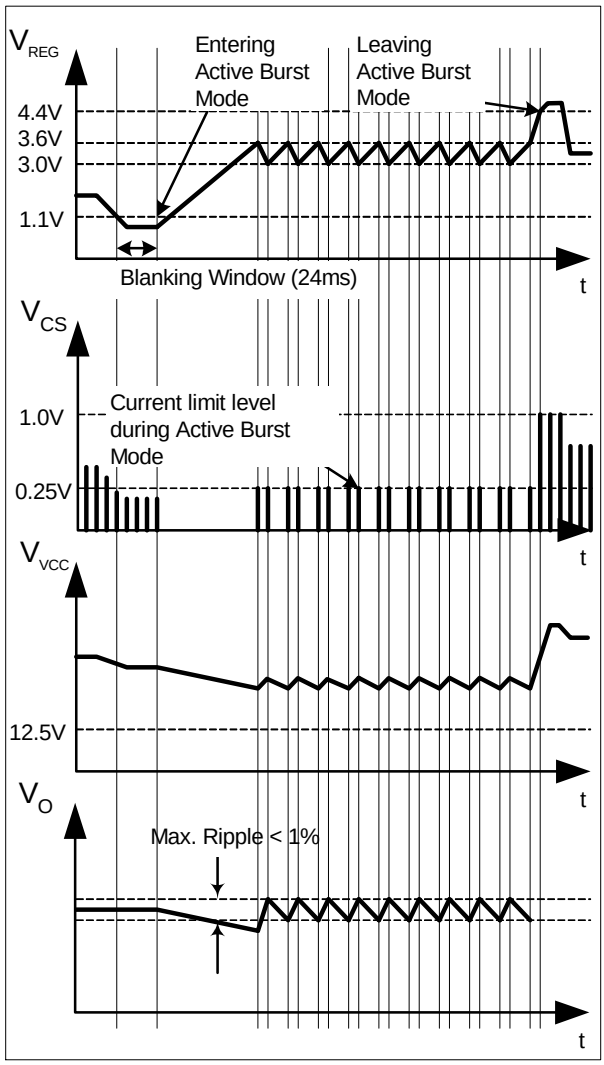


Figure 6 Signals in active burst mode

3.5 Protection Functions

The IC provides full protection functions. The following table summarizes these protection functions.

Table 2 Protection features

VCC Overvoltage	Auto Restart Mode
VCC Undervoltage	Auto Restart Mode
Overload/Open Loop	Auto Restart Mode
Output Overvoltage	Latched Off Mode
Short Winding	Latched Off Mode

During operation, the VCC voltage is continuously monitored. In case of an under- or an over-voltage, the IC is reset and the main power switch is then kept off. After the VCC voltage falls below the threshold V_{VCCUVP}, the power cell is activated. The VCC capacitor is then charged up. Once the voltage exceeds the threshold V_{VCCon}, the IC begins to operate with a new soft-start.

In case of open control loop or output over load, the regulation voltage will be pulled up . After a blanking time of 24ms, the IC enters auto-restart mode. The blanking time here enables the converter to provide a high power in case the increase in V_{REG} is due to a sudden load increase. During off-time of the power switch, the voltage at the zero-crossing pin is monitored for output over-voltage detection. If the voltage is higher than the preset threshold v_{OPOVP}, the IC is latched off after the preset blanking time.

If the voltage at the current sensing pin is higher than the preset threshold v_{csSW} during on-time of the power switch, the IC is latched off. This is short-winding protection.

During latch-off protection mode, the power cell is activated and it keeps the VCC voltage at the level of V_{VCCBL}.

4 Electrical Characteristics

Note: All voltages are measured with respect to ground (Pin 8). The voltage levels are valid if other ratings are not violated.

4.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 7 (VCC) is discharged before assembling the application circuit.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
HV Voltage	V_{HV}	-	500	V	
VCC Supply Voltage	V_{VCC}	-0.3	27	V	
REG Voltage	V_{REG}	-0.3	5.0	V	
ZC Voltage	V_{ZC}	-0.3	5.0	V	
CS Voltage	V_{CS}	-0.3	5.0	V	
OUT Voltage	V_{OUT}	-0.3	27	V	
Junction Temperature	T_j	-40	125	°C	
Storage Temperature	T_S	-55	150	°C	
Thermal Resistance Junction-Ambient	R_{thJA}	-	90	K/W	PG-DIP-8
ESD Capability	V_{ESD}	-	2	kV	Human body model[1)]

1) According to EIA/JESD22-A114-B (discharging a 100pF capacitor through a 1.5kΩ series resistor)

4.2 Operating Range

Note: Within the operating range the IC operates as described in the functional description.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
VCC Supply Voltage	V_{VCC}	V_{VCCUVP}	V_{VCCOVP}	V	
Junction Temperature	T_{jCon}	-25	125	°C	

4.3 Characteristics

4.3.1 Supply Section

Note: The electrical characteristics involve the spread of values guaranteed within the specified supply voltage and junction temperature range T_J from – 25 °C to 125°C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of V_{CC} = 18 V is assumed.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Start-Up Current	$I_{VCCstart}$	-	300	550	µA	V_{VCC} = 21V
VCC Charge Current	$I_{VCCcharge1}$	-	-	5.0	mA	V_{VCC} = 0V
	$I_{VCCcharge2}$	0.55	1.05	1.60	mA	V_{VCC} = 1V
	$I_{VCCcharge3}$	-	0.88	-	mA	V_{VCC} = 21V
Leakage Current of Power Cell	$I_{StartLeak}$	-	0.2	50	µA	V_{HV}= 610V at T_j = 100°C
Supply Current in normal operation	I_{VCCop}	-	2.5	3.6	mA	Output low
Supply Current in Auto Restart Mode with Inactive Gate	$I_{VCCrestart}$	-	300	-	µA	
Supply Current in Latch-off Mode	$I_{VCClatch}$	-	300	-	µA	
Supply Current in Burst Mode with Inactive Gate	$I_{VCCburst}$	-	500	950	µA	V_{REG} = 2.5V
Supply Voltage with no power from auxiliary winding in burst mode or in latch-off mode	V_{VCCBL}	-	12.5	-	V	V_{HV} = 100V
VCC Turn-On Threshold	V_{VCCon}	21.2	22.0	22.8	V	
Internal Reference Voltage	V_{REF}	4.8	5.0	5.2	V	measured at pin REG, I_{REG} = 0

4.3.2 PWM Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Regulation Pull-Up Resistor	R_{REG}	14	23	33	kΩ	
PWM-OP Gain	A_V	3.18	3.3	-	-	
Offset for Voltage Ramp	V_{OS}	0.63	0.7	-	V	
Soft-Start time	t_{SOFTS}	18	21	38	ms	
Zero crossing threshold voltage	V_{ZCT1}	20	50	110	mV	
Ringing suppression threshold	V_{ZCT2}		0.7		V	
Minimum ringing suppression time	t_{ZCRST1}	2.2	4.2	5.5	µs	$V_{ZC} > V_{ZCT2}$
Maximum ringing suppression time	t_{ZCRST2}	-	42	-	µs	$V_{ZC} < V_{ZCT2}$
Threshold to set Up/Down Counter to one	V_{RM}	-	3.9	-	V	
Threshold for downward counting	V_{RH}	-	3.2	-	V	
Threshold for upward counting	V_{RL}	-	2.5	-	V	
Counter time[1)]	t_{COUNT}	-	48	-	ms	
Maximum restart time in normal operation	t_{sMax}	33	42	60	µs	$V_{ZC}<V_{ZCT1}$
Leading Edge Blanking	t_{LEB}	200	330	460	ns	
Peak current limitation in normal operation	V_{csth}	0.95	1.0	1.05	V	
Regulation voltage for entering Burst Mode	V_{EB}	-	1.1	-	V	
Regulation voltage for leaving Burst Mode	V_{LB}	-	4.5	-	V	
Regulation voltage for burst-on	V_{BH}	-	3.6	-	V	
Regulation voltage for burst-off	V_{BL}	-	3.0	-	V	
Fixed Switching Frequency in Burst Mode	f_{sB}	64	80	96	kHz	
Max. Duty Cycle in Burst Mode	D_{maxB}	-	0.5	-		
Peak Current Limitation in Burst Mode	V_{csB}	0.22	0.25	0.3	V	

1) The parameter is not subject to production test - verified by design/characterization

4.3.3 Protection

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
VCC overvoltage threshold	V_{VCCOVP}	24	25.0	26	V	
VCC undervoltage threshold	V_{VCCUVP}	10.3	11.0	11.7	V	
Over Load or Open Loop Detection threshold for OLP protection at REG pin	V_{OLP}	-	4.5	-	V	
Over Load or Open Loop Protection Blanking Time	T_{OLP-B}	16	24	35	ms	
Output Overvoltage detection threshold at the ZC pin	V_{OPOVP}	-	4.5	-	V	
Threshold for short winding protection	V_{csSW}	-	1.68	-	V	

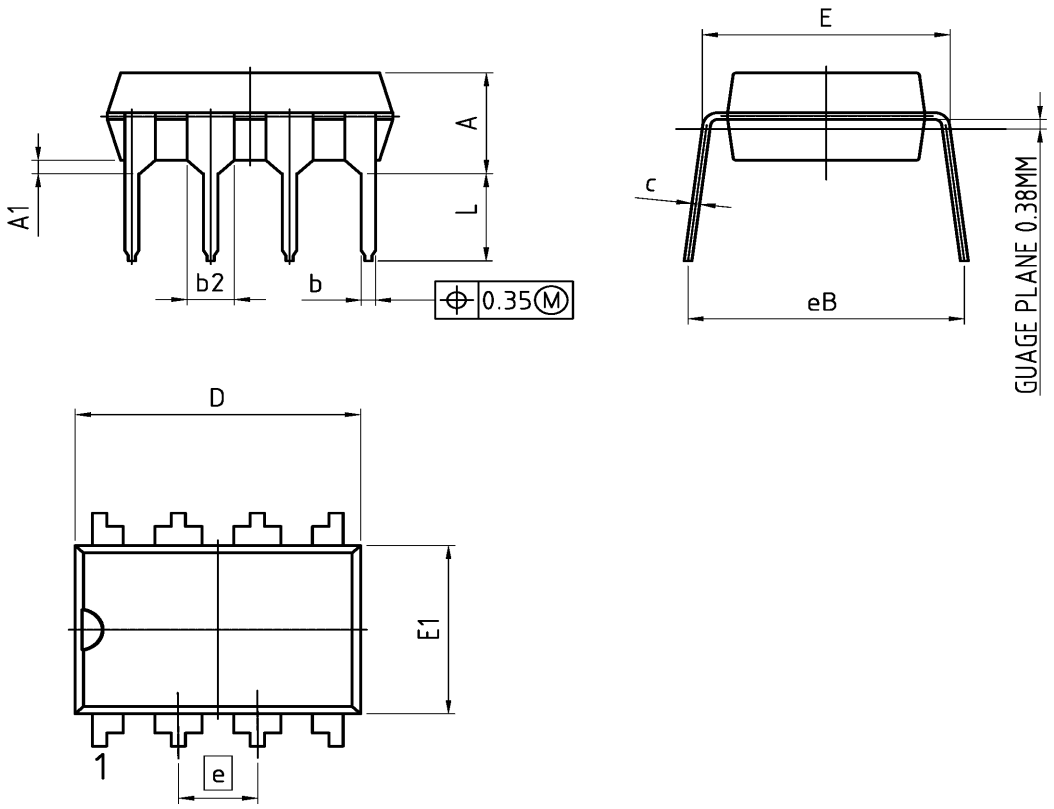
Note: The trend of all the voltage levels in the Control Unit is the same regarding the deviation except V_{VCCOVP}

4.3.4 Gate Driver

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output voltage at logic low	$V_{GATElow}$	-	0.7	-	V	I_{OUT} = 20mA
Output voltage at logic high	$V_{GATEhigh}$	-	10.0	-	V	I_{OUT} = -20mA
Output voltage active shut down	$V_{GATEasd}$	-	1.0	-	V V	V_{VCC} = 7V I_{OUT} = 20mA
Rise Time	t_{rise}	-	100	-	ns	C_{OUT} = 4.7nF
Fall Time	t_{fall}	-	25	-	ns	C_{OUT} = 4.7nF

5 Outline Dimension

PG-DIP-8
(Leadfree Plastic Dual In-Line)



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	4.8	-	0.189
A1	0.38	-	0.015	-
b	0.36	0.56	0.014	0.022
b2	-	1.700	-	0.067
c	0.15	0.36	0.006	0.014
D	9.100	9.770	0.358	0.385
E	7.490	8.260	0.295	0.325
E1	6.100	6.600	0.150	0.157
e	2.54 BSC		0.1 BSC	
N	8		8	
eB	7.9	9.9	0.311	0.390
L	3	-	0.118	-

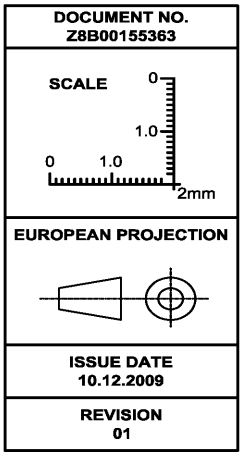


Figure 7 PG-DIP-8

Total Quality Management

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Unternehmensweit orientieren wir uns dabei auch an „top“ (Time Optimized Processes), um Ihnen durch größere Schnelligkeit den entscheidenden Wettbewerbsvorsprung zu verschaffen.

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