M81019FP

1200V HIGH VOLTAGE HALF BRIDGE DRIVER

DESCRIPTION

M81019FP is high voltage Power MOSFET and IGBT gate driver for half bridge applications.

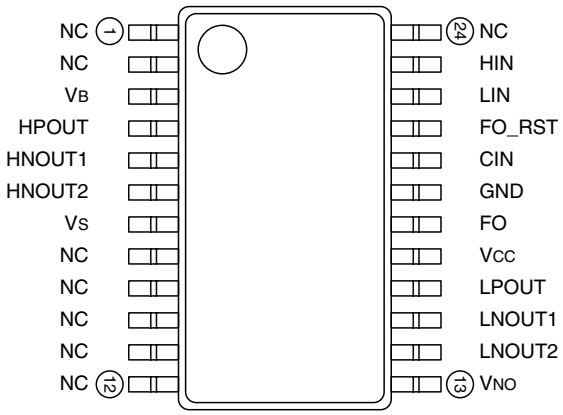
FEATURES

- Floating supply voltage up to 1200V
- Low quiescent power supply current
- Separate sink and source current output up to ±1A (typ)
- Active Miller effect clamp NMOS with sink current up to –1A (typ)
- Input noise filters
- Over-current detection and output shutdown
- High side under voltage lockout
- FO pin which can input and output Fault signals to communicate with controllers and synchronize the shut down with other phases
- Pb-free
- 24-Lead SSOP package

APPLICATIONS

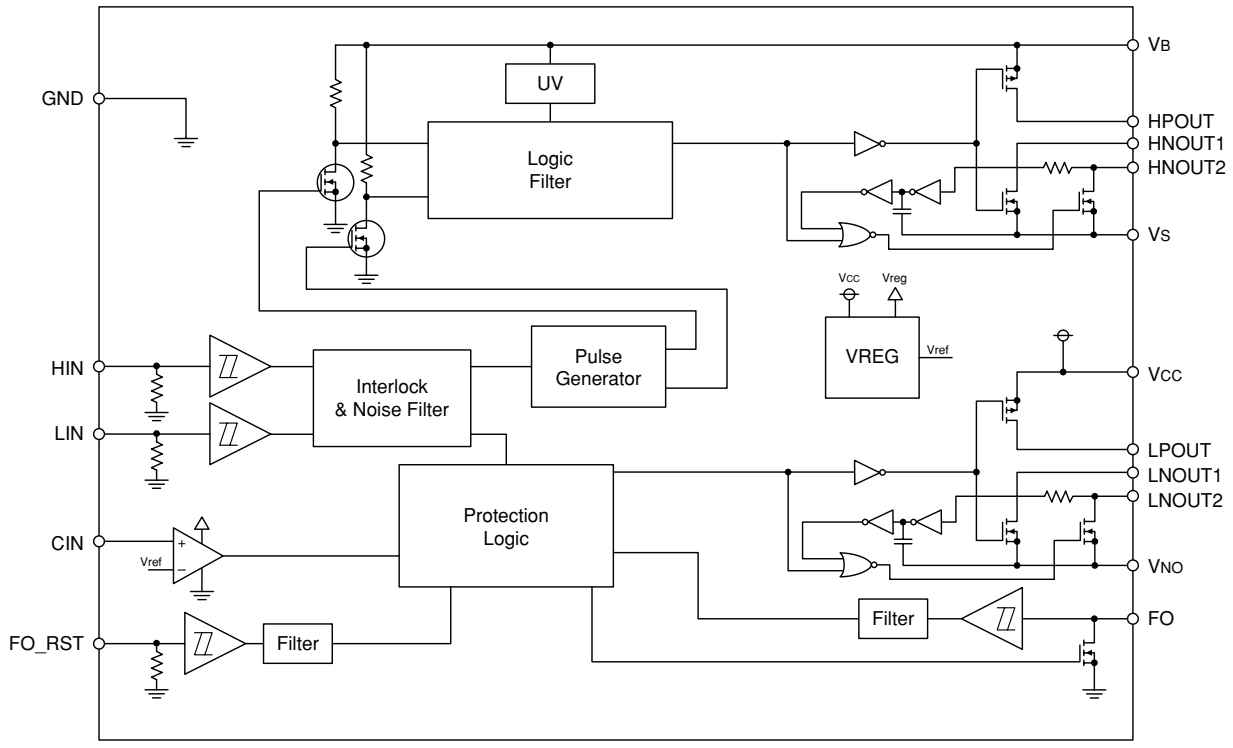
Power MOSFET and IGBT gate driver for Medium and Micro inverter or general purpose.

PIN CONFIGURATION (TOP VIEW)



Outline: 24P2Q

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings indicate limitation beyond which destruction of device may occur. All voltage parameters are absolute voltage reference to GND unless otherwise specified.

Symbol	Parameter	Test conditions	Ratings	Unit
V_B	High side floating supply absolute voltage		–0.5 ~ 1224	V
V_S	High side floating supply offset voltage		V_B–24 ~ V_B+0.5	V
V_{BS}	High side floating supply voltage	$V_{BS} = V_B–V_S$	–0.5 ~ 24	V
V_{HO}	High side output voltage		V_S–0.5 ~ V_B+0.5	V
V_{CC}	Low side fixed supply voltage		–0.5 ~ 24	V
V_{NO}	Power ground		V_{CC}–24 ~ V_{CC}+0.5	V
V_{LO}	Low side output voltage		V_{NO}–0.5 ~ V_{CC}+0.5	V
V_{IN}	Logic input voltage	HIN, LIN, FO_RST	–0.5 ~ V_{CC}+0.5	V
V_{FO}	FO input/output voltage		–0.5 ~ V_{CC}+0.5	V
V_{CIN}	CIN input voltage		–0.5 ~ V_{CC}+0.5	V
dVs/dt	Allowable offset voltage slew rate		±50	V/ns
Pd	Package power dissipation	Ta = 25°C, On PCB	1.6	W
Kθ	Linear derating factor	Ta > 25°C, On PCB	16	mW/°C
Rth(j-c)	Junction-case thermal resistance		60	°C/W
Tj	Junction temperature		–40 ~ 125	°C
Topr	Operation temperature		–40 ~ 100	°C
Tstg	Storage temperature		–40 ~ 125	°C

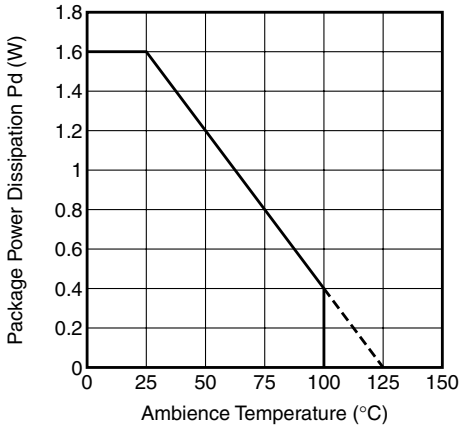
RECOMMENDED OPERATING CONDITIONS

For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to GND unless otherwise specified.

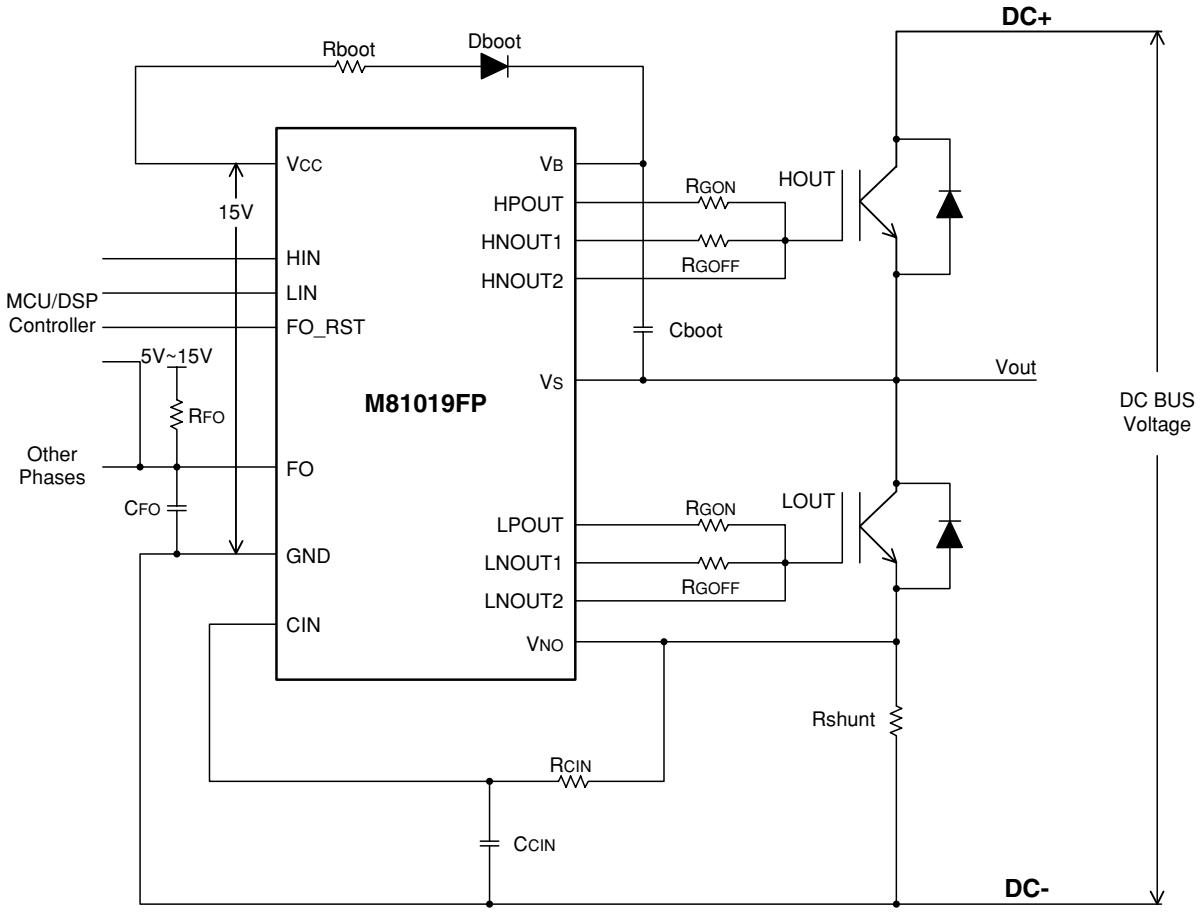
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_B	High side floating supply absolute voltage		V_S+13.5	V_S+15	V_S+20	V
V_S	High side floating supply offset voltage	V_{BS} > 13.5V	–5	—	900	V
V_{BS}	High side floating supply voltage	$V_{BS} = V_B–V_S$	13.5	15	20	V
V_{HO}	High side output voltage		V_S	—	V_S+20	V
V_{CC}	Low side fixed supply voltage		13.5	—	20	V
V_{NO}	Power ground		–0.5	—	5	V
V_{LO}	Low side output voltage		V_{NO}	—	V_{CC}	V
V_{IN}	Logic input voltage	HIN, LIN, FO_RST	0	5	V_{CC}	V
V_{FO}	FO input/output voltage		0	—	V_{CC}	V
V_{CIN}	CIN input voltage		0	—	5	V

Note : For proper operation, the device should be used within the recommend conditions.

THERMAL DERATING FACTOR CHARACTERISTIC



TYPICAL CONNECTION



Note: If HVIC is working in high noise environment, it is recommended to connect a 1nF ceramic capacitor (C_{FO}) to FO pin.

ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=V_{BS} (=V_B–V_S)=15V, unless otherwise specified)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{FS}	High side leakage current	V_B = V_S = 1200V	—	—	1.0	μA
I_{BS}	V_{BS} quiescent supply current	HIN = LIN = 0V	—	0.5	0.8	mA
I_{CC}	V_{CC} quiescent supply current	HIN = LIN = 0V	—	1	1.5	mA
V_{OH}	High level output voltage	I_O = –20mA, HPOUT, LPOUT	14.5	—	—	V
V_{OL}	Low level output voltage	I_O = 20mA, HNOUT1, LNOUT1	—	—	0.5	V
V_{IH}	High level input threshold voltage	HIN, LIN, FO_RST	4.0	—	—	V
V_{IL}	Low level input threshold voltage	HIN, LIN, FO_RST	—	—	0.6	V
I_{IH}	High level input bias current	V_{IN} = 5V	0.6	1	1.4	mA
I_{IL}	Low level input bias current	V_{IN} = 0V	–0.01	0	0.01	mA
tFilter	Input signals filter time	HIN, LIN, FO_RST, FO	80	200	500	ns
V_{HNO2}	High side active Miller clamp NMOS input threshold voltage	V_{IN} = 0V	2.0	3.4	5	V
V_{LNO2}	Low side active Miller clamp NMOS input threshold voltage	V_{IN} = 0V	6.0	7.6	9	V
tV_{NO2}	Active Miller clamp NMOS filter time	V_{IN} = 0V	—	400	—	ns
V_{OLFO}	Low level FO output voltage	I_{FO} = 1mA	—	0.4	0.95	V
V_{IHFO}	High level FO input threshold voltage		4.0	—	—	V
V_{ILFO}	Low level FO input threshold voltage		—	—	0.6	V
V_{BSuvr}	V_{BS} supply UV reset voltage		10.5	11.3	12.1	V
V_{BSuvt}	V_{BS} supply UV trip voltage		10	10.8	11.6	V
V_{BSuvh}	V_{BS} supply UV hysteresis voltage	V_{BSuvh} = V_{BSuvr}–V_{BSuvt}	0.2	0.5	0.8	V
tV_{BSuv}	V_{BS} supply UV filter time		4	8	16	μs
V_{CIN}	CIN trip voltage		0.4	0.5	0.6	V
V_{POR}	POR trip voltage		4	5.5	7.5	V
I_{OH}	Output high level short circuit pulsed current	HPOUT (LPOUT) = 0V, HIN = 5V, PW < 5μs	—	1	—	A
$I_{OL}1$	Output low level short circuit pulsed current	HNOUT1 (LNOUT1) = 15V, LIN = 5V, PW < 5μs	—	–1	—	A
$I_{OL}2$	Active Miller clamp NMOS output low level short circuit pulsed current	HNOUT2 (LNOUT2) = 15V, LIN = 5V, PW < 5μs	—	–1	—	A
R_{OH}	Output high level on resistance	I_O = –1A, R_{OH} = (V_{OH}–V_O) /I_O	—	15	—	Ω
$R_{OL}1$	Output low level on resistance	I_O = 1A, $R_{OL}1$ = V_O/I_O	—	15	—	Ω
$R_{OL}2$	Active Miller clamp NMOS output low level on resistance	I_O = 1A, $R_{OL}2$ = V_O/I_O	—	15	—	Ω
tdLH(HO)	High side turn-on propagation delay	HPOUT short to HNOUT1 and HNOUT2, CL = 1nF	1	1.27	1.8	μs
tdHL(HO)	High side turn-off propagation delay	HPOUT short to HNOUT1 and HNOUT2, CL = 1nF	0.9	1.21	1.8	μs
tdLH(LO)	Low side turn-on propagation delay	LPOUT short to LNOUT1 and LNOUT2, CL = 1nF	1	1.39	1.9	μs
tdHL(LO)	Low side turn-off propagation delay	LPOUT short to LNOUT1 and LNOUT2, CL = 1nF	0.9	1.19	1.7	μs
tr	Output turn-on rise time	CL = 1nF	—	40	—	ns
tf	Output turn-off fall time	CL = 1nF	—	40	—	ns
Δ tdLH	Delay matching, high side turn-on and low side turn-off	tdLH (HO)-tdHL (LO)	—	80	—	ns
Δ tdHL	Delay matching, high side turn-off and low side turn-on	tdLH (LO)-tdHL (HO)	—	180	—	ns

Note: Typ is not specified.

FUNCTION TABLE (Q: Keep previous status)

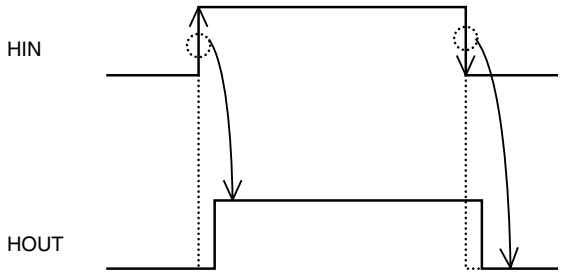
HIN	LIN	FO_RST	CIN	FO (Input)	VBS/UV	VCC/POR	HOUT	LOUT	FO (Output)	Behavioral status
H→L	L	L	L	–	H	H	L	L	H	
H→L	H	L	L	–	H	H	L	H	H	
L→H	L	L	L	–	H	H	H	L	H	
L→H	H	L	L	–	H	H	Q	Q	H	Interlock active
X	H	X	H	–	X	H	L	L	L	CIN tripping when LIN=H
X	L	X	H	–	X	H	Q	Q	H	CIN not tripping when LIN=L
X	X	X	X	L	X	H	L	L	L	Output shuts down when FO=L
X	X	X	X	–	X	L	L	L	H	VCC power reset
X	L	L	L	–	L	H	L	L	H	VBS power reset
X	H	L	L	–	L	H	L	H	H	VBS power reset is tripping when LIN=H

Note1 : "L" status of VBS/UV indicates a high side UV condition; "L" status of VCC/POR indicates a VCC power reset condition.

2 : In the case of both input signals (HIN and LIN) are "H", output signals (HOUT and LOUT) keep previous status.

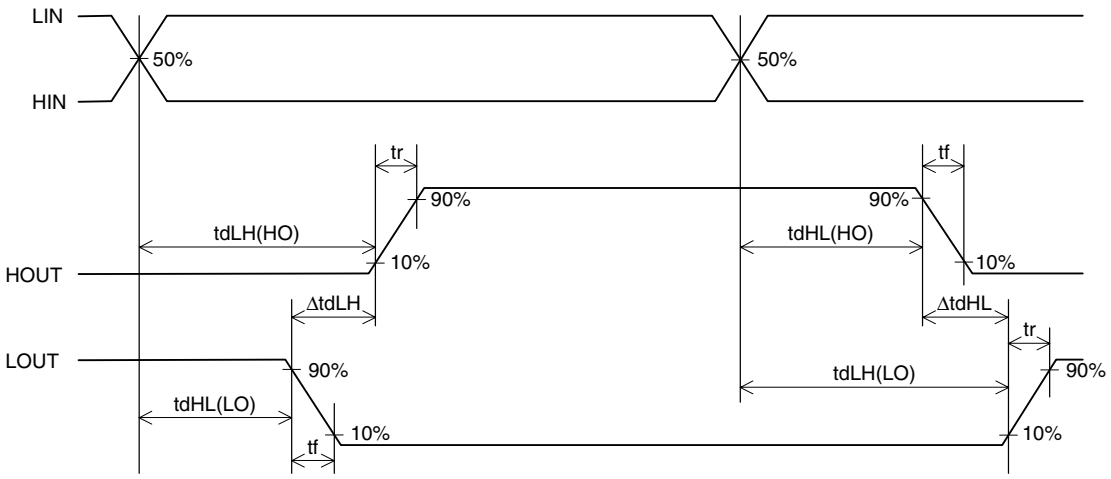
3 : X (HIN) : L→H or H→L. Other : H or L.

4 : Output signal (HOUT) is triggered by the edge of input signal.



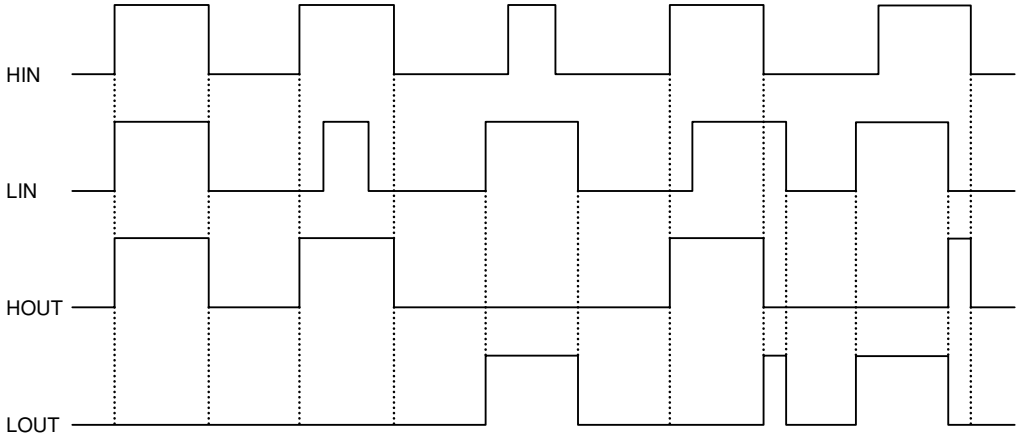
FUNCTIONAL DESCRIPTION

1. INPUT/OUTPUT TIMING DIAGRAM



2. INPUT INTERLOCK TIMING DIAGRAM

When the input signals (HIN/LIN) are high level at the same time, the outputs (HOUT/LOUT) keep their previous status. But if signals (HIN/LIN) are going to high level simultaneously, HIN signals will get active and cause HOUT to enter “H” status.



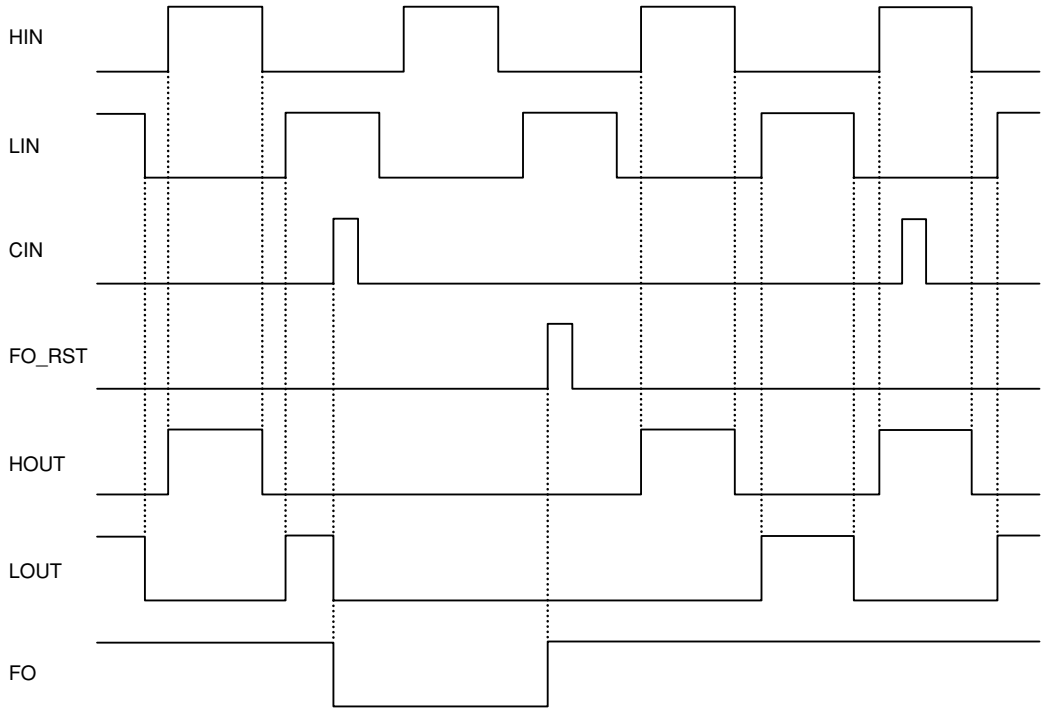
Note1: The minimum input pulse width at HIN/LIN should be to more than 500ns (because of HIN/LIN input noise filter circuit).

Note2: If a high-high status of input signals (HIN/LIN) is ended with only one input signal entering low level and another still being in high level, the output will enter high-low status after the delay match time (not shown in the figure above).

Note3: Delay times between input and output signals are not shown in the figure above.

3. SHORT CIRCUIT PROTECTION TIMING DIAGRAM

When an over-current is detected by exceeding the threshold at the CIN and LIN is at high level at the same time, the short circuit protection will get active and shutdown the outputs while FO will issue a low level (indicating a fault signal). The fault output latch is reset by a high level signal at FO_RST pin and then FO will return to high level while the output of the driver will respond to the following active input signal.

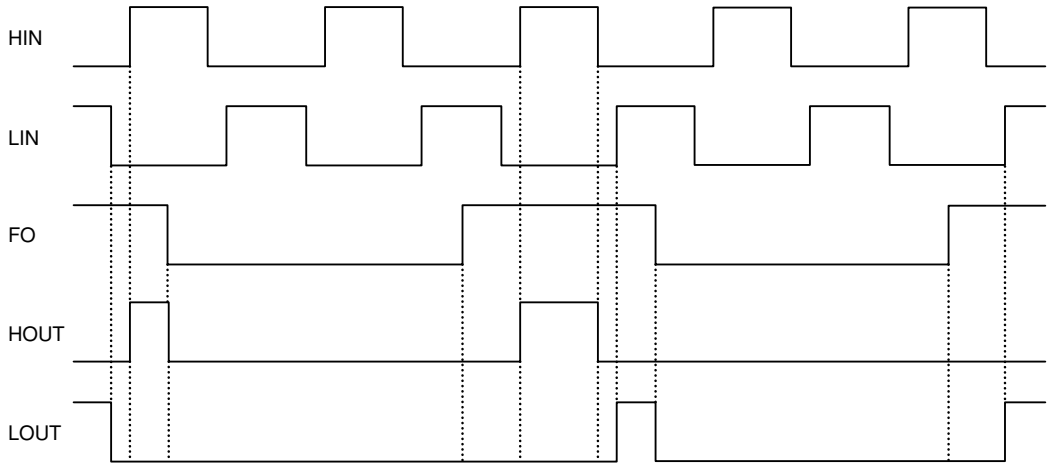


Note1 : Delay times between input and output signals are not shown in the figure above.

Note2 : The minimum FO_RST pulse width should be more than 500ns (because of FO_RST input filter circuit).

4. FO INPUT TIMING DIAGRAM

When FO is pulled down to low level in case the FO of other phases becomes low level (fault happened) or the MCU/DSP sets FO to low level, the outputs (HOUT, LOUT) of the driver will be shut down. As soon as FO goes high again, the output will respond to the following active input signal.

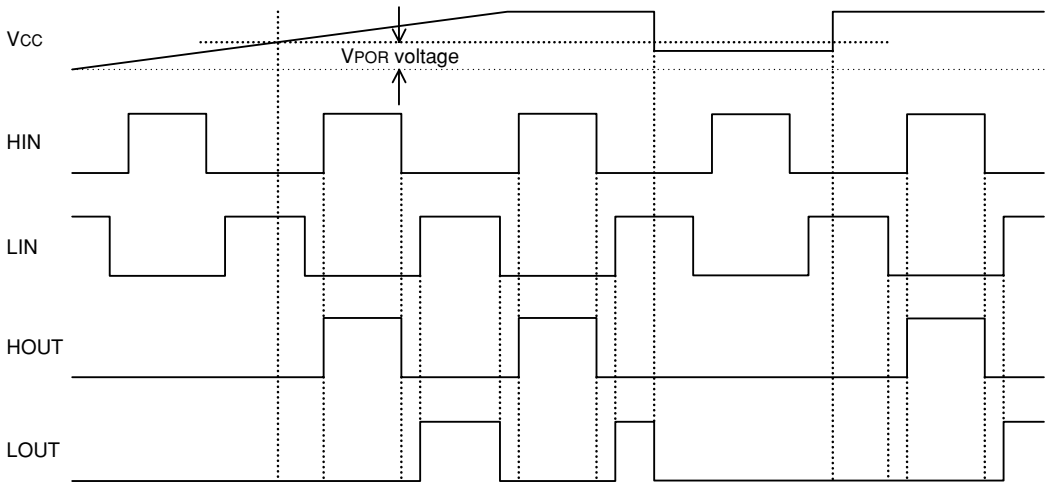


Note1: Delay times between input and output signals are not shown in the figure above.

Note2: The minimum FO pulse width should be more than 500ns (because of FO input filter circuit).

5. LOW SIDE V_{CC} SUPPLY POWER RESET SEQUENCE

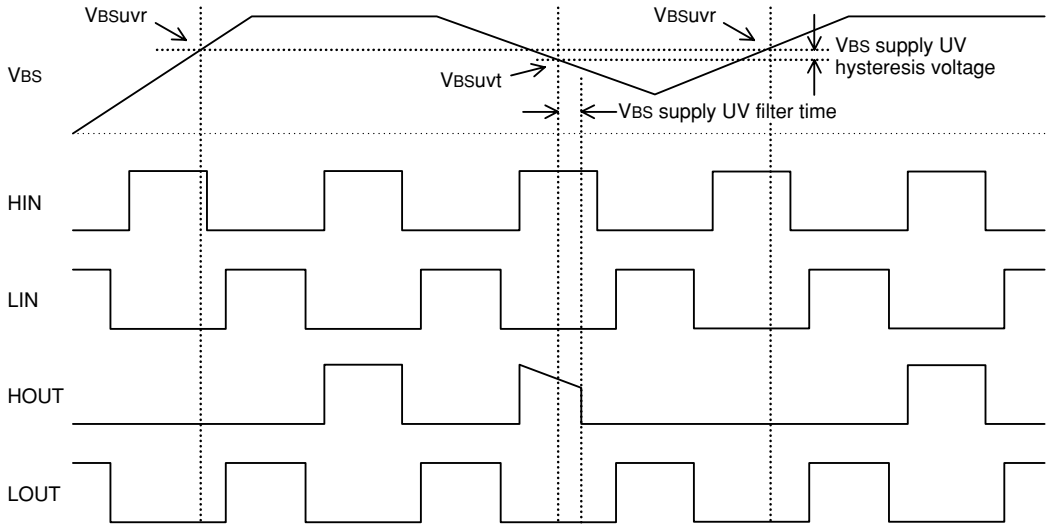
When the V_{CC} supply voltage is lower than power reset trip voltage, the power reset gets active and the outputs (HOUT/LOUT) become "L". As soon as the V_{CC} supply voltage goes higher than the power reset trip voltage, the outputs will respond to the following active input signals.



Note1: Delay times between input and output signals are not shown in the figure above.

6. HIGH SIDE V_{BS} SUPPLY UNDER VOLTAGE LOCKOUT SEQUENCE

When V_{BS} supply voltage drops below the V_{BS} supply UV trip voltage and the duration in this status exceeds the V_{BS} supply UV filter time, the output of the high side is locked. As soon as the V_{BS} supply voltage rises above the V_{BS} supply UV reset voltage, the output will respond to the following active HIN signal.



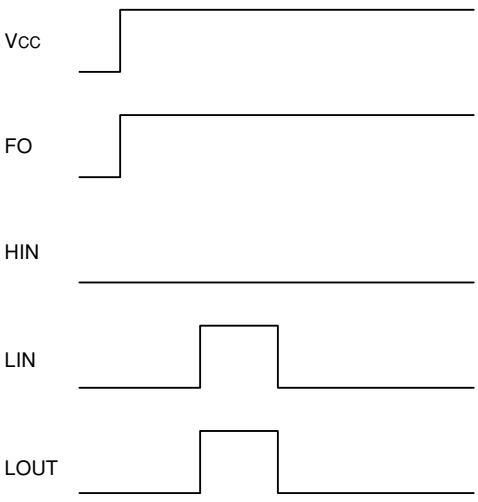
Note1: Delay times between input and output signals are not shown in the figure above.

7. POWER START-UP SEQUENCE

At power supply start-up the following sequence is recommended when bootstrap supply topology is used.

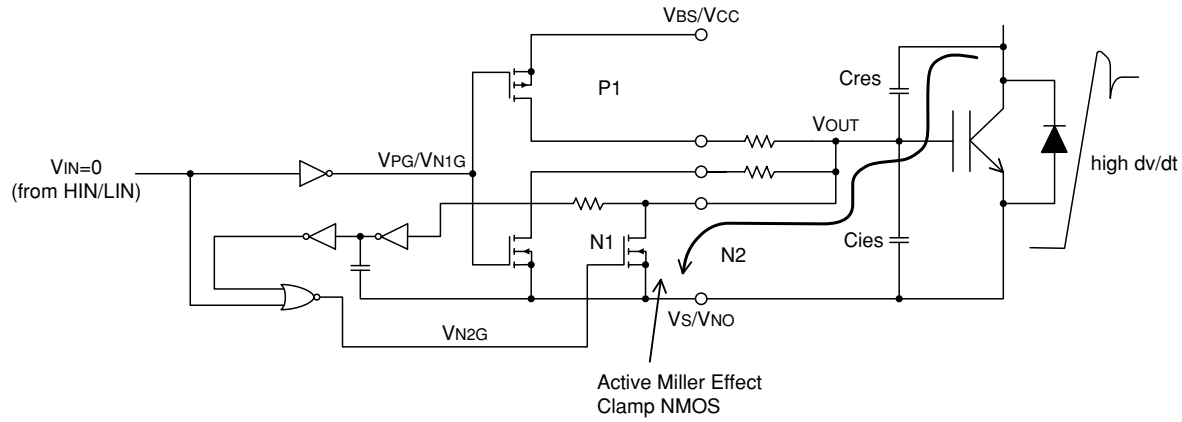
(1). Apply V_{CC}.
(2). Make sure that FO is at high level.
(3). Set LIN to high level and HIN to low level so that bootstrap capacitor could be charged.
(4). Set LIN to low level.

Note: If two power supply are used for supplying V_{CC} and V_{BS} individually, it is recommended to set V_{CC} first and then set V_{BS}.

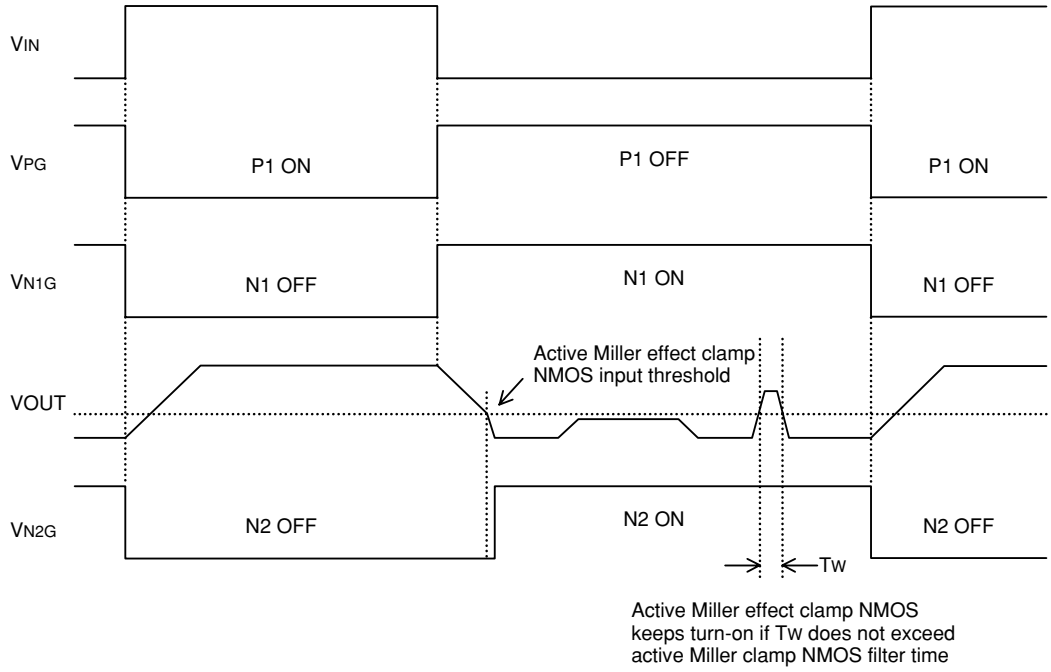


8. ACTIVE MILLER EFFECT CLAMP NMOS OUTPUT TIMING DIAGRAM

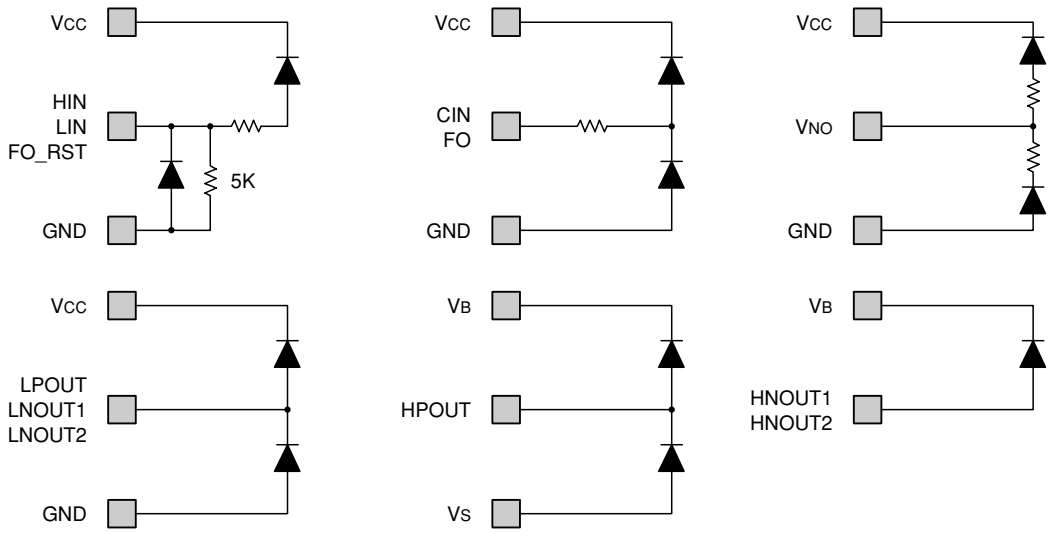
The structure of the output driver stage is shown in following figure. This circuit structure employs a solution for the problem of the Miller current through Cres in IGBT switching applications. Instead of driving the IGBT gate to a negative voltage to increase the safety margin, this circuit structure uses a NMOS to establish a low impedance path to prevent the self-turn-on due to the parasitic Miller capacitor in power switches.



When HIN/LIN is at low level and the voltage of the VOUT (IGBT gate voltage) is below active Miller effect clamp NMOS input threshold voltage, the active Miller effect clamp NMOS is being turned on and opens a low resistive path for the Miller current through Cres.

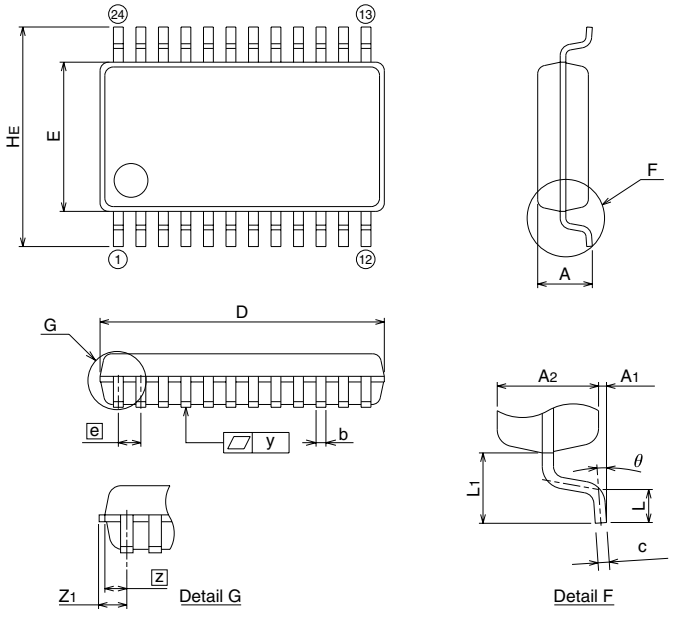


INTERNAL DIODE CLAMP CIRCUITS FOR INPUT AND OUTPUT PINS



PACKAGE OUTLINE

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP24-P-300-0.80	–	0.2	Cu Alloy



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.1
A1	0	0.1	0.2
A2	–	1.8	–
b	0.3	0.35	0.45
c	0.18	0.2	0.25
D	10.0	10.1	10.2
E	5.2	5.3	5.4
e	–	0.8	–
HE	7.5	7.8	8.1
L	0.4	0.6	0.8
L1	–	1.25	–
Z	–	0.65	–
Z1	–	–	0.8
y	–	–	0.1
θ	0°	–	8°
b2	–	0.5	–
e1	–	7.62	–
l2	1.27	–	–

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