STW34NB20

N-CHANNEL 200V - 0.062 Ω - 34A TO-247
PowerMESH™ MOSFET

Table 1. General Features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STW34NB20	200 V	< 0.075 Ω	34 A

FEATURES SUMMARY

- TYPICAL $R_{DS(on)}$ = 0.062 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED

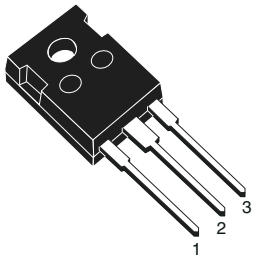
DESCRIPTION

Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performances. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest $R_{DS(on)}$ per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

APPLICATIONS

- SWITCH MODE POWER SUPPLIES (SMPS)
- DC-AC CONVERTERS FOR WELDING EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLIES AND MOTOR DRIVE
- HIGH CURRENT, HIGH SPEED SWITCHING

Figure 1. Package



TO-247

Figure 2. Internal Schematic Diagram

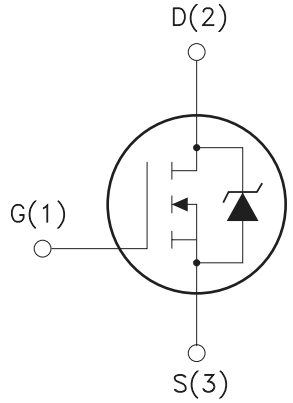


Table 2. Order Codes

Part Number	Marking	Package	Packaging
STW34NB20	W34NB20	TO-247	TUBE

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	200	V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	200	V
V_{GS}	Gate-source Voltage	± 30	V
I_D	Drain Current (cont.) at T_C = 25 °C	34	A
I_D	Drain Current (cont.) at T_C = 100 °C	21	A
I_{DM} (1)	Drain Current (pulsed)	136	A
P_{tot}	Total Dissipation at T_C = 25 °C	180	W
	Derating Factor	1.44	W°/C
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

Note: 1. Pulse width limited by safe operating area

Table 4. Thermal Data

Symbol	Parameter		Value	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	0.69	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	30	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		300	°C

Table 5. Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, δ < 1%)	34	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C; I_D = I_{AR}; V_{DD} = 50 V)	650	mJ

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Table 6. Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 μA V_{GS} = 0	200			V
I_{DSS}	Zero Gate Voltage	V_{DS} = Max Rating			1	μA
	Drain Current (V_{GS} = 0)	V_{DS} = Max Rating Tc = 125 °C			10	μA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 30 V			± 100	nA

Table 7. On (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}; I_D = 250 μA	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V; I_D = 17 A		0.062	0.075	Ω

Note: 1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %

Table 8. Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$; I_D = 17 A	8	17		S
C_{iss}	Input Capacitance	V_{DS} = 25 V; f = 1 MHz; V_{GS} = 0		2400	3300	pF
C_{oss}	Output Capacitance			650	900	pF
C_{rss}	Reverse Transfer Capacitance			90	130	pF

Note: 1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %

Table 9. Switching On

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
td(on)	Turn-on Time	V_{DD} = 100 V; I_D = 17 A; R_G = 4.7 Ω		30	40	ns
tr	Rise Time	V_{GS} = 10 V (see test circuit, Figure 16)		40	55	ns
Q_g	Total Gate Charge	V_{DD} = 160 V; I_D = 34 A; V_{GS} = 10 V		60	80	nC
Q_{gs}	Gate-Source Charge			19		nC
Q_{gd}	Gate-Drain Charge			29		nC

Table 10. Switching Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	V_{DD} = 160 V; I_D = 34 A; R_G = 4.7 Ω		17	23	ns
t_f	Fall Time	V_{GS} = 10 V (see test circuit, Figure 18)		18	24	ns
t_c	Cross-over Time			35	47	ns

Table 11. Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				34	A
I_{SDM} (1)	Source-drain Current (pulsed)				136	A
V_{SD} (2)	Forward On Voltage	I_{SD} = 34 A; V_{GS} = 0			1.5	V
t_{rr}	Reverse Recovery Time	I_{SD} = 34 A; di/dt = 100 A/µs			290	ns
Q_{rr}	Reverse RecoveryCharge	V_{DD} = 50 V; T_j = 150 °C (see test circuit, Figure 18)			2.7	µC
I_{RRAM}	Reverse RecoveryCharge				18.5	A

Note: 1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

Figure 3. Safe Operating Area

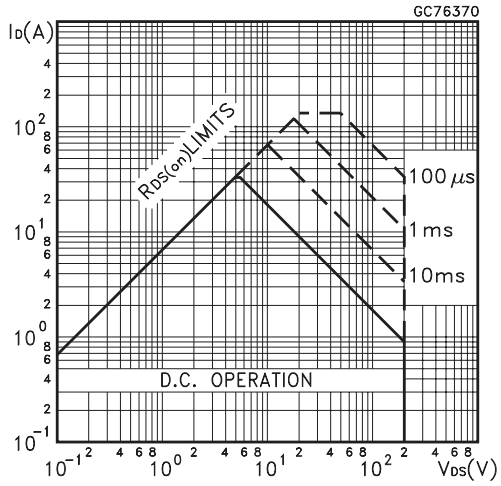


Figure 4. Thermal Impedance

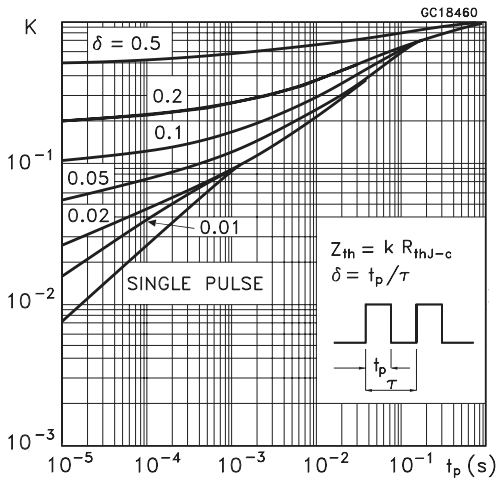


Figure 5. Output Characteristics

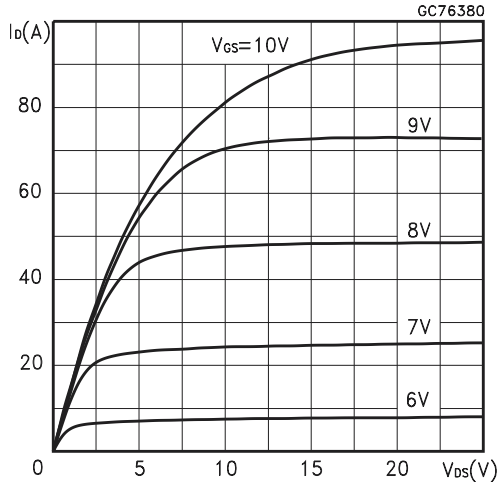


Figure 6. Transfer Characteristics

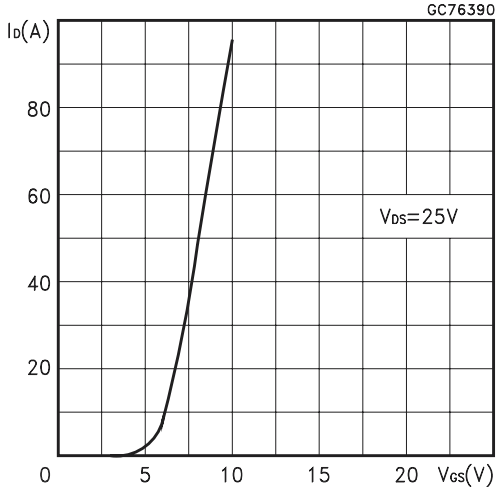


Figure 7. Transconductance

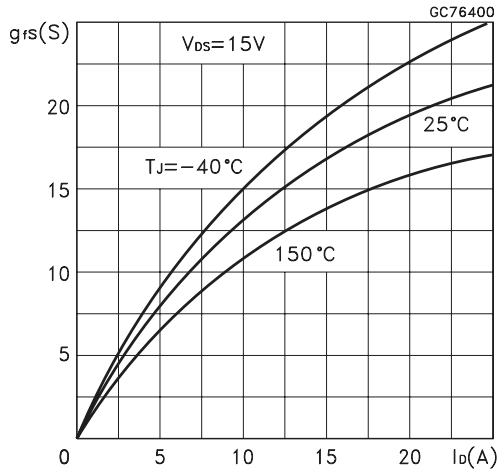


Figure 8. Static Drain-source On Resistance

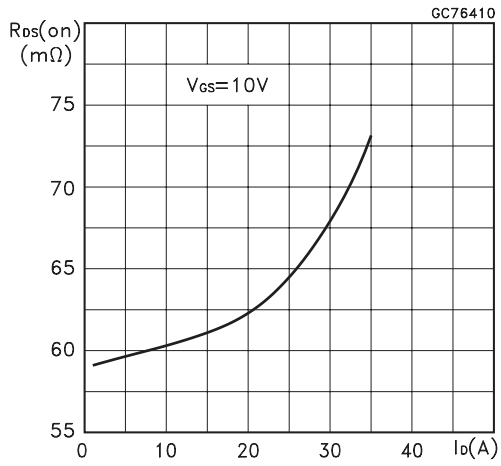


Figure 9. Gate Charge vs Gate-source Voltage

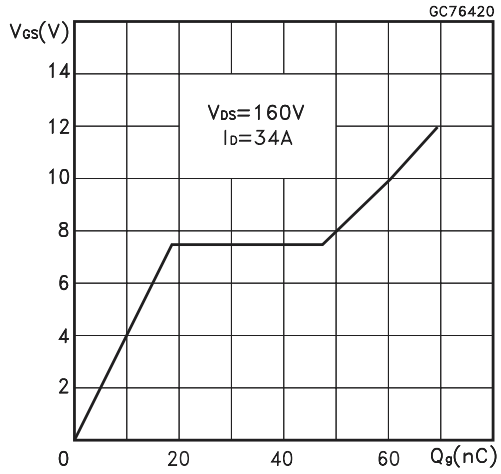


Figure 10. Capacitance Variations

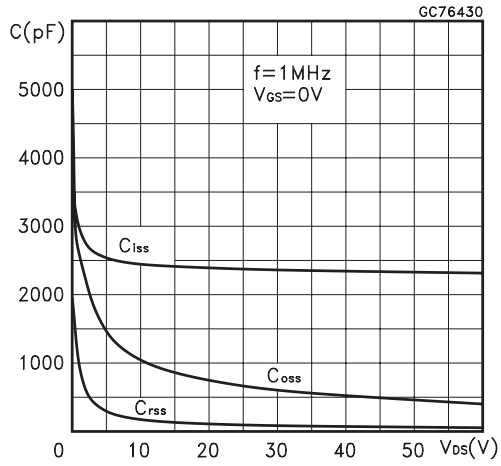


Figure 11. Normalized Gate Thresold Voltage vs Temperature

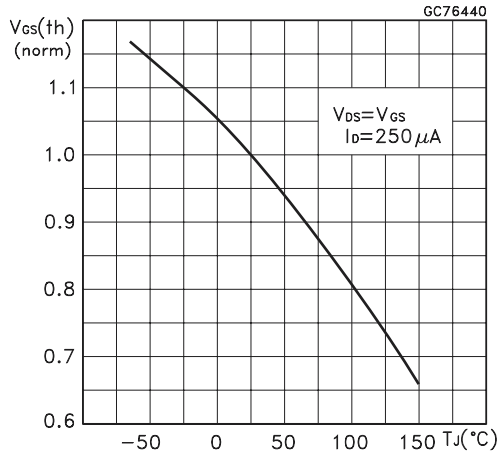


Figure 12. Normalized On Resistance vs Temperature

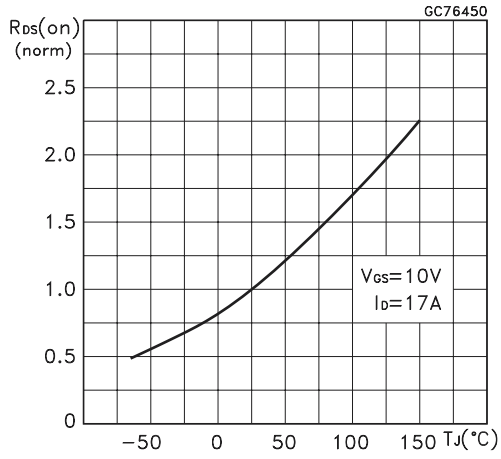


Figure 13. Source-drain Diode Forward Characteristics

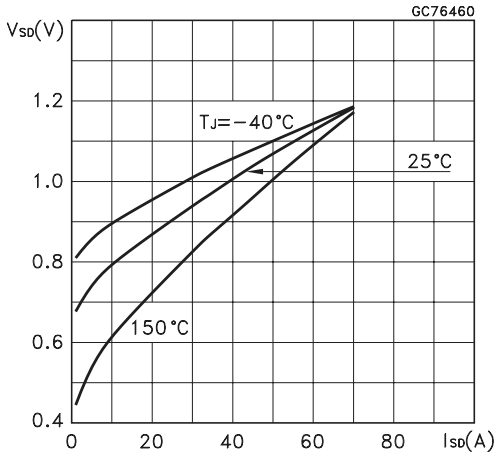


Figure 14. Unclamped Inductive Load Test Circuit

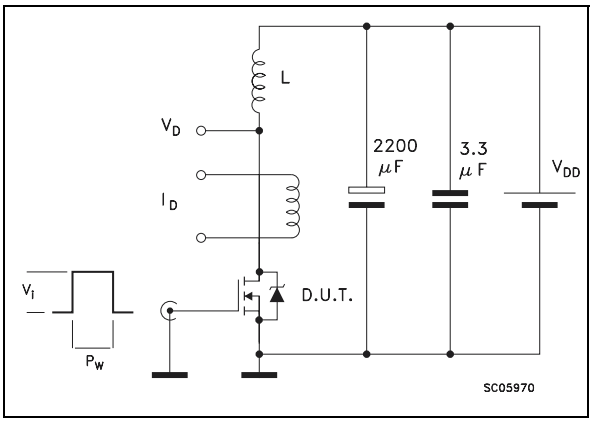


Figure 15. Unclamped Inductive Waveforms

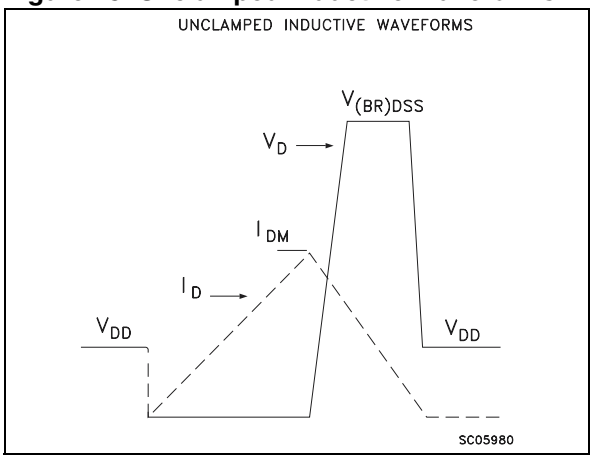


Figure 16. Switching Times Test Circuits For Resistive Load

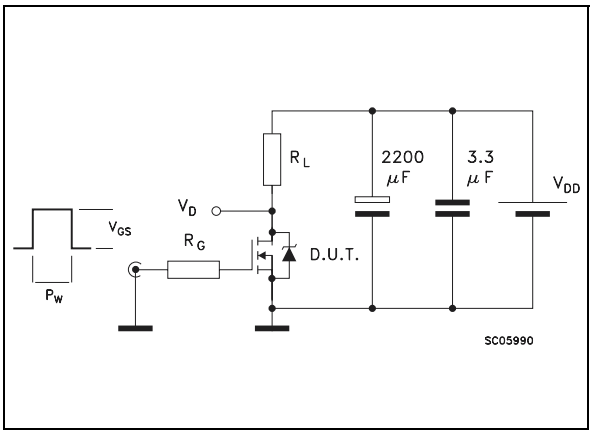


Figure 17. Gate Charge Test Circuit

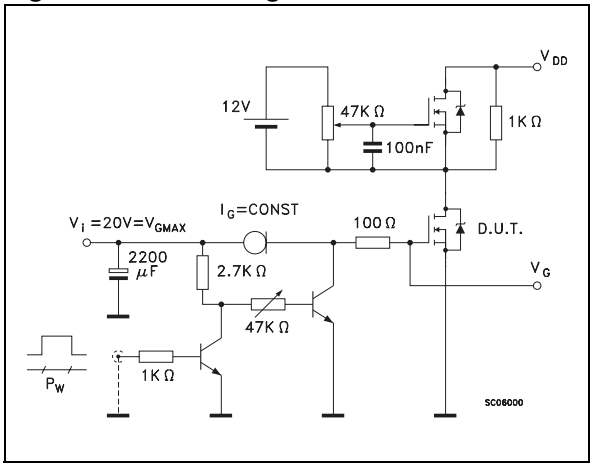
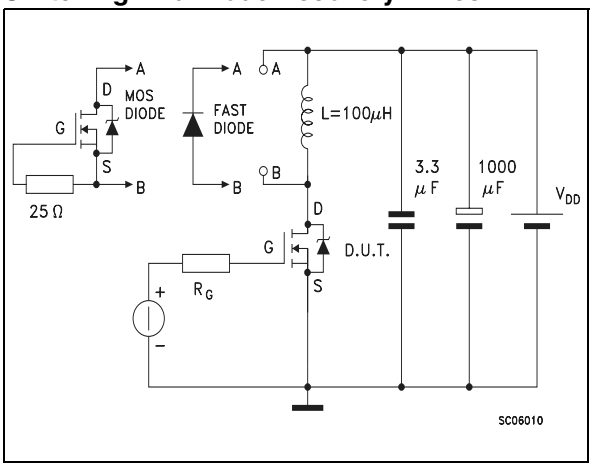


Figure 18. Test Circuit For Inductive Load Switching And Diode Recovery Times

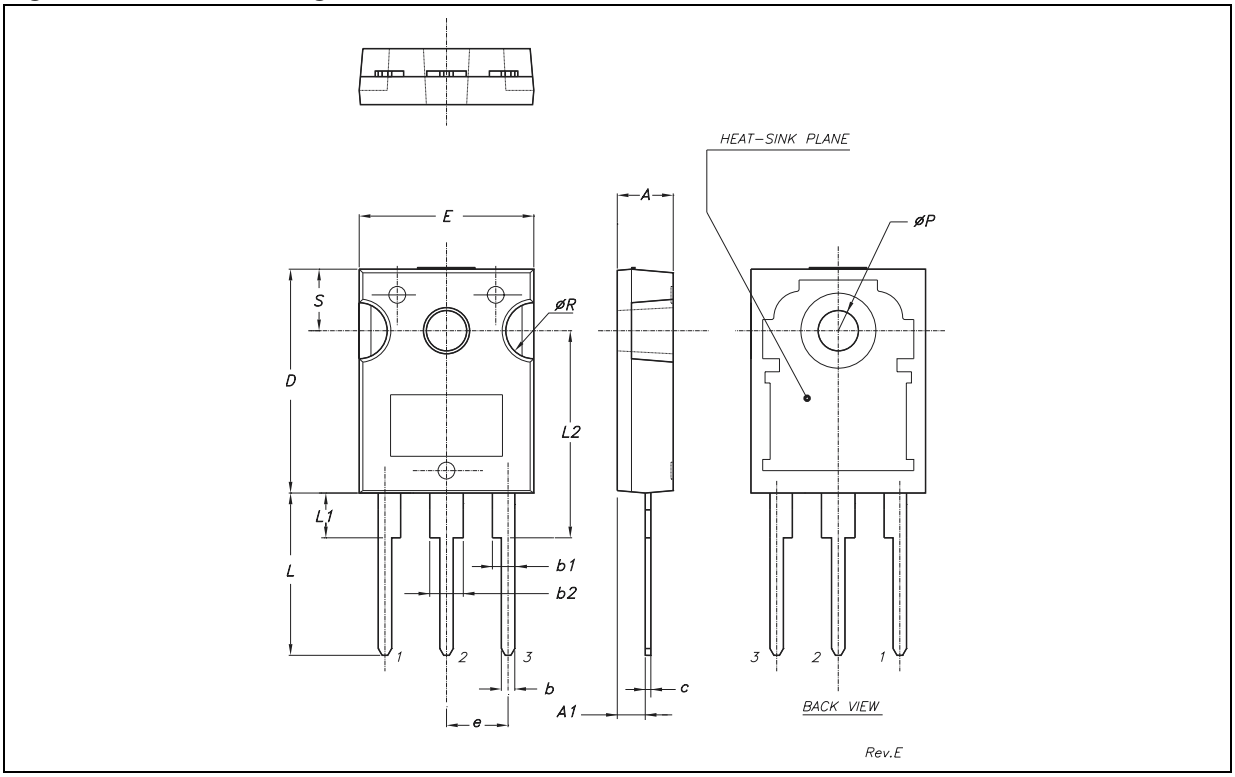


PACKAGE MECHANICAL

Table 12. TO-247 Mechanical Data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
ØP	3.55		3.65	0.140		0.143
ØR	4.50		5.50	0.177		0.216
S		5.50			0.216	

Figure 19. TO-247 Package Dimensions



Note: Drawing is not to scale.

REVISION HISTORY

Table 13. Revision History

Date	Revision	Description of Changes
January-1998	1	First Issue
14-Apr-2004	2	Stylesheet update. No content change.

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