RTD2270L/ RTD2280L

Flat Panel Display Controller
Brief Specification

Ordering Information

Part	VGA	Max. Resolution	Output	PKG
RTD2270L-CG	Yes (210MHz)	1680x1050@75Hz	LVDS (170Mhz)	LQFP64 7x7 (Green package)
RTD2280L-CG	Yes (210MHz)	1920x1080@75Hz	LVDS (186Mhz)	LQFP64 7x7 (Green package)

Preliminary
Version 1.01
Last updated: 2010/11/4

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Features

General
- Embedded DDC with DDC1/2B/CI
- Embedded one MCU with SPI flash controller.
- Require only one crystal to generate all timing.
- Programmable internal low-voltage-reset (LVR)
- High resolution 6 channels PWM output, and wide range selectable PWM frequency.
- Support input format up to FHD
- Embedded BJT control circuit for 1.2V regulator replacement

Analog RGB Input Interface
- One Analog input supported
- Integrated 8-bit triple-channel 210MHz ADC/PLL(option)
- Embedded programmable Schmitt trigger of HSYNC
- Support Sync-On-Green (SOG) and various kinds of composite sync modes
- On-chip high-performance hybrid PLLs
- High resolution true 64 phase ADC PLL

Embedded MCU
- Industrial standard 8051 core with external serial flash
- Low speed ADC for various application
- I2C Master or Slave hardware supported

Auto Detection /Auto Calibration
- Input format detection
- Compatibility with standard VESA mode and support user-defined mode
- Smart engine for Phase/Image position/Color calibration

Scaling
- Fully programmable zoom ratios
- Independent horizontal/vertical scaling
- Advanced zoom algorithm provides high image quality
- Sharpness/Smooth filter enhancement
- Support non-linear scaling from 4:3 to 16:9 or 16:9 to 4:3

Color Processor
- True 10 bits color processing engine
- sRGB compliance
- Advanced dithering logic for 18-bit panel color depth enhancement
- Brightness and contrast control
- Programmable 10-bit gamma support
- Peaking/Coring function for video sharpness

VividColor™
- Independent color management (ICM)
- Dynamic contrast control (DCC)

Output Interface
- Fully programmable display timing generator
- Flexible data pair swapping for easier system design.
- Single or Dual display interface supported up to 186MHz, FHD resolution
- LVDS output interface
- Support 8 bits LVDS output
- Spread-Spectrum DPLL to reduce EMI
- Fixed Last Line output for perfect panel capability

Embedded OSD
- Embedded 16.5K SRAM dynamically stores OSD command and fonts
- Support multi-color RAM font, 1, 2 and 4-bit per pixel
- 64 color palette
- Maximum 10 window with alpha-blending/ gradient / gradient target color / gradient reversed color/ dynamic fade-in/fade-out, bordering/ shadow/3D window type
- Rotary 90,180,270 degree
- Independent row shadowing/bordering
- Programmable blinking effects for each character
- OSD-made internal pattern generator for factory mode
- Support 12x18~4x18 proportional font
- Hardware decompression for OSD font
- Special function for closed-caption
- Support 2 independent font base

Power & Package
- 3.3V / 1.2V power supply
- 64 pin LQFP 7x7 package

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Pin Diagram

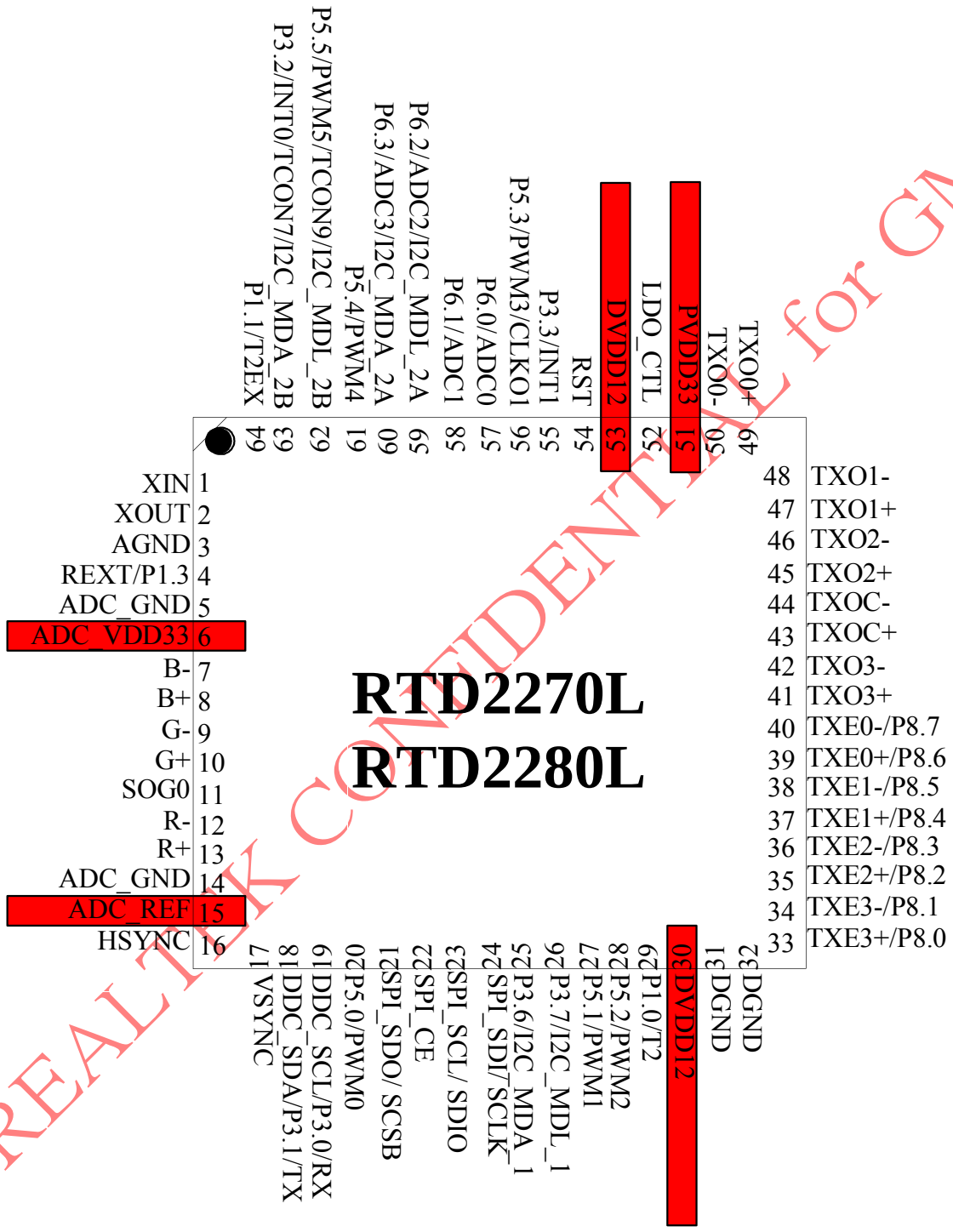

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Table of LQFP-64 pin assignment

I:input, O:output, P:power, G:gnd

PIN NO.	Name	I/O/P/G	Description	PWR OFF 5V tolerance	PWR ON 5V tolerance	PWR ON 3.3v tolerance	NOTE
1	XIN	I	Crystal input			Y	
2	XOUT	O	Crystal output			Y	
3	AGND	G		-	-	-	
4	REXT/GPIO	I/O		Y	Y		
5	ADC_GND	G	ADC Power	-	-	-	
6	ADC_VDD33	P		-	-	-	3.3V
7	BIN1-	I	VGA INPUT signal			Y	
8	BIN1+	I				Y	
9	GIN1-	I				Y	
10	GIN1+	I				Y	
11	SOG0	I				Y	
12	RIN1-	I				Y	
13	RIN1+	I				Y	
14	ADC_GND	G		-	-	-	
15	ADC_REF	P	ADC_Reference Power	-	-	-	1.2V
16	HSYNC	I		Y	Y		Adjustable Schmitt Trigger
17	VSYNC	I		Y	Y		General Schmitt Trigger
18	DDC_SDA/GPIO/TX	I/O	DDC SDA/MCU GPIO/TX	Y	Y		
19	DDC_SCL/GPIO/RX	I/O	DDC SCL/MCU GPIO/ RX	Y	Y		
20	GPIO/PWM0	I/O	MCU GPIO/ PWM output	Y	Y		
21	SPI_SDO/ SCSB	O	SPI flash serial data output/ Host Interface_SCSB		Y		
22	SPI_CE	O	SPI flash chip enable Note: POL pin, 1:internal MCU, 0:ext. MCU		Y		
23	SPI_SCL/ SDIO	O	SPI flash clk/ Host Interface_SDIO		Y		

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24	SPI_SDI/ SCLK	I	SPI flash serial data input/ Host Interface_SCLK		Y		
25	GPIO/I2C_MDA_1	I/O	MCU GPIO/ I2C master	Y	Y		
26	GPIO/I2C_MDL_1	I/O	MCU GPIO/ I2C master	Y	Y		
27	GPIO/PWM1	I/O	MCU GPIO/PWM output	Y	Y		
28	GPIO/PWM2	I/O	MCU GPIO/PWM output	Y	Y		
29	GPIO/T2	I/O	MCU GPIO/ T2	Y	Y	-	
30	DVDD12	P	Digital Power	-	-	-	1.2V
31	DGND	G	DGND	-	-	-	
32	DGND	G	DGND	-	-	-	
33	TXE3+/GPIO	O	LVDS Output/ MCU GPIO	N	N	Y	
34	TXE3-/GPIO	O		N	N	Y	
35	TXE2+/GPIO	O		N	N	Y	
36	TXE2-/GPIO	O		N	N	Y	
37	TXE1+/GPIO	O		N	N	Y	
38	TXE1-/GPIO	O		N	N	Y	
39	TXE0+/GPIO	O		N	N	Y	
40	TXE0-/GPIO	O		N	N	Y	
41	TXO3+	O	LVDS Output			Y	
42	TXO3-	O				Y	
43	TXOC+	O				Y	
44	TXOC-	O				Y	
45	TXO2+	O				Y	
46	TXO2-	O				Y	
47	TXO1+	O				Y	
48	TXO1-	O				Y	
49	TXO0+	O				Y	
50	TXO0-	O				Y	
51	PVDD33	P	Analog Power (for LVDS & I/O)	-	-	-	3.3V
52	LDO_CTL	O	Regular control (3.3->1.2)		Y		
53	DVDD12	P	Digital power	-	-	-	1.2V
54	RST	I	Chip Reset		Y		HIGH ACTIVE
55	GPIO/INT1	I/O	MCU GPIO/INT1	Y	Y		

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56	GPIO/PWM3/CLKO1	I/O	MCU GPIO/PWM output/ clk output	Y	Y		
57	GPIO/ADC0	I/O	MCU GPIO/ ADC input	Y	Y		
58	GPIO/ADC1	I/O	MCU GPIO/ ADC input	Y	Y		
59	GPIO/ADC2/ I2C_MDL_2A	I/O	MCU GPIO/ ADC input/I2C	Y	Y		
60	GPIO/ADC3/ I2C_MDA_2A	I/O	MCU GPIO/ ADC input/I2C	Y	Y		
61	GPIO/PWM4	I/O	MCU GPIO/ PWM output	Y	Y		
62	GPIO/PWM5/TCON9/ I2C_MDL_2B	I/O	MCU GPIO/ PWM output/ TCON/ I2C	Y	Y		
63	GPIO/INT0/TCON7/ I2C_MDA_2B	I/O	MCU GPIO/INT0/TCON/ I2C	Y	Y		
64	GPIO/T2EX	I/O	MCU GPIO	Y	Y		

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● Electric Specification

DC Characteristics

Table 1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Voltage on Input (5V tolerant)	V_{IN}	-1		5	V
Supply Voltage	PVCC	3.0	3.3	3.6	V
Supply Voltage	VCCK	1.08	1.2	1.32	V
Electrostatic Discharge	V_{ESD}		±2.5		kV
Latch-Up	I_{LA}			±100	mA
Ambient Operating Temperature	T_A	0		70	ºC
Storage temperature (plastic)	T_{STG}	-55		125	ºC
Thermal Resistance (Junction to Air)	θ_{JA}			TBD	ºC/W
Junction Acceptable Temperature	T_j			125	ºC

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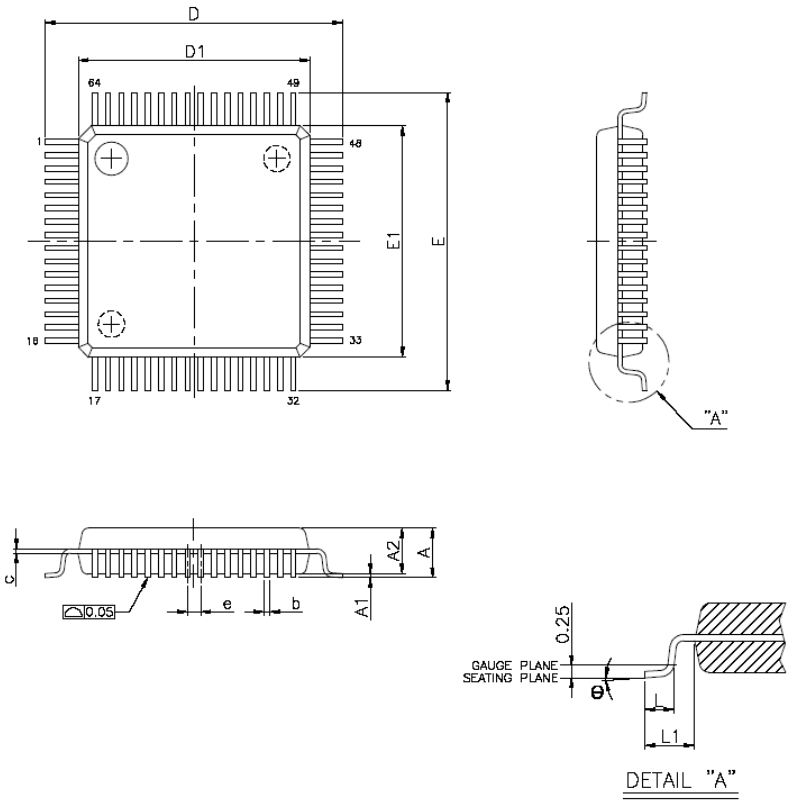
• Mechanical Specification

64 Pin Package

Low Profile Plastic Quad Flat Package 64 Leads 7x7mm^2 Outline



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.40 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

NOTES:
1. JEDEC OUTLINE : MS-026 BBD
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

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