# Low Droop Rate/Accurate Sample-and-Hold Amplifiers

# SMP-10/SMP-11

## FEATURES

**SMP-10**

- **Low Droop Rate ..... 5.0μV/ms**
- **Linearity Error ..... 0.005%**
- **High Sample/Hold Current Ratio ..... $2 \times 10^9$**

**SMP-11**

- **Low Droop Rate Over Temperature ..... 2400μV/ms**
- **High Sample/Hold Current Ratio ..... $1.7 \times 10^8$**

**BOTH SMP-10 AND SMP-11**

- **Fast Acquisition Time, 10V Step to 0.1% ..... 3.5μs**
- **High Slew Rate ..... 10V/μs**
- **Low Aperture Time ..... 50ns**
- **Trimmed for Minimum Zero-Scale Error ..... 0.45mV**
- **Feedthrough Attenuation Ratio ..... 96dB**
- **Low Power Dissipation ..... 160mW**
- **DTL, TTL & CMOS Compatible Logic Input**
- **HA-2420, HA-2425, SHM-IC-1, and AD583 Socket Compatible**
- **Available in Die Form**

## ORDERING INFORMATION †

| $T_A = +25°C$ | | | | |
|---|---|---|---|---|
| | | PACKAGE | | |
| $V_{ZS}$ (mV) | DROOP RATE IN μV/ms | 14-PIN DIP HERMETIC | LCC | OPERATING TEMPERATURE RANGE |
| 1.5 | 20 | SMP10AY* | – | MIL |
| 1.5 | 20 | SMP10EY | – | COM |
| 3.0 | 50 | SMP10FY | – | COM |
| 1.5 | 200 | SMP11AY* | – | MIL |
| 3.0 | 500 | SMP11BY* | SMP11BRC/883 | MIL |
| 1.5 | 200 | SMP11EY | – | COM |
| 3.0 | 500 | SMP11FY | – | COM |
| 7.0 | 900 | SMP11GY | – | COM |
| 7.0 | 900 | SMP11GS | – | XIND |
| 7.0 | 900 | SMP11GP | – | XIND |

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

## GENERAL DESCRIPTION

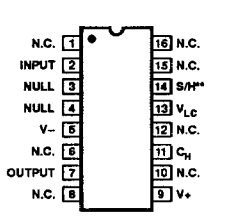
The SMP-10/11 are precision sample-and-hold amplifiers that provide the high accuracy, the low droop rate and the fast acquisition time required in data acquisition and signal processing systems. Both devices are essentially noninverting unity gain circuits consisting of two very high input impedance buffer amplifiers connected together by a diode bridge switch.

### HIGH ACCURACY AND LOW DROOP RATE

The high input impedance and the low droop rates of the SMP-10 and the SMP-11 are achieved by using bipolar Darlington circuits and an ion implant process that creates "super beta" transistors.

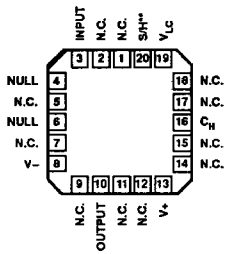
The output buffer's input stage converts to a super beta Darlington configuration during the hold mode, which results in a very low droop rate with no penalty in acquisition time. The use of bipolar transistors achieves a low change in droop rate over the operating temperature range. *Continued*

## PIN CONNECTIONS

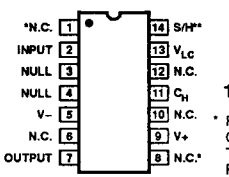



**16-PIN SOL**
**(S-Suffix)**

** SAMPLE/HOLD CONTROL



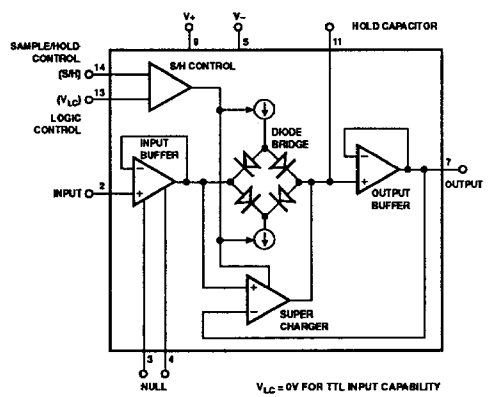

**SMP-11BRC/883**
**LCC PACKAGE**
**(RC-Suffix)**




**14-PIN DIP (Y-Suffix)**
**14-PIN EPOXY DIP (P-Suffix)**

* PINS 1 AND 8 ARE NOT INTERNALLY CONNECTED, IN UNITY GAIN APPLICATIONS, SMP-10 AND SMP-11 CAN REPLACE HA-2425, HA-2420, SHM-IC-1 AND AD-583 DIRECTLY.

## FUNCTIONAL DIAGRAM




| S/H | MODE |
|---|---|
| 0 | Sample |
| 1 | Hold |

Manufactured under the following patents: 4,109,215 and 4,142,117.

## GENERAL DESCRIPTION *Continued*

### FAST ACQUISITION

A unique super charger provides up to 50mA of charging current to the hold capacitor, which results in smooth, fast charging with minimum noise. As the hold capacitor voltage nears its final value, the low current diode bridge controls the final settling time. This unique combination of linear functions in a monolithic circuit enables the system designer to achieve superior performance.

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V+ minus V–) ..... 36V
Derate Above 100°C ..... 10mW/°C
Input Voltage ..... Equal to Supply Voltage
Logic and Logic Reference
Voltage ..... Equal to Supply Voltage
Output Short-Circuit Duration ..... Indefinite
Hold Capacitor Short-Circuit Duration ..... 60 sec
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Operating Temperature Range
SMP-10AY ..... –55°C to +125°C
SMP-10EY, FY ..... 0°C to +70°C
SMP-11AY, BY, BRC ..... –55°C to +125°C
SMP-11EY, FY, GY ..... 0°C to +70°C
SMP11GS, GP ..... –40°C to +85°C
Junction Temperature ($T_j$) ..... –65°C to +150°C

| PACKAGE TYPE | $\theta_{JA}$ (Note 2) | $\theta_{JC}$ | UNITS |
|---|---|---|---|
| 14-Pin Hermetic DIP (Y) | 108 | 16 | °C/W |
| 14-Pin Epoxy DIP (P) | 83 | 39 | °C/W |
| 16-Pin SOL (S) | 98 | 30 | °C/W |
| 20-Contact LCC (RC) | 98 | 38 | °C/W |

**NOTES:**
1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.
2. $\theta_{JA}$ is specified for worst case mounting conditions, i.e., $\theta_{JA}$ is specified for device in socket for CerDIP and LCC packages.

## ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $C_H = 0.005\mu F$, $V_{LC}$ connected to ground, $T_A = +25°C$, unless otherwise noted.

| | | | SMP-10A/E SMP-11A/E | | | SMP-10F SMP-11B/F | | | SMP-11G | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | UNITS |
| Zero-Scale Error (Hold Mode) | $V_{ZS}$ | $V_{IN} = 0$<br>$V_{S/H} = 3.5V$, (Note 2) | – | 0.45 | 1.5 | – | 0.60 | 3.0 | – | 1.5 | 7.0 | mV |
| Input Bias Current | $I_B$ | $V_{IN} = 0$ | – | 35 | 65 | – | 55 | 90 | – | 90 | 160 | nA |
| Leakage (Droop) Current | $I_{DR}$ | SMP-10<br>SMP-11 | –<br>– | –<br>– | 0.10<br>1.00 | –<br>– | –<br>– | 0.25<br>2.50 | –<br>– | –<br>– | –<br>4.5 | nA |
| Droop Rate | $dV_{CH}/dt$ | SMP-10<br>SMP-11 | –<br>– | 5<br>60 | 20<br>200 | –<br>– | 5<br>70 | 50<br>500 | –<br>– | –<br>80 | –<br>900 | µV/ms |
| Input Resistance | $R_{IN}$ | (Note 1) | 2.0 | 3.0 | – | 1.4 | 2.5 | – | – | 2.0 | – | GΩ |
| Voltage Gain | $A_V$ | Sample Mode<br>$V_{IN} = \pm10V$, $R_L = 5k\Omega$<br>or $V_{IN} = \pm5V$, $R_L = 2.5k\Omega$ | 0.99963 | 0.99983 | – | 0.99953 | 0.99978 | – | 0.99940 | 0.99975 | – | V/V |
| Acquisition Time | $t_{aq}$ | 10V Step to Within 10mV of Final Value (0.1%)<br>10V Step to Within 1.0mV of Final Value (0.01%) | –<br>– | 3.5<br>5.0 | –<br>– | –<br>– | 3.5<br>5.0 | –<br>– | –<br>– | 3.5<br>5.0 | –<br>– | µs<br>µs |
| Aperture Time | $t_{ap}$ | | – | 50 | – | – | 50 | – | – | 50 | – | ns |
| Hold Mode Settling Time | $t_{Hm}$ | Settling to 1mV of Final Value. SMP-10<br>SMP-11 | –<br>– | 7<br>1.5 | –<br>– | –<br>– | 7<br>1.5 | –<br>– | –<br>– | 7<br>1.5 | –<br>– | µs |
| Charge Transfer | Qt | $V_{IN} = 0$<br>$V_{S/H} = 3.5V$ | – | 5 | – | – | 5 | – | – | 5 | – | pC |
| Slew Rate | SR | $V_{IN} = \pm10V$<br>$R_L = 2.5k\Omega$ | – | 10 | – | – | 10 | – | – | 10 | – | V/µs |
| Hold Capacitor Charging Current | $I_{CH}$ | $V_{IN} - V_{OUT} \geq \pm3V$ | 30 | 50 | – | 20 | 50 | – | – | 50 | – | mA |
| Sample/Hold Current Ratio | $I_{CH}/I_{DR}$ | SMP-10<br>SMP-11 | $3x10^8$<br>– | $2x10^9$<br>$1.7x10^8$ | –<br>– | $8x10^7$<br>– | $8x10^8$<br>$1.5x10^8$ | –<br>– | –<br>– | –<br>$1.5x10^8$ | –<br>– | mA/mA |
| Feedthrough Attenuation Ratio | $F_A$ | Input = $20V_{p-p}$ 1kHz<br>$R_L = 5k\Omega$, (Note 1) | 86 | 98 | – | 80 | 90 | – | – | 90 | – | dB |
| Full Power Bandwidth | $F_p$ | $\pm10V_{p-p}$<br>(Dissipation Limited) | – | 100 | – | – | 100 | – | – | 100 | – | kHz |

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm15V$, $C_H = 0.005\mu F$, $V_{LC}$ connected to ground, $T_A = +25°C$, unless otherwise noted. *Continued*

| PARAMETER | SYMBOL | CONDITIONS | SMP-10A/E SMP-11A/E MIN | SMP-10A/E SMP-11A/E TYP | SMP-10A/E SMP-11A/E MAX | SMP-10F SMP-11B/F MIN | SMP-10F SMP-11B/F TYP | SMP-10F SMP-11B/F MAX | SMP-11G MIN | SMP-11G TYP | SMP-11G MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Input Voltage Range and/or Output Voltage Swing | | $R_L = 2.5k\Omega$ | ±11 | ±11.5 | – | ±10.5 | ±11.5 | – | ±10.5 | ±11.5 | – | V |
| Output Resistance | $R_O$ | | – | 0.15 | – | – | 0.15 | – | – | 0.15 | – | Ω |
| Power Supply Rejection Ratio | PSRR | Sample Mode $V_S = \pm9V$ to $\pm18V$ | 82 | 92 | – | 77 | 92 | – | 72 | 92 | – | dB |
| Power Consumption (DC) | $P_D$ | Sample Mode $V_{IN} = 0$ | – | 160 | 180 | – | 170 | 210 | – | 180 | 240 | mW |

**NOTES:**
1. Guaranteed by design.
2. Measured 500µs after hold command.

**ELECTRICAL CHARACTERISTICS – SMP-10 ONLY** at $V_S = \pm15V$, $C_H = 0.005\mu F$, $V_{LC} = 0V$, $T_A = +25°C$, device fully warmed up, unless otherwise noted.

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| PARAMETER | SYMBOL | CONDITIONS | SMP-10A/E MIN | SMP-10A/E TYP | SMP-10A/E MAX | SMP-10F MIN | SMP-10F TYP | SMP-10F MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Hold Step | $V_{HS}$ | $V_{IN} = 0$ | –1.0 | +1.5 | +4.0 | –3.0 | +1.5 | +6.0 | mV |
| Linearity Error | NL | $V_{IN} = \pm10V$, $R_L = 5k\Omega$ | – | 0.005 | – | – | 0.007 | – | % of 10V |
| Output Noise | $E_{N\,(RMS)}$ | Wideband Noise 100Hz to 100kHz Sample Mode | – | 40 | – | – | 50 | – | $\mu V_{RMS}$ |

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm15V$, $C_H = 0.005\mu F$, $V_{LC}$ connected to ground, $0°C \le T_A \le +70°C$, unless otherwise noted.

| PARAMETER | SYMBOL | CONDITIONS | SMP-10E SMP-11E MIN | SMP-10E SMP-11E TYP | SMP-10E SMP-11E MAX | SMP-10F SMP-11F MIN | SMP-10F SMP-11F TYP | SMP-10F SMP-11F MAX | SMP-11G MIN | SMP-11G TYP | SMP-11G MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Zero-Scale Error | $V_{ZS}$ | $V_{IN} = 0$, $V_{S/H} = 3.5V$, (Note 1) | – | 0.75 | 2.0 | – | 1.0 | 4.0 | – | 2.7 | 10 | mV |
| Input Bias Current | $I_B$ | $V_{IN} = 0V$ | – | 50 | 90 | – | 80 | 140 | – | 120 | 250 | nA |
| Leakage (Droop) Current | $I_{DR}$ | SMP-10 | – | 0.05 | 0.25 | – | 0.080 | 0.65 | – | – | – | nA |
| | | SMP-11 | – | 0.5 | 1.8 | – | 0.6 | 2.8 | – | 0.7 | 5 | |
| Droop Rate | $dV_{CH}/dt$ | SMP-10 | – | 10 | 50 | – | 16 | 130 | – | – | – | µV/ms |
| | | SMP11 | – | 100 | 360 | – | 120 | 560 | – | 140 | 1000 | |
| Voltage Gain | $A_V$ | Sample Mode $V_{IN} = \pm10V$, $R_L = 5k\Omega$ or $V_{IN} = \pm5V$, $R_L = 2.5k\Omega$ | 0.99955 | 0.99976 | – | 0.99950 | 0.99972 | – | 0.99930 | 0.99970 | – | V/V |
| Power Supply Rejection Ratio | PSRR | Sample Mode $V_S = \pm9V$ to $\pm18V$ | 80 | 90 | – | 75 | 80 | – | 70 | 90 | – | dB |
| Logic Control Input Current | $I_{LC}$ | $V_{LC} = 0V$ | – | –1 | –2 | – | –1 | –3 | – | –1 | –4 | µA |
| Logic Input | $I_{S/H}$ | Sample Mode $V_{S/H} = 0.6V$ | – | –5 | –15 | – | –5 | –15 | – | –5 | –15 | µA |
| | | Hold Mode $V_{S/H} = 5.0V$ | – | 0.2 | – | – | 0.2 | – | – | 0.2 | – | nA |
| Differential Logic Threshold | $V_{TH}$ | | 0.8 | 1.3 | 2.0 | 0.8 | 1.3 | 2.0 | 0.8 | 1.3 | 2.0 | V |

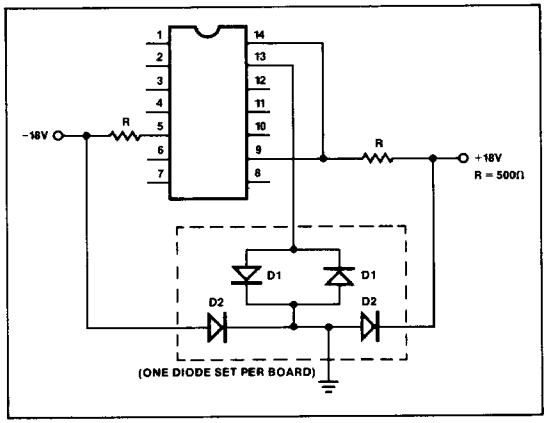
**NOTE:**
1. Measured 500µs after hold command.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $C_H = 0.005\mu F$, $V_{LC}$ connected to ground, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

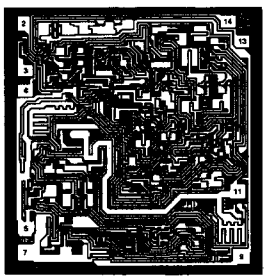
| PARAMETER | SYMBOL | CONDITIONS | | SMP-10A SMP-11A MIN | SMP-10A SMP-11A TYP | SMP-10A SMP-11A MAX | SMP-10 SMP-11B MIN | SMP-10 SMP-11B TYP | SMP-10 SMP-11B MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| Zero-Scale Error | $V_{ZS}$ | $V_{IN} = 0$, $V_{S/H} = 3.5V$, (Note 1) | | — | 1.25 | 3.0 | — | 1.60 | 5.5 | mV |
| Input Bias Current | $I_B$ | $V_{IN} = 0V$ | | — | 90 | 180 | — | 160 | 280 | nA |
| Leakage (Droop) Current | $I_{DR}$ | $T_A = -55°C$ | SMP-10 | — | 0.050 | 0.50 | — | 0.080 | 1.22 | nA |
| | | $T_A = +125°C$ | SMP-10 | — | 12 | 20 | — | 16 | 25 | |
| | | $T_A$ = Full Range | SMP-11 | — | 12 | 20 | — | 16 | 25 | |
| Droop Rate | $dV_{CH}/dt$ | $T_A = -55°C$ | SMP-10 | — | 10 | 100 | — | 16 | 250 | μV/ms |
| | | $T_A = +125°C$ | SMP-10 | — | 2400 | 4000 | — | 3200 | 5000 | |
| | | $T_A$ = Full Range | SMP-11 | — | 2400 | 4000 | — | 3200 | 5000 | |
| Voltage Gain | $A_V$ | Sample Mode<br>$V_{IN} = \pm 10V$, $R_L = 5k\Omega$<br>or $V_{IN} = \pm 5V$, $R_L = 2.5k\Omega$ | | 0.99950 | 0.99972 | — | 0.99940 | 0.99968 | — | V/V |
| Power Supply Rejection Ratio | PSRR | Sample Mode<br>$V_S = \pm 9V$ to $\pm 18V$ | | 78 | 88 | — | 72 | 90 | — | dB |
| Logic Control Input Current | $I_{LC}$ | $V_{LC} = 0V$ | | — | −1 | −3 | — | −1 | −5 | μA |
| Logic Input | $I_{S/H}$ | Sample Mode<br>$V_{S/H} = 0.6V$ | | — | −5 | −15 | — | −5 | −15 | μA |
| | | Hold Mode<br>$V_{S/H} = 5.0V$ | | — | 0.2 | — | — | 0.2 | — | nA |
| Differential Logic Threshold | $V_{TH}$ | | | 0.6 | 1.3 | 2.0 | 0.6 | 1.3 | 2.0 | V |

**NOTES:**
1. Measured 500μs after hold command.

## BURN-IN CIRCUIT



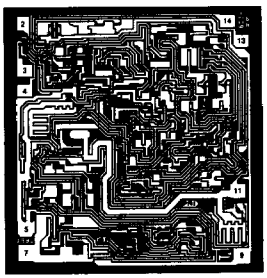
## DICE CHARACTERISTICS



SMP-10

2. INPUT
3. NULL
4. NULL
5. NEGATIVE SUPPLY (SUBSTRATE)
7. OUTPUT
9. POSITIVE SUPPLY
11. HOLD CAPACITOR ($C_H$)
13. LOGIC THRESHOLD CONTROL ($V_{LC}$)
14. SAMPLE/HOLD COMMAND

DIE SIZE 0.088 × 0.083 inch, 7304 sq. mils (2.235 × 2.108 mm, 4.711 sq. mm)



SMP-11

2. INPUT
3. NULL
4. NULL
5. NEGATIVE SUPPLY (SUBSTRATE)
7. OUTPUT
9. POSITIVE SUPPLY
11. HOLD CAPACITOR ($C_H$)
13. LOGIC THRESHOLD CONTROL ($V_{LC}$)
14. SAMPLE/HOLD COMMAND

**WAFER TEST LIMITS** at $V_S = \pm 15V$, $C_H = 0.005\mu F$, $V_{LC}$ connected to ground, $T_A = 25°C$, unless otherwise noted.

| PARAMETER | SYMBOL | CONDITIONS | SMP-10N SMP-11N LIMIT | SMP-10G SMP-11G LIMIT | UNITS |
|---|---|---|---|---|---|
| Zero-Scale Error | $V_{ZS}$ | $V_{IN} = 0$, $V_{S/H} = 3.5V$ Hold Mode, (Note 2) | 1.5 | 3.0 | mV MAX |
| Input Bias Current | $I_B$ | $V_{IN} = 0V$ | 60 | 90 | nA MAX |
| Leakage (Droop) Current | $I_{DR}$ | SMP-10<br>SMP-11 | 0.10<br>1 | 0.25<br>2.5 | nA MAX |
| Droop Rate | $dV_{CH}/dt$ | SMP-10<br>SMP-11 | 20<br>200 | 50<br>500 | μV/ms MAX |
| Voltage Gain | $A_V$ | Sample Mode $V_{IN} = \pm 10V$ or $V_{IN} = \pm 5V$ | 0.99963 | 0.99953 | V/V MIN |
| Hold Capacitor Charging Current | $I_{CH}$ | $V_{IN} - V_{OUT} \geq \pm 3V$ | 30 | 20 | mA MIN |
| Input Voltage Range and/or Output Voltage Swing | | $R_L = 2.5k\Omega$ | ±11 | ±10.5 | V MIN |
| Power Supply Rejection Ratio | PSRR | Sample Mode $V_S = \pm 9V$ to $\pm 18V$ | 82 | 77 | dB MIN |
| Power Consumption | $P_D$ | Sample Mode $V_{IN} = 0$ | 180 | 210 | mW MAX |
| Logic Control Input Current | $I_{LC}$ | $V_{LC} = 0V$ | −2 | −3 | μA MAX |
| Logic Input | $I_{S/H}$ | Sample Mode $V_{S/H} = 0.6V$<br>Hold Mode $V_{S/H} = 5V$ | −15<br>0 | −15<br>0 | μA MAX<br>nA MAX |
| Differential Logic Threshold | $V_{TH}$ | $V_{LC} = 0$ | 2.0<br>0.8 | 2.0<br>0.8 | V MAX<br>V MIN |

**NOTES:**
1. Measured 500μs after hold command.

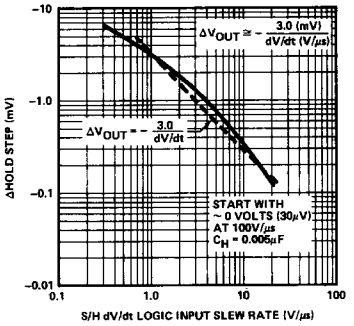
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

**TYPICAL ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $C_H = 0.005\mu F$, $V_{LC}$ connected to ground, $T_A = 25°C$, unless otherwise noted.

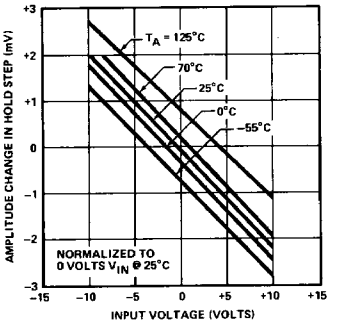
| PARAMETER | SYMBOL | CONDITIONS | SMP-10N SMP-11N TYPICAL | SMP-10G SMP-11G TYPICAL | UNITS |
|---|---|---|---|---|---|
| Acquisition Time | $t_{aq}$ | 10V step to 0.1% of final value | 3.5 | 3.5 | μs |
| Aperture Time | $t_{ap}$ | | 50 | 50 | ns |
| Charge Transfer | $Q_t$ | $V_{IN} = 0$, $V_{S/H} = 3.5V$ | 5 | 5 | pC |
| Slew Rate | SR | $V_{IN} = \pm 10V$, $R_L = 2.5k\Omega$ | 10 | 10 | V/μs |

## TYPICAL PERFORMANCE CHARACTERISTICS

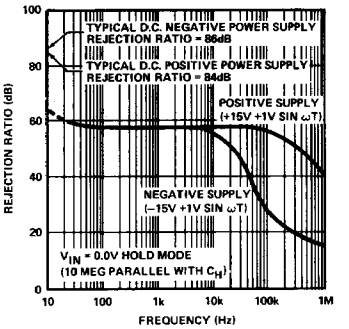
### CHANGE IN HOLD STEP vs S/H $\frac{dV}{dt}$



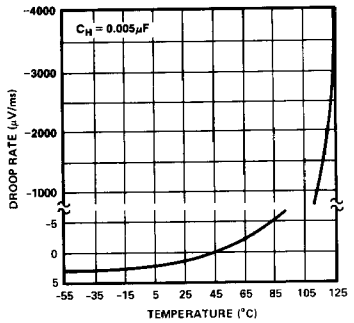

### AMPLITUDE CHANGE IN HOLD STEP vs INPUT VOLTAGE



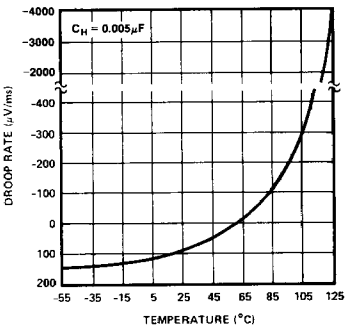

### HOLD MODE POWER SUPPLY REJECTION



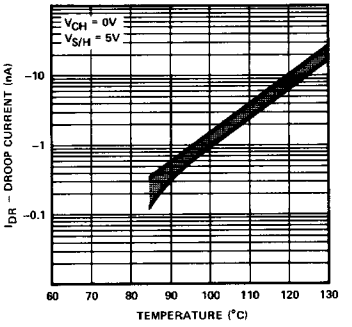

### SMP-10 DROOP RATE vs TEMPERATURE



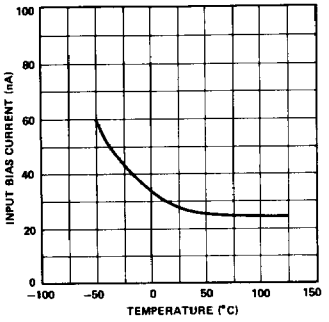

### SMP-11 DROOP RATE vs TEMPERATURE



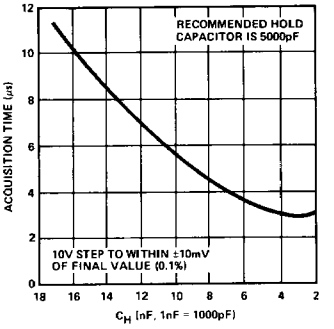

### DROOP CURRENT vs TEMPERATURE



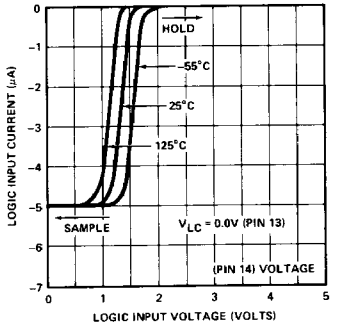

### INPUT BIAS CURRENT vs TEMPERATURE




### ACQUISITION TIME vs HOLD CAPACITOR

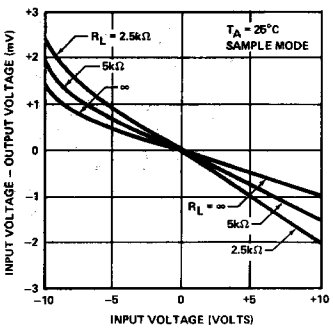



### LOGIC INPUT CURRENT

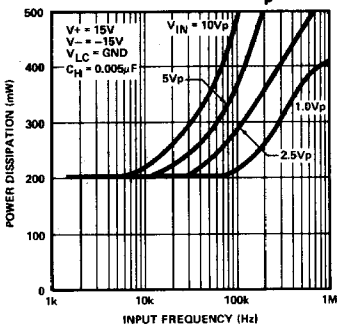


## TYPICAL PERFORMANCE CHARACTERISTICS

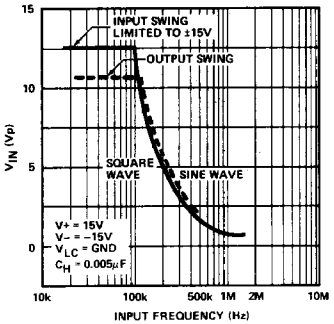
### GAIN ERROR



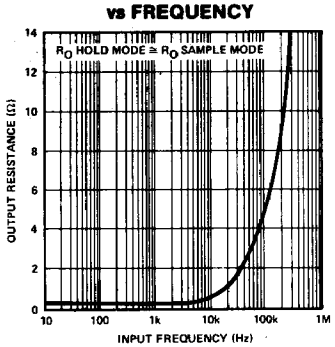

### POWER DISSIPATION vs INPUT FREQUENCY = $V_p$ SIN $\omega$T



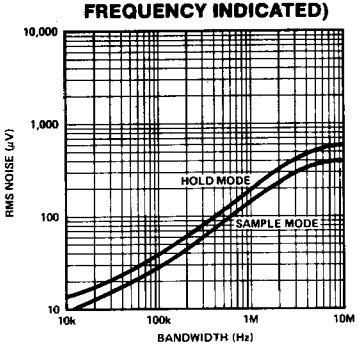

### MAXIMUM INPUT SIGNAL AMPLITUDE vs FREQUENCY



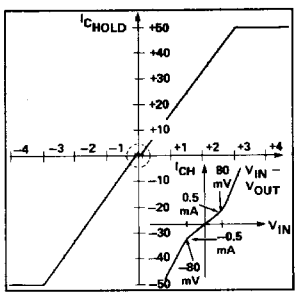

### OUTPUT RESISTANCE vs FREQUENCY



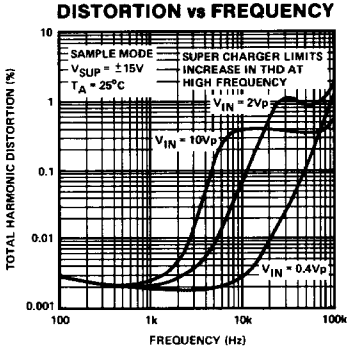

### OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



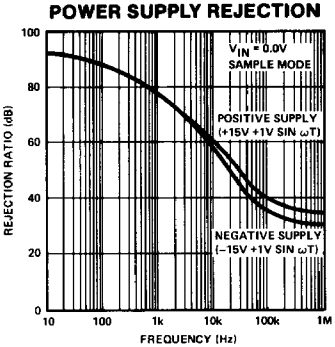

### HOLD CAPACITOR CHARGING CURRENT vs INPUT OUTPUT VOLTAGE



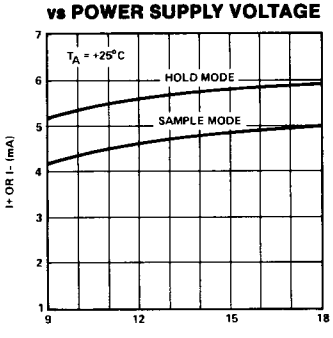

### TOTAL HARMONIC DISTORTION vs FREQUENCY




### SAMPLE MODE POWER SUPPLY REJECTION



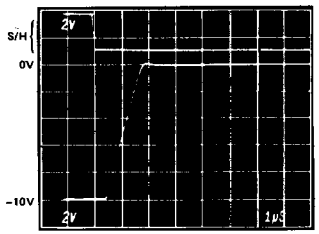

### POWER SUPPLY CURRENT vs POWER SUPPLY VOLTAGE



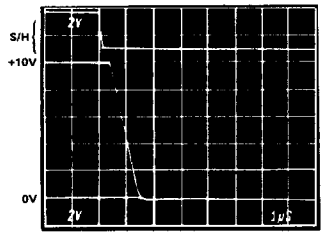

4

## SMP-10/SMP-11 ACQUISITION TIMES

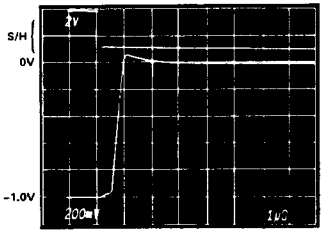
**ACQUISITION TIME −10V to 0V**



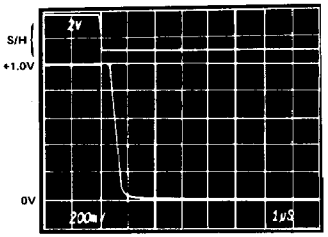

**ACQUISITION TIME +10V to 0V**



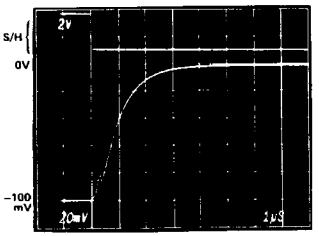

**ACQUISITION TIME −1.0V to 0V**



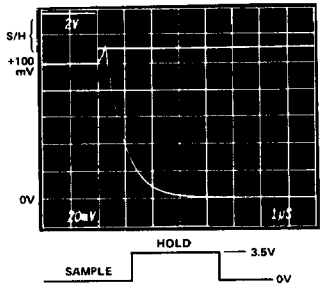

**ACQUISITION TIME +1.0V to 0V**




**ACQUISITION TIME −100mV to 0V**




**ACQUISITION TIME +100mV to 0V**

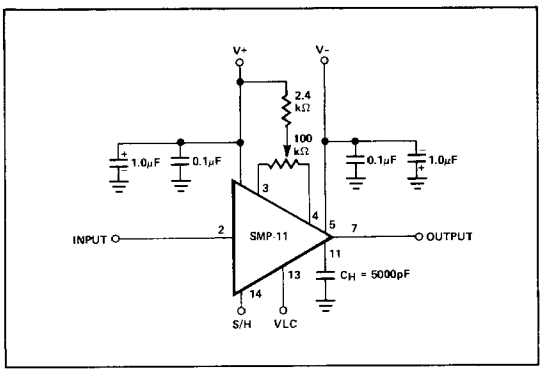



## APPLICATIONS INFORMATION

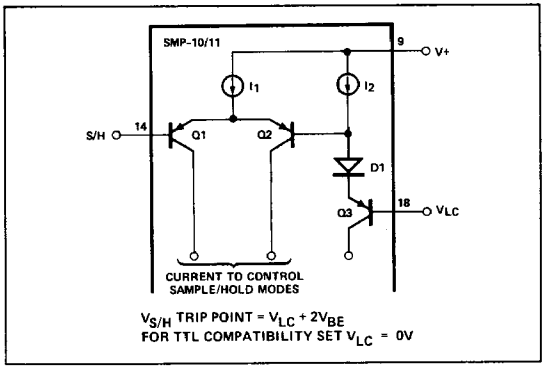
During the null adjustment, the amplifier should be switched continuously between the "sample" and "hold" mode. The error should be adjusted to read zero when the unit is in the "hold" mode. In this way, both offset voltage errors and charge transfer errors are adjusted to zero.

As shown in the Figure, the sample/hold mode control is accomplished by steering the current ($I_1$) through Q1 or Q2, thus providing high-speed switching and a predictable logic threshold. For TTL and DTL interface, simply ground $V_{LC}$ (Pin 13). For CMOS, HTL and HNIL interface, the appropriate

### ZERO-SCALE NULL ADJUSTMENT



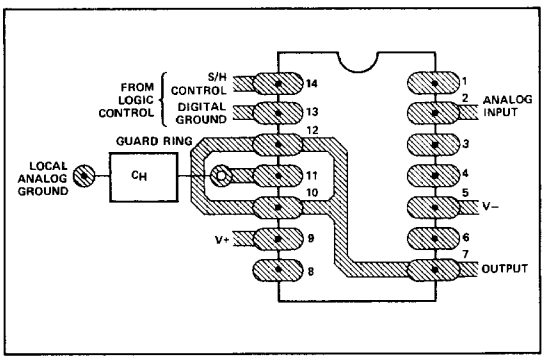

### LOGIC CONTROL



threshold voltage, allowing for 2 diode drops for D1 and $V_{BE}$ of Q3, should be applied to $V_{LC}$.

For proper operation, the $V_{LC}$ (logic control) must always be at least 3.5V below the positive supply and 2.0V above the negative supply.

Sample-and-hold control voltage (S/H) must always be at least 2.8V above the negative supply.




## GUARDING AND GROUNDING LAYOUT

The use of a ground plane is strongly recommended to minimize ground path resistances. Separate analog and digital grounds should be used, and it is advisable to keep these two ground systems isolated until they are tied back to the common system ground. Digital currents should not flow back to the system ground through the analog ground path.

## HOLD CAPACITOR RECOMMENDATIONS

The hold capacitor ($C_H$) acts as a memory element and also as a compensating capacitor for the sample-and-hold amplifier. For stable operation, a minimum value of 2000pF is recommended, with no limit set for the maximum value. The devices have been internally trimmed for $C_H$=5000pF. Other values of $C_H$ will cause a zero-scale shift, which can be calculated from the following equation:

$$\Delta V_{ZS}(mV) = \frac{5\,(pC) \times 10^3}{C_H\,(pF)} - 1$$

The hold capacitor should have very high insulation resistance and low dielectric absorption. For temperatures below 85°C, polystyrene capacitors are recommended, while teflon capacitors are recommended for higher temperature applications.

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