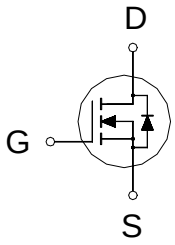
NIKO-SEM

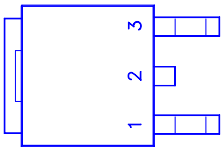
N-Channel Logic Level Enhancement Mode Field Effect Transistor

P75N02LDG
TO-252 (DPAK)
Lead-Free

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
25	5mΩ	75A





1. GATE
2. DRAIN
3. SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	75	A
	T_C = 100 °C		50	
Pulsed Drain Current[1]		I_{DM}	170	
Avalanche Current		I_{AR}	60	
Avalanche Energy	L = 0.1mH	E_{AS}	140	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	E_{AR}	5.6	
Power Dissipation	T_C = 25 °C	P_D	60	W
	T_C = 100 °C		32.75	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	275	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		2.3	°C / W
Junction-to-Ambient	$R_{\theta JA}$		62.5	
Case-to-Heatsink	$R_{\theta CS}$	0.6		

[1]Pulse width limited by maximum junction temperature.
[2]Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	25			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1	1.5	3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±250	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0V			25	μA
		V_{DS} = 20V, V_{GS} = 0V, T_J = 125 °C			250	

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On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	70			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 30A		5	7	mΩ
		V_{GS} = 7V, I_D = 24A		6	8	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15V, I_D = 30A		16		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz		5000		pF
Output Capacitance	C_{oss}			1800		
Reverse Transfer Capacitance	C_{rss}			800		
Total Gate Charge[2]	Q_g	V_{DS} = 0.5$V_{(BR)DSS}$, V_{GS} = 10V, I_D = 35A		140		nC
Gate-Source Charge[2]	Q_{gs}			40		
Gate-Drain Charge[2]	Q_{gd}			75		
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DS} = 15V, R_L = 1Ω, $I_D \cong$ 30A, V_{GS} = 10V, R_{GS} = 2.5Ω		7		nS
Rise Time[2]	t_r			7		
Turn-Off Delay Time[2]	$t_{d(off)}$			24		
Fall Time[2]	t_f			6		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				75	A
Pulsed Current[3]	I_{SM}				170	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.3	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100A / µS		37		nS
Peak Reverse Recovery Current	$I_{RM(REC)}$			200		A
Reverse Recovery Charge	Q_{rr}			0.043		µC

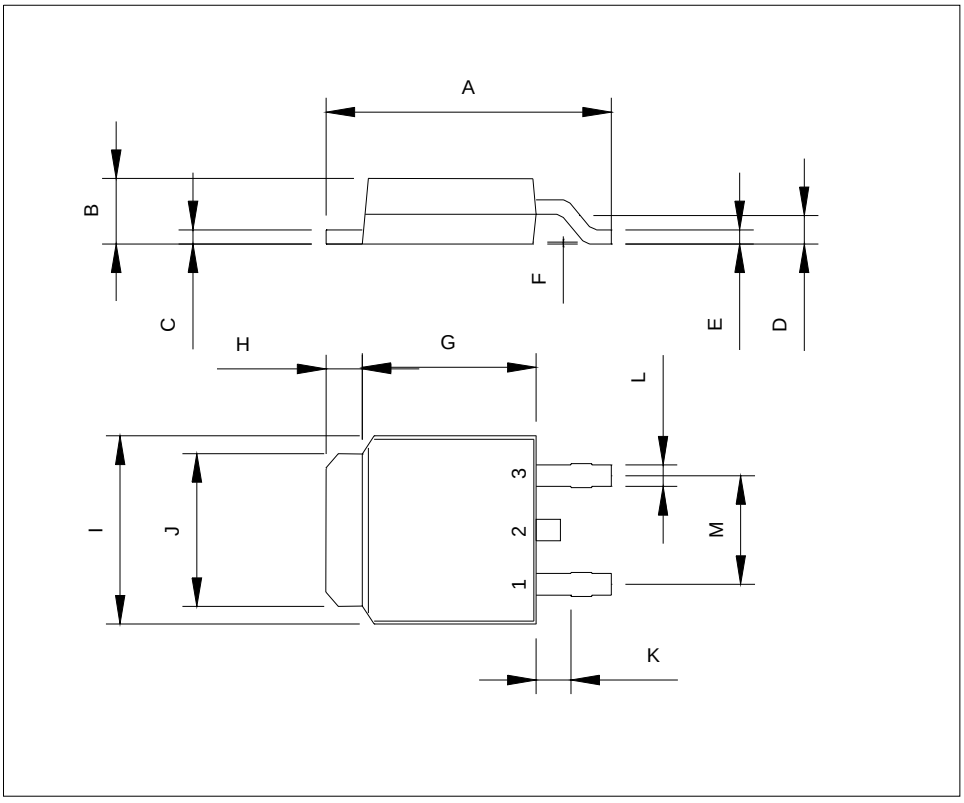
[1]Pulse test : Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

REMARK: THE PRODUCT MARKED WITH "P75N02LDG", DATE CODE or LOT #

Orders for parts with Lead-Free plating can be placed using the PXXXXXXXG parts name.

TO-252 (DPAK) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	9.35		10.4	H	0.89		2.03
B	2.2		2.4	I	6.35		6.80
C	0.45		0.6	J	5.2		5.5
D	0.89		1.5	K	0.6		1
E	0.45		0.69	L	0.5		0.9
F	0.03		0.23	M	3.96	4.57	5.18
G	5.2		6.2	N			



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