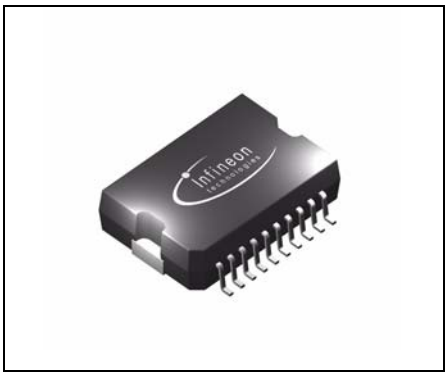
Final Datasheet

1 Overview



1.1 Features

- Operating supply voltage 5 V to 28 V
- Typical R_{DSon} = 150 mΩ for each output transistor (at 25 °C)
- Continuous DC load current 5 A (T_C < 100 °C)
- Output current limitation at typ. 6.6 A ± 1.1 A
- Short circuit shut-down for output currents over 8 A
- Logic- inputs TTL/CMOS-compatible
- Output switching frequency up to 30 kHz
- Rise and fall times optimized for 0.5-2 kHz
- Over-temperature protection
- Short circuit protection
- Undervoltage disable function
- Diagnostic by SPI or Status-Flag (configurable)
- Enable and Disable inputs
- P-DSO-20-12 power package

Type	Ordering Code	Package
TLE 7209-2R	Q67007-A9702	P-DSO-20-12

Functional Description

The TLE 7209-2R is an intelligent full H-Bridge, designed for the control of DC and stepper motors in safety critical applications and under extreme environmental conditions.

The H-Bridge is protected against over-temperature and short circuits and has an under voltage lockout for all the supply voltages "V_S" (main DC power supply). All malfunctions cause the output stages to go tristate.

The device is configurable by the DMS pin. When grounded, the device gives diagnostic information via a simple error flag. When supplied with V_{CC} = 5 V, the device works in SPI mode. In this mode, detailed failure diagnosis is available via the serial interface.

1.2 Pin Configuration

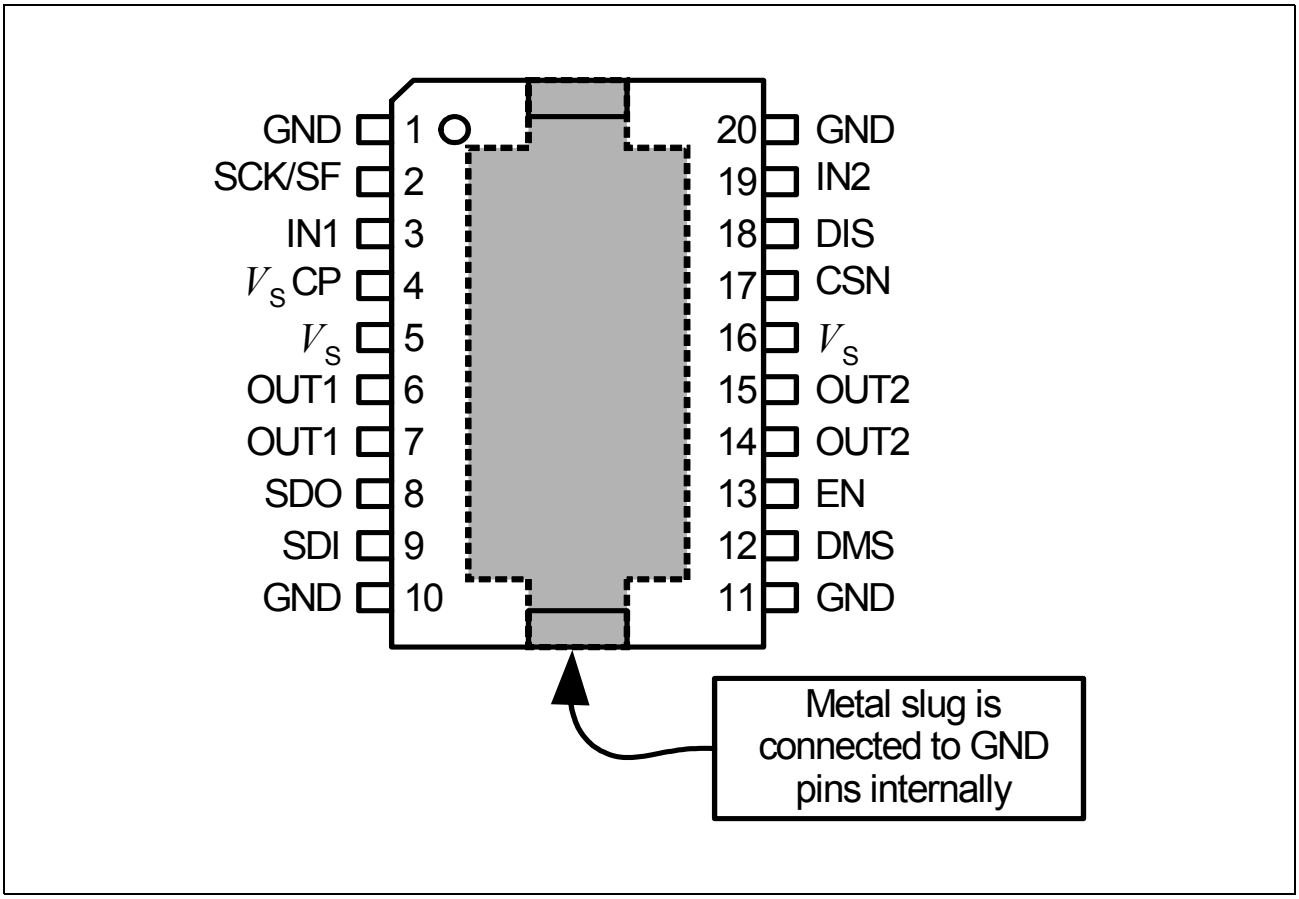


Figure 1 Pinout TLE 7209-2R

Table 1 Pin Definitions and Functions

Pin. No.	Symbol	Function
1	GND	Ground
2	SCK/SF	SPI-Clock/Status-flag
3	IN1	Input 1
4	V_SCP	Supply voltage for internal charge pump
5, 16	V_S	Supply voltage; connect pins externally
6, 7	OUT1	Output 1; connect pins externally
8	SDO	Serial data out
9	SDI	Serial data in
10	GND	Ground
11	GND	Ground

Table 1 Pin Definitions and Functions (cont'd)

Pin. No.	Symbol	Function
12	DMS	Diagnostic-Mode selection (+ Supply voltage for SPI-Interface)
13	EN	Enable
14, 15	OUT2	Output 2; connect pins externally
17	CSN	Chip Select (low active)
18	DIS	Disable
19	IN2	Input 2
20	GND	Ground

1.3 Block Diagram

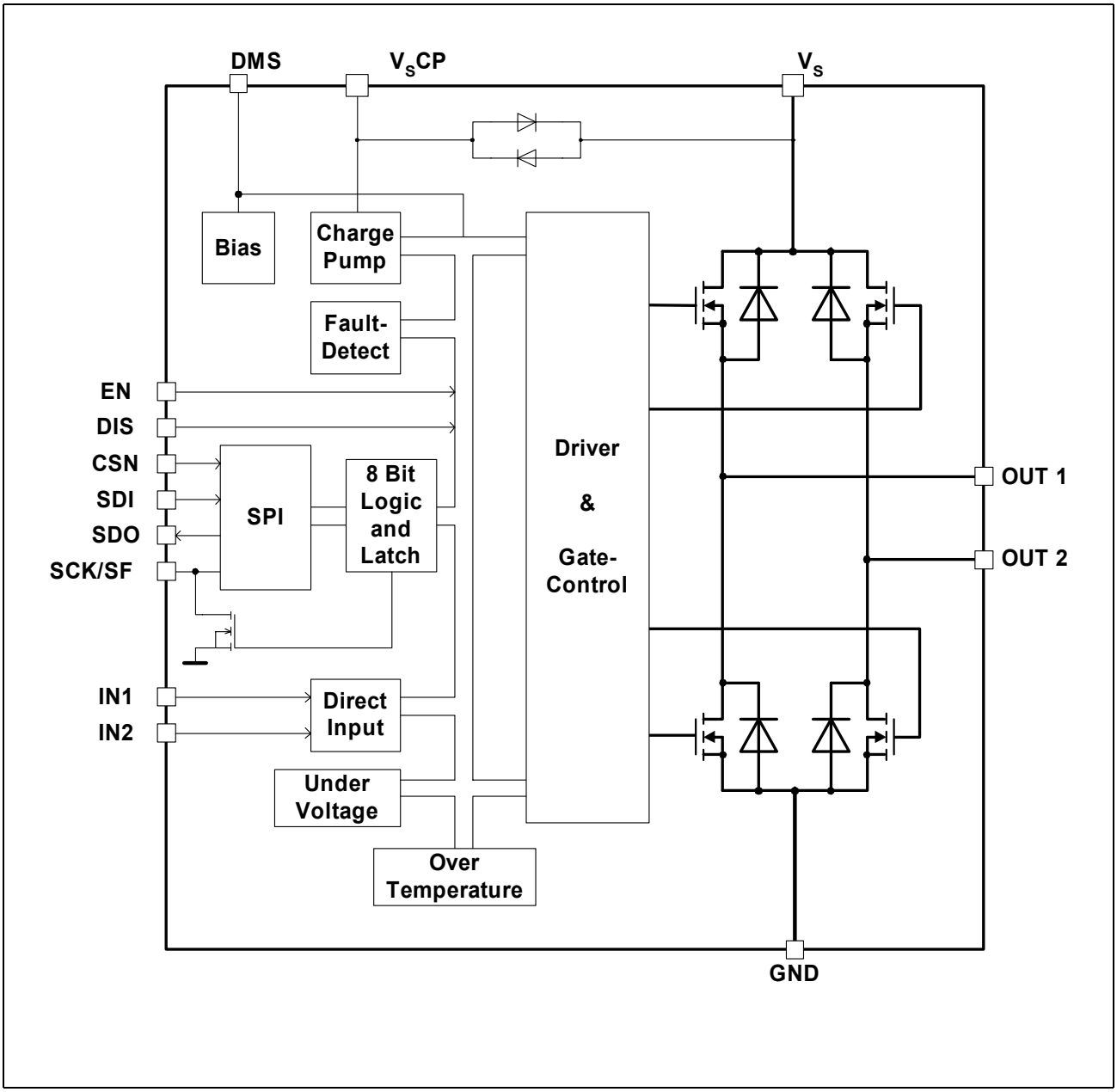


Figure 2 Block Diagram TLE 7209-2R

2 Circuit Description

2.1 Control Inputs

The bridge is controlled by the Inputs IN1, IN2, DIS and EN as shown in **Table 2**. The outputs OUT1 and OUT2 are set to High or Low by the parallel inputs IN1 and IN2, respectively. In addition, the outputs can be disabled (set to tristate) by the Disable and Enable inputs DIS and EN.

Inputs IN1, IN2 and DIS have an internal pull-up. Input EN has an internal pull-down.

Table 2 Functional Truth Table

Pos.	DIS	EN	IN1	IN2	OUT1	OUT2	SF[1)]	SPI[2)] DIA_REG
1. Forward	L	H	H	L	H	L	H	see **Chapter 2.4.2**
2. Reverse	L	H	L	H	L	H	H	
3. Free-wheeling low	L	H	L	L	L	L	H	
4. Free-wheeling high	L	H	H	H	H	H	H	
5. Disable	H	X	X	X	Z	Z	L	
6. Enable	X	L	X	X	Z	Z	L	
7. IN1 disconnected	L	H	Z	X	H	X	H	
8. IN2 disconnected	L	H	X	Z	X	H	H	
9. DIS disconnected	Z	X	X	X	Z	Z	L	
10. EN disconnected	X	Z	X	X	Z	Z	L	
11. Current limit. active	L	H	X	X	Z	Z	H	
12. Under Voltage	X	X	X	X	Z	Z	L	
13. Over-temperature	X	X	X	X	Z	Z	L	
14. Over-current	X	X	X	X	Z	Z	L	

1) If Mode “Status-Flag” is selected (see **Chapter 2.4**)

2) If Mode “SPI-Diagnosis” is selected (see **Chapter 2.4**)

2.2 Power Stages

Four n-channel power-DMOS transistors build up the output H-bridge. Integrated circuits protect the outputs against over current and over-temperature if there is a short-circuit to ground, to the supply voltage or across the load. Positive and negative voltage spikes, which occur when switching inductive loads, are limited by integrated freewheeling diodes. To drive the gates of the high-side DMOS, an internal charge pump is integrated to generate a voltage higher than the supply voltage.

2.2.1 Chopper Current Limitation

To limit the output current at low power loss, a chopper current limitation is integrated as shown in **Figure 3**. The current is measured by sense cells integrated in the low-side switches. When the current limit I_L has been exceeded for a time t_b, all output stages are switched off for a fixed time t_a.

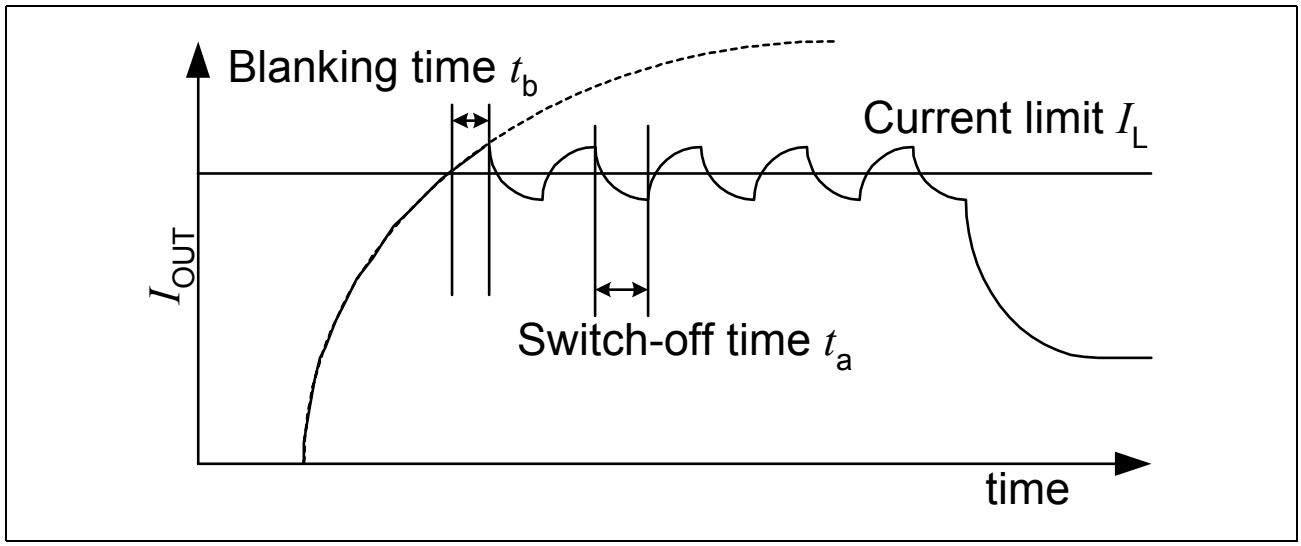


Figure 3 Chopper current limitation

2.2.2 Temperature-depending Current Reduction

For $T_{ILR} < T_j < T_{SD}$ the current limit decreases from I_L = 6.6 A ± 1.1 A to I_L = 2.5 A ± 1.1 A as shown in **Figure 4**

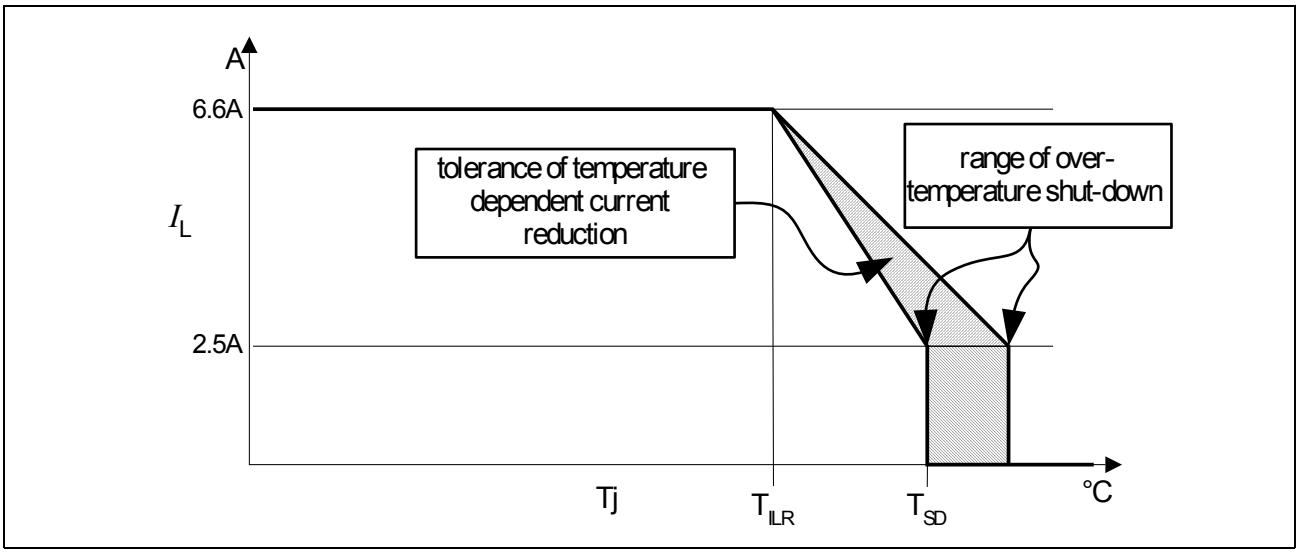


Figure 4 Temperature dependent current reduction

2.3 Protection

The TLE 7209-2R is protected against short circuits, overload and invalid supply voltage by the following measures:

2.3.1 Short circuit to Ground

The high-side switches are protected against a short of the output to ground by an over current shut-down. If a high-side switch is turned on and the current rises above the short circuit detection current I_{OUK} all output transistors are turned off after a typical filter time of 2 µs, and the error bit “Short Circuit to Ground on output 1 (2)”, SCG1 (SCG2) is stored in the internal status register.

2.3.2 Short circuit to V_S

Due to the chopper current regulation, the low-side switches are already protected against a short to the supply voltage. To be able to distinguish a short circuit from normal current limit operation, the current limitation is deactivated for the blanking time t_b after the current has exceeded the current limit threshold I_L. If the short circuit detection current I_{OUK} is reached within this blanking time, a short circuit is detected (see **Figure 5**). All output transistors are turned OFF and the according error bit “Short Circuit to Battery on output 1 (2)”, SCB1 (SCB2) is set.

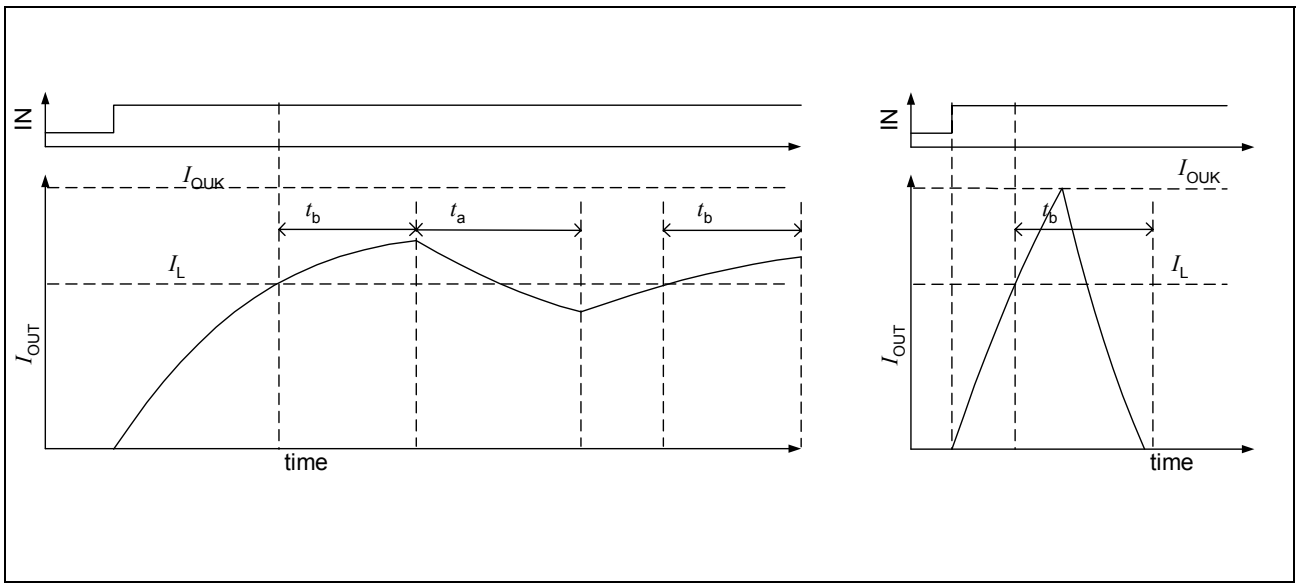


Figure 5 Short to Vs detection. Left: normal operation. Right: short circuit is detected

2.3.3 Short circuit across the load

If short circuit messages from high- and low-side switch occur simultaneously within a delay time of typically 2µs, the error bit “Short Circuit Over Load”, SCOL is set.

2.3.4 Over-Temperature

In case of high DC-currents, insufficient cooling or high ambient temperature, the chip temperature may rise above the thermal shut-down temperature T_{SD}. In that case, all output transistors are shut-down and the error-bit “Over-Temperature”, OT is set.

2.3.5 Under-Voltage shut-down

If the supply-voltage at the V_S pins falls below the under-voltage detection threshold, the outputs are set to tristate and the error-bit “Under-Voltage at V_S“ is set.

2.4 Diagnosis

The Diagnosis-Mode can be selected between SPI-Diagnosis and Status-Flag Diagnosis. The choice of the Diagnosis-Mode is selected by the voltage-level on Pin 12 (DMS Diagnosis Mode Selection):

- DMS = GND, Status-Flag Mode
- DMS = V_{CC}, SPI-Diagnosis Mode

For the connection of Pins SDI, SDO, CSN and SCK/SF see **Figure 14** and **Figure 15**.

2.4.1 Status-Flag (SF) Mode (DMS = GND)

2.4.1.1 SF output

In SF-mode, pin 2 is used as an open-drain output status-flag. The pin has to be pulled to the logic supply voltage with a pull-up resistor, 47 kOhm recommended.

In case of any failure that leads to a shut-down of the outputs, the status-flag is set (e.g. SF pin pulled to low). These failures are:

– Under Voltage on V_S
– Short circuit of OUT1 or OUT2 against V_S or GND
– Short circuit between OUT1 and OUT2
– Over-current
– Over-temperature

SF is also pulled low when the outputs are disabled by EN or DIS.

2.4.1.2 Fault storage and reset

– In case of **under-Voltage**, the failure is not latched. As soon as V_S falls below the under-Voltage detection threshold, the output stage switches in tristate and the status-flag is set from high level to low-level. If the voltage has risen above the specified value again, the output stage switches on again and the status-flag is reset to high-level. The Under Voltage failure is shown at the SF pin for V_S in the voltage range below the detection threshold (typical 4.2V) down to 2.5V.
– In the SF-mode, all internal circuitry is supplied by the voltage on V_S. For that reason, a loss of V_S supply voltage leads to a reset of all stored information (**Power-ON-Reset**). This Power-ON-Reset occurs as soon as under-Voltage is detected on V_S
– In case of **short circuit, over-current or over-temperature**, the fault will be stored. The output stage remains in tristate and the status-flag at low-level until the error is reset by one of the following conditions: H -> L on DIS, L -> H on EN or Power-ON Reset.

2.4.2 SPI-Mode (DMS = 5V)

2.4.2.1 SPI-Interface

The serial SPI interface establishes a communication link between TLE 7209-2R and the systems microcontroller. The TLE 7209-2R always operates in slave mode whereas the controller provides the master function. The maximum baud rate is 2 MBaud (200pF on SDO).

By applying an active slave select signal at CSN the TLE 7209-2R is selected by the SPI master. SDI is the data input (Slave In), SDO the data output (Slave Out). Via SCK (Serial Clock Input) the SPI clock is provided by the master. In case of inactive slave select signal (High) the data output SDO goes into tristate.

The first two bits of an instruction may be used to establish an extended device-addressing. This gives the opportunity to operate up to 4 Slave-devices sharing one common CSN signal from the Master-Unit (see **Figure 7**)

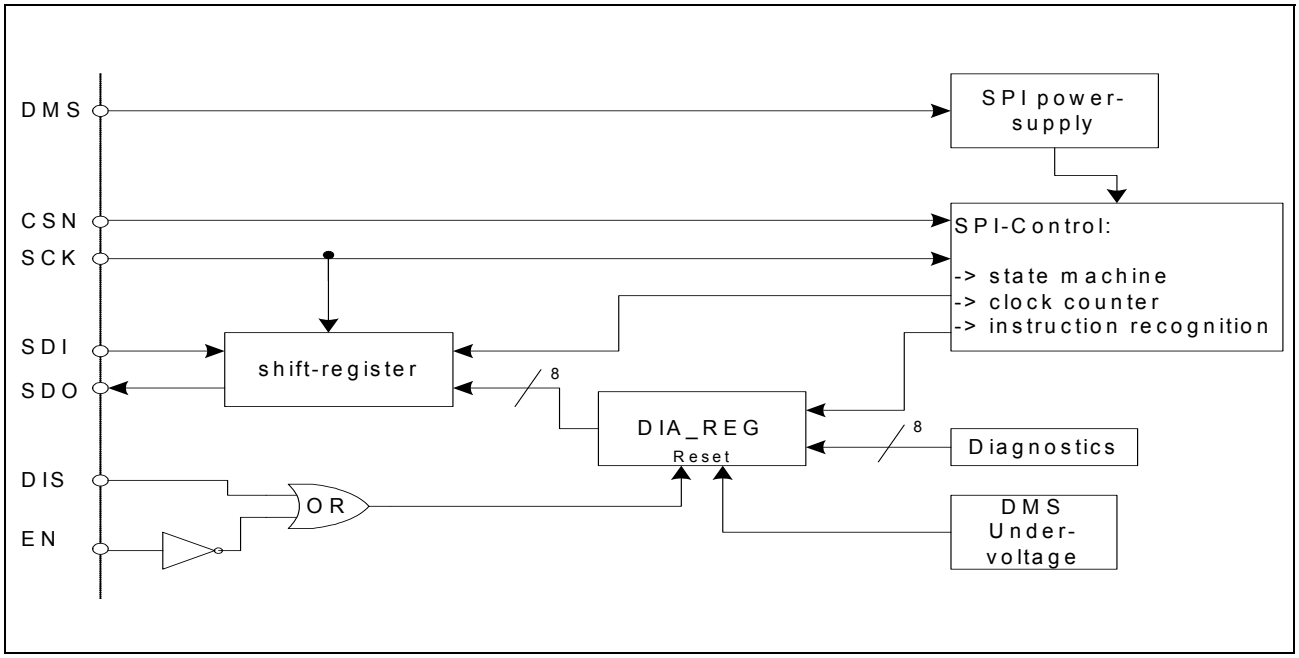


Figure 6 SPI block-diagram

2.4.2.2 Characteristics of the SPI Interface

1. When DMS is > 3.5V, the SPI is active, independently of the state of EN or DIS. During active reset conditions (DMS < 3.5V) the SPI is driven into its default state. When reset becomes inactive, the state machine enters into a wait-state for the next instruction.
2. If the slave select signal at CSN is inactive (high), the state machine is forced to enter the wait-state, i.e. the state machine waits for the following instruction.
3. During active (low) state of the select signal CSN the falling edge of the serial clock signal SCK will be used to latch the input data at SDI. Output data at SDO are driven with the rising edge of SCK (see timing diagram **Figure 13**)
4. Chip-address:
   In order to establish the option of extended addressing the uppermost two bits of the instruction-byte (i.e the first two SDI-bits of a Frame) are reserved to send a chip-address. To avoid a bus conflict the output SDO must stay high impedance during the addressing phase of a frame (i.e. until the address-bits are recognized as valid chip-address). If the chip-address does not match, the data at SDI will be ignored and SDO remains high impedance for the complete frame. See also **Figure 7**
5. Verification byte:
   Simultaneously to the receipt of an SPI instruction TLE 7209-2R transmits a verification byte via the output SDO to the controller. Refer to **Figure 8**. This byte indicates normal or abnormal operation of the SPI. It contains an initial bit pattern and a flag indicating an error occurred during the previous access.

6. Because only read access is used in the TLE 7209-2R, the SDI data-bits (2nd byte) are not used
7. Invalid instruction/access:
   An instruction is invalid if an unused instruction code is detected (see tables with SPI instructions). In case an unused instruction code occurred, the data byte “ff_{hex}” (no error) will be transmitted after having sent the verification byte. This transmission takes place within the same SPI-frame that contained the unused instruction byte. In addition any transmission is invalid if the number of SPI clock pulses (falling edge) counted during active CSN differs from exactly 16 clock pulses. If an invalid instruction is detected, bit TRANS_F in the following verification byte (next SPI transmission) is set to HIGH. The TRANS_F bit must not be cleared before it has been sent to the microcontroller.
8. Transfer error bit TRANS_F:
   The bit TRANS_F indicates an error during the previous transfer. An error is considered to have occurred when an invalid command was sent, the number of SPI clock pulses (falling edge) counted during active CSN was less than or greater than 16 clock pulses, or SPI clock (SCK) was logical high during falling edge of CSN.

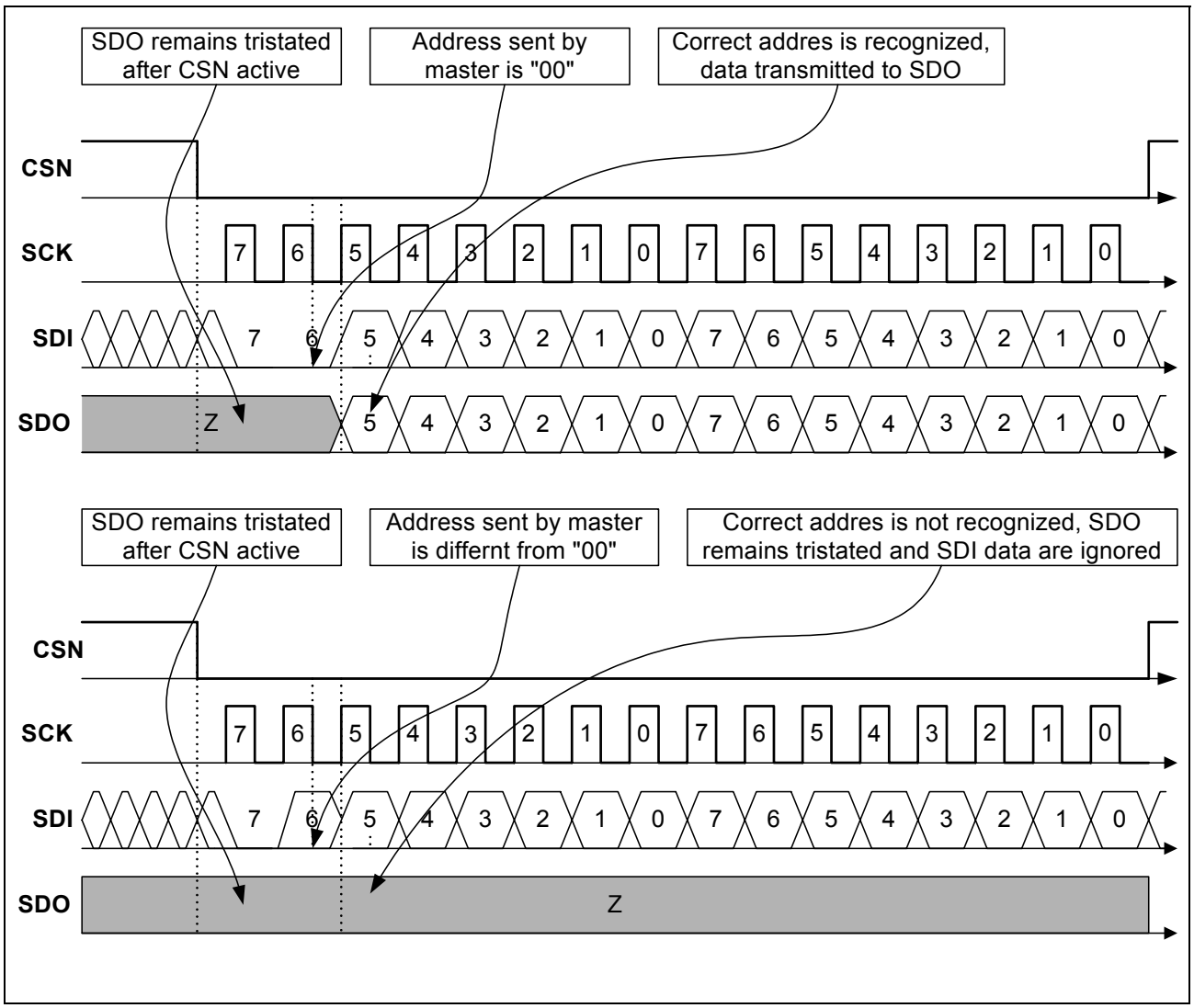


Figure 7 Bus-arbitration by chip-address

2.4.2.3 SPI-Communication

The 16 input bits consist of the SPI-instruction byte and a second, unused byte. The 16 output bits consist of the verification-byte and the data-byte (see also **Figure 8**). The definition of these bytes is given in the subsequent sections.

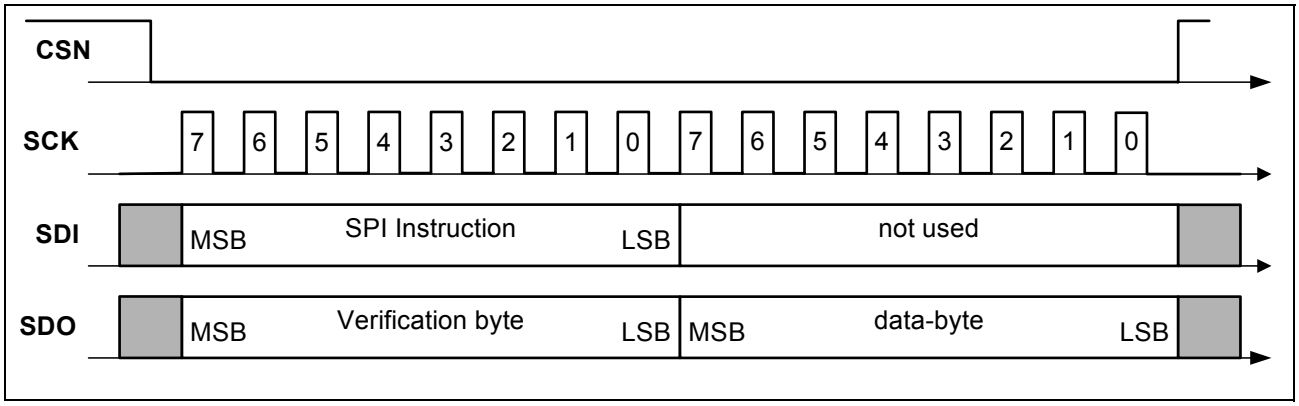


Figure 8 SPI communication

2.4.2.4 SPI instruction

The uppermost 2 bit of the instruction byte contain the chip-address. The chip-address of the TLE 7209-2R is 00. During read-access, the output data according to the register requested in the instruction byte are applied to SDO within the same SPI frame. That means, the output data corresponding to an instruction byte sent during one SPI frame are transmitted to SDO during the same SPI frame.

Table 3 SPI Instruction Format

MSB							
7	6	5	4	3	2	1	0
0	0	INSTR4	INSTR3	INSTR2	INSTR1	INSTR0	INSW

Table 4 SPI instruction Description

Bit	**Name**	**Description**
7,6	CPAD1,0	Chip Address (has to be ‘0’, ‘0’)
5-1	INSTR (4-0)	SPI instruction (encoding)
0	INSW	Even parity

Table 5 SPI Instruction-Bytes Encoding

SPI Instruction	Encoding			Description
	bit 7,6 CPAD1,0	bit 5-1 INSTR(4-0)	Bit 0 INSW	
RD_IDENT	00	00000	0	read identifier
RD_VERSION	00	00001	1	read version
RD_DIA	00	00100	1	read DIA_REG
–	00	all others	x	unused, TRANS_F is set to high, ff_hex is sent as data bit
–	all others	xxxxx	x	invalid address, SDO remains tristate during entire SPI frame

2.4.2.5 Verification Byte

Table 6 Verification Byte Format

MSB							
7	6	5	4	3	2	1	0
Z	Z	1	0	1	0	1	TRANS_F

Table 7 Verification Byte Description

Bit	Name	Description
0	TRANS_F	Bit = 1: error detected during previous transfer Bit = 0: previous transfer was recognized as valid
1		Fixed to High
2		Fixed to Low
3		Fixed to High
4		Fixed to Low
5		Fixed to High
6		send as high impedance
7		send as high impedance

The default value after power-up at DMS of the TRANS_F bit is L (previous transfer valid)

2.4.2.6 Data-byte: Diagnostics/Encoding of Failures (Register DIA_REG, SPI Instruction RD_DIA)

Table 8 DIA_REG Format

MSB							
7	6	5	4	3	2	1	0
EN/DIS	OT	CurrRed	CurrLim	DIA21	DIA20	DIA11	DIA10

Table 9 DIA_REG Description

Default value after reset is FF_{hex}. Access by controller is read only

Bit	**Name**	**Description**	**latch behavior**
0	DIA 10	Diagnosis-Bit1 of OUT1	see below
1	DIA 11	Diagnosis-Bit2 of OUT1	see below
2	DIA 20	Diagnosis-Bit1 of OUT2	see below
3	DIA 21	Diagnosis-Bit2 of OUT2	see below
4	CurrLim	is set to „0“ in case of current limitation.	latched
5	CurrRed	is set to „0“ in case of temperature dependent current limitation	latched
6	OT	is set to „0“ in case of over-temperature	latched
7	EN/DIS	is set to „0“ in case of EN = L or DIS = H	not latched

EN	**DIS**	**DIA_REG_7**
H	L	1
L	L	0
H	H	0
L	H	0

Table 10 Encoding of the Diagnostic Bits of OUT1 and OUT2

DIA21	DIA20	DIA11	DIA10	Description	latch behavior
1	1	0	0	Short circuit over load (SCOL)	latched
-	-	0	1	Short circuit to battery on OUT1 (SCB1)	latched
-	-	1	0	Short circuit to ground on OUT1 (SCG1)	latched
-	-	1	1	No error detected on OUT1	-
0	0	1	1	Open load (OL)	latched
0	1	-	-	Short circuit to battery on OUT2 (SCB2)	latched
1	0	-	-	Short circuit to ground on OUT2 (SCG2)	latched
1	1	-	-	No error detected on OUT2	-
0	0	0	0	Under Voltage on Pin Vs	not latched

Failure Encoding in case of multiple faults

If multiple faults are stored in the failure register, the faults that are encoded in the DIAxx bits can not be displayed simultaneously due to the encoding scheme that is used. In this case, errors are encoded according to the following priority list.

– Priority 1: Under Voltage (please note that after removal of Under Voltage, the original error will be restored, see below)
– Priority 2: Short circuit across the load
– Priority 3: all other short circuits
– Priority 4: open load

If a failure of higher priority is detected, the failures of lower priority are no longer visible in the encoded SPI message.

Fault storage and reset of the Diagnosis Register DIA_REG

Register DIA_REG is reset upon the following conditions:

– With the rising edge of the CSN-Signal after the SPI-instruction RD_DIA. This reset only takes place if the correct number of 16 SCK pulses has been counted.
– When the voltage on DMS exceeds the threshold for detecting SPI-Mode (after Under Voltage condition). Under Voltage on Vs (typ. < 5,0V) sets Bit 0.... Bit 3 of DIA_REG to 0000. If Vs rises above the Under Voltage level, Bits of DIA_REG are restored (when DMS > 3.5V).
– A rising edge on EN while DIS=0 or a falling edge on DIS while EN=1 re-activates the output power-stages, and resets the DIA_REG register.

2.4.2.7 Data-byte: Device Identifier and Version (SPI instructions RD_IDENT and RD_VERSION)

The IC's identifier (device ID) and version number are used for production test purposes and features plug & play functionality depending on the systems software release. The two numbers are read-only accessible via the SPI instructions RD_IDENT and RD_VERSION as described in **Section 2.4.2.4**.

The device ID is defined to allow identification of different IC-Types by software and is fixed for the TLE 7209-2R.

The Version number may be utilized to distinguish different states of hardware and is updated with each redesign of the TLE 7209-2R. The contents is divided into an upper 4 bit field reserved to define revisions (SWR) corresponding to specific software releases and a lower 4 bit field utilized to identify the actual mask set revision (MSR).

Both (SWR and MSR) will start with 0000b and are increased by 1 every time an according modification of the hardware is introduced.

Reading the IC Identifier (SPI Instruction: RD_IDENT):

Table 11 Device Identifier Format

MSB							
7	6	5	4	3	2	1	0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Table 12 Device Identifier Description

Bit	**Name**	**Description**
7...0	device-ID(7...0)	ID-No.: 10100010

Reading the IC version number (SPI Instruction: RD_VERSION):

Table 13 IC version number Format

MSB							
7	6	5	4	3	2	1	0
SWR3	SWR2	SWR1	SWR0	MSR3	MSR2	MSR1	MSR0

Table 14 IC version number Description

Bit	**Name**	**Description**
7...4	SWR(3...0)	This register is set to 0
3...0	MSR(3...0)	Version corresponding to Mask set

2.4.2.8 Open-Load Diagnosis

Open-load diagnostic in OFF-state is only possible in the SPI-mode (DMS = 5 V) if the device is Disabled (EN = L or DIS = H). The detection mechanism is depicted in **Figure 9**. The according diagnostic information can be read out via the SPI diagnostic register. The resulting overall diagnostic truth-table is shown as **Table 15**

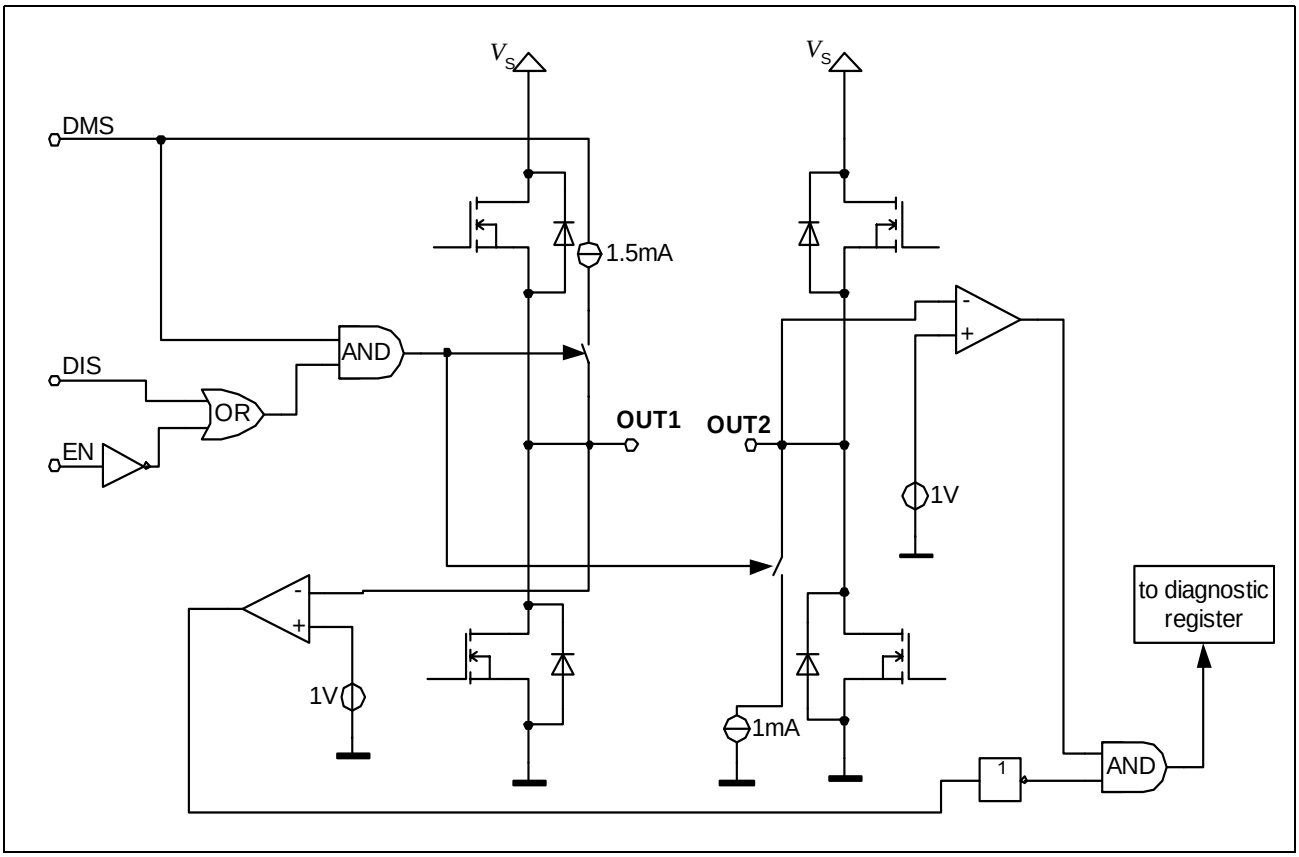


Figure 9 Functional block diagram of open-load detection

Table 15 Diagnosis Truth Table for open load detection

Output stage inactive, EN = low or DIS = high, DMS > 4.5 V

	OUT1	OUT2	
Load available	H	H	
Open Load	H	L	OL detected
SC -> GND on OUT1 and Open Load	L	L	OL not detected – double Fault
SC -> GND on OUT2 and Open Load	H	L	OL detected
SC -> V_S on OUT1 and Open Load	H	L	OL detected
SC -> V_S on OUT2 and Open Load	H	H	OL not detected – double Fault

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Pos.	Parameter	Sym-bol	Limit Values		Unit	Test Conditions
			min.	max.		
3.1.1	Junction temperature	T_j	-40	+150	°C	–
			–	+175	°C	dynamic: t < 1 s
3.1.2	Storage temperature	T_s	-55	+125	°C	–
3.1.3	Ambient temperature	T_a	-40	+125	°C	–
3.1.4	Supply voltage	V_S	-1	40	V	static destruction proof
			-2	40	V	dynamic destruction proof t < 0.5 s (single pulse, T_j < 85 °C)
3.1.5	Voltage at logic inputs IN1, IN2, DIS, EN, SDI, SCK/SF	V	-0.5	18	V	In status-flag-mode, SF pull-up $R \geq 10\ k\Omega$
3.1.6	Voltage at logic input CSN	V	-0.5	40	V	
3.1.7	Voltage at logic input DMS	V_{DMS}	-0.5	13	V	–
3.1.8	Voltage at logic output SDO	V	-0.5	V_{DMS} +0.5	V	–
3.1.9	Voltage at VsCP	V_{CP}	V_S - 0.5	V_S + 0.5	V	-
3.1.10	ESD voltage human body model (MIL STD 883D / ANSI EOS\ESD S5.1)	V_{ESD}	–	–	4kV	all pins
3.1.11		$V_{ESD--OUT}$	–	–	8kV	only pins 6, 7, 14 and 15 (outputs)

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

3.2 Operating Range

Pos.	Parameter	Sym-bol	Limit Values		Unit	Remark
			min.	max.		
3.2.1	Supply Voltage	V_S	5	28	V	
3.2.2	DMS Supply Voltage	V_{DMS}	3.5	5.5	V	Device in SPI-mode
3.2.3	PWM frequency	f	–	30	kHz	May be limited to lower values in the application due to switching losses or duty cycle requirements
3.2.4	Junction Temperature	T_J	-40	150	°C	

Note: In the operating range, the circuit functionality as described in the circuit description is fulfilled.

3.3 Thermal Resistance

3.3.1	Junction-case	R_{thJC}	–	1.5	K/W	specified by design
3.3.2	Junction-ambient	R_{thJA}	–	50	K/W	minimal footprint

3.4 Electrical Characteristics

5V < V_S < 28V; – 40 °C < T_j < 150 °C; unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Power Supply							
3.4.1	Under voltage at V_S	$V_{UV\ OFF}$	3.4	4.2	5	V	Switch off threshold
		$V_{UV\ ON}$	3.6	4.4	5.2		Switch on threshold
		$V_{UV\ HY}$	100	–	1000	mV	Hysteresis
3.4.2	Supply current	I_{UB}	–	–	30	mA	f = 20 kHz, I_{OUT} = 0 A
			–	–	20	mA	f = 0 Hz, I_{OUT} = 0 A

3.4 Electrical Characteristics (cont'd)

5V < V_S < 28V; – 40 °C < T_j < 150 °C; unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Logic Inputs IN1, IN2, DIS, EN							
3.4.3	Input "high"	V_{IH}	2	–	–	V	–
3.4.4	Input "low"	V_{IL}	–	–	1	V	–
3.4.5	Input hysteresis	$V_{IH}Y$	0.1	–	0.6	V	–
3.4.6	pull-up current IN1, IN2, DIS	I_{IL}	-200	-125	–	µA	$U \leq 1$ V
3.4.7	pull-down current EN	I_{IH}	–	–	100	µA	$U \geq 2$ V
Power Outputs OUT1, OUT2							
3.4.8	Switch on resistance	–	–	–	300	mΩ	R_{OUT-UB}, $R_{OUT-GND}$ V_S > 5 V, I_{OUT} = 3 A
3.4.9	Switch-off current	$\|I_L\|$	5.5	6.6	7.7	A	-40 °C < T_j < T_{ILR}
			1.4	2.5	3.6	A	$T_j = T_{SD}$; specified by design
3.4.10	Switch-off time	t_a	8	16	26	µs	Vs=13.2 V, L=2.2 mH, R=0.23 Ω
3.4.11	Blanking time	t_b	8	13	19	µs	Vs=13.2 V, L=2.2 mH, R=0.23 Ω
3.4.12	Switch-off Tracking	t_a/t_b	1.0	–	–	–	Vs=13.2 V, L=2.2 mH, R=0.23 Ω
3.4.13	Short circuit detection current	$\|I_{OUK}\|$	8	–	18	A	–
3.4.14	Current Tracking	$\|I_{OUK}\|$-$\|I_L\|$	2	3.5	–	A	specified by design
3.4.15	Reactivation time after internal shut-down	t	–	–	200	µs	Over-current- or over-temperature shut-down to reactivation of the output stage

Note: Reactivation time is not subject to production test; specified by design

3.4 Electrical Characteristics (cont'd)

5V < V_S < 28V; – 40 °C < T_j < 150 °C; unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
3.4.16	Leakage current	–	–	–	200	µA	Output stage switched off
3.4.17	Free-wheel diode forward voltage	U_D	–	–	2	V	I_{OUT} = 3 A
3.4.18	Free-wheel diode reverse recovery time	t_{rr}	–	–	100	ns	Reverse recovery time is not subject to production test; specified by design
Output Status-flag, Open Drain Output DMS < 0.8 V							
3.4.19	Output "high" (SF not set)	I_{SF}	–	–	20	µA	V_{SF} = 5 V
3.4.20	Output "low" (SF set)	I_{SF}	300	–	–	µA	V_{SF} = 1 V
			100	–	–	µA	V_{SF} = 0.5 V
Timing							
3.4.21	Output ON-delay	t_{don}	–	–	6	µs	IN1 --> OUT1 resp. IN2 --> OUT2, I_{OUT} = 3 A
3.4.22	Output OFF-delay	t_{doff}	–	–	6	µs	IN1 --> OUT1 resp. IN2 --> OUT2, I_{OUT} = 3 A
3.4.23	Output switching time	t_r, t_f	–	–	5	µs	OUT1H --> OUT1L, OUT2H --> OUT2L, I_{OUT} = 3 A OUT1L --> OUT1H, OUT2L --> OUT2H
3.4.24	Disable delay time	t_{ddis}	–	–	2	µs	DIS --> OUTn, EN --> OUTn
3.4.25	Power on delay time	–	–	–	1	ms	V_S = on --> output stage active; no load
3.4.26	Delay time for fault detection	t_{df}	1.0	2	–	µs	specified by design
3.4.27	Minimum pulse width	t_{den}	–	1.6	2.2	µs	EN/DIS-->Reset DIA_REG

3.4 Electrical Characteristics (cont'd)

5V < V_S < 28V; – 40 °C < T_j < 150 °C; unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Input SCK, SPI Clock Input							
3.4.28	Low Level	U_{SCKL}	–	–	1	V	–
3.4.29	High Level	U_{SCKH}	2	–	–	V	–
3.4.30	Hysteresis	ΔU_{SCK}	0.1	–	0.4	V	–
3.4.31	Input Capacity	C_{SCK}	–	–	20	pF	–
3.4.32	Input Current	$-I_{SCK}$	–	20	50	µA	Pull-up current source connected to V_{CC}
Input CSN, Chip Select Signal							
3.4.33	Low Level	U_{CSNL}	–	–	1	V	TLE 7209-2R is selected
3.4.34	High Level	U_{CSNH}	2	–	–	V	–
3.4.35	Hysteresis	ΔU_{CSN}	0.1	–	0.4	V	–
3.4.36	Input Capacity	C_{CSN}	–	–	20	pF	–
3.4.37	Input Current	$-I_{CSN}$	–	20	50	µA	Pull up current source connected to V_{CC}
Input SDI, SPI Data Input							
3.4.38	Low Level	U_{SDIL}	–	–	1	V	–
3.4.39	High Level	U_{SDIH}	2	–	–	V	–
3.4.40	Hysteresis	ΔU_{SDI}	0.1	–	0.4	V	–
3.4.41	Input Capacity	C_{SDI}	–	–	20	pF	–
3.4.42	Input Current	$-I_{SDI}$	–	20	50	µA	Pull up current source connected to V_{CC}

3.4 Electrical Characteristics (cont'd)

5V < V_S < 28V; – 40 °C < T_j < 150 °C; unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Output SDO							
Tristate Output of the TLE 7209-2R (SPI output);							
3.4.43	Low Level	V_{SDOL}	–	–	0.4	V	I_{SDO} = 2 mA
3.4.44	High Level	V_{SDOH}	V_{DMS} - 0.75	–	–	V	I_{SDO} = -2 mA
3.4.45	Capacity	C_{SDO}	–	–	30	pF	Capacity of the pin in tristate
3.4.46	Leakage Current	I_{SDO}	-10	–	10	µA	In tristate
Note: All in- and output pin capacities are not subject to production test; specified by design							
Input DMS							
Supply-Input for the SPI-Interface and Selection Pin for SPI- or SF-Mode							
3.4.47	Input Voltage	V_{DMS}	3.5	–	–	V	SPI-Mode
		V_{DMS}	–	–	0.8	V	Status-Flag-Mode
3.4.48	Input Current	I_{DMS}	–	–	10	mA	SPI-Mode
Open-Load Diagnosis							
3.4.49	Diagnostic Threshold	V_{OUT1}	0.8	–	2.0	V	DMS > 4.5 V, EN < 0.8 V or DIS > 4.5 V; no load
		V_{OUT2}	0.8	–	2.0	V	
3.4.50	Pull-up Current	$-I_{OUT1}$	1000	1500	2000	µA	V_{OUT1}=0 V, DMS > 4.5 V, EN < 0.8 V or DIS > 4.5 V; no load
3.4.51	Pull-down Current	I_{OUT2}	700	1000	1400	µA	V_{OUT2}=5 V, DMS > 4.5 V, EN < 0.8 V or DIS > 4.5 V; no load
3.4.52	Tracking Diag. C	–	1.2	1.5	1.7	–	I_{OUT1}/I_{OUT2}
3.4.53	Delay Time	t_D	30	–	100	ms	–
Note: Open Load is detected if V_{OUT1} > 2 V AND V_{OUT2} < 0.8 V (refer to fig. 9).							

3.4 Electrical Characteristics (cont'd)

5V < V_S < 28V; – 40 °C < T_j < 150 °C; unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
SPI Timing (see Figure 13)							
3.4.54	Cycle-Time (1)	t_{cyc} (1)	200	–	–	ns	referred to master
3.4.55	Enable Lead Time	t_{lead} (2)	100	–	–	ns	referred to master
3.4.56	Enable Lag Time	t_{lag} (3)	150	–	–	ns	referred to master
3.4.57	Data Valid	t_v (4)	– –	– –	40 150	ns ns	C_L = 40 pF C_L = 200 pF referred to TLE 7209-2R
3.4.58	Data Setup Time	t_{su} (5)	50	–	–	ns	referred to master
3.4.59	Data Hold Time	t_h (6)	20	–	–	ns	referred to master
3.4.60	Disable Time	t_{dis} (7)	–	–	100	ns	referred to TLE 7209-2R; specified by design
3.4.61	Transfer Delay	t_{dt} (8)	150	–	–	ns	referred to master
3.4.62	Select time	t_{CSN} (9)	50	–	–	ns	referred to master
3.4.63	Access time	t_{acc} (10)	8.35	–	–	µs	referred to master
3.4.64	Clock inactive before chip select becomes valid	(11)	200	–	–	ns	–
3.4.65	Clock inactive after chip select becomes invalid	(12)	200	–	–	ns	–
Temperature Thresholds							
3.4.66	Start of current limit reduction	T_{ILR}	150	165	–	°C	
3.4.67	Thermal Shut-down	T_{SD}	175	–	–	°C	
Note: Temperature thresholds are not subject to production test; specified by design							

4 Timing Diagrams

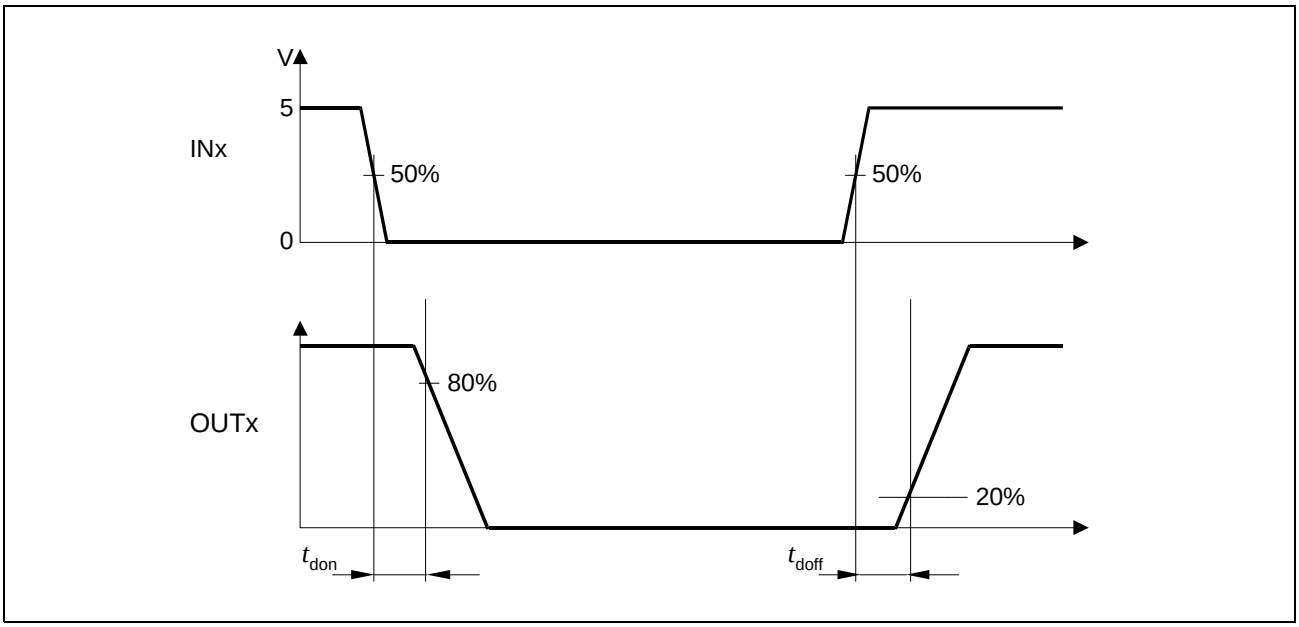


Figure 10 Output Delay Time--Depicted for Low-Side FETs

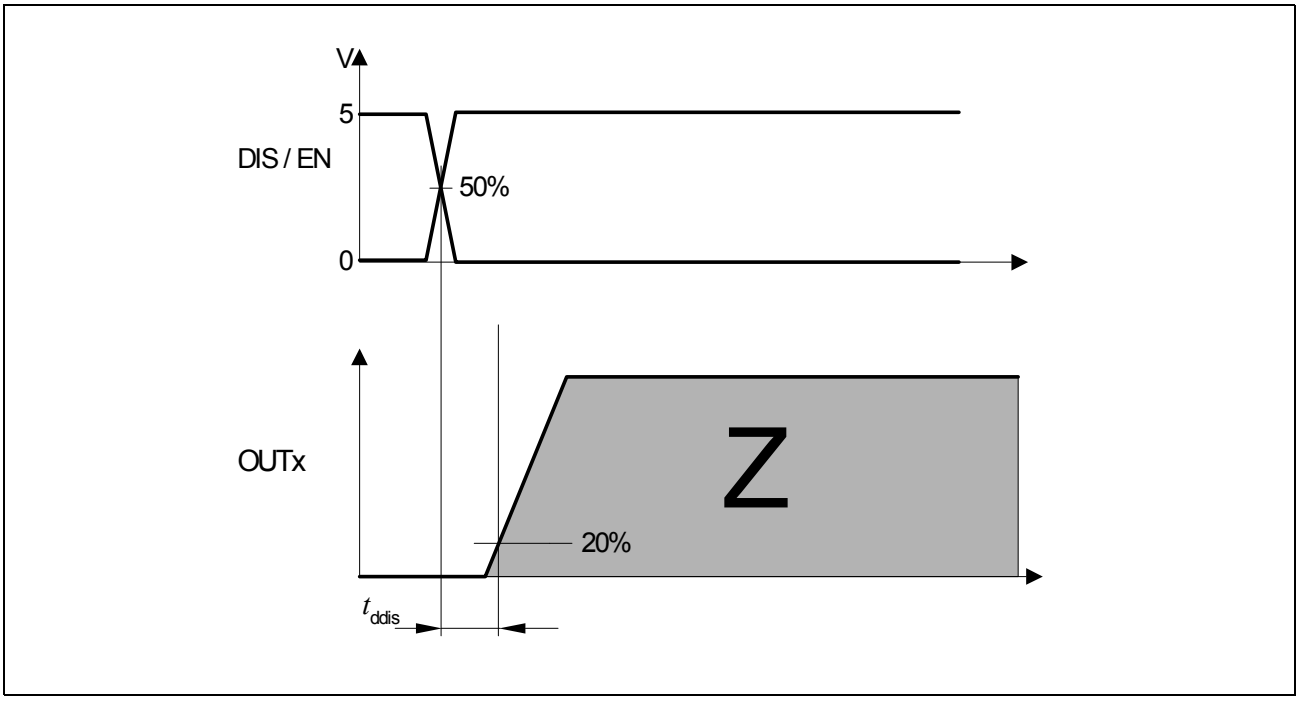


Figure 11 Disable Delay Time

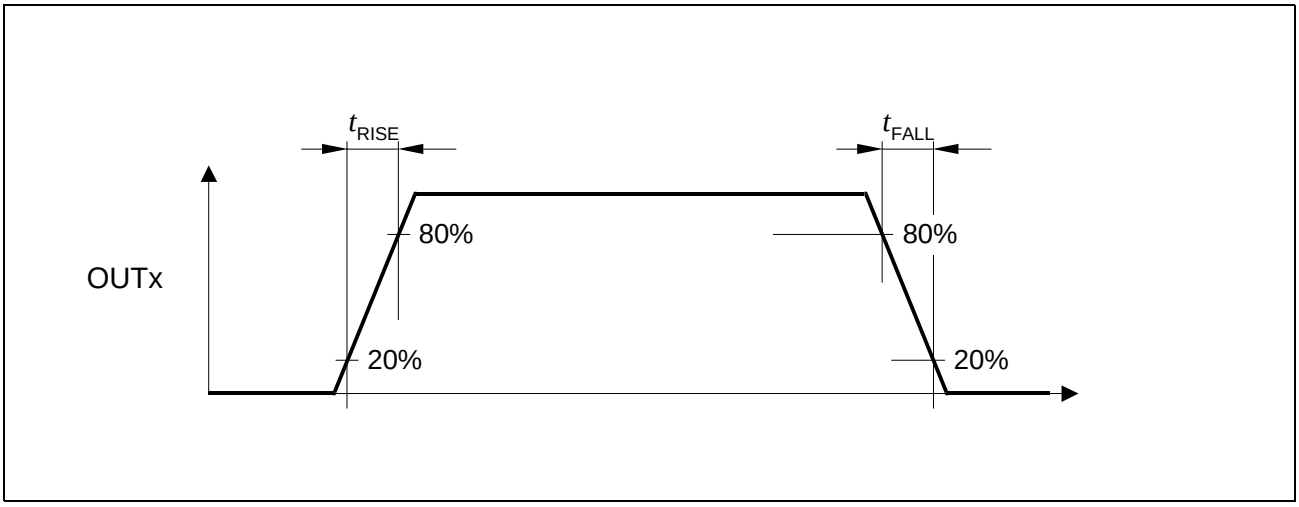


Figure 12 Output Switching Time

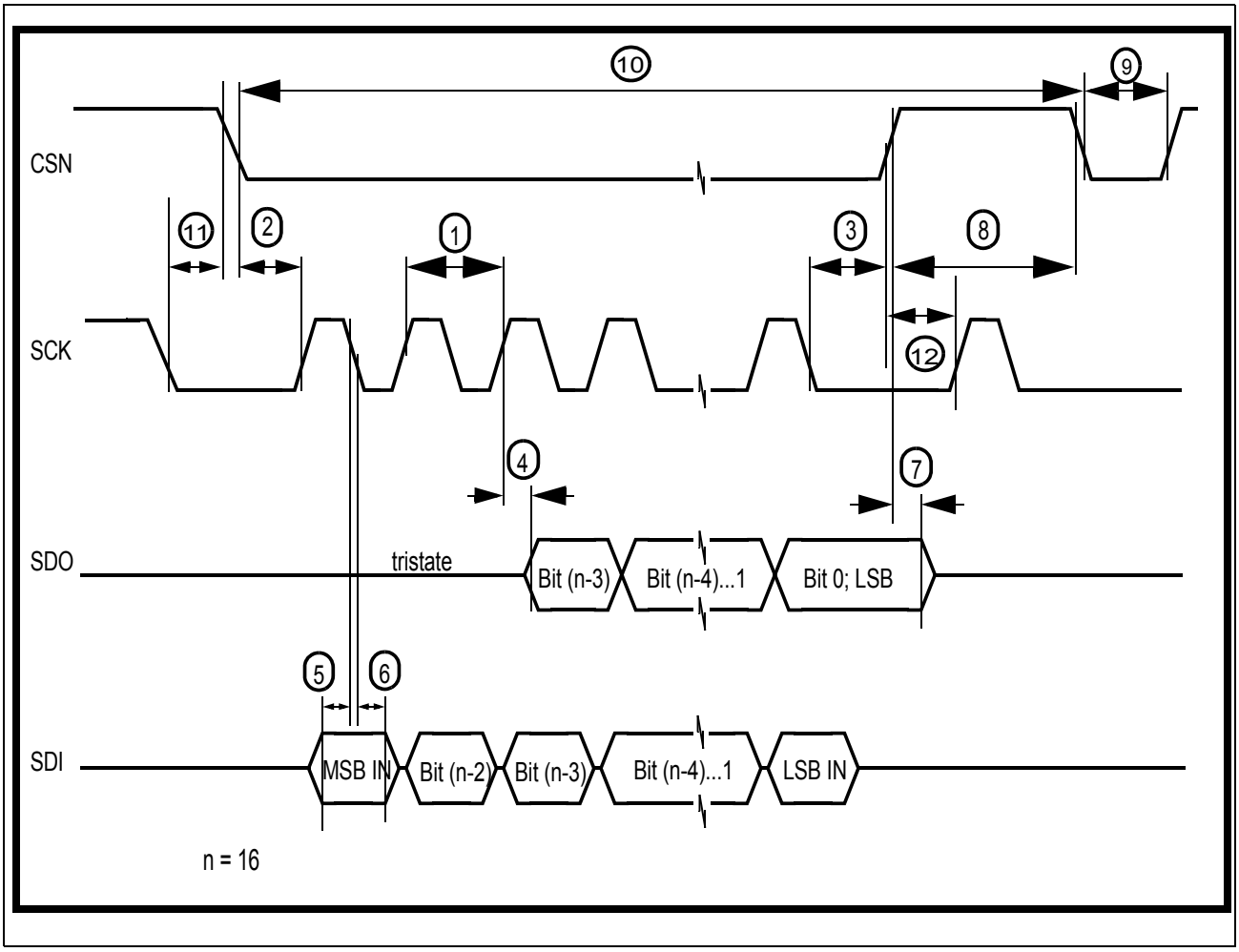


Figure 13 SPI-timing

5 Application

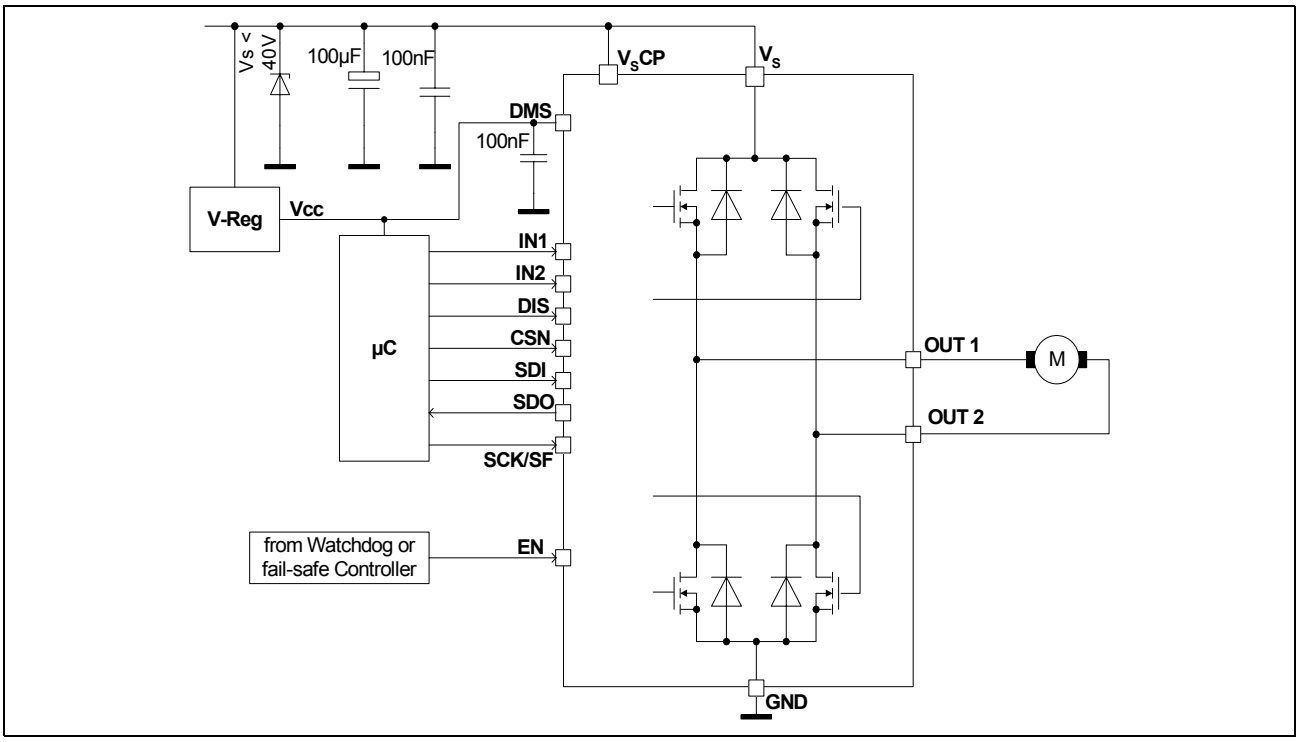


Figure 14 Application Example with SPI-Interface

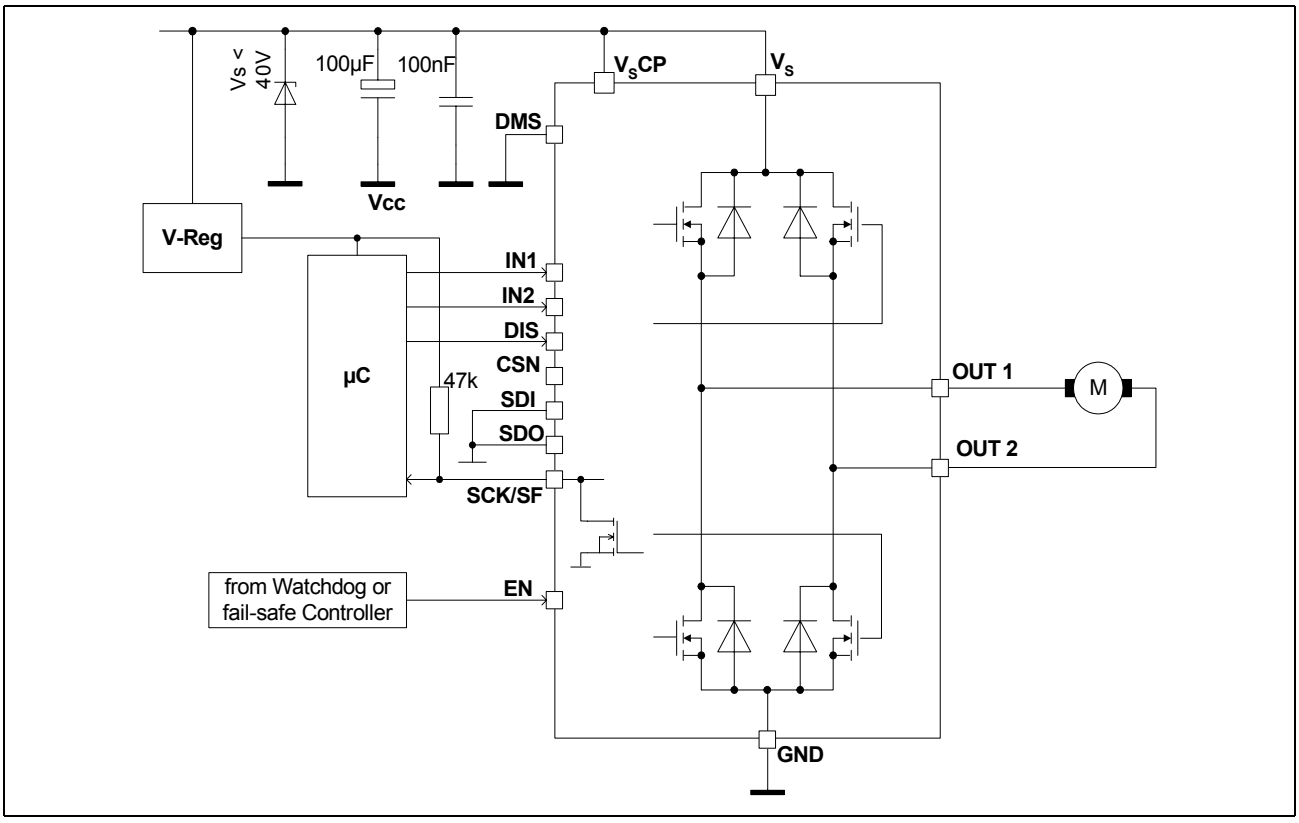


Figure 15 Application Example with Status-Flag

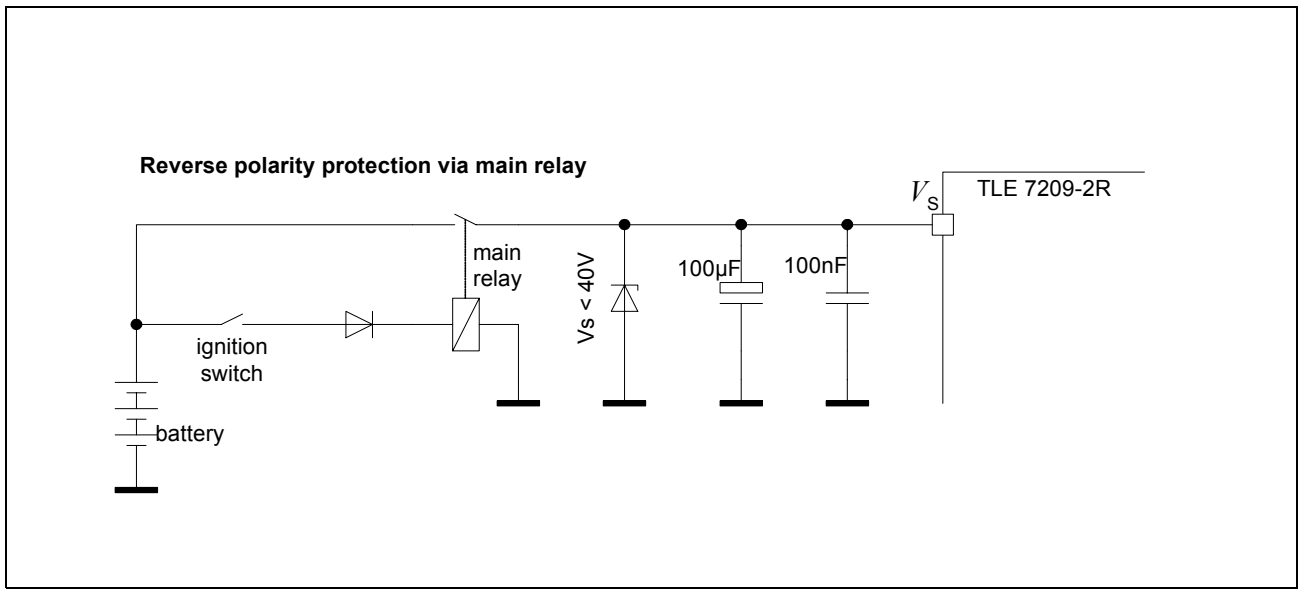
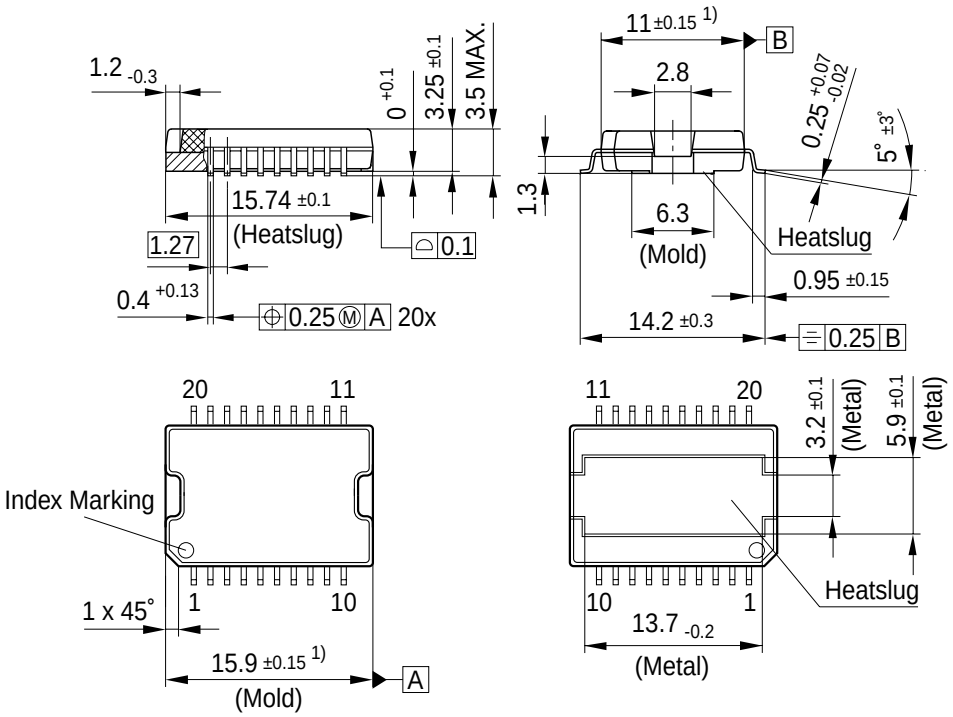


Figure 16 Application Examples for Over-Voltage- and Reverse-Voltage Protection

6 Package Outlines

P-DSO-20-12
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPS05791

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm

7 Revision History

TLE 7209-2R	**2005-jan-11**	V1.3
Previous Version:	Final Datasheet V1.2, 2004-jul-01	
Section	Subjects (major changes since last revision)	
3.4.31	SCK input capacity max limit changed from 10 to 20 pF	
3.4.36	CSN input capacity max limit changed from 10 to 20 pF	
3.4.41	SDI input capacity max limit changed from 10 to 20 pF	
3.4.45	SDO output capacity max limit changed from 10 to 30 pF	
5	Decoupling capacicors and suppressor diode added to application circuits, figure 14 and 15	
TLE 7209-2R	**2004-jul-01**	V1.2
Previous Version:	Final Datasheet V1.1, 2004-may-25	
Section	Subjects (major changes since last revision)	
3.4.25	Added “no load” to Test Conditions	
3.4.26	Added 1.0 µsec minimum	
3.4.49	Clarified Open Load diagnostic threshold	
4	Figure 10 is depicted for low-side FETs	

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