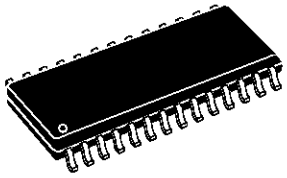
SGS-THOMSON MICROELECTRONICS

STV5730A

MULTISTANDARD ON-SCREEN DISPLAY FOR VCR, PAY-TV, SATELLITE RECEIVER

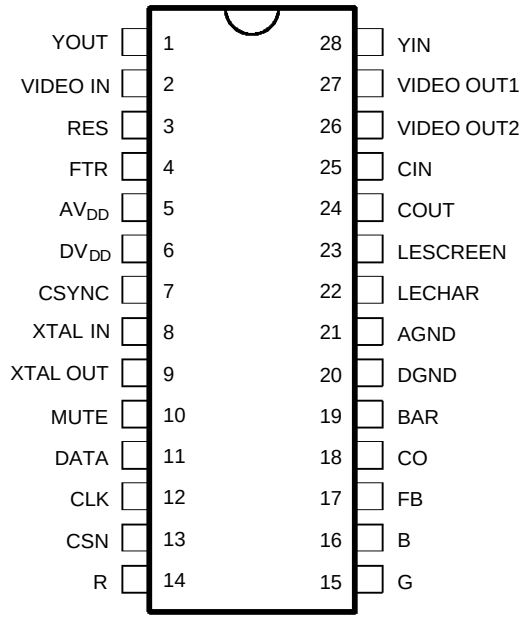
- A CHARACTER GENERATOR WITH ASCII RAM AND CHARACTER ROM :
  - 128 characters
  - 12 dots x 18 lines character composition
  - 11 rows x 28 characters page composition
- ACCURATE INTERNAL BANDGAP VOLTAGE REFERENCE
- LINE LOCKED PLL
- VIDEO TIMING GENERATOR
- INPUT CVBS CLAMP AND SYNC EXTRACTOR
- VERTICAL SYNC SEPARATOR
- INPUT CVBS SYNC RE-INSERTION
- INPUT CVBS PRESENCE DETECTOR
- PAL/NTSC CHROMA ENCODER
- DEDICATED PINS FOR LUMA AND CHROMA EXTERNAL FILTERING
- GAIN ON CVBS OUTPUT FOR EITHER 0dB OR 6dB CAPABILITY
- MULTISTANDARD TRANSLUCENT MIXED MODE
- OPAQUE MIXED MODE
- NORMAL FULL PAGE MODE
- VIDEO FULL PAGE MODE
- SUITABLE FOR S-VHS
- THREE DIFFERENT MARKERS CAN BE GENERATED SIMULTANEOUSLY
- THREE WIRE SERIAL INTERFACE FOR MICROPROCESSOR CONTROL



SO28
(Plastic Micropackage)

ORDER CODE : STV5730A

PIN CONNECTIONS



5730A-01.EPS

DESCRIPTION

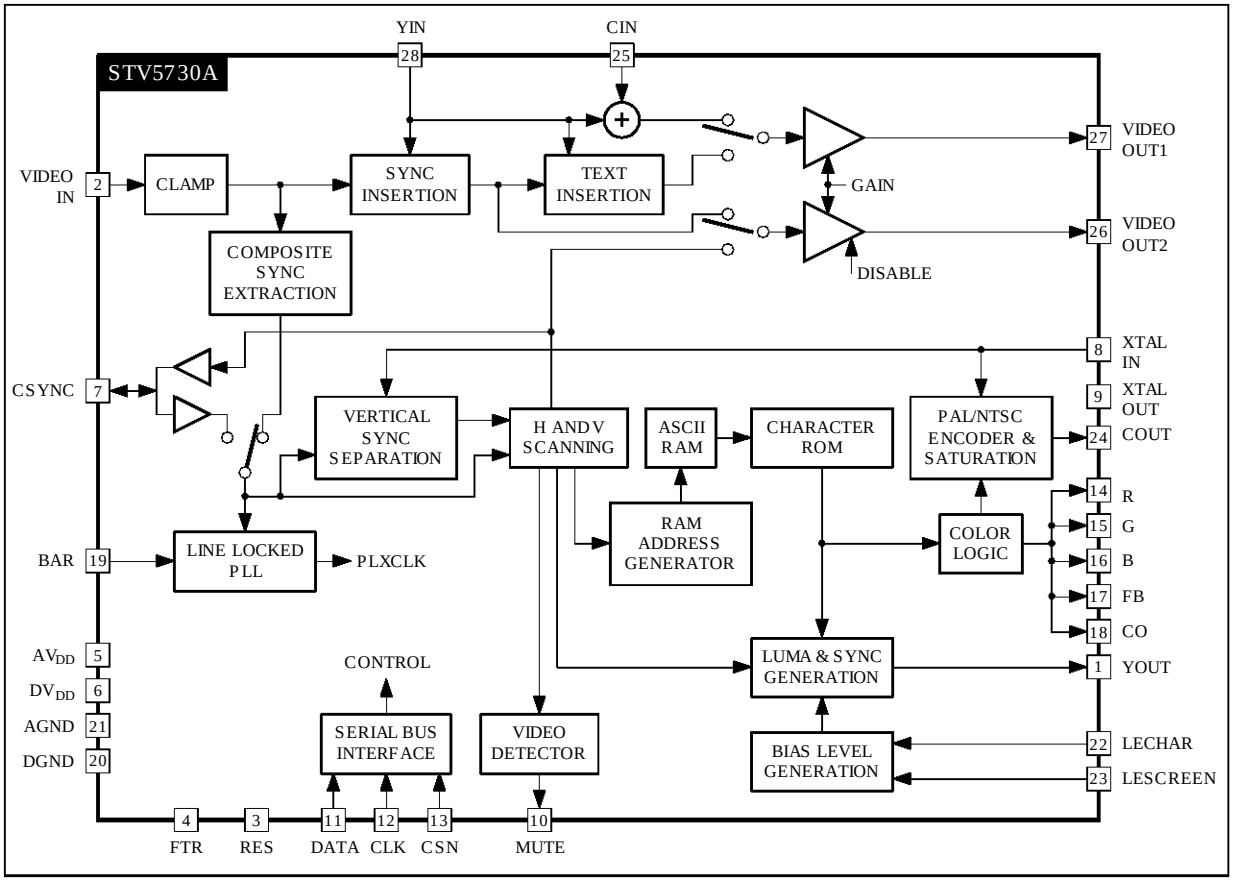
The STV5730A IC is intended to be used in VCR, Satellite receiver and PAY-TV systems for CVBS or R/G/B text/graphics insertion.

PIN DESCRIPTION

N°	Name	Type	Description
1	YOUT	Analog Output	This pin outputs the luma to allow the user to notch filter it. This pin may be connected to the YIN input for minimum cost applications.
2	VIDEO IN	Analog Input	This is the CVBS input. An external capacitor is needed for clamp operation. The STV5730A extracts the sync from this signal when the C7 control bit is set.
3	RES	Analog Pin	it must be tied to an external resistor to control the PLL f0 frequency.
4	FTR	Analog Pin	it must be tied to the line PLL loop filter.
5	AV_{DD}	Supply Pin	5V analog supply pin.
6	DV_{DD}	Supply Pin	5V digital supply pin.
7	CSYNC	Bidirectional Pin	This pin inputs the mixed mode composite sync when the C7 control bit is cleared. It outputs the video in extracted sync when the C7 control bit is set.
8	XTAL IN	Digital Input	This is the 4*fsc quartz input. The quartz may be started or stopped under control of dedicated serial interface messages. Alternatively, a 4fsc clock can be input directly. The stop message must not be used in this case.
9	XTAL OUT	Digital Output	This is the 4*fsc quartz output. The quartz may be started or stopped under control of dedicated serial interface messages.
10	MUTE	Digital Output	This pin indicates if the CVBS input signal is present on VIDEO IN input pin. It is forced low if the M2 mode bit is cleared.
11	DATA	Digital Input	This is the serial interface data input.
12	CLK	Digital Input	This is the serial interface clock input.
13	CSN	Digital Input	This is the serial interface chip select input.
14	R	Digital Output	This is the Red signal output. It is forced low during the horizontal and vertical blanking intervals.
15	G	Digital Output	This is the Green signal output. It is forced low during the horizontal and vertical blanking intervals.
16	B	Digital Output	This is the Blue signal output. It is forced low during the horizontal and vertical blanking intervals.
17	FB	Digital Output	This is the fast blanking output. It is delivered to control an external R/G/B switch for R/G/B or TV applications.
18	CO	Digital Output	This is the character activity output. It indicates if a character foreground is being displayed, and can be used to control its intensity.
19	BAR	Digital Input	This input forces the PLL in free run mode when active. It is enabled if the M0 mode bit is set.
20	DGND	Supply Pin	0V digital ground.
21	AGND	Supply Pin	0V analog ground.
22	LECHAR	Analog Input	This pin determines the character intensity level in external bias mode (ie when the C10 control bit is set). This level must be defined relative to the internal black reference. A variable luminance signal may be entered. To be grounded if not used.
23	LESCREEN	Analog Input	This pin determines the screen intensity level in external bias mode (ie when the C10 control bit is set). This level must be defined relative to the internal black reference. A variable luminance signal may be entered. To be grounded if not used.
24	COUT	Analog Output	This pin outputs the full page mode chroma for external filtering (and attenuation if necessary). This pin may be connected to CIN for minimum cost applications.
25	CIN	Analog Input	This pin inputs the filtered chroma.
26	VIDEO OUT2	Analog Output	If the M7 mode bit is cleared : this pin is a CVBS output that delivers the VIDEO IN signal. The sync is re-inserted if the M4 mode bit is set. The output amplitude may be either 0dB or +6dB according to the M5 mode bit. If the M7 mode bit is set : It outputs the currently active synchronism. The signal amplitude is controlled by the M5 mode bit. If the M8 mode bit is cleared : VIDEO OUT2 is in high impedance state.
27	VIDEO OUT1	Analog Output	This is a CVBS output. It delivers the VIDEO IN + text in mixed mode and the CVBS text in full page mode. The output signal amplitude may be either 0dB or 6dB according to the M5 mode bit. The sync is re inserted if the M4 mode bit is set.
28	YIN	Analog Input	This pin inputs the notch filtered luma.

5730A-01.TBL

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
DV_{DD}	Digital Supply Voltage	7	V
AV_{DD}	Analog Supply Voltage	7	V
T_j	Junction Temperature	150	^oC

5730A-02.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	Typ.	70	$^oC/W$

5730A-03.TBL

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, AV_{DD} = DV_{DD} = 5V, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
DV_{DD}	Digital Supply Voltage DV_{DD} - DGND	4.75	5.0	5.25	V
DI_{DD}	Digital Supply Current			10	mA
AV_{DD}	Analog Supply Voltage	4.75	5.0	5.25	V
AI_{DD}	Analog Supply Current			25	mA
AV_{DD}-DV_{DD}	Analog to Digital Supply Voltage Difference	-200	0	200	mV
DV_{OH}	Digital Output Voltage High Level (I_{LOAD} = -1mA)	DV_{DD} - 0.5			V
DV_{OL}	Digital Output Voltage Low Level (I_{LOAD} = +1mA)			DGND + 0.5	V
DV_{IH}	Digital Input Voltage High Level	0.75 x (DV_{DD} - DGND)			V
DV_{IL}	Digital Input Voltage Low Level			0.15 x (DV_{DD} - DGND)	V
DI_{IH}	Digital Input Current High Level			1	µA
DI_{IL}	Digital Input Current Low Level	-1			µA
BW	Bandwidth at pins : VIDEO IN, VIDEO OUT1, VIDEO OUT2, CIN, YIN, YOUT, COUT		8.0		MHz
VIDEO IN (Pin 2)					
V_{SYNCIN}	Sync Pulse Range	100		650	mV
V_{CL}	Clamp Voltage	1.10	1.30	1.50	V
C_{IN}	External Capacitor		2.2		µF
VIDEO OUT1 (Pin 27)					
V_{OUT1}	Output Dynamic Range	2.0		4.4	V
	Black Level Voltage	2.20	2.45	2.70	V
C_{L1}	Output Capacitor Load			20	pF
R_{L1}	Output Resistor Load			10	kΩ
Z_{OUT1}	Output Impedance		250		Ω
VIDEO OUT2 (Pin 26)					
V_{OUT2}	Output Dynamic Range	2.0		4.4	V
	Black Level Voltage	2.20	2.45	2.70	V
C_{L2}	Output Capacitor Load			20	pF
R_{L2}	Output Resistor Load			10	kΩ
Z_{OUT2}	Output Impedance		250		Ω
GAIN (Pins 26- 27)					
	Gain Dispersion 0dB 6dB	-1 5	0 6	+1 7	dB dB
CIN (Pin 25)					
C_{CIN}	Input Capacitance		0.5		pF
R_{CIN}	Input Resistance		50		kΩ
YIN (Pin 28)					
C_{YIN}	Input Capacitance		0.5		pF
YOUT (Pin 1)					
V_{YOUT}	Output Dynamic Range	0.5		3.5	V
C_{LYOUT}	Output Capacitor Load			15	pF
R_{LYOUT}	Output Resistor Load			10	kΩ
COUT (Pin 24)					
V_{COUT}	Output Dynamic Range	0.5		3.5	V
C_{LCOUT}	Output Capacitor Load			15	pF
R_{LCOUT}	Output Resistor Load			10	kΩ

5730A-04.TBL

ELECTRICAL CHARACTERISTICS

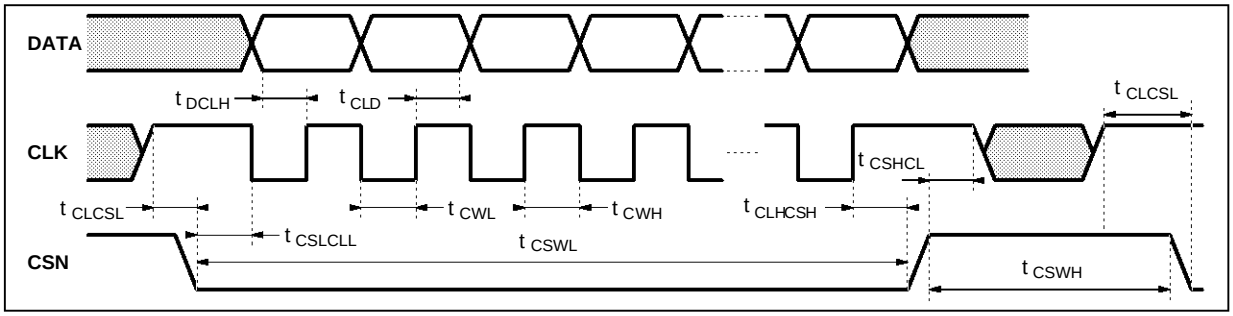
(T_A = 0°C to 70°C, AV_{DD} = DV_{DD} = 5V, unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
LESCREEN (Pin 23)					
V_{LESCR}	Input Level	1.0		3.0	V
LECHAR (Pin 22)					
V_{LECH}	Input Level	1.0		3.0	V
INTERNAL SIGNAL LEVELS (Pins 1- 24)					
V_{SYNC}	Internal Sync Level		0.95		V
V_{BLACK}	Internal Black Level	1.1	1.25	1.4	V
V_{SCREEN}	Internal LESCREEN		1.4		V
V_{CHAR}	Internal LECHAR		1.9		V
$\Delta V1$	Difference Level between Black and Sync Level	250	300	350	mV
$\Delta V2$	Difference Level between Screen and Black Level	100	150	200	mV
$\Delta V3$	Difference Level between Char. and Screen Level	450	515	580	mV
$V_{BURSTPP}$	Burst Amplitude		320		mV_{PP}
V_{CH1PP} V_{CH2PP}	Chroma Amplitude for blue or yellow colors for red, magenta, green or cyan colors		420 580		mV_{PP} mV_{PP}
BUS (Pins 11- 12 - 13)					
f_{CLK}	CLK Frequency Range	0		2	MHz
t_{CWL}	CLK Width Low	200			ns
t_{CWH}	CLK Width High	200			ns
t_{CSWL}	CSN Width Low	maxHZ* x 4			µs
t_{CSWH}	CSN Width High	maxHZ* x 4			µs
t_{DCLH}	DATA Valid to CLK High	100			ns
t_{CLD}	CLK High to DATA Unvalid	100			ns
t_{CLCSL}	CLK Valid to CSN Low	100			ns
t_{CSLCLL}	CSN Low to CLK Low	100			ns
t_{CLHCSH}	CLK High to CSN High	100			ns
t_{CSHCL}	CSN High to CLK Unvalid	100			ns

5730A-05.TBL

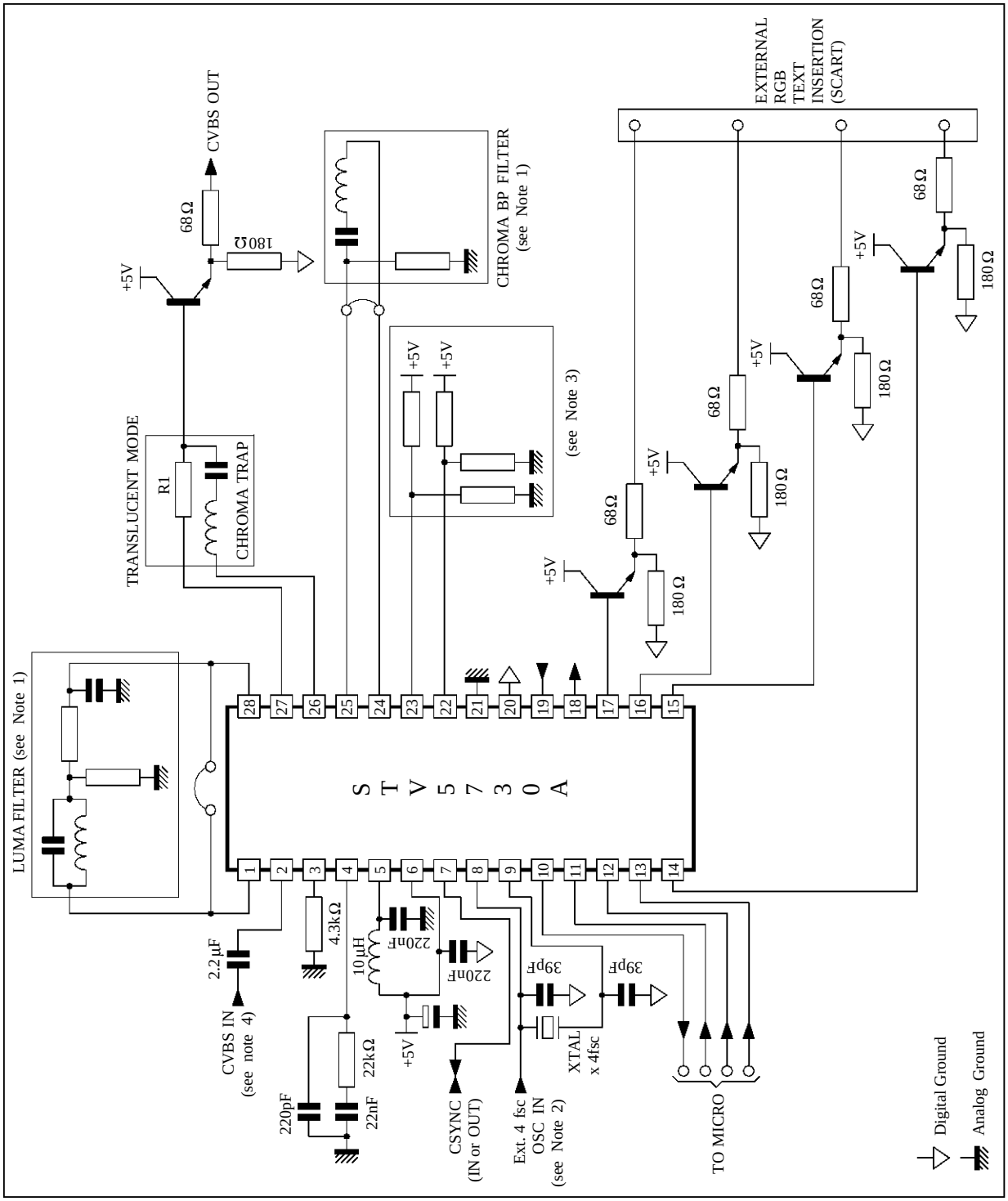
* maxHZ is the maximum horizontal zoom factor that is used

Figure 1



5730A-03.EPS

TYPICAL PAL/NTSC/SECAM APPLICATION



Notes : 1. Optional filter. For low cost applications, short circuit.
2. The 4fsc (17.734MHz PAL, 14.318MHz NTSC) crystal may be ommited if this signal is already available in a system.
3. External bias level can be set by resistor ratio as required. The level at pins LECHAR and LESCREEN must not exceed 3.0 Vdc.
4. Output impedance of the driving stage should be less than 300Ω.

FUNCTIONAL DESCRIPTION

The STV5730A operates in "mixed mode" or "full page mode" :

- Mixed mode : the device is line locked to the incoming CVBS signal. The text is superimposed over the CVBS input either in B&W or translucent. It may also be superimposed in color by using the R/G/B outputs.
- Full page mode : the device generates a colored PAL or NTSC CVBS output and simultaneous R/G/B outputs. Both "normal full page" and "video full page" modes are supported by the STV5730A. In the "normal full page" the screen background is uniformely colored, while the "video full page" mode permits to display the unlocked VIDEO IN signal in the screen background area.

It performs the following text features :

- Page composition : 11 rows X 28 characters
- Number of displayed characters : 308 (max)
- Character composition : 12 dots X 18 lines
- ROM character set : 128 user definable characters
- Screen display positions : 58 horizontal positions, 63 vertical positions
- Row position offset , each row : Xoffset from 0 to +15, Yoffset from -17 to +17
- Display enable : each row or page
- Character color : 1 out of 8, each character
- Character background color : 1 out of 8, character and page enabled or set identical to character color
- Character border color : 1 out of 8, row enabled or set identical to character color
- Page background color : 1 out of 8
- Zoom : 3 independant zoom factors for rows 0, 1 to 9 and 10.
- Zoom factors : four independant X and Y zoom factors
- Blink : character and page enabled
- Blink frequency : 0.5 or 1.0 second
- Blink duty cycle : 0.25, 0.5 or 0.75

1 - THE INTERNAL RAM BUFFER

It stores the page (i.e. the text definition) and the row attributes.

1.1 - Page

The page includes 11 row buffers, numbered from 0 to 10. Each row buffer includes 28 characters, numbered from 0 to 27. The characters may be written one by one by the microprocessor for random access. They also may be written sequentially, starting with any character address.

1.2 - Character Format and Attributes

11	10	9	8	7	6	0
BE	R	G	B	BK	CHARACTER CODE	

CHARACTER CODE : 1 character out of 128 from the character ROM

BK : BK=0 : character blink disabled
BK=1 : character blink enabled

R/G/B : Character color :

000	black
001	blue
010	green
011	cyan
100	red
101	magenta
110	yellow
111	white

BE : BE=0 : the character background is disabled
BE=1 : the character background is enabled

FUNCTIONAL DESCRIPTION (continued)

1.3 - Row Attributes

There are 11 row attributes, numbered from 0 to 10. They may be written one by one or sequentially.

The row attribute format is as follows :

11 8	7	6	5 0
HPOS OFFSET	RE	FBE	VPOS OFFSET

VPOS OFFSET : the MSB is the sign bit (0 : positive, 1 : negative). If the offset is positive (from 0 to +17), then the corresponding number of lines are added on top of the row (i.e. it moves downwards). These extra lines are colored according to the character background rules. If the offset is negative (from -1 to -17), then the corresponding number of lines are subtracted from the display of the row.

FBE : FBE=0 : the characters are displayed without border
FBE=1 : the characters are displayed with border

RE : RE=0 : the characters of the row are not displayed.
They are replaced by the page background color.
RE=1 : the characters of the row are displayed.

HPOS OFFSET : The display of the row is shifted to the right by the corresponding number of pixels (from 0 to 15).

1.4 - The Control Registers

There are 5 registers for microprocessor control. They can be written individually or sequentially :

- the ZOOM register address : 12
- the COLOR register 13
- the CONTROL register 14
- the POSITION register 15
- the MODE register 16

1.4.1 - Zoom Register

11	10	9	8	7	6	5	4	3	2	1	0
VZb1	VZb0	HZb1	HZb0	VZm1	VZm0	HZm1	HZm0	VZt1	VZt0	HZt1	HZt0

HZt[1:0] : Top row horizontal zoom factor (ie row 0)
HZt[1:0] = 00 : 1 pixel per character dot
01 : 2 pixels per character dot
10 : 3 pixels per character dot
11 : 4 pixels per character dot

VZt[1:0] : Top row vertical zoom factor
VZt[1:0] = 00 : 1 pixel per character line
01 : 2 pixels per character line
10 : 3 pixels per character line
11 : 4 pixels per character line

HZm[1:0] : Same as HZt[1:0], for middle rows (ie rows 1 to 9)

VZm[1:0] : Same as VZt[1:0], for middle rows

HZb[1:0] : Same as HZt[1:0], for bottom row (ie row 10)

VZb[1:0] : Same as VZt[1:0], for bottom row

The output of this register is synchronized by the horizontal synchronism. The RESET message clears this register.

FUNCTIONAL DESCRIPTION (continued)

1.4.2 - Color Register (page attributes)

11	10	9	8	7	6				2	1	0
R	G	B	R	G	B	//	//	//	R	G	B
	SBC			FBC						BCC	

SBC : screen background color
FBC : character border color
BCC : character background color

The output of this register is synchronized by the horizontal synchronism.

1.4.3 - Control Register

11	10	9	8	7	6	5	4	3	2	1	0
C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

C0 : C0 = 0 : mixed mode
C0 = 1 : full page mode

C1 : C1 = 0 : the character background is controlled by BE (see character word description)
C1 = 1 : all displayed character backgrounds are disabled

C2 : C2 = 0 : display off
C2 = 1 : display on

C3 : C3 = 0 : the characters are colored according to the character attribute and the color register values (i.e. CBACKG and CBORD)
C3 = 1 : the character foreground, border and background colors are all set to the character attribute value (see paragraph 1.2). This option is mainly intended for full page mode, CVBS or Y/C output

C4 : C4 = 0 : 1.0 second blinking period
C4 = 1 : 0.5 second blinking period

C[6:5] : C[6:5] = 00 : blinking off
01 : 0.75 blinking duty cycle
10 : 0.5 blinking duty cycle
11 : 0.25 blinking duty cycle

C7 : C7 = 0 an external input composite sync is taken from the CSYNC pin
C7 = 1 the sync is extracted by the STV5730A.The currently active sync is output on the CSYNC pin

C8 : C8 = 0 : the standard is NTSC, 60Hz
C8 = 1 : the standard is PAL or SECAM with M6 = 0, 50Hz

C9 : C9 = 0 : character color encoding is disabled
C9 = 1 : character color encoding is enabled

C10 : C10 = 0 : the luminance levels are generated internally
C10 = 1 : the luminance levels are provided by the LESCREEN and LECHAR input pins.

C11 : C11 = 0 : Video Full Page Mode. A stable full page mode text is displayed while the screen background is the unlocked video input signal.
C11 = 1 : Normal full page mode is active.

The output of this register is synchronized by the horizontal sync (except C7). The RESET message clears this register.

FUNCTIONAL DESCRIPTION (continued)

1.4.4 - Position Register

11	6	5	0
VERTICAL POSITION		HORIZONTAL POSITION	

HORIZONTAL POSITION Any value from 6 to 63
VERTICAL POSITION Any value from 1 to 63

1.4.5 - Mode Register

11	10	9	8	7	6	5	4	3	2	1	0
M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0

M0 : M0 = 0 : the BAR pin is disabled
M0 = 1 : the BAR pin has an action on the line PLL
M1 : M1 = 0 : the missing sync pulses are not detected
M1 = 1 : the missing sync pulses are detected
M2 : M2 = 0 : the MUTE pin is forced to 0
M2 = 1 : the MUTE pin delivers the internal MUTE signal
M3 : M3 = 0 : the MUTE time constant is 8 lines
M3 = 1 : the MUTE time constant is 32 lines
M4 : M4 = 0 : the sync is not re-inserted
M4 = 1 : the sync is re-inserted for improved text stability
M5 : M5 = 0 : the gain of pins VIDEO OUT1 & VIDEO OUT2 is 0dB.
M5 = 1 : the gain of pins VIDEO OUT1 & VIDEO OUT2 is 6dB.
M6 : M6 = 0 : the color encoder is enabled (PAL or NTSC)
M6 = 1 : the color encoder is disabled (B&W or SECAM)
M7 : M7 = 0 : the VIDEO OUT2 pin outputs the VIDEO IN signal
M7 = 1 : the VIDEO OUT2 pin outputs the composite sync
M8 : M8 = 0 : the VIDEO OUT2 pin is in low impedance state
M8 = 1 : the VIDEO OUT2 pin is in high impedance state
M9 : M9 = 0 : Normal mode
M9 = 1 : CSYNC Pin outputs the burst gate, BAR Pin outputs the VSYNC (see Note)
M10 : M10 = 0 : No delay compensation
M10 = 1 : It enables the delay compensation of the internal sync extractor.
M11 : M11 = 0 : The mute signal output is synchronized on vertical sync in order to limit its transitions.
M11 = 1 : The mute signal is not synchronized on vertical sync thus accelerating the VIDEO IN presence detection (useful in full page mode).

Note : This mode overides the normal functions of Pins CSYNC and BAR.

FUNCTIONAL DESCRIPTION (continued)

2 - THE MICROPROCESSOR SERIAL INTERFACE

The STV5730A is down loaded by the microprocessor through a three wire serial interface : DATA, CLK, CSN. The CLK and CSN signals are internally ORed in order to validate the transfer when the STV5730A is chip selected only (i.e. CSN = 0). The CSN rising edge validates the internal data transfer.

2.1 - Message Formats (see Figure 2)

16-bit, 8-bit and 0-bit formats are available. The 8-bit and 0-bit message formats may be useful to speed up the STV5730A down loading.

15			12	11	8	7	6	5	4	0	
0	0	0	0	BUF[11:8]		STRU[7:6]		0	DEPL[4:0]		ADDRESS

This 16-bit address message loads the serial interface write pointer. This address is incremented after each data message.

15			12	11	0	
0	0	0	1	DATA[11:0]		DATA

This 16-bit data message writes the data at the location indicated by the write pointer.

7	0	
DATA[7:0]		DATA

This 8-bit data message writes the data at the location indicated by the write pointer. The 4-bit data MSB is copied from the last previous 16-bit data message.

The 0-bit data message writes a data at the location indicated by the write pointer. The last data is used from the previous 8-bit or 16-bit data message.

15			12	11	0	
0	0	1	0	don't care		CONTROL

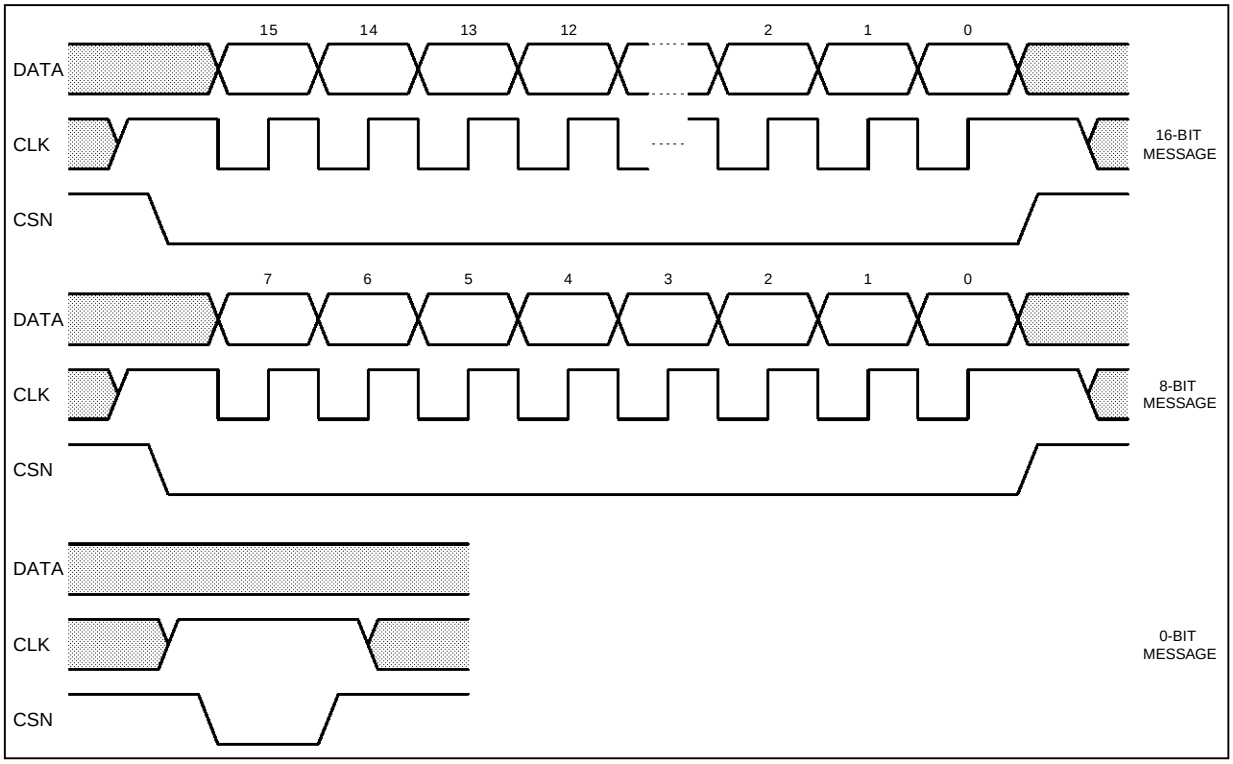
This 16-bit control message stops the 4*fsc quartz oscillator.

15			12	11	0	
0	0	1	1	don't care		CONTROL

This 16-bit control message resets the circuit and starts the 4*fsc quartz oscillator. This message should not be used if an external 4 x fsc clock is used instead of the quartz. It is mandatory that reset operation is as described in paragraph 2.3.

FUNCTIONAL DESCRIPTION (continued)

Figure 2



2.2 - The Write Pointer

As described in the "message format" paragraph, an address consists of three fields : STRU[7:6], BUF[11:8], DEPL[4:0].

The STRU[7:6] field indicates whether it is a PAGE address or a ROW ATTRIBUTE / REGISTER address. It also determines the address incrementation scheme.

- STRU[7:6] = 00 :
  It is a PAGE address. BUF provides the row number (from 0 to 10) and DEPL provides the character number (from 0 to 27). DEPL is incremented after each data message. When the write of a row is completed, the write pointer is automatically set to the next row first character.
- STRU[7:6] = 01 :
  It is also a PAGE address but the incrementation scheme is a bit different : when the write of a row is completed, the write pointer is automatically set to the first character of the same row.
- STRU[7:6] = 11 :
  It is a row attribute or a register address. The BUF field must be set to 0000 and the DEPL field is incremented after each data access.

2.2.1 - Address Map

PAGE : ROW 0 : STRU[7:6] = 0 or 1 - BUF[11:8] = 0 - DEPL[4:0] from 0 to 27
ROW 1 : STRU[7:6] = 0 or 1 - BUF[11:8] = 1 - DEPL[4:0] from 0 to 27
..... : ....
ROW 10 : STRU[7:6] = 0 or 1 - BUF[11:8] = 10 - DEPL[3:0] from 0 t0 27

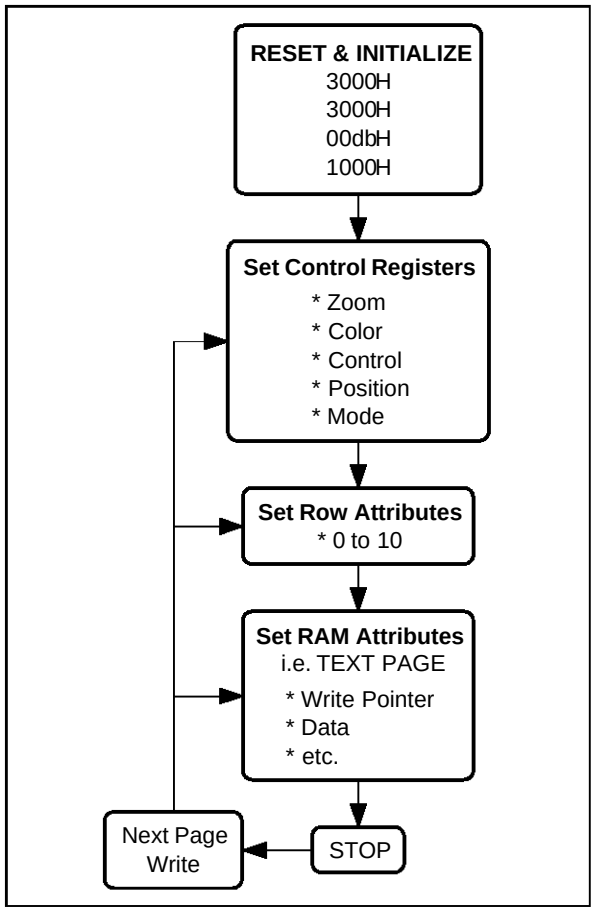
ROW ATTRIBUTES : STRU[7:6] = 11 - BUF[11:8] = 0 - DEPL[4:0] from 0 to 10

REGISTERS : STRU[7:6] = 11 - BUF[11:8] = 0
DEPL[4:0] = 12 for ZOOM register, 13 for COLOR register,
14 for CONTROL register, 15 for POSITION register,
16 for MODE register

FUNCTIONAL DESCRIPTION (continued)

2.3 - Initialization and Down-loading Sequence
It is important that the STV5730A is correctly reset and initialized after the circuit is powered prior to any writing. This routine is shown in Figure 3. The two initialization bytes (00db 1000) must procede the reset instruction (x2) every time it is transmitted.

Figure 3



3 - THE LINE LOCKED PLL

The PLL frequency is 504 * f_H = 7.875MHz.

3.1 - Mixed Mode Behavior
In mixed mode, the internal PLL is line locked to the incoming CVBS signal. The sync is either extracted by the STV5730A (if C7 control bit is set) or provided by the application in a composite form on the CSYNC pin (if C7 control bit is cleared). The STV5730A separates the vertical sync from the composite synchronism.

The STV5730A PLL features built-in protection mechanisms against missing and parasitic horizontal sync pulses. These mechanisms are activated when the loop is locked.

The STV5730A PLL is also insensitive to the head switching disturbing the synchronism in VTR applications (playback).

The missing pulses may be detected. The M1 mode bit enables the detection.

In addition, the BAR input pin is available to enter a signal that forces the PLL in free-run mode. This capability may be used for search mode in VTRs, to improve the loop robustness against the noise bar. The BAR input is enabled by the M0 mode bit.

3.2 - Horizontal Sync Re-insertion
This mechanism is of interest in mixed mode, to cancel the text horizontal jitter when the sync signal is too bad. It is activated by the M4 mode bit and must be turned off in full page mode.

The active part of the line is protected against parasitic sync insertion. The modified sync is active on all output pins (ie CSYNC if C7 is set, VIDEO OUT1, VIDEO OUT2).

A jitter greater than 0.42usec cannot be cancelled.

3.3 - Full Page Mode Behavior
In this case, the PLL is locked on an internal 64usec reference derived from the 4*fsc quartz.

The STV5730A generates a non interlace output.

4 - MUTE

The STV5730A monitors the sync to determine whether it is a stable signal or not.

MUTE = high : no stable signal
MUTE = low : stable CVBS input signal

The MUTE search time constant may be either 8 lines or 32 lines, according to the M3 mode bit.
The signal that is delivered to the MUTE output pin is synchronized on the vertical sync if M11 is cleared. It is forced low if the M2 mode bit is low. This signal may be monitored by the microprocessor to switch the STV5730A from mixed mode to full page mode and vice versa (using the C0 control bit).

5 - THE LUMA GENERATOR

The luma signal is generated by the STV5730A from timing information created by the character and video timing generators and voltage levels created by the internal bias level generator or entered on the LESCREEN and LECHAR pins (as selected by the C10 control bit).

The luma signal is output on the YOUT pin to allow the user to notch filter it. It is then re-input on the YIN pin. YOUT and YIN may be connected together for minimal cost applications.

FUNCTIONAL DESCRIPTION (continued)

5.1 - Internal Bias Mode

This mode is intended for minimal cost applications. C10 must be cleared.
The luma levels of the OSD output signal are as follows :

- LEBLACK : black level
  nominal value : 1.25V
- LESYNC : sync level
  nominal value : LEBLACK - 300mV
- LESCREEN : page background level
  nominal value : LEBLACK + 150mV
- LECHAR : character level
  nominal value : LEBLACK + 650mV

LEBLACK is also used to clamp the VIDEO IN signal and to create the character border.

5.2 - External Bias Mode

This mode is intended to give more flexibility to the user. C10 must be set.
The LESCREEN and LECHAR levels may be user defined relatively to the internal LEBLACK level.
The final luma amplitude should not be greater than the peak white level.
These levels may be static or dynamic.
Dynamic levels can be easily generated by analog sum of the R/G/B and CO STV5730A outputs (a few resistors are necessary) to give grey scale character shading in the mixed mode.
C0 is useful to control the character foreground luma level.

6 - THE CHROMA GENERATOR

The STV5730A encoder operates in full page mode only. It may perform PAL or NTSC encoding according to the C8 control bit.

A 4*fsc chroma quartz crystal is necessary (fsc = 4.43MHz for PAL, 3.58MHz for NTSC).

The encoder can be turned off by the M6 mode bit for black & white or for SECAM applications.

The character encoding is controlled by the C9 control bit.

The chroma signal is output on the COUT pin for external filtering and for attenuation if necessary. It is then re-entered on the CIN pin and added to the YIN pin signal to create the final CVBS output signal.

The chroma saturation is controlled by the STV5730A :

- burst nominal amplitude : 320mV$_{PP}$
- blue or yellow colors nominal amplitude : 420mV$_{PP}$
- red, magenta, green or cyan colors nominal amplitude : 580mV$_{PP}$

7 - THE MARKERS

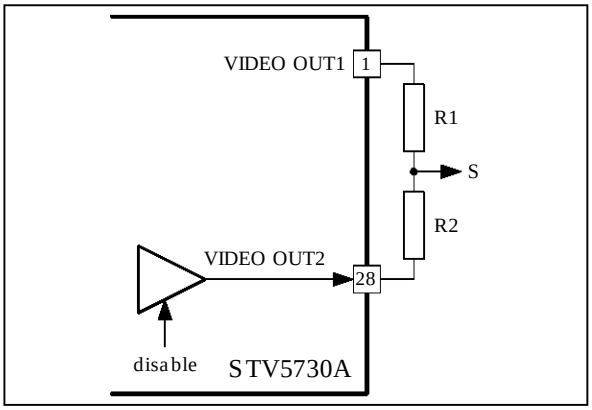
The STV5730A can generate 3 different markers that can be activated simultaneously (i.e. on the same page).

The following marker features are performed :

- Blinking character, character background off.
  The character foreground blinks (BK = 1, BE = 0 or C1 = 1).
- Not blinking character, character background on (C1 = 0, BE = 1).
- Blinking character, character background on.
  The character foreground blinks and the character background remains (BK = 1, BE = 1, C1 = 0).

8 - THE TRANSLUCENT MIXED MODE

Figure 4 : The Translucent Mixed Mode Output Configuration



The VIDEO OUT1 and VIDEO OUT2 outputs may be summed via two external resistors to create a translucent text (mixed mode). In this case, the background picture is still visible behind the text.
The background picture visibility (or level of translucence is controlled by the resistor ratio.
Another benefit from this function is to allow PAL/SECAM/NTSC multistandard applications to be built with no SECAM chroma re-insertion filter and no additional control switches.
The sum may be cancelled by setting the M8 mode bit. In this case, the VIDEO OUT2 pin is in high impedance state and the resistor network delivers VIDEO OUT1 only.

When using the resistor network, please set M8 in the following cases :

- in full page mode
- when OSD in not displayed
- to select opaque text. This allows the viewer to select by software the preferred display mode.

The DC levels of the VIDEO OUT1, VIDEO OUT2 and the sum signals are high enough to directly drive a NPN emitter follower driver (see Table 1).

FUNCTIONAL DESCRIPTION (continued)

9 - VIDEO FULL PAGE MODE

In addition to the normal full page mode in which a uniformely colored screen background is generated, the STV5730A is able to perform a "video full page mode".

Normal and video full page mode are selected by the control bit C11 (respectively set high and low).

By using the video full page mode the channel capture operation can be easily monitored on the screen since the signal at the VIDEO IN input is displayed, unlocked, in the screen background area ; the text being stable and colored, with or without colored background.

Presence detection is permanently active to keep the microcontroller informed of the input signal quality. The information is delivered by the MUTE pin.

This information can be used by the microcontroller to force the STV5730A into the mixed mode (set C0 low) when the input signal becomes good enough.

In the video full page mode, it can be usefull to set the M11 (mode register) bit high, so that the mute signal is not synchronized on the vertical sync, thus accelerating the VIDEO IN presence detection.

10 - S-VHS APPLICATION (see Figure 5)

The STV5730A can be used in S-VHS applications easily.

The Y signal must be delivered to the VIDEO IN input. The VIDEO OUT1 output then delivers a Y + text signal, whilst the VIDEO OUT2 delivers the Y input signal, provided that the CIN input is connected to a bias DC level.

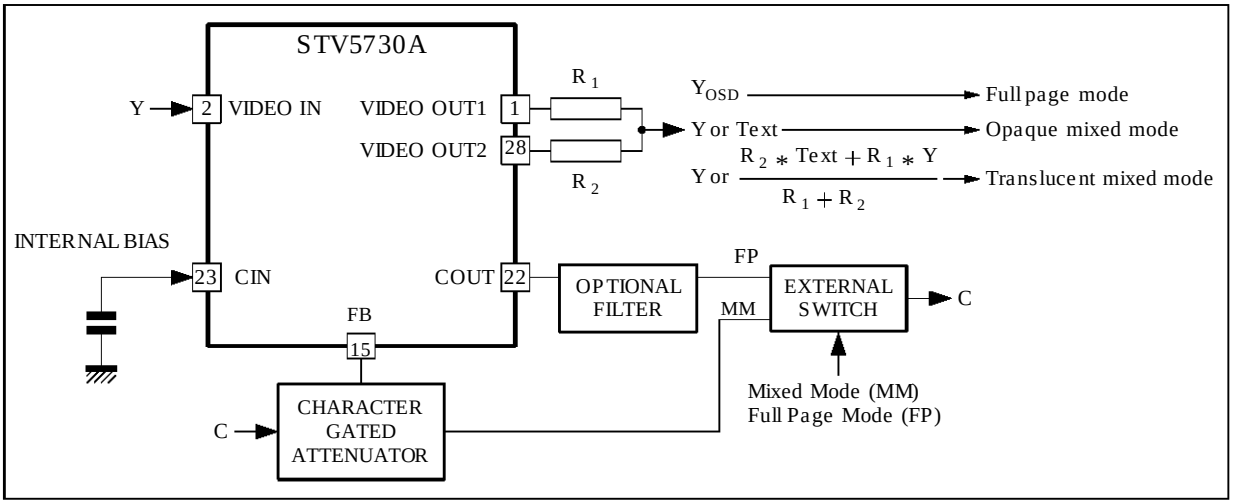
An external switch must be used to select the C signal in mixed mode or the COUT output signal in full page mode.

In mixed mode the chroma signal (C) can be externally attenuated (multistandard translucent operation) or killed (PAL/NTSC opaque operation only) during the character gate controlled by the fast blanking signal.

Table 1

	FULL PAGE PAL/NTSC	MIXED MODE	
		TRANSLUCENT PAL/NTSC/SECAM	OPAQUE PAL/NTSC
VIDEO OUT1	CVBS (OSD)	VIDEO IN or Text	VIDEO IN or Text
VIDEO OUT2	High impedance	VIDEO IN	High Impedance
S	CVBS (OSD)	VIDEO IN or $\frac{R_2 \times Text + R_1 \times VIDEO\ IN}{R_1 + R_2}$	VIDEO IN or Text

Figure 5 : S-VHS Input/Output Configuration



FUNCTIONAL DESCRIPTION (continued)

11 - THE CVBS OUTPUT PICTURE

The following tables show the picture design in CVBS output mode (VIDEOout1 analog output pin) according to :

- Blink on/off (BK character attribute & C[6:5] control bits)
- Character background on/off (BE character attribute & C1 control bit)
- Character border on/off (FBE row attribute)

11.1 - Mixed Mode

	CHARACTER FOREGROUND	CHARACTER BORDER if on	CHARACTER BORDER if off	CHARACTER BACKGROUND	PAGE BACKGROUND
Not Blinking and Char Backg off	LECHAR	LEBLACK	video		
Not Blinking and Char Backg on	LECHAR	LEBLACK	LESCREEN		video
Blinking and Char Backg off	video				
Blinking and Char Backg on	LESCREEN				video

11.2 - Full Page Mode

	CHARACTER FOREGROUND	CHARACTER BORDER if on	CHARACTER BORDER if off	CHARACTER BACKGROUND	PAGE BACKGROUND
Not Blinking and Char Backg off	LECHAR + CCHAR	LEBLACK + CBORD	LESCREEN + CSCREEN		
Not Blinking and Char Backg on	LECHAR + CCHAR	LEBLACK + CBORD	LESCREEN + CBACKG		LESCREEN + CSCREEN
Blinking and Char Backg off	LESCREEN + CSCREEN				
Blinking and Char Backg on	LESCREEN + CBACKG				LESCREEN + CSCREEN

CCHAR is a character attribute.

C3 = 0 : CSCREEN, CBACKG and CBORD are page attributes, defined by the color register.

C3 = 1 : CSCREEN is defined by the color register. CBACKG and CBORD are identical to CCHAR and thus are character attributes.

FUNCTIONAL DESCRIPTION (continued)

12 - THE R/G/B OUTPUT PICTURE

The following tables show the picture design in R/G/B output mode, according to :
- Blink on/off (BK character attribute & C[6:4] control bits)
- Character background on/off (BE character attribute & C1 control bit)
- Character border on/off (FBE row attribute)
- C3 = 0 : CSCREEN, CBACKG and CBORD are page attributes, defined by the color register.
- C3 = 1 : CSCREEN is defined by the color register. CBACKG and CBORD are identical to CCHAR and thus are character attributes. It is recommended to use CO output signal in this case.

An R/G/B external switch must be controlled by the STV5730AFB output to perform the character insertion. C0 may be used as an additional character intensity signal.

12.1 - Mixed Mode

	CHARACTER FOREGROUND	CHARACTER BORDER if on	CHARACTER BORDER if off	CHARACTER BACKGROUND	PAGE BACKGROUND
Not Blinking and Char Backg off	CCHAR	CBORD	video		
Not Blinking and Char Backg on	CCHAR	CBORD	CBACKG		video
Blinking and Char Backg off	video				
Blinking and Char Backg on	CBACKG				video

12.2 - Full Page Mode

	CHARACTER FOREGROUND	CHARACTER BORDER if on	CHARACTER BORDER if off	CHARACTER BACKGROUND	PAGE BACKGROUND
Not Blinking and Char Backg off	CCHAR	CBORD	CSCREEN		
Not Blinking and Char Backg on	CCHAR	CBORD	CBACKG		CSCREEN
Blinking and Char Backg off	CSCREEN				
Blinking and Char Backg on	CBACKG				CSCREEN

CCHAR is a character attribute.

C3 = 0 : CSCREEN, CBACKG and CBORD are page attributes, defined by the color register.

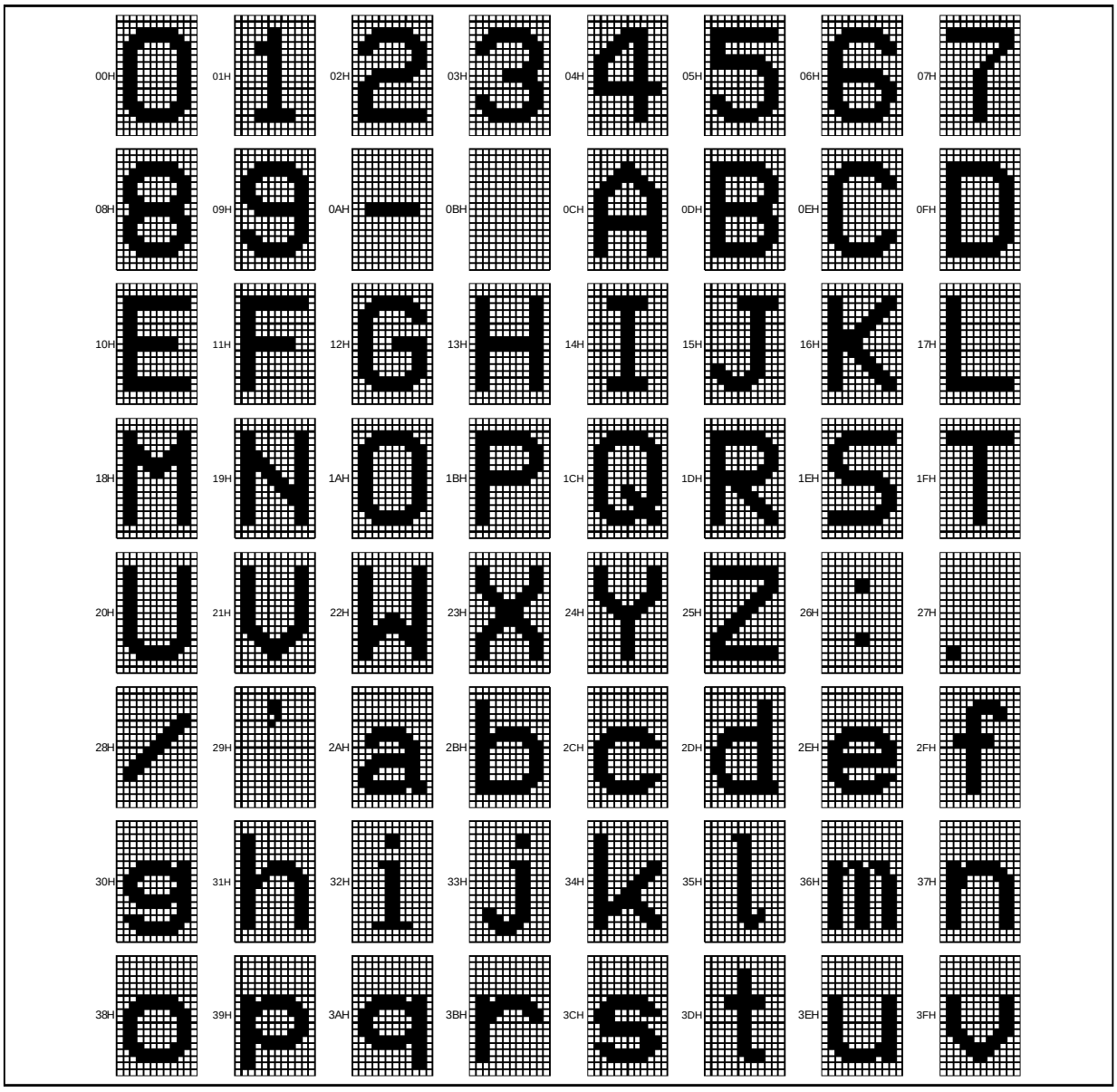
C3 = 1 : CSCREEN is defined by the color register. CBACKG and CBORD are identical to CCHAR and thus are character attributes.

FUNCTIONAL DESCRIPTION (continued)

13 - STANDARD CHARACTERS

The default device is delivered with a standard set of ROM based characters (see Figure 6).
The user can redefine the total character set (except for the character 00H (zero)).

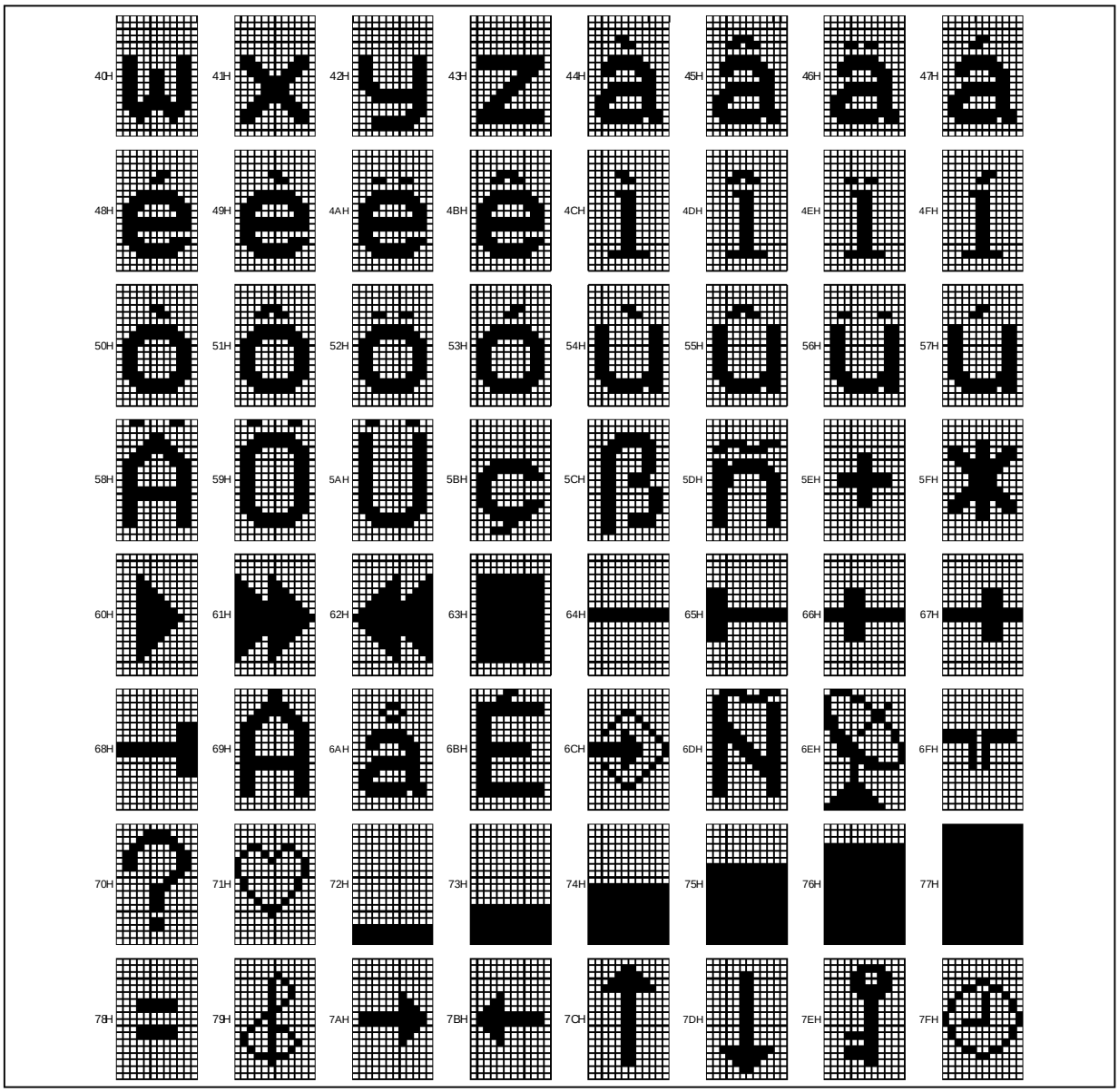
Figure 6



FUNCTIONAL DESCRIPTION (continued)

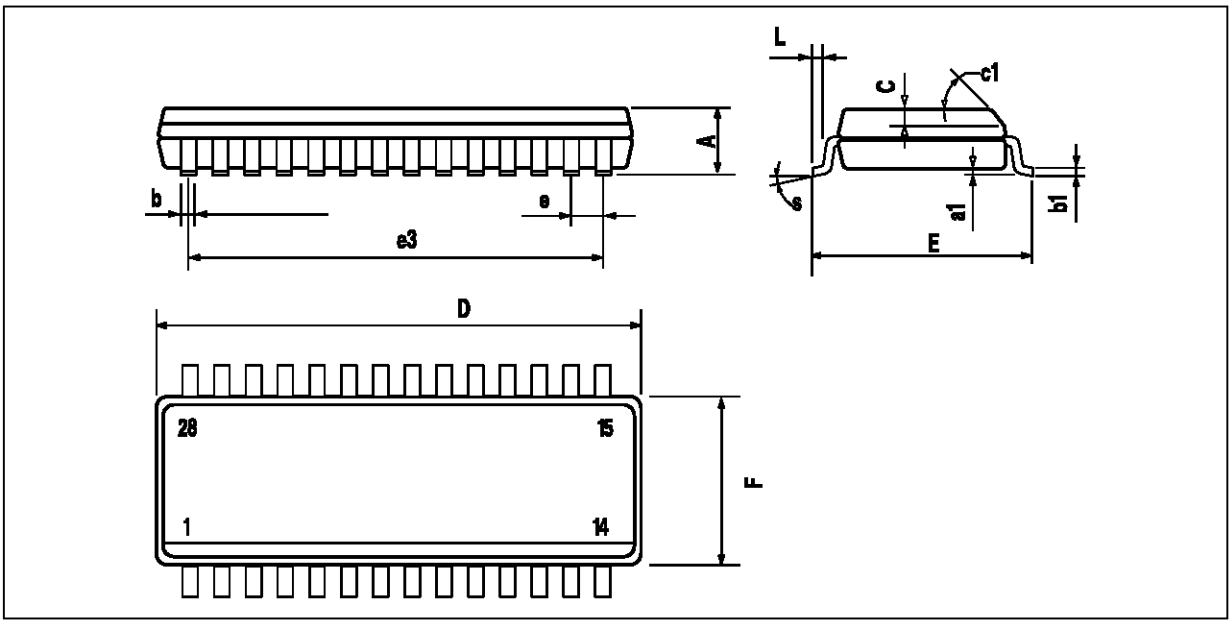
13 - STANDARD CHARACTERS (continued)

Figure 6 (continued)



PACKAGE MECHANICAL DATA

28 PINS - PLASTIC MICROPACKAGE



PM-SO28.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45^o (Typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8^o (Max.)					

SO28.TBL

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