DATA SHEET

NE/SA/SE532
LM258/358/A/2904
Low power dual operational amplifiers

Product data
Supersedes data of 2002 Jan 22

2002 Jul 12

Philips
Semiconductors

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Low power dual operational amplifiers

NE/SA/SE532/ LM258/358/A/2904

DESCRIPTION

The 532/358/LM2904 consists of two independent, high gain, internally frequency-compensated operational amplifiers internally frequency-compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages. Operation from dual power supplies is also possible, and the low power supply current drain is independent of the magnitude of the power supply voltage.

UNIQUE FEATURES

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage. The unity gain cross frequency is temperature-compensated. The input bias current is also temperature-compensated.

FEATURES

- Internally frequency-compensated for unity gain
- Large DC voltage gain: 100 dB
- Wide bandwidth (unity gain): 1 MHz (temperature-compensated)
- Wide power supply range single supply: 3 V_{DC} to 30 V_{DC}, or dual supplies: ±1.5 V_{DC} to ±15 V_{DC}
- Very low supply current drain (400 µA)—essentially independent of supply voltage (1 mW/op amp at +5 V_{DC})
- Low input biasing current: 45 nA_{DC} temperature-compensated
- Low input offset voltage: 2 mV_{DC}, and offset current: 5nA_{DC}
- Differential input voltage range equal to the power supply voltage
- Large output voltage: 0 V_{DC} to V+ 1.5 V_{DC} swing

PIN CONFIGURATION

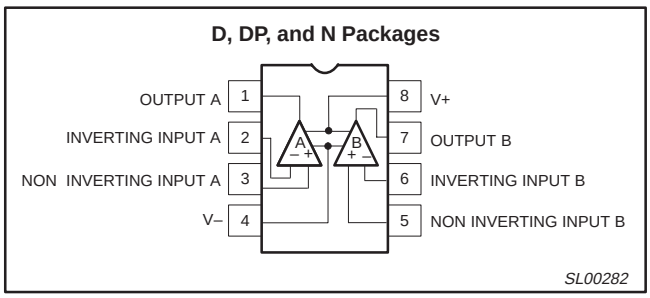


Figure 1. Pin configuration.

EQUIVALENT CIRCUIT

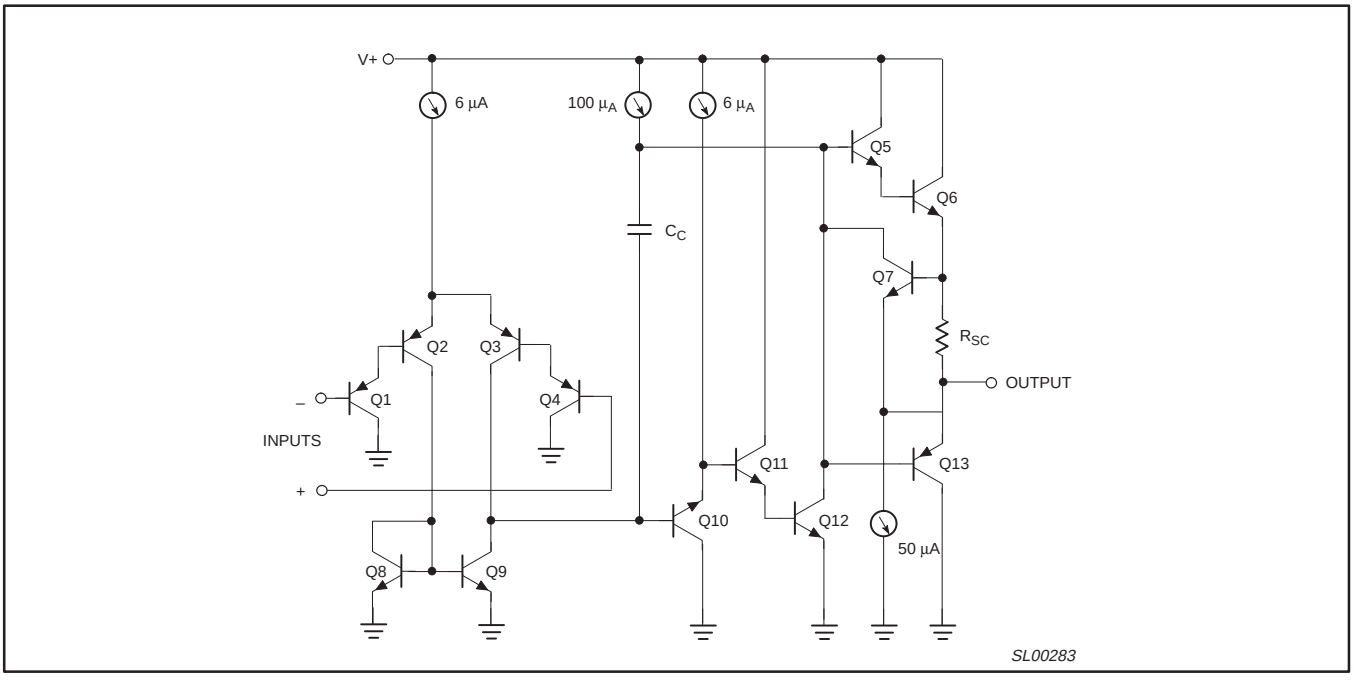


Figure 2. Equivalent circuit.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	0 °C to +70 °C	NE532D	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	0 °C to +70 °C	NE532N	SOT97-1
8-Pin Plastic Small Outline (SO) Package	–40 °C to +85 °C	SA532D	SOT96-1
8-Pin Plastic Small Outline (SO) Package	–40 °C to +125 °C	LM2904D	SOT96-1
8-Pin Plastic Thin Shrink Small Outline Package (TSSOP)	–40 °C to +125 °C	LM2904DP	SOT505-1
8-Pin Plastic Dual In-Line Package (DIP)	–40 °C to +125 °C	LM2904N	SOT97-1
8-Pin Plastic Small Outline (SO) Package	–25 °C to +125 °C	LM258D	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	–25 °C to +125 °C	LM258N	SOT97-1
8-Pin Plastic Small Outline (SO) Package	0 °C to +70 °C	LM358D	SOT96-1
8-Pin Plastic Thin Shrink Small Outline Package (TSSOP)	0 °C to +70 °C	LM358DP	SOT505-1
8-Pin Plastic Dual In-Line Package (DIP)	0 °C to +70 °C	LM358N	SOT97-1
8-Pin Plastic Small Outline (SO) Package	0 °C to +70 °C	LM358AD	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	0 °C to +70 °C	LM358AN	SOT97-1
8-Pin Plastic Dual In-Line Package (DIP)	–55 °C to +125 °C	SE532N	SOT97-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage, V+	32 or ±16	V_{DC}
	Differential input voltage	32	V_{DC}
V_{IN}	Input voltage	–0.3 to +32	V_{DC}
P_D	Maximum power dissipation T_{amb} = 25 °C (Still air)[1] N package D package DP package	 1160 780 714	 mW mW mW
	Output short-circuit to GND[2] V+ < 15 V_{DC} and T_{amb} = 25 °C	 Continuous	
T_{amb}	Operating ambient temperature range NE532/LM358/LM358A LM258 LM2904 SA532 SE532	 0 to +70 –25 to +85 –40 to +125 –40 to +85 –55 to +125	 °C °C °C °C °C
T_{stg}	Storage temperature range	–65 to +150	°C
T_{sld}	Lead soldering temperature (10 sec max)	230	°C

NOTE:

1. Derate above 25 °C, at the following rates:
   N package at 9.3 mW/°C
   D package at 6.2 mW/°C
   DP package at 5.72 mW/°C
2. Short-circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of V+. At values of supply voltage in excess of +15 V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.

DC ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C; V+ = +5 V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE532, LM258			NE/SA532/ LM358/LM2904			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage[1]	R_S = 0 Ω		±2	±5		±2	±7	mV
		R_S = 0 Ω; over temp.			±7			±9	mV
V_{OS}	Drift	R_S = 0 Ω; over temp.		7			7		μV/°C
I_{OS}	Offset current	$I_{IN(+)} - I_{IN(-)}$		±3	±30		±5	±50	nA
		Over temp.			±100			±150	nA
I_{OS}	Drift	Over temp.		10			10		pA/°C
I_{BIAS}	Input current[2]	$I_{IN(+)}$ or $I_{IN(-)}$		45	150		45	250	nA
		$I_{IN(+)}$ or $I_{IN(-)}$; Over temp.		40	300		40	500	nA
I_B	Drift	Over temp.		50			50		pA/°C
V_{CM}	Common-mode voltage range[3]	V+ = 30 V	0		V+–1.5	0		V+–1.5	V
		V+ = 30 V; Over temp.	0		V+–2.0	0		V+–2.0	V
CMRR	Common-mode rejection ratio	V+ = 30 V	70	85		65	70		dB
V_{OH}	Output voltage swing	R_L ≥ 2 kΩ; V+ = 30 V; over temp.	26			26			V
		R_L ≥ 10 kΩ; V+ = 30 V; over temp.	27	28		27	28		V
V_{OL}	Output voltage swing	R_L ≥ 10 kΩ; over temp.		5	20		5	20	mV
I_{CC}	Supply current	R_L = ∞; V+ = 30 V		0.5	1.0		0.5	1.0	mA
		R_L=∞ on all amplifiers; V+ = 30 V; over temp.		0.6	1.2		0.6	1.2	mA
A_{VOL}	Large-signal voltage gain	R_L ≥ 2 kΩ; V_{OUT} ±10 V	50	100		25	100		V/mV
		V+=15V (for large V_O swing); over temp.	25			15			V/mV
PSRR	Supply voltage rejection ratio	R_S = 0 Ω	65	100		65	100		dB
	Amplifier-to-amplifier coupling[4]	f = 1 kHz to 20 kHz (input referred)		–120			–120		dB
I_{OUT}	Output current (Source)	V_{IN+} = +1 V_{DC}; V_{IN-} = 0 V_{DC}; V+ = 15 V_{DC}	20	40		20	40		mA
		V_{IN+} = +1 V_{DC}; V_{IN-} = 0 V_{DC}; V+ = 15 V_{DC}; over temp.	10	20		10	20		mA
	Output current (Sink)	V_{IN-} = +1 V_{DC}; V_{IN+} = 0 V_{DC}; V+ = 15 V_{DC}	10	20		10	20		mA
		V_{IN-} = +1 V_{DC}; V_{IN+} = 0 V_{DC}; V+ = 15 V_{DC}; over temp.	5	8		5	8		mA
		V_{IN+} = 0 V; V_{IN-} = +1 V_{DC}; V_O = 200 mV	12	50		12	50		μA
I_{SC}	Short circuit current[5]			40	60		40	60	mA
	Differential input voltage[6]				V+			V+	V
GBW	Unity gain bandwidth	T_{amb} = 25 °C		1			1		MHz
SR	Slew rate	T_{amb} = 25 °C		0.3			0.3		V/μs
V_{NOISE}	Input noise voltage	T_{amb} = 25 °C; f = 1 kHz		40			40		nV/√Hz

(Notes on next page).

DC ELECTRICAL CHARACTERISTICS (continued)

T_{amb} = 25 °C; V+ = +5 V; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM358A			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage[1]	R_S = 0 Ω		±2	±3	mV
		R_S = 0 Ω; over temp.			±5	mV
V_{OS}	Drift	R_S = 0 Ω; over temp.		7	20	µV/°C
I_{OS}	Offset current	$I_{IN(+)} - I_{IN(-)}$		5	±30	nA
		Over temp.			±75	nA
I_{OS}	Drift	Over temp.		10	300	pA/°C
I_{BIAS}	Input current[2]	$I_{IN(+)}$ or $I_{IN(-)}$		45	100	nA
		$I_{IN(+)}$ or $I_{IN(-)}$; Over temp.		40	200	nA
I_B	Drift	Over temp.		50		pA/°C
V_{CM}	Common-mode voltage range[3]	V+ = 30 V	0		V+–1.5	V
		V+ = 30 V; Over temp.	0		V+–2.0	V
CMRR	Common-mode rejection ratio	V+ = 30 V	65	85		dB
V_{OH}	Output voltage swing	R_L ≥ 2 kΩ; V+ = 30 V; over temp.	26			V
		R_L ≥ 10 kΩ; V+ = 30 V; over temp.	27	28		V
V_{OL}	Output voltage swing	R_L ≥ 10 kΩ; over temp.		5	20	mV
I_{CC}	Supply current	R_L = ∞, V+ = 30 V		0.5	1.0	mA
		R_L = ∞ on all amplifiers; V+ = 30 V; over temp.		0.6	1.2	mA
A_{VOL}	Large-signal voltage gain	R_L ≥ 2 kΩ; V_{OUT} ±10 V	25	100		V/mV
		V+ = 15 V (for large V_O swing); over temp.	15			V/mV
PSRR	Supply voltage rejection ratio	R_S = 0 Ω	65	100		dB
	Amplifier-to-amplifier coupling[4]	f=1kHz to 20kHz (input referred)		–120		dB
I_{OUT}	Output current (Source)	V_{IN+} = +1 V_{DC}; V_{IN-} = 0 V_{DC}; V+ = 15 V_{DC}	20	40		mA
		V_{IN+} = +1 V_{DC}; V_{IN-} = 0 V_{DC}; V+ = 15 V_{DC}; over temp.	10	20		mA
	Output current (Sink)	V_{IN-} = +1 V_{DC},;V_{IN+} = 0 V_{DC}; V+ = 15 V_{DC}	10	20		mA
		V_{IN-} = +1 V_{DC}; V_{IN+} = 0 V_{DC};V+ = 15 V_{DC}; over temp.	5	8		mA
		V_{IN+} = 0 V; V_{IN-} = +1 V_{DC}; V_O = 200 mV	12	50		µA
I_{SC}	Short circuit current[5]			40	60	mA
	Differential input voltage[6]				V+	V
GBW	Unity gain bandwidth	T_{amb} = 25 °C		1		MHz
SR	Slew rate	T_{amb} = 25 °C		0.3		V/µs
V_{NOISE}	Input noise voltage	T_{amb} = 25 °C; f = 1 kHz		40		nV/√Hz

NOTES:

1. $V_O \approx 1.4$ V, R_S = 0 Ω with V+ from 5 V to 30 V; and over the full input common-mode range (0 V to V+ –1.5 V).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V+ –1.5 V, but either or both inputs can go to +32 V without damage.
4. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance coupling increases at higher frequencies.
5. Short-circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of V+. At values of supply voltage in excess of +15 V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V+ –1.5 V, but either or both inputs can go to +32 V_{DC} without damage.

TYPICAL PERFORMANCE CHARACTERISTICS

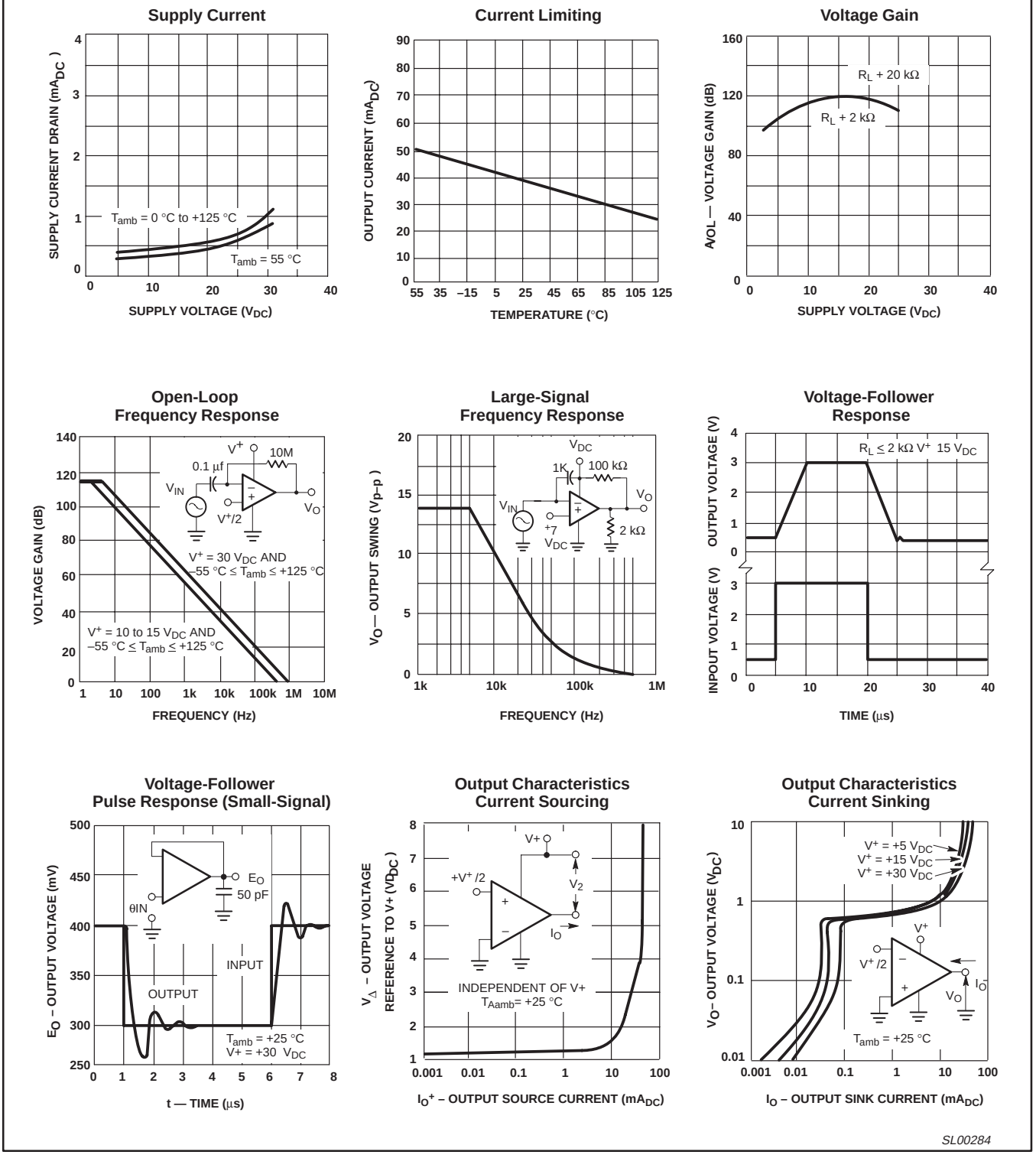


Figure 3. Typical performance characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

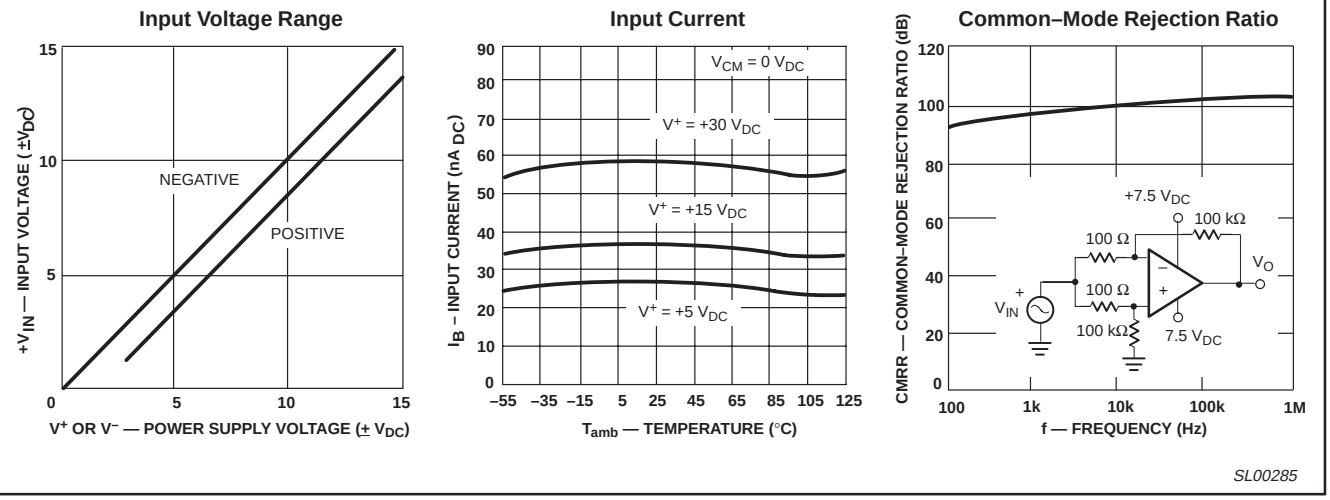


Figure 4. Typical performance characteristics (continued)**.**

TYPICAL APPLICATIONS

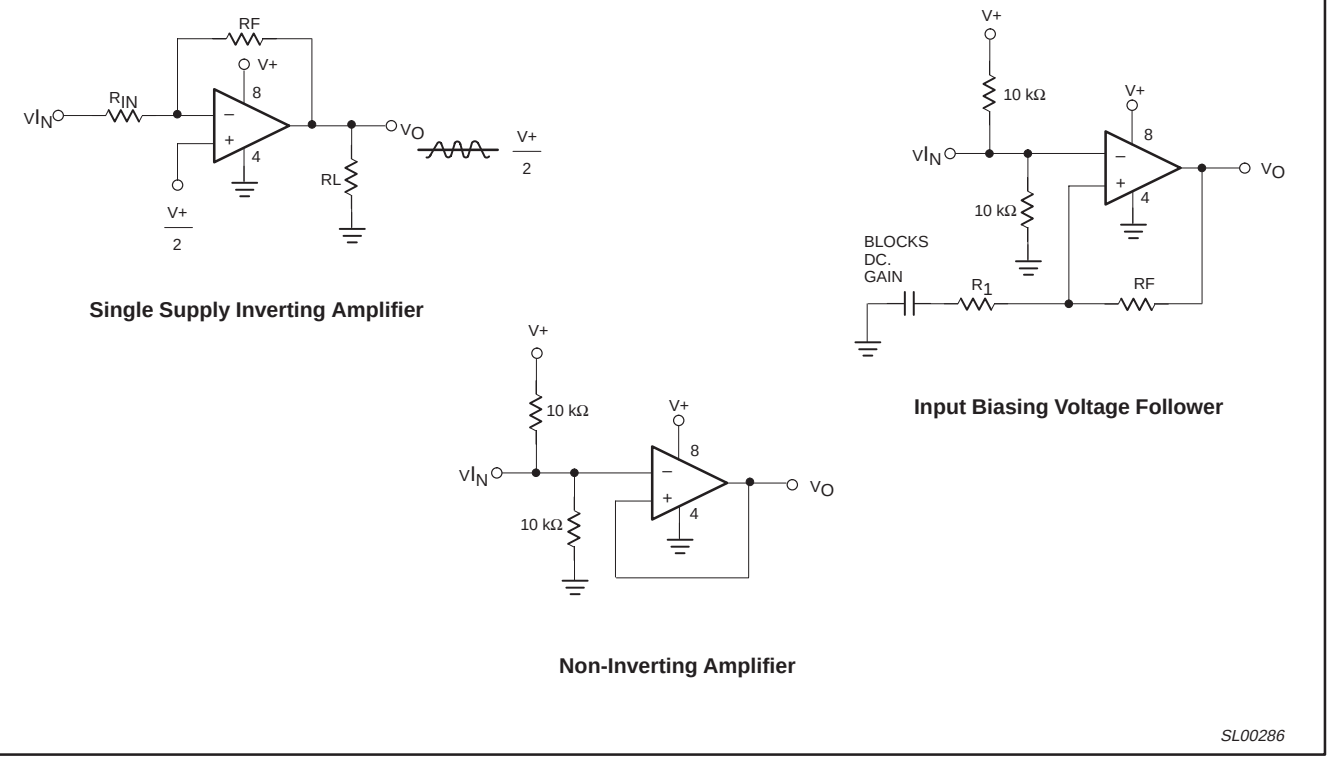
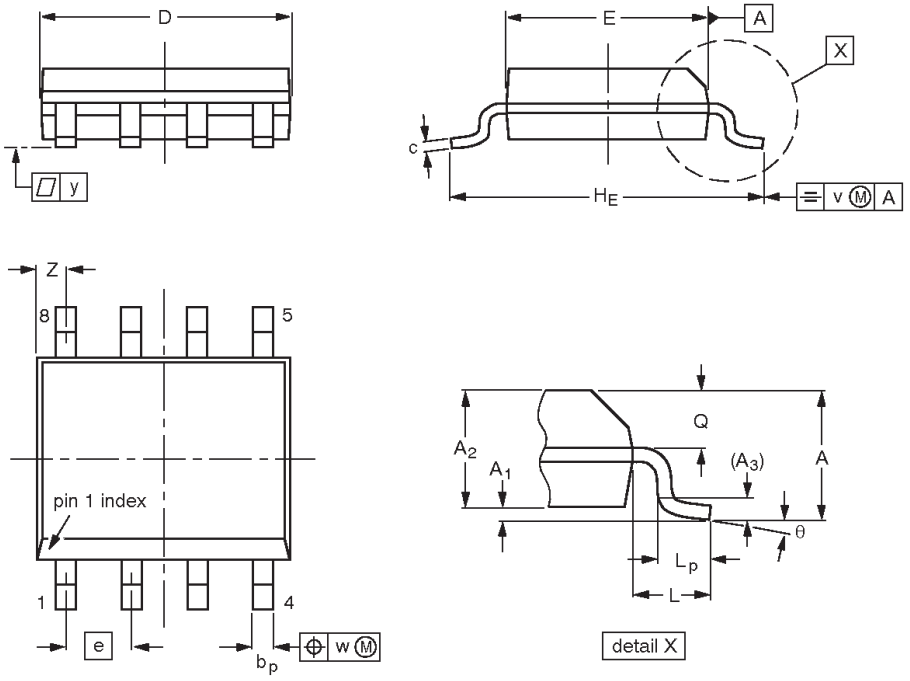
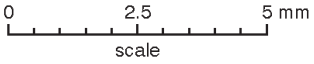


Figure 5. Typical applications.

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

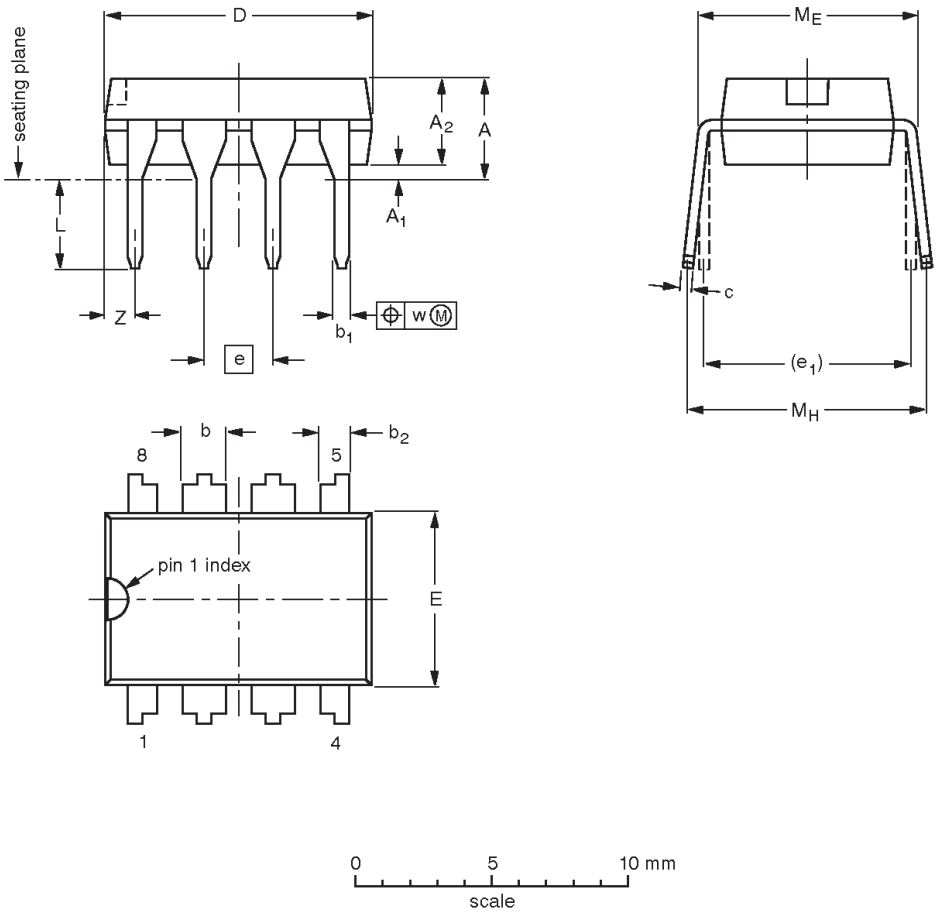
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				~~97-05-22~~ 99-12-27

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

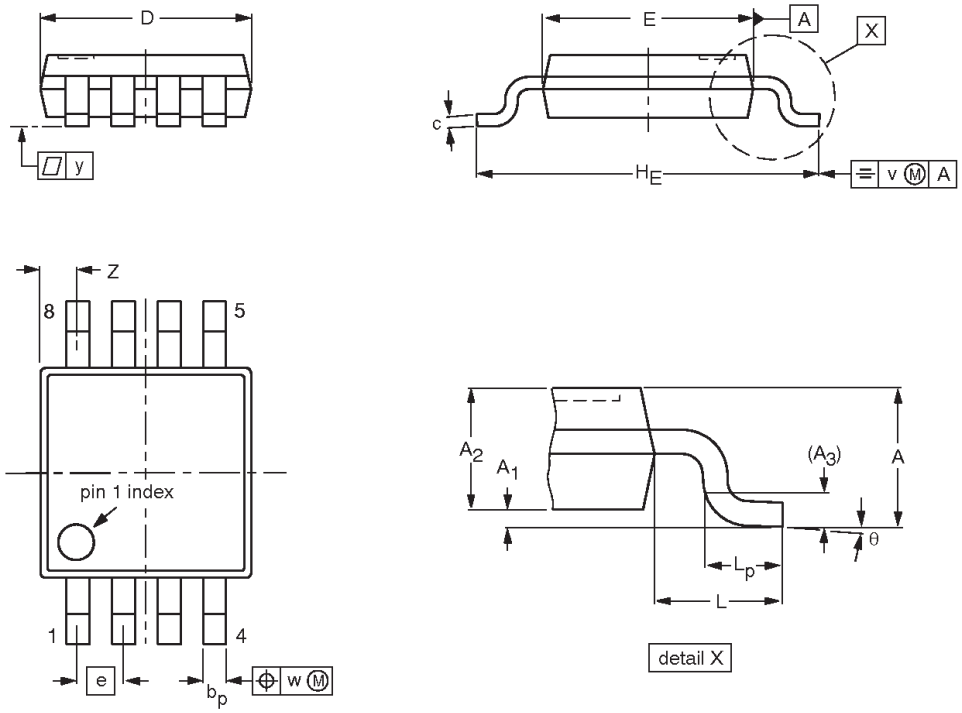
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

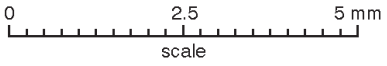
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001	SC-504-8			~~95-02-04~~ 99-12-27

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.10 2.90	3.10 2.90	0.65	5.10 4.70	0.94	0.70 0.40	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT505-1						99-04-09

NOTES

Data sheet status

Data sheet status [1]	Product status [2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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